

Article

Integrated Three-Voltage-Booster DC-DC Converter to Achieve High Voltage Gain with Leakage-Energy Recycling for PV or Fuel-Cell Power Systems

Chih-Lung Shen *, Hong-Yu Chen and Po-Chieh Chiu

Department of Electronic Engineering, National Kaohsiung First University of Science and Technology, Kaohsiung 82445, Taiwan; E-Mails: u0152804@nkfust.edu.tw (H.-Y.C.); u0352801@nkfust.edu.tw (P.-C.C.)

* Author to whom correspondence should be addressed; E-Mail: clshen@nkfust.edu.tw; Tel.: +886-7-601-1000; Fax: +886-7-601-1386.

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Abstract: In this paper, an integrated three-voltage-booster DC-DC (direct current to direct current) converter is proposed to achieve high voltage gain for renewable-energy generation systems. The proposed converter integrates three voltage-boosters into one power stage, which is composed of an active switch, a coupled-inductor, five diodes, and five capacitors. As compared with conventional high step-up converters, it has a lower component count. In addition, the features of leakage-energy recycling and switching loss reduction can be accomplished for conversion efficiency improvement. While the active switch is turned off, the converter can inherently clamp the voltage across power switch and suppress voltage spikes. Moreover, the reverse-recovery currents of all diodes can be alleviated by leakage inductance. A 200 W prototype operating at 100 kHz switching frequency with 36 V input and 400 V output is implemented to verify the theoretical analysis and to demonstrate the feasibility of the proposed high step-up DC-DC converter.

Keywords: PV (photovoltaic) module; fuel cell; high step-up converter; leakage-energy recycling

1. Introduction

In recent years, owing to the shortage of fossil fuels and the serious problems of environmental pollution, discovering and developing alternative energy resources has become more and more important. To alleviate the problems of rising global temperatures and the serious emission of greenhouse gases, green energy sources such as photovoltaic (PV) power, wind energy, or fuel cells have been the center of attention [1,2]. Generally, a grid-tied renewable-energy system needs a DC bus voltage falling in the range from 380 to 420 V, as shown in Figure 1. Unfortunately, the terminal voltages of PV module, fuel cells, or battery set are less than 45 V. That is, these green-energy generation units require a high step-up converter to serve as a voltage boosting interface between the generation unit and the utility.

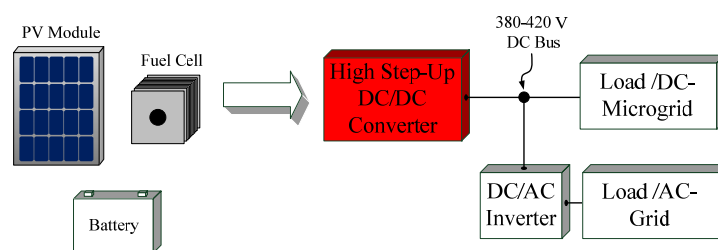


Figure 1. A block diagram to illustrate the grid-tied green-energy power system.

Conventional boost converters can achieve high voltage gains by means of extreme duty ratio operation [3–6]. However, this will result in large current ripple, significant conduction loss, and heavy current stress on power devices. That is, converter efficiency drops dramatically. In order to resolve this problem, converters with transformers, such as flyback, forward, and push-pull units, are considered [7–10]. Even though those converters can step up input voltage by adopting high turns-ratio transformers, efficiency is degraded heavily due to the copper loss of windings. Besides, high voltage spikes caused from leakage inductance will be imposed on semiconductor devices. To improve this shortcoming, snubber circuits or active clamp circuits are used but then the cost is increased. In [11–14], transformerless high step-up converters are proposed to mitigate the aforementioned drawbacks. Those converters have the features of simple structure, high voltage gain, and low cost, nevertheless, the problem of voltage gain inflexibility still exists. In the most current trend, switched capacitor and coupled inductor techniques are adopted to design high step-up converters [15–19]. Those high step-up converters have their own advantages and disadvantages, and result in a compromise between power component count, voltage gain, current stress, voltage stress, and power rating. This paper proposes a novel high step-up converter, which incorporates three voltage boosters and then integrates them into one stage. That is, only one active switch is used. As a result, low component count, concise structure, high voltage gain, easy control circuit design, and high efficiency are its inherent features. Figure 2 depicts the configuration of the power stage.

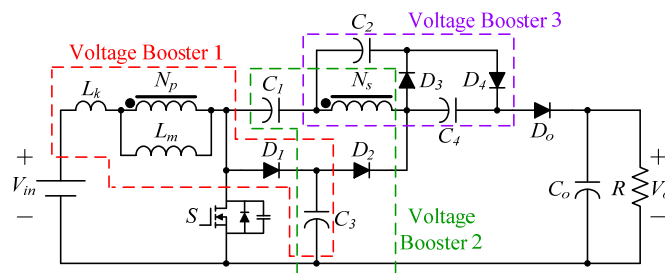


Figure 2. Power circuit of the proposed high step-up converter.

This paper is organized as follows: the operation principle of the proposed converter is described in Section 2. Section 3 deals with steady-state analysis and performance comparison, while practical measurements are given in Section 4. Finally, the conclusions are described in Section 5.

2. Operation Principle of the Proposed Converter

For the description of the operation principle, Figure 3 shows the definition of circuit variables, voltage polarity, and current direction. In Figure 3, the notations V_{in} and I_{in} denote the DC input voltage and current, respectively; L_m is the magnetizing inductance of the coupled inductor, while L_k stands for the associated leakage inductance; S represents the active power switch; C_1 and C_4 are switched capacitors; C_2 and C_3 are boosting capacitors; D_1, D_2, D_3 , and D_4 are rectifier diodes; D_o denotes output diode; V_o and I_o are described as output voltage and current, respectively, while R is the output load. In addition, the turns ratio N_s/N_p is defined as n .

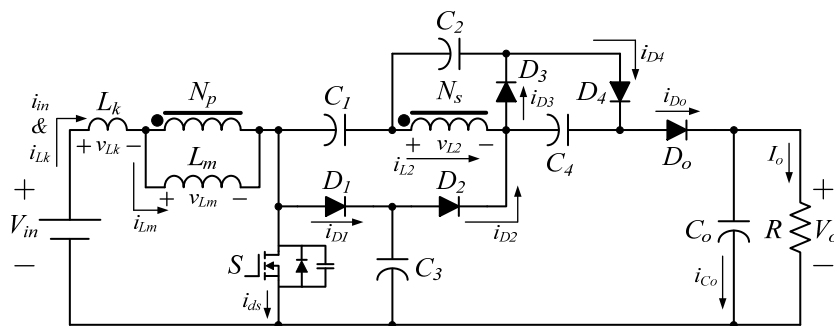


Figure 3. Definition of voltage polarity and current direction.

Assume that the converter is operated in continuous conduction mode (CCM). The operation principle can be divided into six stages over one switching period. Figure 4 shows the corresponding equivalent circuits of the six stages and Figure 5 depicts the associated conceptual waveforms. The operation principle is described in the following paragraphs stage by stage:

Stage 1 [$t_0 \sim t_1$]: At time $t = t_0$, switch S is turned on. Diodes D_1, D_2 and D_4 are reversely biased, but D_3 and D_o are forward biased. In this time interval, the current of leakage-inductor i_{Lk} increases linearly and steeply. The energy stored in magnetizing-inductor L_m is released to the output via D_o and boosts capacitor C_2 via D_3 . Meanwhile, the current following through D_o , i_{D0} , is decreasing. Until the current i_{D0} drops to zero, this operation stage ends. There is no reverse-recovery loss on diode D_o . Figure 4a shows the equivalent circuit of this stage.

Stage 2 [$t_1 \sim t_2$]: This stage begins at time $t = t_1$, of which equivalent circuit is shown in Figure 4b. Switch S remains closed. Diodes D_1 , D_3 and D_o are reversely biased, but D_2 and D_4 are forward biased. In this time interval, the magnetizing-inductor L_m and leakage-inductor L_k absorb energy from the DC source V_{in} . The switched capacitor C_1 is charged by the secondary of the coupled inductor and capacitor C_3 , while the other switched capacitor C_4 is by the secondary of the coupled inductor and capacitor C_2 . During this stage, only the output capacitor C_o provides energy to the load R . When switch S is turned off, operation of this converter enters into the next stage.

Stage 3 [$t_2 \sim t_3$]: Switch S is turned off at $t = t_2$. During this stage, diodes D_1 , D_2 and D_4 are in on-state, but diodes D_3 and D_o are reversely biased. In this time interval, the energy of leakage-inductor L_k releases to the parasitic capacitor of switch S and thus, switch voltage increases. When the voltage across the parasitic capacitor is higher than that of boosting capacitor C_3 , diode D_1 becomes forward and this operation stage is completed. Figure 4c illustrates the corresponding equivalent of Stage 3.

Stage 4 [$t_3 \sim t_4$]: Switch S is still kept in off-state over the period of Stage 4. Diodes D_2 , D_3 and D_o are reversely biased, but diodes D_1 , and D_4 are in forward bias, as shown in Figure 4d. The boosting capacitor C_3 is charged by magnetizing-inductor L_m and leakage-inductor L_k . That is, leakage energy of L_k is recycled to C_3 and the voltage across active switch is clamped by C_3 , which suppresses voltage spike effectively. At the moment the voltage polarity of magnetizing-inductor L_m changes, this stage is finished.

Stage 5 [$t_4 \sim t_5$]: The equivalent circuit is illustrated in Figure 4e. Switch S remains off. The status of diodes D_1 , D_3 and D_o are on but D_2 and D_4 off. In this time interval, the energy of magnetizing-inductor L_m is dumped to ideal transformer, output terminal, and capacitor C_3 simultaneously. The secondary side of coupled inductor charges the boosting capacitor C_2 via diode D_3 . At the same time, the output voltage is stacked by input voltage V_{in} , coupled inductor, and capacitors C_1 and C_4 .

Stage 6 [$t_5 \sim t_6$]: This stage begins as C_3 stops charging. The diode D_1 becomes reversely biased. The corresponding equivalent circuit is shown in Figure 4f. The energy stored in L_m keeps dumping energy to C_2 via ideal transformer. When power switch is turned on again, this stage ends and converter operation over one switching cycle is completed.

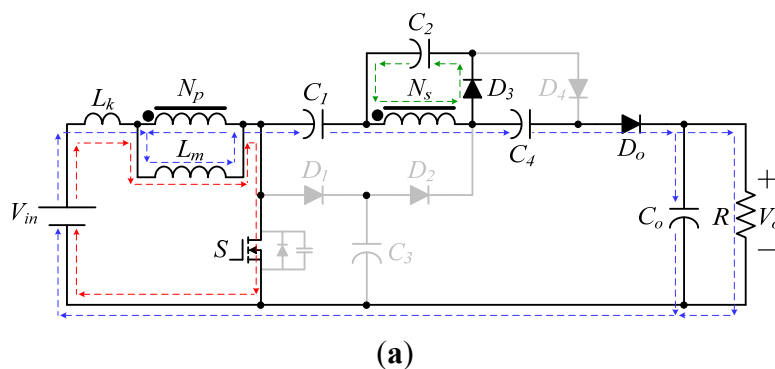


Figure 4. Cont.

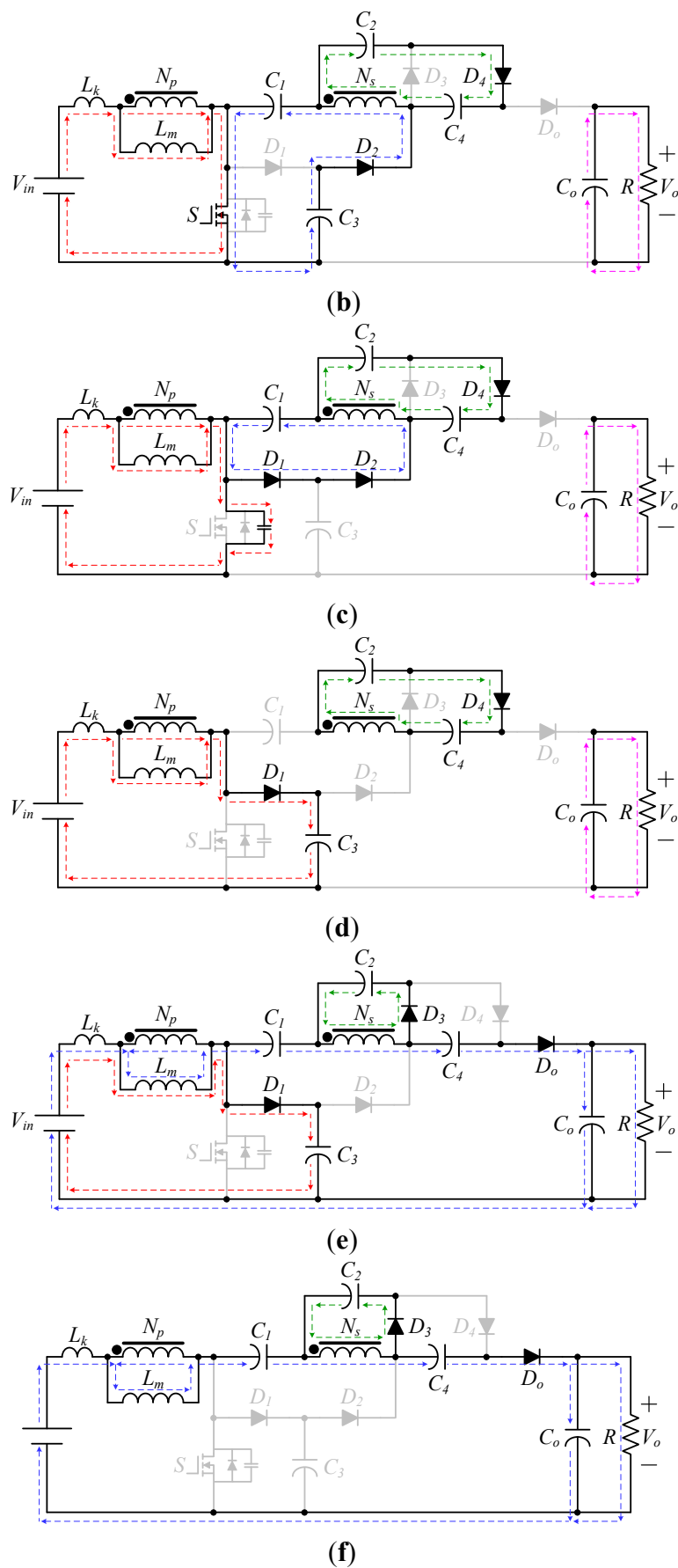


Figure 4. Equivalent circuits of the proposed converter. (a) Stage 1; (b) Stage 2; (c) Stage 3; (d) Stage 4; (e) Stage 5; and (f) Stage 6.

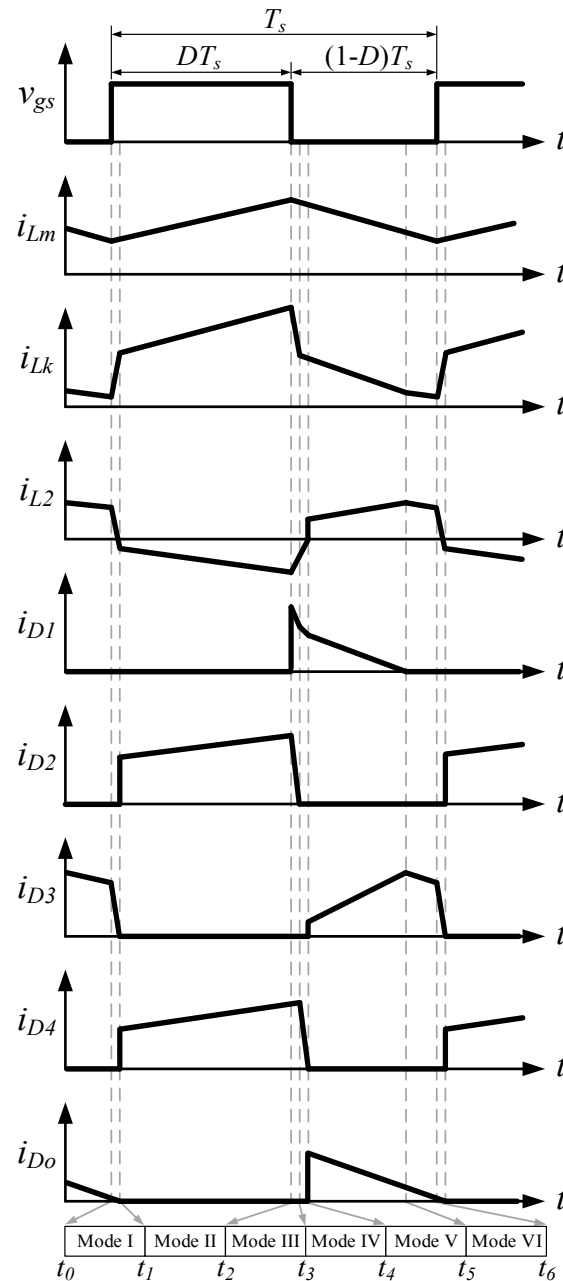


Figure 5. Conceptual key waveforms of the proposed converter.

3. Steady-State Analysis of the Proposed Converter

To simplify the circuit analysis, the transient state of the circuit is ignored. In addition, some assumptions are made as follows:

- (1) The values of all capacitors are large enough so that voltages across all capacitors are considered as constant;
- (2) All semiconductor components in the power circuit are ideal;
- (3) The magnetizing inductance is much greater than leakage inductance. The influence of the leakage inductance can be neglected. That is, the coupling coefficient of coupled inductor k is equal to unity;
- (4) Equivalent series resistance of coupled inductor is ignored;

- (5) The active switch is closed for DT_s and open for $(1-D)T_s$;
- (6) The converter is operated in CCM. According to the preceding assumptions, Figure 4b is referred while switch S closed and Figure 4e is referred while switch S open.

3.1. Derivation of Voltage Gain

To derive the voltage gain of V_o to V_{in} , the voltages of V_{C1} , V_{C2} , V_{C3} , and V_{C4} have to be calculated in advance. When active switch S is turned on, referring to Figure 4b and neglecting L_k , the voltage across the secondary winding of the coupled inductor, $v_{L2(on)}$, is:

$$v_{L2(on)} = nV_{in} \quad (1)$$

Therefore, the magnitudes of the voltages V_{C1} and V_{C4} can be expressed as:

$$V_{C1} = nV_{in} + V_{C3} \quad (2)$$

and:

$$V_{C4} = nV_{in} + V_{C2} \quad (3)$$

respectively. With respect to V_{C2} and V_{C3} , the state of switch off is contacted and the equivalent circuit shown in Figure 4e is referred. Similarly, according to the assumptions, the leakage inductance L_k in Figure 4e is also neglected. The circuit behaviors that input voltage forwards energy to the capacitors C_2 and C_3 are similar to those of flyback and boost converters, respectively. Therefore, the voltages V_{C2} and V_{C3} can be expressed as:

$$V_{C2} = \frac{nD}{1-D} V_{in} \quad (4)$$

and:

$$V_{C3} = \frac{1}{1-D} V_{in} \quad (5)$$

Substituting Equations (4) and (5) into Equations (2) and (3), in turn, yields:

$$V_{C1} = \frac{1+n-nD}{1-D} V_{in} \quad (6)$$

and:

$$V_{C4} = \frac{n}{1-D} V_{in} \quad (7)$$

From Figure 4e, it can be found that the output voltage is the sum of V_{in} , V_{C1} , V_{C4} , and the voltages across N_p and N_s . Thus, the following relationship holds:

$$V_o = 2V_{in} \left(\frac{1}{1-D} + n + \frac{nD}{1-D} \right) \quad (8)$$

Rearranging Equation (8), one can find the voltage gain of the proposed high step-up converter:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+n)}{1-D} \quad (9)$$

To further understand the voltage gain performance of the proposed converter, Figure 6 shows the voltage gain *versus* duty cycle under various turns ratios n . It indicates that when the duty cycle D equals 0.5, the converter achieves an output voltage sixteen times of the input voltage under the turns ratio of 3. As compared with other high step-up converters in the literature [19–21], the proposed converter has a higher voltage gain than that of the conventional converters if $n = 1.5$, which is shown in Figure 7.

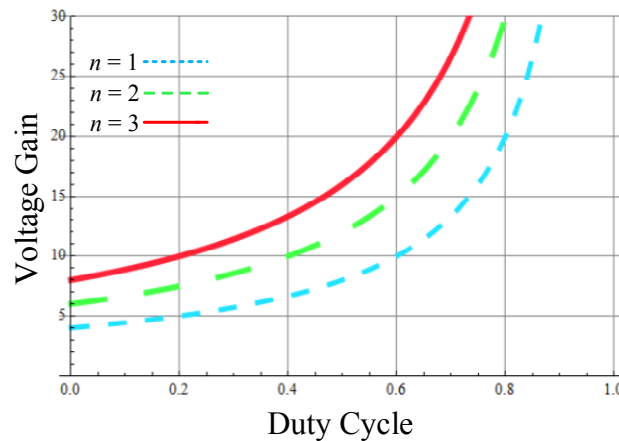


Figure 6. Illustration of voltage gain *versus* duty cycle under different turns ratios.

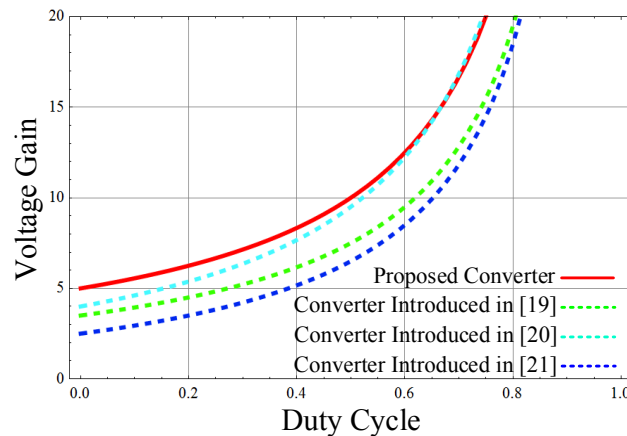


Figure 7. Voltage gain comparison among the proposed converter and conventional converters in [19–21].

3.2. Voltage Stress of Power Device

Voltage stress of power devices is an important parameter for choosing power semiconductor devices. A power semiconductor device with lower voltage stress will inherently have a lower on-state resistance or forward voltage, which dominates converter efficiency. The voltage stresses across D_1 , D_3 and D_o are determined as active switch is closed. On the contrary, the voltage stresses of S , D_2 and D_4 are determined as active switch is open. When the switch is in an on-state, referring to Figure 4b the voltages across D_1 and D_3 are equal to V_{C3} and V_{C4} , respectively. Therefore, the voltage stresses $V_{D1, stress}$ and $V_{D3, stress}$ can be estimated as:

$$V_{D1, stress} = \frac{1}{1-D} V_{in} \quad (10)$$

and:

$$V_{D3, stress} = \frac{n}{1-D} V_{in} \quad (11)$$

Meanwhile, the output diode endures a voltage equal to $V_o - V_{C3} + V_{C4}$, that is:

$$V_{Do, stress} = \frac{1+n}{1-D} V_{in} \quad (12)$$

After switch S is turned off, the voltage of diode D_2 will be clamped to $V_{C1} - V_{L2}$, as shown in Figure 4e. From Equation (6), the sustained voltage $V_{D2, stress}$ is:

$$V_{D2, stress} = \frac{1+n}{1-D} V_{in} \quad (13)$$

In addition, during off-time interval, the blocking voltages of S and D_4 are V_{C3} and V_{C4} , respectively, so that:

$$V_{D4, stress} = \frac{n}{1-D} V_{in} \quad (14)$$

and:

$$V_{ds, stress} = \frac{1}{1-D} V_{in} \quad (15)$$

3.3. Current on Power Devices

Since leakage inductance is neglected, the equivalent circuits of Stage 2 and Stage 5, as shown in Figure 4b,e are considered for switch on and off, respectively. Based on the amp-second balance theorem, the following relationship is suitable for any capacitor in the converter:

$$I_{C, on-state} T_{on-state} + I_{C, off-state} T_{off-state} = 0 \quad (16)$$

In Equation (16), $I_{C, on-state}$ and $T_{on-state}$ stand for capacitor current and time period during on-state, while $I_{C, off-state}$ and $T_{off-state}$ are for off-state. The ratio of output current to input current is reciprocal to that of output voltage to input voltage. From Equation (9), one can find:

$$\frac{I_o}{I_{in}} = \frac{1-D}{2(1+n)} \quad (17)$$

The currents of diodes D_1 , D_3 and D_o can be estimated as the switch is open. Referring to Figure 4e and deriving with Equations (16) and (17), one can obtain the average current following through D_1 , D_3 and D_o :

$$I_{D1} = I_{D3} = I_{Do} = \frac{1}{1-D} I_o = \frac{1}{2(1+n)} I_{in} \quad (18)$$

With a similar derivation procedure, while the switch is closed and Figure 4b is referred, the average currents of D_2 and D_4 can be found as:

$$I_{D2} = I_{D4} = \frac{I_o}{D} = \frac{1-D}{2(1+n)D} I_{in} \quad (19)$$

Owing to capacitors C_2 and C_3 discharging toward C_1 and C_4 during on-state interval, the average current of switch S , I_{ds} , is expressed as:

$$I_{ds} = I_{Lm} + (1+n)I_{D2} + nI_{D4} \quad (20)$$

Equation (20) reveals that the I_{Lm} has to be known in advance for the determination of I_{ds} . From Kirchhoff's current law (KCL), the input current is the sum of magnetizing current and the current following through ideal transformer. That is:

$$I_{Lm} = [I_{in} - n(I_{D2} + I_{D4})]D + [(I_{in} + n(I_{D3} + I_{D4}))](1-D) = I_{in} = \frac{2(1+n)}{1-D} I_o \quad (21)$$

Substituting Equations (18), (19) and (21) into Equation (20), the average current of power switch S can be readily obtained as:

$$I_{ds} = \frac{1+2n+D}{(1-D)D} I_o = \frac{1+2n+D}{2(1+n)D} I_{in} \quad (22)$$

3.4. Design of Energy Storage Component

To ensure that the proposed converter can operate in CCM, the minimum magnetizing inductance has to be calculated. Over whole switch-on period, the net change in magnetizing current, Δi_{Lm} , can be expressed as:

$$\Delta i_{Lm} = \frac{V_{in}}{L_m} DT_s \quad (23)$$

The boundary conduction mode (BCM) occurs when:

$$I_{Lm} - \frac{1}{2} \Delta i_{Lm} = 0 \quad (24)$$

Substituting Equations (9), (17), (21) and (23) into Equation (24) one can then obtain the minimum value of magnetizing inductance for CCM operation, $L_{m,min}$, as follows:

$$L_{m,min} = \frac{V_{in}}{2I_{Lm}} DT_s = \frac{(1-D)^2 DR_o}{8f(1+n)^2} \quad (25)$$

Figure 8 illustrates the relationship between L_m and duty cycle under the conditions that turns ratio $n = 1.5$, switching frequency $f_s = 100$ kHz, and the load resistance $R_o = 3.2$ k Ω .

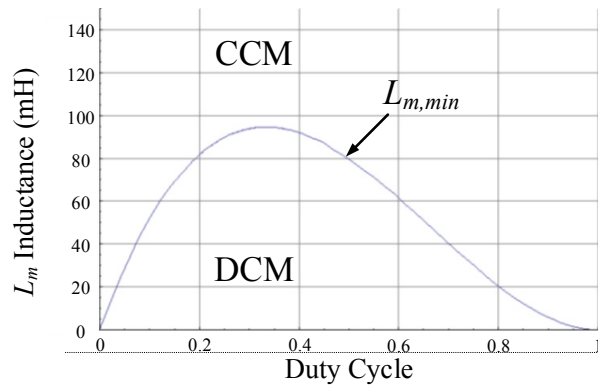


Figure 8. Illustrating the relationship between magnetizing inductance L_m and duty ratio D .

Even though a larger capacitance can result in a lower voltage ripple, it increases cost. Adopting an appropriate capacitance for the converter is necessary. The capacitance is found by:

$$C = \frac{\Delta q}{\Delta v_C} \quad (26)$$

where Δq is the change in charge and Δv_C is the accompanied voltage variation. During the time interval when S is off, capacitors C_2 and C_3 are charged by the currents of I_{D3} and I_{D1} , respectively. Accordingly, from Equations (18) and (26), the following relationships hold:

$$C_2 = \frac{I_{D3}}{\Delta v_{C2}}(1-D)T_s = \frac{I_o T_s}{\Delta v_{C2}} = \frac{I_o}{\Delta v_{C2} f} \quad (27)$$

and:

$$C_3 = \frac{I_{D1}}{\Delta v_{C3}}(1-D)T_s = \frac{I_o T_s}{\Delta v_{C3}} = \frac{I_o}{\Delta v_{C3} f} \quad (28)$$

Opposite to the charge behavior of C_2 and C_3 , both capacitors C_1 and C_4 discharge with the current I_{D0} . Also, one can find C_1 and C_4 from Equations (18) and (26) with the same procedure as for C_2 and C_3 , and then have:

$$C_1 = \frac{I_{D0}}{\Delta v_{C1}}(1-D)T_s = \frac{I_o T_s}{\Delta v_{C1}} = \frac{I_o}{\Delta v_{C1} f} \quad (29)$$

and:

$$C_4 = \frac{I_{D0}}{\Delta v_{C4}}(1-D)T_s = \frac{I_o T_s}{\Delta v_{C4}} = \frac{I_o}{\Delta v_{C4} f} \quad (30)$$

With regard to C_o , the switch off interval is also considered. The magnitude of capacitor current I_{C_o} is the difference between load current I_o and output diode current I_{D0} . Therefore, C_o can be computed by:

$$C_o = \frac{(I_{D0} - I_o)}{\Delta v_{C_o}}(1-D)T_s = \frac{I_o D T_s}{\Delta v_{C_o}} = \frac{I_o D}{\Delta v_{C_o} f} \quad (31)$$

3.5. Performance Comparison

Performance comparison of the proposed converter with other high step-up converters is summarized in Table 1. The proposed converter has a lower power component count. That is, it is cost-effective. In addition, higher voltage gain can be achieved. If the duty ratio is 0.5 and turns ratio is 1, the proposed converter has a voltage gain of 8 and the other two high step-up converters in [19–21] are 6, 7 and 5 in turn. Even though the converter can accomplish higher voltage gain, its voltage stress across power switch is the lowest. This reveals that a power switch with low on-state resistance can be adopted in the converter for power loss reduction. From Table 1, it also can be seen that the switching loss of the converter is small, because the switch voltage in off-time interval is clamped to V_{C3} .

Table 1. Performance comparison of the proposed converter with other high step-up converters.

High step-up converters	Converter introduced in [19]	Converter introduced in [20]	Converter introduced in [21]	Proposed converter
Voltage gain	$\frac{2+n+(n-1)D}{1-D}$	$\frac{1+2n+nD}{1-D}$	$n_2 + \frac{1+(n_2+n_3)D}{1-D}$	$\frac{2(1+n)}{1-D}$
Diodes	3	6	5	5
Capacitors	3	6	5	5
windings	2	2	3	2
Voltage stress on switch	$\frac{V_o}{2+n+(n-1)D}$	$\frac{V_o}{1+2n+nD}$	$\frac{V_o}{1+n_2+n_3D}$	$\frac{V_o}{2(1+n)}$
Conduction loss	small	middle	small	small
Switching loss	small	middle	middle	small

4. Experimental Results

To verify the proposed converter, a prototype is built, with the specifications and parameters listed in Table 2. In the prototype, semiconductor devices will dominate circuit losses. Their details are discussed. The power MOSFET, IRFSL4615PbF, is selected to serve as active switch for controlling the current flow, of which maximum on-state resistance $R_{DS(on)}$ is only 42 mΩ. BYW29E-200 is employed as diode D_1 , of which the forward voltage is 0.895 V and the reverse recovery time is 25 ns. With regard to diodes D_2 , D_3 , D_4 , and D_o , the ultrafast rectifier 8ETH03PbF is considered, which has 1.25 V forward voltage and 35 ns reverse recovery time. Figure 9a shows the measured voltage waveforms of the power switch and associated control gate signal. The switch blocks a voltage of 75 V, which meets the theoretical analysis in Section 3. Figure 9b is the diode currents of i_{D2} and i_{D4} , while i_{D0} and i_{D3} are shown in Figure 9c. From Figure 9b,c it is proven that D_2 and D_4 are forward biased when the switch is closed but D_3 and D_o are forward biased while the switch is open. Figure 9e depicts the waveforms of i_{D1} and the control gate signal, which illustrate that there is no reverse recovery current problem in diode D_1 . Voltages across C_3 and C_o are shown in Figure 9e in which output voltage and V_{C3} are kept at 400 V and 72 V, respectively. This is consistent with Equations (5) and (9). To examine the converter transient response, load changes from half load to full load and from full load to half load are carried out. Figure 9f is the corresponding measurement, from which it can be observed that the proposed converter performs fast response and can provide a constant high voltage even if under step load change.

Figure 10 is the measured efficiency of the prototype. The maximum efficiency is up to 97.1% and an efficiency of 94.9% is achieved at full load.

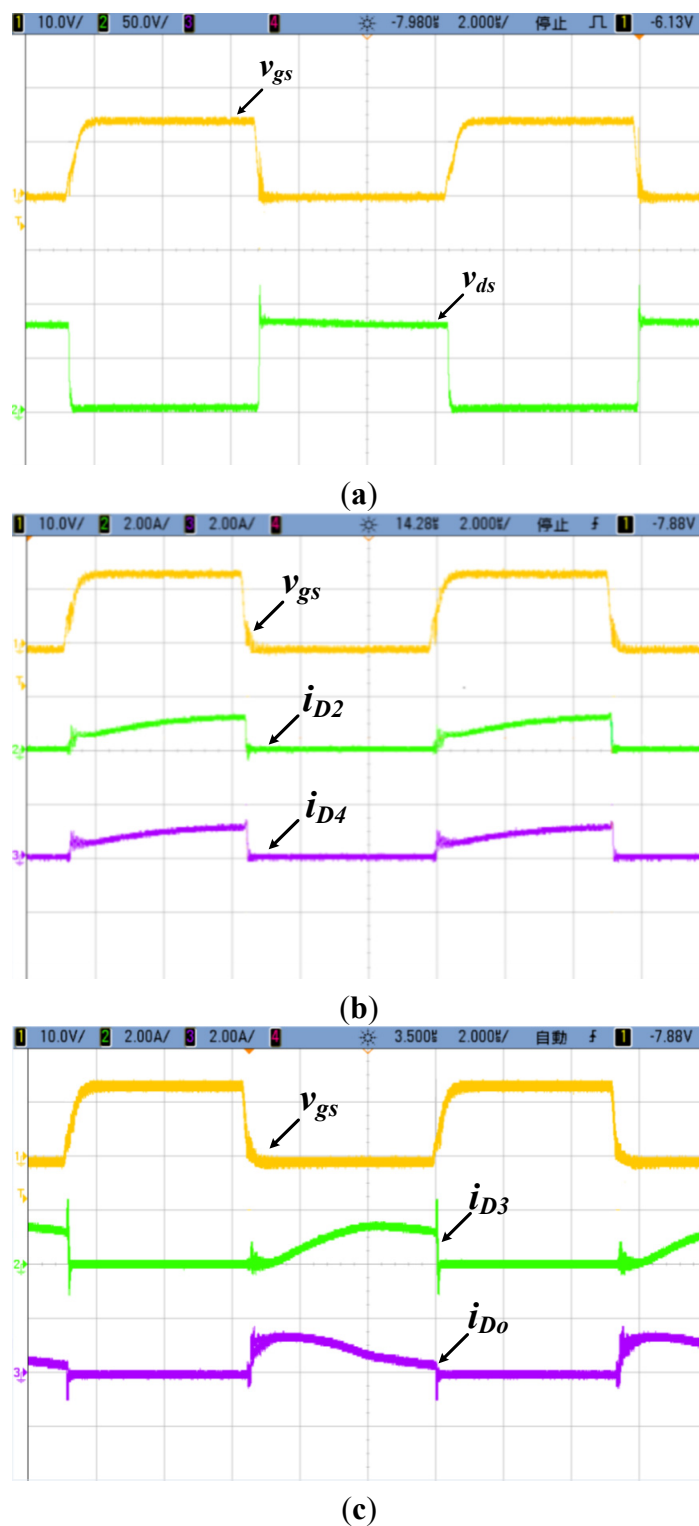


Figure 9. Cont.

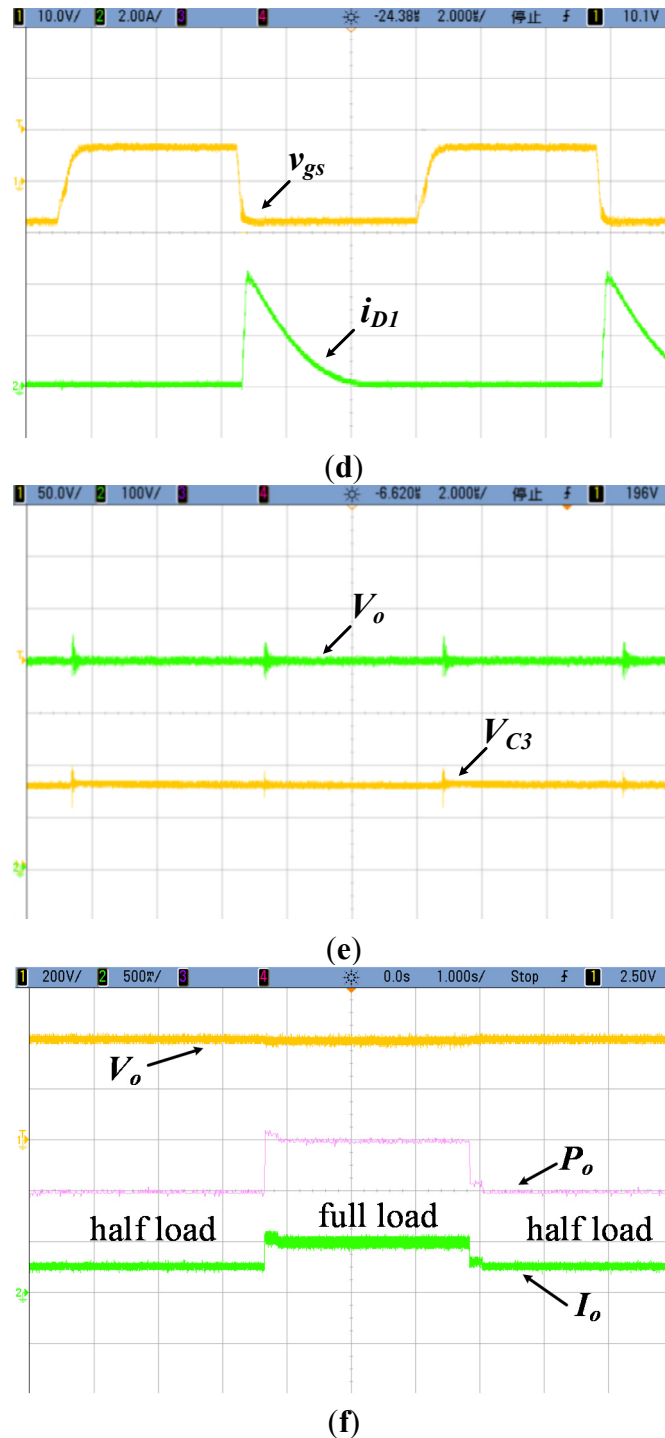
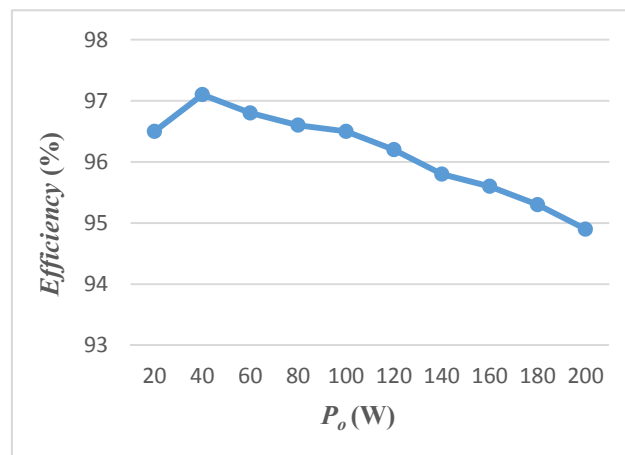


Figure 9. Experimental results at 200 W: (a) Power switch voltage waveforms (v_{gs} : 10 V/div; v_{ds} : 50 V/div; time: 2 μ s/div); (b) Diode currents i_{D2} and i_{D4} , (v_{gs} : 10 V/div; i_{D2} : 2 A/div; i_{D4} : 2 A/div; time: 2 μ s/div); (c) Diode currents i_{D3} and i_{Do} , (v_{gs} : 10 V/div; i_{D3} : 2 A/div; i_{Do} : 2 A/div; time: 2 μ s/div); (d) Diode current i_{D1} , (v_{gs} : 10 V/div; i_{D1} : 2 A/div; time: 2 μ s/div); (e) Waveforms of V_o and V_{C3} , (V_o : 100 V/div; V_{C3} : 50 V/div; time: 2 μ s/div); and (f) Step change between half load and full load, (V_o : 200 V/div; P_o : 200 W/div; I_o : 500 mA/div; time: 1 s/div).

Table 2. Specifications of the prototype.

Symbols	Values & Types
V_{in} (Input voltage)	36 V
V_o (Output voltage)	400 V
P_o (Rated power)	200 W
f_s (Switching frequency)	100 kHz
L_m (Magnetizing inductance)	55 μ H
L_k (Leakage inductance)	1.03 μ H
n (Transformer turns ratio)	1:1.6
C_1 and C_4 (Capacitance)	33 μ F
C_2 and C_3 (Capacitance)	22 μ F
C_o (Capacitance)	82 μ F
S (Active switch)	IRFSL4615PbF (150 V/33 A)
D_1 (Diode)	BYW29E-200 (200 V/8 A)
D_2, D_3, D_4 , and D_o (Diodes)	8ETH03PBF (300 V/8 A)

**Figure 10.** Measured efficiency of the proposed converter.

5. Conclusions

This paper proposes a DC-DC high step-up converter for renewable-energy generation systems. The proposed converter can achieve higher voltage gain though it needs fewer power components. The energy stored in the leakage inductor can be recycled and the voltage power switch can be clamped to a low voltage so as to improve converter efficiency and suppress voltage spikes. Accordingly, low on-state power switches and Schottky diodes can be employed. Finally, a prototype is built to validate the converter. Practical measurements have demonstrated the feasibility and correctness of the proposed high step-up converter.

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Author Contributions

Chih-Lung Shen and Hong-Yu Chen conceived and designed the circuit. Hong-Yu Chen performed the research and analyzed data with guidance from Chih-Lung Shen. Hong-Yu Chen and Po-Chieh Chiu wrote the manuscript, and then Chih-Lung Shen revised for the publication.

Conflicts of Interest

The authors declare no conflict of interest.

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