Energies **2015**, *8*, 1606-1627; doi:10.3390/en8031606

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energies

ISSN 1996-1073

www.mdpi.com/journal/energies

Article

Design of a Four-Branch *LCL*-Type Grid-Connecting Interface for a Three-Phase, Four-Leg Active Power Filter

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Academic Editor: Frede Blaabjerg

Received: 6 January 2015 / Accepted: 16 February 2015 / Published: 27 February 2015

Abstract: Compared with the three-phase, two-split-capacitor active power filter (3P2C-APF), the three-phase, four-leg active power filter (3P4L-APF) has been widely used in three-phase, four-wire grid utility for power quality control due to its numerous advantages, such as higher current output capability, particularly in phase N, lower current and easier voltage control on the DC-side. However, designing the grid-connecting interface, which is between the voltage source converter (VSC) and grid utility, is rather difficult due to the higher requirement for current ripple filtering in phase N, cross-coupling in four phases and lack of relevant design methodology and specification. In this paper, a four-branch LCL-type (4B-LCL) grid-connecting interface is proposed for 3P4L-APF, which features better current ripple filtering performance without decreasing the current output capability in all phases. First, this paper describes the mathematical models of 4B-LCL in the fully-complex-vector form from the zero and non-zero sequence perspective, resulting in two independent and uniform equivalent circuits without cross coupling terms. Then, the *4B-LCL* parameter design method based on the most comprehensive performance index is proposed, including three main stages as the specification: performance index requirement determination, fulfillment of that requirement, and verification. Finally, the validity and effectiveness of the proposed design are proven by the simulated and experimental results of a 3P4L-APF with *4B-LCL*.

Keywords: three-phase four-leg (3P4L); four-branch *LCL* (*4B-LCL*); grid-connecting; active power filter (APF); power quality (PQ); pulse-width-modulated (PWM) converter

1. Introduction

Active power filters (APFs) can be classified into two types according to their grid connection mode: three-phase three-wire (3P3W) and three-phase four-wire (3P4W). The former can only control power quality problems in phase A, B, and C, whereas the latter can also in phase N. Because the low-voltage distribution system is commonly a 3P4W power system along with numerous unbalanced or single-phase harmonic loads, the 3P4W-APF has been more widely utilized in practical applications [1–6].

The power circuit of an APF consists of two main parts: a voltage source converter (VSC) and a grid-connecting interface. According to the structure of the VSC, the 3P4W-APF can be further classified into two types [5,6]: the three-phase, two-split-capacitor type (3P2C) and the three-phase, four-leg type (3P4L), as shown in Figure 1. Compared with the 3P2C-APF, the 3P4L-APF has two key advantages simply at the expense of an additional IGBT in phase N, which include (1) larger current output capacity for its more adequate DC voltage utilization and (2) easy DC-side design and voltage control for its low DC-side current and no need for voltage balancing, such as in the 3P2C. Thus, the 3P4L-APF is more suitable for medium and high-power applications [6]. However, its grid-connecting interface, which connects the VSC and grid utility, is difficult to design because of its higher requirement of current ripple filtering in phase N, cross-coupling in four phases and lack of relevant design methodology and specification. In [5,7–9], the authors conducted various research studies on the three-phase, four-branch APF structure but did not provide an analysis of the above-mentioned issue. Specifically, Sami Pettersson *et al*. adopted the *LCL* interface for phase ABC and the *L* interface for phase N in [5], showing a relatively good filtering effect. However, that study did not provide detailed design steps of decoupling or *LCL* parameters.

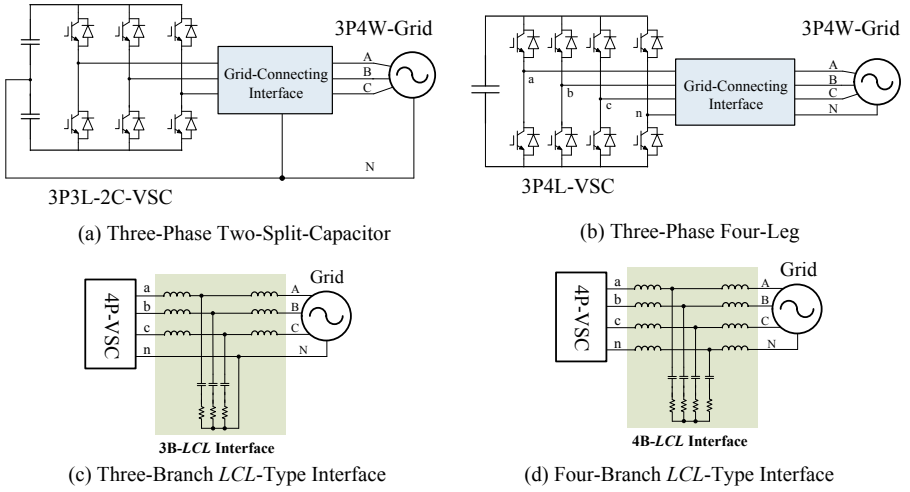


Figure 1. Three-phase, four-wire active power filter and its grid-connecting interface.

There are two common types of grid-connecting interfaces: *L*-type and *LCL*-type [5,10–17], whose functions can be summarized as two aspects: (1) transforming the voltage output from VSC into controllable current injected to the grid with little power loss and (2) filtering out the switching frequency harmonic current from the grid-injecting current, which is caused by the PWM-voltage output of the VSC [18,19]. Compared with the *L*-type grid-connecting interface, the *LCL*-type receives more utilization because it offers better harmonic attenuation and efficiency at a smaller size. The research on current control and design of the *LCL*-type grid-connecting interface in single-phase or three-phase, three-wire applications has been conducted in [20–25]. However, there is little information available describing the systematic design of the *LCL*-type grid-connecting interface for the three-phase, four-wire application, especially for the grid connection of the 3P4L-APF.

In this paper, a four-branch *LCL*-type (*4B-LCL*) grid-connecting interface and detailed parameter design steps are proposed for 3P4L-APF based on mathematical model analysis for decoupling and the most comprehensive performance indexes. Firstly, for removing coupling between each phase, the analysis is processed from the perspective of non-zero-sequence and zero-sequence, respectively. Then, the most comprehensive performance indexes from the designed *LCL* circuit parameters will be obtained in the impedance perspective. Finally, the *4B-LCL* parameter design method based on the most comprehensive performance index is proposed, including three main stages: (1) performance requirements determination; (2) fulfilling the performance requirements and (3) performance requirements verification. The validity and effectiveness of the proposed design are proved by the simulated and experimental results of a 3P4L-APF with *4B-LCL*.

2. System Description and Modeling

2.1. Topology Description

As illustrated in Figure 2, the proposed four-branch *LCL*-type interface connects the *3P4L-VSC* to the grid utility. L_{1abc} and L_{2abc}, denote the converter-side and grid-side *L-R* plant, respectively, in phases A, B, and C. HF_{abc} denotes the filter-side *R-C* plant. L_{1n}, L_{2n} and HF_n denote the corresponding elements in phase N.

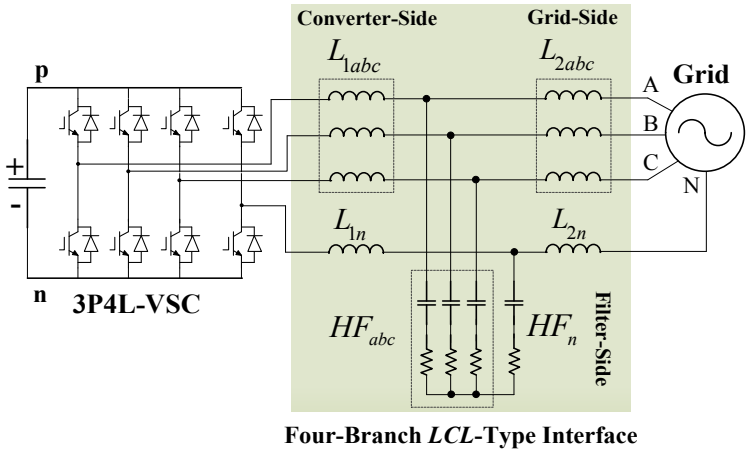


Figure 2. *3P4L-APF* with the proposed *4B-LCL* interface.

The functions of the grid-connecting interface can be summarized into two aspects: (1) transforming the VSC output voltage into controllable current injected to the grid with little power loss, and (2) filtering out the so-called current ripple, which is harmonic current around the integral multiples of the switching frequency and is only caused by the PWM-voltage output of 3P4L-VSC.

Compared with the traditional *3B-LCL* interface, the proposed topology adopts an additional *LCL* branch for phase N, which causes a more satisfactory attenuation effect of current ripple and the decoupling for parameter design in phases A, B, C and N. The related details will be provided below.

2.2. Topology Analysis

Figure 3 illustrates the equivalent circuit for topology analysis. Four controlled voltage sources have replaced the four legs of VSC. The analysis of the circuit will be processed in the *s* domain from two perspectives.

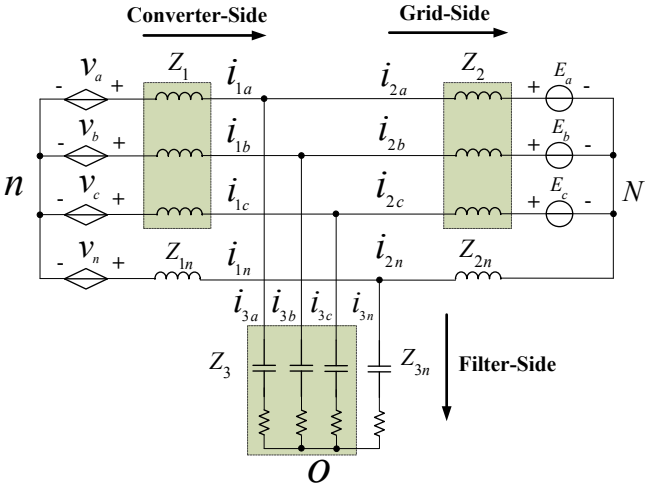


Figure 3. Equivalent circuit.

Z_1 and Z_2 denote the converter-side and grid-side branch impedance, respectively, in phases A, B, and C. Z_{1n} and Z_{2n} denote the converter-side and grid-side branch impedance, respectively, in phase N. Z_3 and Z_{3n} denote the filter-side branch impedance in phases A, B, C and phase N, respectively.

2.2.1. Analysis in the Per-Phase Perspectives

When the voltages between *nO* and *NO* are replaced by the voltage sources U_{nO} and U_{NO}, the equivalent circuit in Figure 3 can be divided into four groups in unified form, as shown in Figure 4.

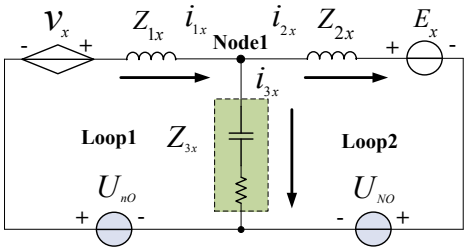


Figure 4. Equivalent circuit in each phase (x = A, B, C, N).

According to the basis theory of circuits, four groups of Equations (1)–(4), can be deduced from Figure 4.

Deduced from Loop 1:

$$\begin{bmatrix} I_{1a}(s)Z_{1a}(s) \\ I_{1b}(s)Z_{1b}(s) \\ I_{1c}(s)Z_{1c}(s) \\ I_{1n}(s)Z_{1n}(s) \end{bmatrix} + \begin{bmatrix} I_{3a}(s)Z_{3a}(s) \\ I_{3b}(s)Z_{3b}(s) \\ I_{3c}(s)Z_{3c}(s) \\ I_{3n}(s)Z_{3n}(s) \end{bmatrix} = \begin{bmatrix} V_a(s) \\ V_b(s) \\ V_c(s) \\ V_n(s) \end{bmatrix} + \begin{bmatrix} U_{nO}(s) \\ U_{nO}(s) \\ U_{nO}(s) \\ U_{nO}(s) \end{bmatrix} \tag{1}$$

Deduced from Loop 2:

$$-\begin{bmatrix} I_{2a}(s)Z_{2a}(s) \\ I_{2b}(s)Z_{2b}(s) \\ I_{2c}(s)Z_{2c}(s) \\ I_{2n}(s)Z_{2n}(s) \end{bmatrix} + \begin{bmatrix} I_{3a}(s)Z_{3a}(s) \\ I_{3b}(s)Z_{3b}(s) \\ I_{3c}(s)Z_{3c}(s) \\ I_{3n}(s)Z_{3n}(s) \end{bmatrix} = \begin{bmatrix} E_a(s) \\ E_b(s) \\ E_c(s) \\ E_n(s) \end{bmatrix} + \begin{bmatrix} U_{NO}(s) \\ U_{NO}(s) \\ U_{NO}(s) \\ U_{NO}(s) \end{bmatrix} \tag{2}$$

Deduced from Node 1:

$$\begin{bmatrix} I_{2a}(s) \\ I_{2b}(s) \\ I_{2c}(s) \\ I_{2n}(s) \end{bmatrix} = \begin{bmatrix} I_{1a}(s) \\ I_{1b}(s) \\ I_{1c}(s) \\ I_{1n}(s) \end{bmatrix} - \begin{bmatrix} I_{3a}(s) \\ I_{3b}(s) \\ I_{3c}(s) \\ I_{3n}(s) \end{bmatrix} \tag{3}$$

Deduced from Nodes n, o, and N:

$$\begin{bmatrix} I_{1a}(s) \\ I_{2a}(s) \\ I_{3a}(s) \end{bmatrix} + \begin{bmatrix} I_{1b}(s) \\ I_{2b}(s) \\ I_{3b}(s) \end{bmatrix} + \begin{bmatrix} I_{1c}(s) \\ I_{2c}(s) \\ I_{3c}(s) \end{bmatrix} = -\begin{bmatrix} I_{1n}(s) \\ I_{2n}(s) \\ I_{3n}(s) \end{bmatrix} \tag{4}$$

Equations (1) and (2) illustrate that U_{nO} and U_{NO} cause coupling between each phase. Thus, the equivalent circuit in Figure 4 is not suitable for the design of *LCL* parameters and grid-injecting current control.

2.2.2. Analysis in the Non-Zero-Sequence and Zero-Sequence Perspectives

To remove U_{nO} and U_{NO} for decoupling, the analysis is processed from the perspectives of non-zero-sequence and zero-sequence, respectively.

The complex vector s-transfer function in Equation (5) for describing the non-zero-sequence circuit can be obtained by conducting symmetrical parameter design in phase ABC and substituting the Clarke transformation matrix 2/3 [1, $e^{j2\pi/3}$, $e^{-j2\pi/3}$] into both sides of Equations (1)–(3).

$$\begin{cases} I_1(s)Z_1(s)+I_3(s)Z_3(s)=V(s) \\ -I_2(s)Z_2(s)+I_3(s)Z_3(s)=E(s) \\ I_2(s)=I_1(s)-I_3(s) \end{cases} \tag{5}$$

where

$$Z_1(s)=Z_{1a}(s)=Z_{1b}(s)=Z_{1c}(s)$$
$$Z_2(s)=Z_{2a}(s)=Z_{2b}(s)=Z_{2c}(s)$$
$$Z_3(s)=Z_{3a}(s)=Z_{3b}(s)=Z_{3c}(s)$$

From Equations (1)–(4), the real s-transfer function for the zero-sequence circuit can be obtained as shown in Equation (6).

$$\begin{cases} I_{1n}(s)Z_{1n\_eq}(s)+I_{3n}(s)Z_{3n\_eq}(s)=V_{n\_eq}(s) \\ -I_{2n}(s)Z_{2n\_eq}(s)+I_{3n}(s)Z_{3n\_eq}(s)=-E_0(s) \\ I_{2n}(s)=I_{1n}(s)-I_{3n}(s) \end{cases} \quad (6)$$

where

$$V_{n\_eq}(\mathrm{s})=V_n(\mathrm{s})-V_0(\mathrm{s})$$
$$Z_{xn\_eq}(\mathrm{s})=Z_x(\mathrm{s})/3+Z_{xn}(\mathrm{s}) \quad (x=1,2,3)$$

From Equations (5) and (6), two independent equivalent circuits have been obtained, as illustrated in Figure 5. U_{nO} and U_{NO} have disappeared, which brings the decoupling of each phase. In addition, the left of Figure 5b shows that the additional *LCL* branch for phase N brings the design of the zero-sequence circuit independent from the non-zero-sequence. Thus, the design of the 4-branch *LCL* parameter and 4-phase grid-injecting current control becomes the design simply for two independent equivalent circuits in the non-zero-sequence and zero-sequence.

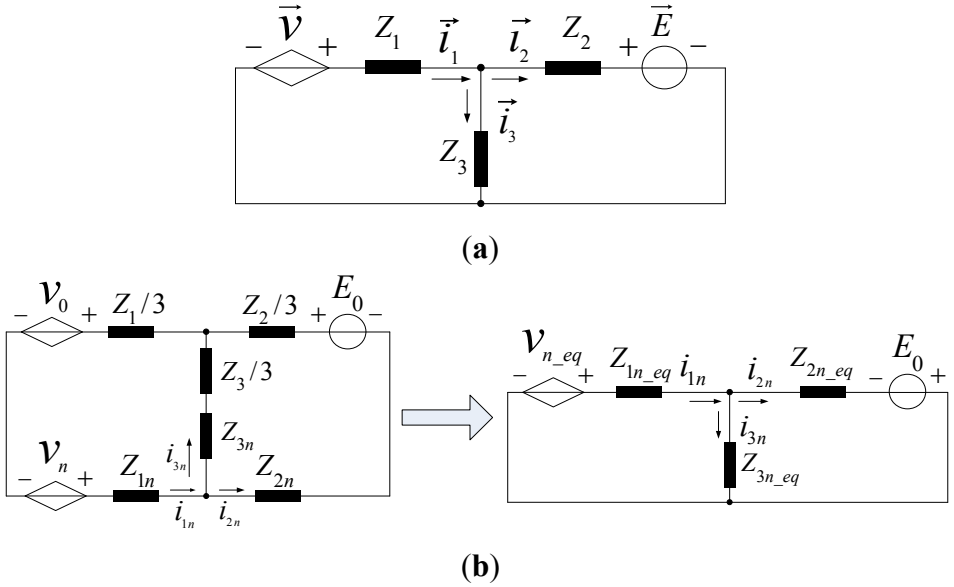


Figure 5. Equivalent circuit in (**a**) the non-zero-sequence and (**b**) zero-sequence.

2.3. Model for Parameter Design

Figure 6 illustrates two s-transfer function blocks deduced from the two independent equivalent circuits in Figure 5. When the real signal in the zero-sequence block was regarded as a special complex

signal whose imaginary part always equals zero, the two blocks can be entirely in the same style with the unified complex vector form. Furthermore, the s-transfer function matrix can be obtained for the analysis of the characteristic of the *LCL* circuit, which will be shown in next section.

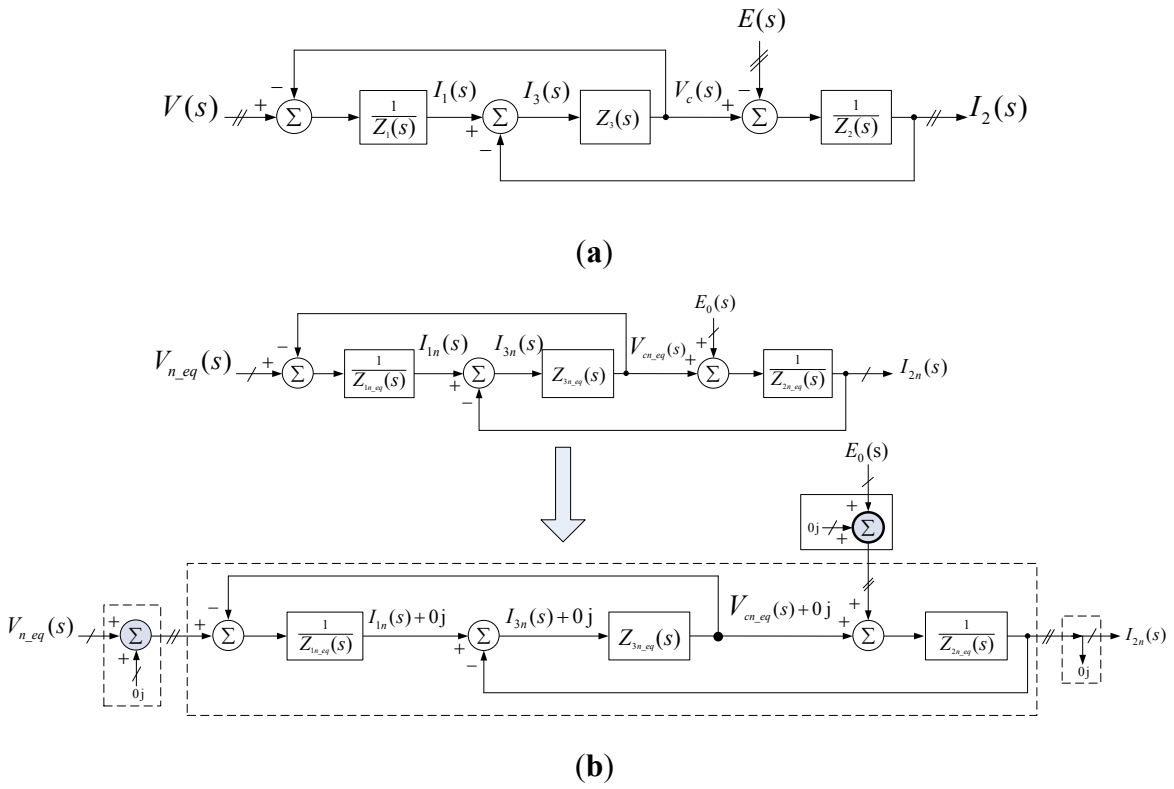


Figure 6. 4B-*LCL* model in the (**a**) non-zero-sequence and (**b**) zero-sequence.

3. Parameter Design

3.1. Circuit Characteristic

The s-transfer function for Matrixes (7) and (8) are deduced from the 4B-*LCL* complex vector model in the non-zero-sequence and zero-sequence in Figure 6. Because the zero-sequence grid voltage equals approximately zero in practical situations, the zero-sequence concerned is not included in Matrix (8).

$$\begin{bmatrix} I_1(s) \\ I_2(s) \\ I_3(s) \end{bmatrix} = \begin{bmatrix} \dfrac{1}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} & \dfrac{\left(1+\dfrac{Z_1(s)}{Z_3(s)}\right)}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} \\ \dfrac{\left(1+\dfrac{Z_2(s)}{Z_3(s)}\right)}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} & \dfrac{1}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} \\ \dfrac{\dfrac{Z_2(s)}{Z_3(s)}}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} & \dfrac{\dfrac{Z_1(s)}{Z_3(s)}}{\{Z_1(s)+Z_2(s)\}\left(1+\dfrac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)} \end{bmatrix} \begin{bmatrix} V(s) \\ -E(s) \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} I_{1n}(s) \\ I_{2n}(s) \\ I_{3n}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{1}{\left\{Z_{1n\_eq}(s)+Z_{2n\_eq}(s)\right\}\left(1+\dfrac{Z_{1n\_eq}(s)//Z_{2n\_eq}(s)}{Z_{3n\_eq}(s)}\right)} \\ \dfrac{\left(1+\dfrac{Z_{2n\_eq}(s)}{Z_{3n\_eq}(s)}\right)}{\left\{Z_{1n\_eq}(s)+Z_{2n\_eq}(s)\right\}\left(1+\dfrac{Z_{1n\_eq}(s)//Z_{2n\_eq}(s)}{Z_{3n\_eq}(s)}\right)} \\ \dfrac{\dfrac{Z_{2n\_eq}(s)}{Z_{3n\_eq}(s)}}{\left\{Z_{1n\_eq}(s)+Z_{2n\_eq}(s)\right\}\left(1+\dfrac{Z_{1n\_eq}(s)//Z_{2n\_eq}(s)}{Z_{3n\_eq}(s)}\right)} \end{bmatrix} V_{n\_eq}(s) \quad (8)$$

where

$$Z_1(s) = L_1 s + R_1,\ Z_2(s) = L_2 s + R_2,\ Z_3(s) = 1/Cs + R$$

Because the s-transfer functions in Matrixes (7) and (8) have a unified form, only the former one has been considered in the circuit characteristic analysis. The bode plots shown in Figure 7 are obtained from Matrix (7), in which L_1 = 0.23 mH, L_2 = 0.03 mH, C = 30 μF, and R = 0.1 Ω. The two amplitude-frequency curves have the same shape, sharing characteristics of three stages: an initial decrease, followed by an increase and sharp decrease, and finally a continuous decrease.

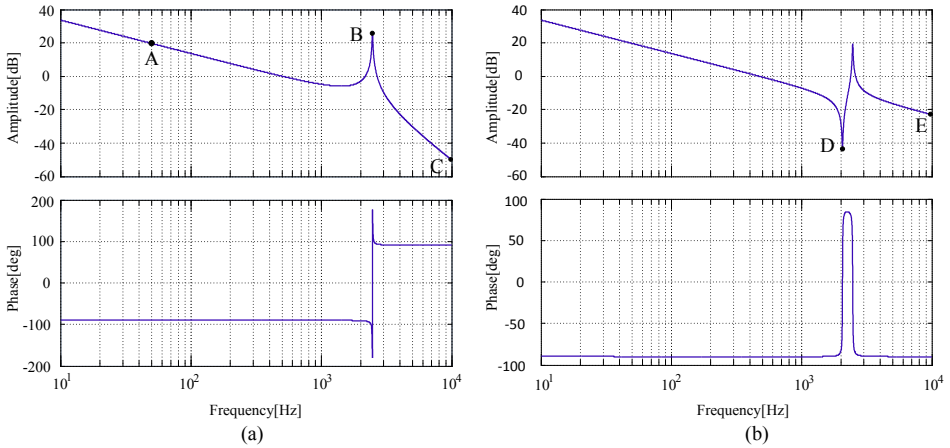


Figure 7. Bode diagrams (**a**) $I_2(s)/V(s)$, (**b**) $I_1(s)/V(s)$.

Five points will be illustrated in detail as follows; whose values alone fully indicate the performance of the designed LCL circuit. In Figure 7a, point A is in the fundamental frequency corresponding position. Point B is in the peak position. Point C is in the switching frequency position. In Figure 7b, Point D is in the lowest position of the curve. Point E is in the switching frequency position. Two events have occurred in Points B and D, which are the so-called series resonance and parallel resonance. To combine the qualitative and quantitative analyses, four types of impedance s-transfer functions are introduced for further analysis in Equations in (9)–(11).

$$G_{11}(s)=\frac{\{Z_1(s)+Z_2(s)\}\left(1+\frac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)}{\left(1+\frac{Z_2(s)}{Z_3(s)}\right)} \tag{9}$$

$$G_{22}(s)=\frac{\{Z_1(s)+Z_2(s)\}\left(1+\frac{Z_1(s)//Z_2(s)}{Z_3(s)}\right)}{\left(1+\frac{Z_1(s)}{Z_3(s)}\right)} \tag{10}$$

$$G_{12}(s)=G_{21}(s)=\{Z_1(s)+Z_2(s)\}\left(1+\frac{Z_1(s)//Z_2(s)}{Z_3(s)}\right) \tag{11}$$

G_{11} is the impedance between the PWM voltage and converter-side current, referred to as the converter-side impedance. G_{22} is the impedance between the grid-voltage and grid-side current, named grid-side impedance. G_{12} is the impedance between the PWM voltage and grid-side current. G_{21} is the impedance between the grid-voltage and converter-side current. Because of the symmetry of the *LCL* circuit, the impedance G_{21} equals G_{12}. Thus, G_{21} and G_{12} are both named the dual-side impedance.

In the proposed impedance perspective, the most comprehensive performance indexes from the designed *LCL* circuit parameters (L_1, L_2, C, and R) are described in detail below:

(1) Dual-side impedance amplitude within the output current frequency band:

$$P_1=\left|G_{12}\right|_{s=\mathrm{j}n\omega_1}\approx\left|\{Z_1(s)+Z_2(s)\}\right|_{s=\mathrm{j}n\omega_1}\approx(L_1+L_2)n\omega_1\quad(n=1,2,3...N) \tag{12}$$

This index in (12) (where N is the highest order of the output current frequency) indicates the capacity of an APF with a finite DC voltage and a certain grid voltage at the aspect of the output current's di/dt, which is referred to as the APF output capacity [12]. A lower impedance amplitude value indicates a higher APF output capacity, and *vice versa*. In the frequency domain, lower impedance amplitude means higher capacity in outputting high-order frequency current in some other conditions [19]. Because the impedance amplitude is proportional to its frequency within the output current frequency band, the dual-side impedance amplitude in the fundamental frequency is selected for this performance index in practical use, which is $(L_1 + L_2)\omega_1$. A certain APF output capacity requirement corresponds to its upper limit value.

(2) Dual-side impedance amplitude in the switching frequency:

$$P_2=\left|G_{12}\right|_{s=\mathrm{j}\omega_s}\approx\left|\{Z_1(s)\,Z_2(s)/Z_3(s)\}\right|_{s=\mathrm{j}\omega_s}\approx L_1L_2C\omega_s^3 \tag{13}$$

This index indicates the content of the grid-side current ripple produced by a certain PWM voltage. A smaller grid-side current ripple results in a better performance of the designed *LCL* [25]. Thus, this principal and critical index should be kept larger than a lower limit.

(3) Converter-side impedance amplitude in the switching frequency:

$$P_3=\left|G_{11}\right|_{s=\mathrm{j}\omega_s}\approx\left|Z_1(s)\right|_{s=\mathrm{j}\omega_s}\approx L_1\omega_s \tag{14}$$

This index indicates the content of the converter-side current ripple produced by a certain PWM voltage. Although the converter-side current ripple will be mostly filtered out from injecting into the grid by the filter-side *RC*-plant (as shown in Figure 8), it is related to some practical considerations:

the maximum current of the semiconductor switching devices, the saturation characteristic of the inverter-side inductance, the EMI of the APF, and so on [25]. Thus, this index should be kept larger than a lower limit as well.

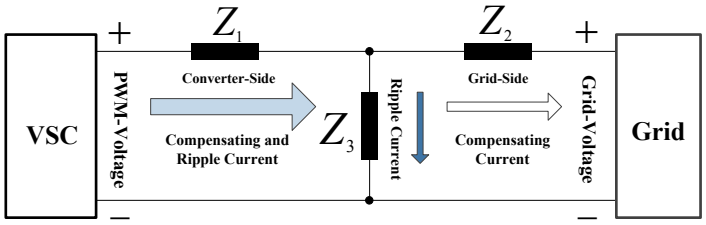


Figure 8. Diagram of the current flow path in the LCL circuit.

(4) Series resonant frequency:

$$\omega_{res} = \sqrt{\frac{1}{L_p C}} \tag{15}$$

where $L_p = L_1L_2/(L_1 + L_2)$

The index indicates the same series resonant event in both sides of the *LCL* circuit, which can be considered as the frequency in which the numerator term $Z_p(s) + Z_3(s)$ in Equations (9)–(11) becomes a real resistor impendence. The index should be selected between the output current upper-limit frequency and half of the controller sampling frequency, which is half of or equal to the switching frequency. In [9], the recommended value is $2\omega_n < \omega_{res} < 0.5\omega_s$.

(5) Parallel resonant frequency:

$$\omega_{01} = \sqrt{\frac{1}{L_2 C}} \tag{16}$$

$$\omega_{02} = \sqrt{\frac{1}{L_1 C}} \tag{17}$$

The indexes in Equations (16) and (17) indicate the two parallel resonant events on the converter side and grid side of the *LCL* circuit, which can be considered as the frequency where the denominator terms $Z_2(s) + Z_3(s)$ and $Z_1(s) + Z_3(s)$ in Equations (9)–(10) become a real resistor impendence. Because the direct grid-side current control is adopted commonly, only the index in Equation (17) needs to be considered. A lower index indicates that the high-order background harmonics of the grid voltage have a greater influence over the current controller [19]. Thus, the index should be kept larger than a lower limit value.

(6) Filter-side impedance amplitude in the fundamental frequency:

$$P_4 = \left|Z_3(s)\right|_{s=j\omega_1} \approx \frac{1}{C\omega_1} \tag{18}$$

This index indicates the content of the main fundamental frequency component in the filter-side current produced by the grid voltage, which also mainly consists of the fundamental frequency

component. A higher impedance amplitude leads to a lower filter-side current. Thus, this index should be restricted to limit the power loss in the filter-side branch.

(7) Dual-side impedance amplitude in the series resonant frequency:

$$P_5 = \left|G_{12}\right|_{s=j\omega_{res}} \approx (L_1 + L_2)CR\omega_{res}^2 = R/(1-\alpha)/\alpha \tag{19}$$

where $\alpha = L_1/(L_1 + L_2)$

This index indicates the damping effect of the designed *LCL* circuit directly. A higher impedance amplitude results in a lower peak value of the amplitude-frequency curve in the Bode plots and thus a stronger damping effect. The index is determined by the series resistance *R* if the total inductance and the capacitance C have been determined. In [25], the recommended value is $R < 1/3/C/\omega_{res}$.

3.2. Design Procedure

The most comprehensive performance indexes have been obtained above. The essential aspect of the *LCL* parameter design is to meet the performance requirements. Generally, a good performance index will inevitably increase the cost, size, and weight of the *LCL* components (L_1, L_2, C or R). Hence, a compromise should be made to keep a balance between performance and cost, size, and weight.

The algorithm for designing the *LCL* circuit is shown in Figure 9. It contains three tasks: determining the performance index, meeting the performance requirement and verifying the performance index.

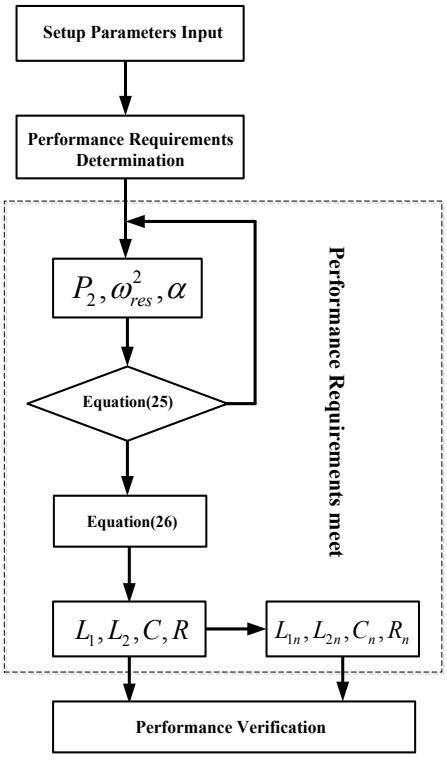


Figure 9. Flowchart of the *LCL* design.

3.2.1. Determination of the Performance Requirements

(1) Calculate the maximum limitation of P_1 which is determined by the total inductance $L = L_1 + L_2$. To ensure the rated current output capacity of the APF, the following inequality should be satisfied:

$$I_{rms}P_1 \le mV_{dc} - nE_{rms} \tag{20}$$

where I_{rms} is the rated output current of the APF, E_{rms} is the rms of the grid rated line voltage, n is the ratio of voltage fluctuation (generally 5%–10%), V_{dc} is the DC-side voltage, and m is the ratio of DC voltage utilization, which is determined by the adopted PWM strategy (e.g., $1/2/\sqrt{2}$ if the per-phase PWM strategy is adopted, $1/\sqrt{3}/\sqrt{2}$ if the space vector PWM strategy is adopted).

(2) Estimate the maximum value of the PWM voltage ripple in the switching frequency denoted by V_r and further calculate the limitations of P_2 and P_3 according to Equation (21). The maximum values of the converter-side and grid-side current ripple in the switching frequency are denoted by I_{r1} and I_{r2}. There are various harmonic components in the PWM voltage. The high-frequency harmonic components, which are determined by the type of modulation, DC link voltage, and waveform of the PWM reference voltage (e.g., modulation index), appear on switching and its multiple frequencies, and the uppermost component is around the switching frequency [9]. V_r can also be obtained from the simulation of a practical situation.

$$\begin{cases} V_r / P_3 \le I_{r1} \\ V_r / P_2 \le I_{r2} \end{cases} \tag{21}$$

(3) Determine the range of the series and parallel resonant frequency, which is shown in Equation (22). ω_{gh} is the highest frequency of the grid background harmonics voltage.

$$\begin{cases} 2\omega_n < \omega_{res} < 0.5\omega_s \\ 2\omega_{gh} < \omega_{02} \end{cases} \tag{22}$$

(4) Determine the range of the R and C in the filter-side branch according to P4 and P5. I_{c1} is the maximum fundamental frequency current in the filter-side branch, which is caused by the grid. P5 should be above one for the close-loop control stability [12]. Thus, the range of R is obtained via Equation (24).

$$E_1 / P_4 < I_{c1} \tag{23}$$

$$\alpha(1-\alpha) < R < \frac{1}{3C\omega_{res}} \tag{24}$$

3.2.2. Meeting the Performance Requirements

The inequality in Equation (25) can be obtained based on Equations (20)–(24). According to the flowchart of the *LCL* design in Figure 9, the *LCL* parameters can be determined by a simple trial-and-error process. The essential aspect of the process is utilizing the performance indexes P_2, ω_{res} and α to deduce the proper L_1, $L2$, C, R that can meet the inequality in Equation (25) and reach the optimal target, which is to maximize P_2/L.

$$\begin{cases} P_2 \geq P_{2\min} \\ \dfrac{1}{4\omega_n^2} \geq \omega_{res}^2 \geq \dfrac{4}{\omega_s^2} \\ 1 > \alpha \geq 0.5 \\ \\ P_1 = \omega_{res}^2 P_2 (\dfrac{\omega_1}{\omega_s^3}) \leq P_{1\max} \\ P_3 = \omega_{res}^2 P_2 \alpha (\dfrac{1}{\omega_s^3}) \geq P_{3\min} \\ P_4 = \alpha(1-\alpha)\omega_{res}^4 P_2 (\dfrac{1}{\omega_s^3 \omega_1}) \geq P_{4\min} \\ \omega_{01}^2 = \omega_{res}^2 (1-\alpha) \geq 4\omega_{gh}^2 \end{cases} \tag{25}$$

$$\begin{cases} L_1 = \omega_{res}^2 P_2 \alpha (\dfrac{1}{\omega_s^3}) \\ L_2 = \omega_{res}^2 P_2 (1-\alpha) (\dfrac{1}{\omega_s^3}) \\ C = \dfrac{\omega_s^3}{\alpha(1-\alpha)\omega_{res}^4 P_2} \\ \dfrac{1}{3C\omega_{res}} > R > \alpha(1-\alpha) \end{cases} \tag{26}$$

3.2.3. Verification of the Performance Index

The *LCL* performance index output table should be contained in an integral *LCL* design procedure for the design specification. Additionally, the selected parameters in a practical situation may differ from the calculated ones. Thus, a practical performance index output table is necessary.

4. Simulation

The simulation model is established in MATLAB/Simulink. The purpose of the simulation is to verify the current ripple filtering effect of the designed *4B-LCL*; therefore, it is carried out by the open-loop method excluding the APF's controller. The parameters of the designed *4B-LCL* are obtained by the method mentioned above. All simulation parameters are shown in Tables 1–4.

Table 1. Setup parameters.

Symbol	Quantity	Value
E_{rms}	Phase grid voltage	200–240 V
f_{gh}	Highest background voltage harmonics frequency	550 Hz
h	Highest frequency order of the output current harmonics	20
m	DC Voltage Utilization Ratio	$1/\sqrt{3}/\sqrt{2}$
V_{dc}	DC Link Voltage	800 V
f_s	Switching Frequency	10 KHz
I_{rms}	Rated Output Current in phases A, B, C, and N	100 A
I_{r1}	Converter-side current ripple rms in phases A, B, C, and N	≤12 A
I_{r2}	Grid-side current ripple rms in phases A, B, C, and N	≤1 A

Table 2. Table of performance requirements in phases A, B, C, and N.

Symbol	Quantity	Value
P_1	Dual-side impedance amplitude in the fundamental frequency	≤0.87 Ω
P_2	Dual-side impedance amplitude in the switching frequency	≥295.2 Ω
P_3	Converter-side impedance amplitude in the switching frequency	≥10.0 Ω
P_4	Filter-side impedance amplitude in the fundamental frequency	≥40.0 Ω
P_5	Dual-side impedance amplitude in the series resonant frequency	approximately 1.0 Ω
f_{res}	Dual-side series resonant frequency	[2.0 KHz, 5.0 KHz)
f_{01}	Grid-side parallel resonant frequency	[1.1 KHz, f_{res})

Table 3. Parameters selected and its performance index in phases A, B, and C.

Symbol	Quantity	Value: the selected (the calculated)
L_1	Converter-side inductance	0.23 mH (0.273 mH)
L_2	Grid-side inductance	0.10 mH (0.086 mH)
C	Filter-side capacitance	60 μF (56.92 μF)
R	Filter-side resistance	0.2 Ω (0.196 Ω)
P_1	Performance Index Output in phases A, B, and C	0.1 Ω
P_2		301.0 Ω
P_3		14.2 Ω
P_4		53.1 Ω
P_5		0.93 Ω
f_{res}		2.46 KHz
f_{01}		2.05 KHz

Table 4. Parameters selected and its performance index in phase N.

Symbol	Quantity	Value: the selected (the calculated)
L_{1n}	Converter-side inductance	0.32 mH (0.312 mH)
L_{2n}	Grid-side inductance	0.14 mH (0.138 mH)
C_n	Filter-side capacitance	42 μF (41.74 μF)
R_n	Filter-side resistance	0.15Ω (0.145 Ω)
L_{1n_eq}	Equivalent Value in phase N	0.40 mH
L_{2n_eq}		0.16 mH
C_{n_eq}		33.53 μF
R_{n_eq}		0.21 Ω
P_{1n}	Performance Index Output in phase N	0.028 Ω
P_{2n}		559.4 Ω
P_{3n}		19.2 Ω
P_{4n}		94.88 Ω
P_{5n}		1.23 Ω
f_{res_n}		2.53 KHz
f_{01_n}		2.21 KHz

4.1. Current Ripple Filtering in Different PWM Voltage Modulation Indexes

Table 5 illustrates that the magnitude of the switching frequency output voltage ripples is inversely proportional to the modulation index. With the increase of the modulation index, the grid-side current ripple of the switching frequency was reduced steadily. When the index is 1.0, by installing the proposed 4B-LCL interface, the switching frequency ripple currents in phases A and N have been reduced from 12.13 A and 20.65 A to 0.21 A and 0.84 A, respectively, which has provided great filtering results.

Table 5. Results of the current ripple filtering in different PWM voltage modulation indexes.

PWM Voltage		Switching frequency current rms/A		Damping resister power loss (w)
Modulation index	**Switching frequency voltage**	**Converter-side (A,N)**	**Grid-side (A,N)**	
0.0	357.93, 600.93	90.04, 120.33	4.09, 6.04	1632 W
0.2	300.12, 463.46	60.02, 98.12	3.09, 5.83	800 W
0.4	260.34, 300.62	50.17, 70.58	2.09, 3.92	300 W
0.6	190.83, 263.91	30.18, 50.11	1.09, 1.93	93 W
1.0	90.34, 220.46	12.13, 20.65	0.21, 1.19	21 W

Figure 10 shows the simulation waveforms indicating the ripple current filtering effect by the designed *4B-LCL* interface.

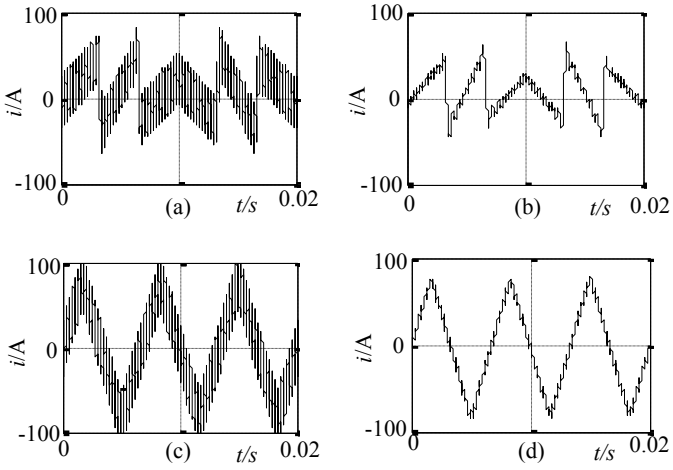


Figure 10. Comparison between converter-side and grid-side current in phases A and N. (**a**) and (**c**) show the current waveforms in the converter side in phases A and N. (**b**) and (**d**) show the current waveforms in the grid side in phases A and N. The figure clearly shows the filtering effect by the proposed 4B-LCL interface. The grid-side current waveform is considerably smoother than that of the converter side.

4.2. Current Ripple Filtering by the LCL Branch in Phase N

Figure 11 shows the grid-side current waveforms of phase N at the *RC*-plant switching time. It can be seen that i_{sa} and i_{sn} have many high frequency current ripples before the *RC*-plant in n-phase has been switched on, but the high frequency current ripples have almost disappeared after it has been switched on. In particular, the current ripple in i_{sn} has been decreased from 10 A–0.9 A. This result verifies the good effect on current ripple filtering of the *LCL*-branch in phase N.

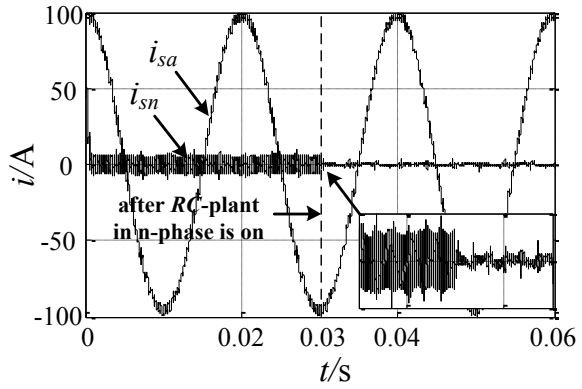


Figure 11. Comparison with and without the *LCL* branch in phase N.

5. Experimental Results

5.1. Experimental Platform

Figure 12a shows the experimental platform, where SKM400GB176D from SEMIKRON was selected as the power module IGBT, and TMS320F28335 from Texas Instruments was selected as

the main controller chip for digital signal processing. In addition, the platform has adopted the power quality analyzer (Fluke 434B) and Oscilloscope (Tektronix 2024B) as measurement instruments in Figure 12b,c. The actual *4B-LCL* circuit implemented is shown in Figure 13.

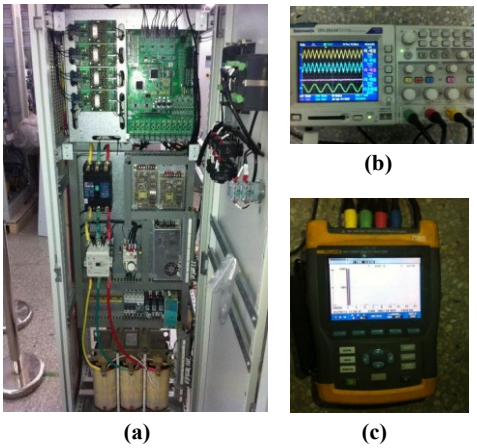


Figure 12. Experimental platform and measurement instruments.

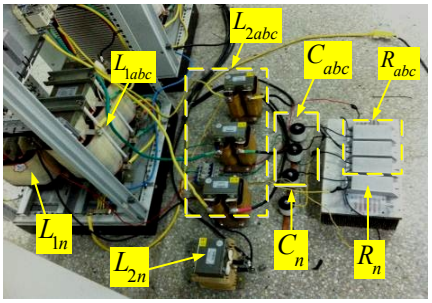


Figure 13. Implemented *4B-LCL* circuit.

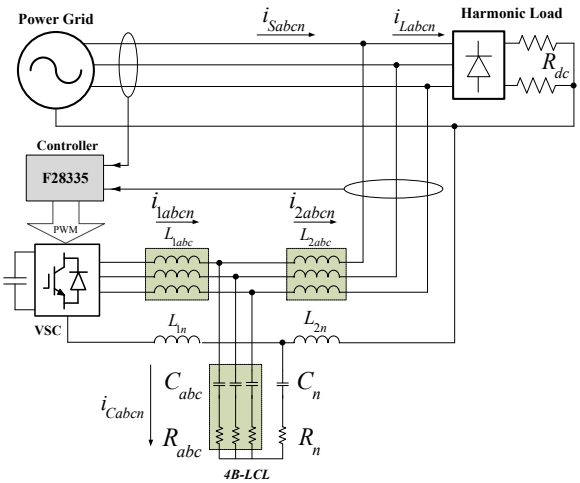


Figure 14. Experimental system.

The experimental system consists of the controller, voltage source converter (VSC), harmonic load, three-phase four-wire power grid, and proposed four-branch (4B) *LCL* grid-connecting interface, as shown in Figure 14. The APF controller sampled the grid-side current to directly regulate the output current,

which is injected into the grid to fully compensate for the load current harmonics. The harmonic load was modified from the typical three-phase uncontrolled rectifier bridge, where the midpoint of the resistors on the DC side was connected to phase N of the power grid for the purpose of getting the current harmonics in this phase. In addition, the parameters of the experiment are the same as in the simulation above.

5.2. Experimental Results

5.2.1. Current Ripple Filtering

Figure 15a,b show the current waveforms of the proposed *4B-LCL* in phase A and N, when the APF is fully compensating the load current harmonics. In this figure, I_{1a} & I_{1n}, I_{Ca} & I_{Cn}, I_{2a} & I_{2n}, and E_{an} are the converter-side current, filter-side current, grid-side current, and grid voltage, respectively, between phases A and N. Because the three phases are symmetric, it is not necessary to demonstrate the waveforms in phases B and C. These waveforms illustrate that I_{1a} & I_{1n} have a massive high-frequency current ripple, which has been filtered out into I_{ca} & I_{cn}. I_{2a} & I_{2n} have a smoother waveform than I_{1a} & I_{1n}. Furthermore, Figure 15c is a zoomed-in view of the dashed box in Figure 15. The period of the high-frequency ripple wave in I_{1n} and I_{Cn} is approximately 0.1 ms (which is just the switching period of IGBT), and their amplitudes are nearly identical. The current ripple of the grid-side current I_{2n} has been greatly reduced, and the waveform of the grid voltage E_{an} is also extremely smooth. Therefore, the designed *4B-LCL* has obtained a good performance in the current ripple filtering.

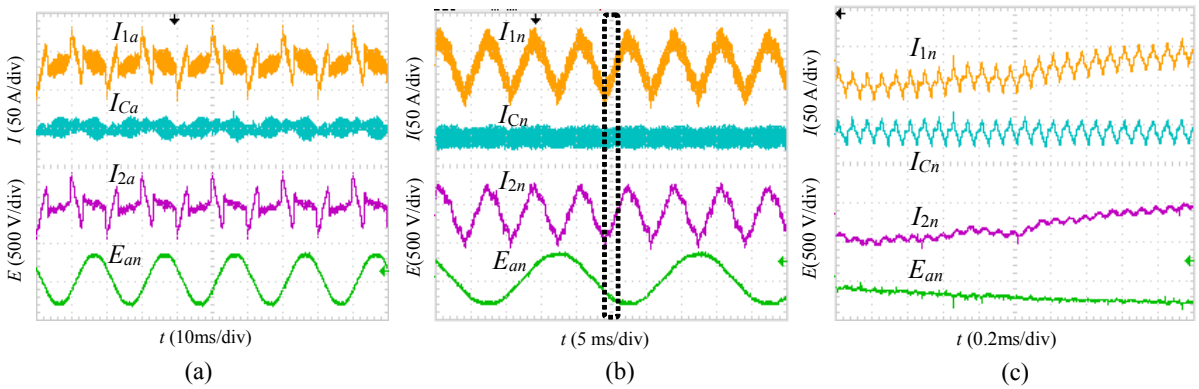


Figure 15. Waveforms of the *4B-LCL* (**a**) in phase A (**b**) in phase N (**c**) Zoomed-in view.

Figure 16a,b show the FFT results of the converter-side and grid-side current in phase N. A large amount of current ripples around the switching frequency are contained in the converter-side current. The ripple content reaches approximately 32 dB at the switching frequency *fs* and 3*fs*, whereas that in the grid-side current has been evidently reduced to approximately 10 dB around f_s and to a negligible level around other integral multiples of f_s. This experimental result has further verified the current ripple reduction effect in phase N of the designed *4B-LCL* circuit.

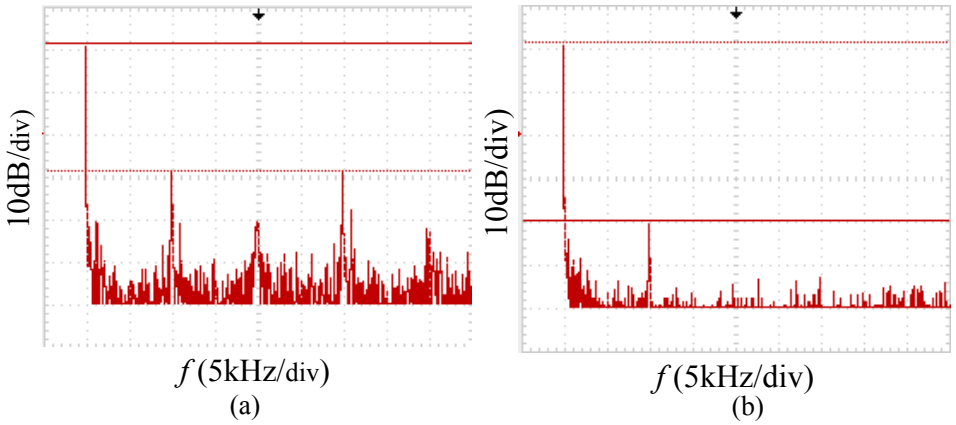


Figure 16. FFT of the current in phase N (**a**) converter-side (**b**) grid-side.

5.2.2. Harmonic Compensation

Figure 17a,b are the current waveforms in phase A and N when the APF is fully compensating the load current harmonics. I_{La} & I_{Ln}, I_{2a} & I_{2n}, I_{Sa} & I_{Sn} are the load current, compensating current, and grid current, respectively, in phases A and N. E_{an} is the grid voltage between phases A and N. In Figure 17a, the load current I_{La} is considerably distorted. However, the grid current I_{Sa} has a good sinusoidal waveform due to the compensating current I_{2a}. In Figure 17b, the period of the load current I_{Ln} in phase N is approximately 7 *ms*, which indicates the existence of a large amount of the third harmonic current. The compensating current I_{2n} from the APF almost equals the lode current I_{Ln} in both amplitude and phase. Thus, the grid current in phase N is approximately zero, which means that the current harmonics in phase N are well compensated.

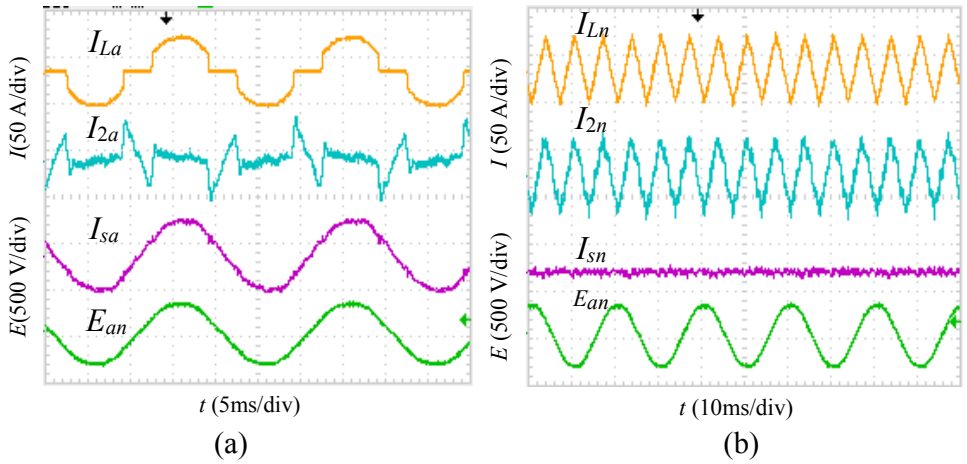
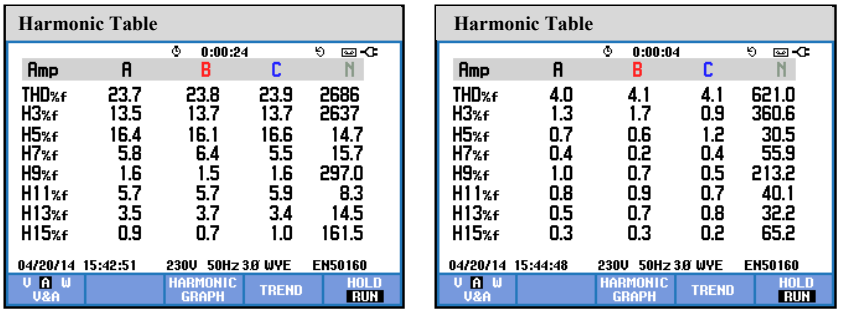


Figure 17. Waveforms in harmonic compensation (**a**) in phase A (**b**) in phase N.

Figure 18a,b shows the THD and ratio of harmonic frequency content in the load current and grid current. The current THD dropped from 23.7%, 23.8%, and 23.9% in the load current to 4.0%, 4.1%, and 4.1%, respectively, in the grid current. The experimental result has met the requirement of THD in GB/T 14549-93. Each frequency harmonic distortion has dropped from over 1% in the load current to below 1% in the grid current. The good harmonic compensation result has further verified the effectiveness of the designed 4B-*LCL* grid-connecting interface.



(a) (b)

Figure 18. Harmonic forms of the (**a**) load current and (**b**) grid current.

6. Conclusions

Based on an analysis via mathematical models for decoupling and the most comprehensive performance indexes in the proposed impedance perspective, this paper has proposed a four-branch *LCL*-type grid-connecting interface and detailed parameter design procedure for a three-phase, four-leg active power filter. This paper focuses on two aspects: (1) describing the mathematical models of *4B-LCL* in the full complexity vector form from the zero and non-zero sequence perspectives, resulting in two independent and uniform equivalent circuits without cross-coupling terms; (2) proposing the *4B-LCL* parameter design method based on the most comprehensive performance index, including three main stages as the specification: performance requirements determination, fulfillment and verification. The Simulink results established in MATLAB and the experimental results obtained from the APF platform with the 4B-LCL type grid-connecting interface demonstrate that the 4B-LCL interface yields better current ripple filtering performance, which verifies the validity and effectiveness of the proposed design method.

Acknowledgments

This work is supported in part by grants from the National Natural Science foundation of China (Project No. 51477030), Innovation foundation for Combination of Industry and Scientific Research of Jiangsu Province, China (Project No. BY2014127-15).

Author Contributions

Wu Cao and Jianfeng Zhao designed the research; Wu Cao and Kangli Liu performed the research; Wu Cao, Yongchao Ji and Yigang Wang wrote the paper. All authors read and approved the final manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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