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Article

Voltage Support Provided by STATCOM in Unbalanced Power Systems

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Abstract: The presence of an unbalanced voltage at the point of common coupling (PCC) results in the appearance of a negative sequence current component that deteriorates the control performance. Static synchronous compensators (STATCOMs) are well-known to be a power application capable of carrying out the regulation of the PCC voltage in distribution lines that can suffer from grid disturbances. This article proposes a novel PCC voltage controller in synchronous reference frame to compensate an unbalanced PCC voltage by means of a STATCOM, allowing an independent control of both positive and negative voltage sequences. Several works have been proposed in this line but they were not able to compensate an unbalance in the PCC voltage. Furthermore, this controller includes aspects as antiwindup and droop control to improve the control system performance.

Keywords: PCC voltage control; STATCOM; unbalanced voltage

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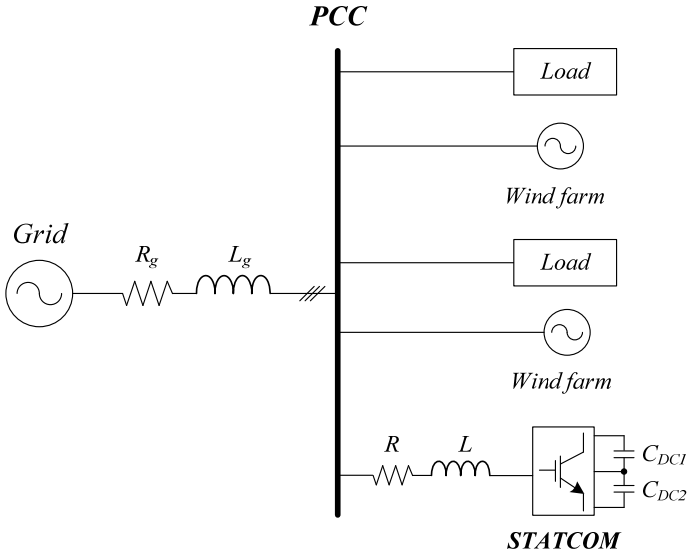
1. Introduction

The ongoing large-scale integration of wind energy into the power system demands the continuous revision of grid codes and power quality standards in order to fulfill restrictive constraints. Furthermore, most host utilities also require that wind farms must tolerate system disturbances [1]. These requirements become of paramount importance in remote locations where the feeders are long and operated at a medium voltage level, providing a weak grid connection. The main feature of this type of connection is the increased voltage regulation sensitivity to changes in load [2]. Thus, the system's ability to regulate voltage at the point of common coupling (PCC) to the electrical system is a key factor for the successful operation of the wind farm [3], even in the face of voltage flicker caused by wind gusts or post fault electromechanical swings in the power grid [1].

Nowadays, there are grid operators that allow providing unbalanced currents so that the power at the PCC remains constant. This is very useful in weak grids because it allows connecting all loads to a balanced PCC voltage, which is especially important for sensitive loads that could disconnect if the AC voltage does not meet restrictive voltage standards.

This task can be accomplished by means of a STATCOM, which is a Voltage-Source Converter (VSC) system whose prime function is to exchange reactive power with the host AC system [4] and control the power factor. In a distribution system, it is mainly used for voltage regulation [5]. This has a major application in weak grids, whose significant grid impedance may lead to large PCC voltage variations compared to that of strong grids. The general system under investigation is shown in Figure 1. Several loads and wind farms are connected to the same PCC along with a STATCOM, which is in charge of the PCC voltage regulation. In this figure, L and R are the grid filter parameters, L_g and R_g are the grid impedance parameters, C_{DC1} and C_{DC2} are the DC-link capacitors and the STATCOM is a three-level neutral point clamped (NPC) converter.

Figure 1. Overview of the general system under investigation.



One of the most typical disturbances in power systems is an unbalance in the PCC voltage [6], which is a difference in the magnitude of the phase-to-neutral (or phase-to-phase) voltages of a three-phase system. There is no standardized mathematical expression to quantify the unbalance of a

three-phase system. Three definitions of unbalance are reviewed in [7]; one was developed by the National Equipment Manufacturer's Association (NEMA), another was developed by the IEEE and the other is the most common definition used by engineering community (the so-called true definition). The latter expresses the voltage unbalance factor (VUF) in percent as:

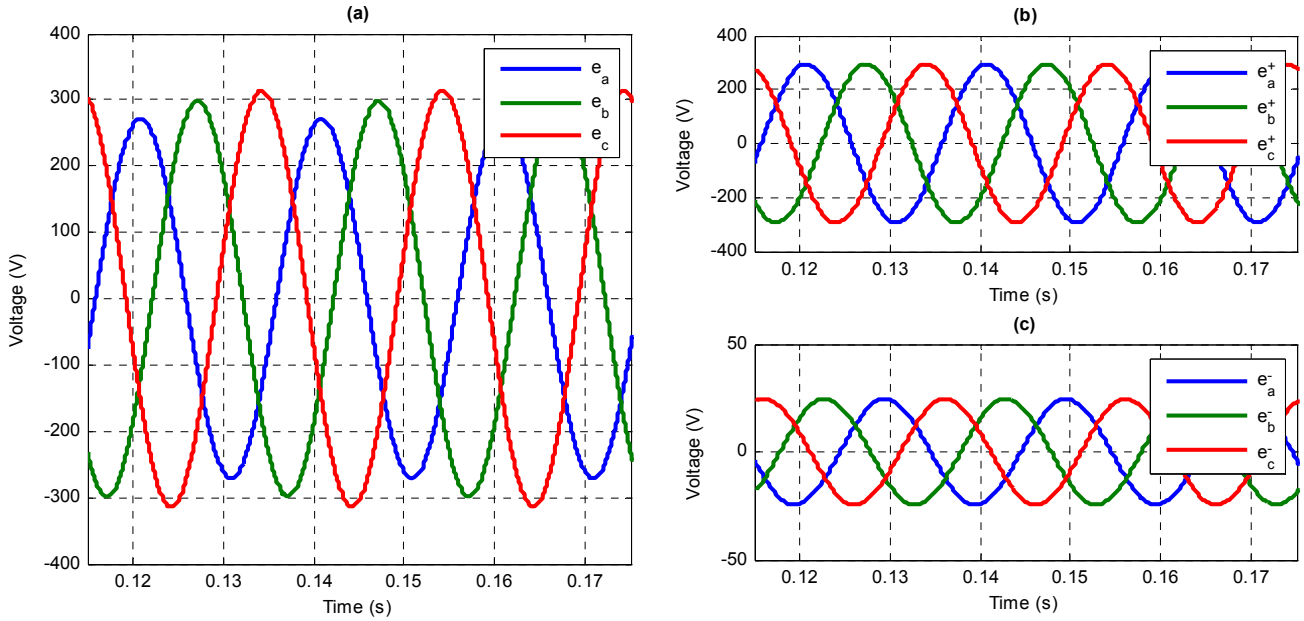
$$\text{VUF}(\%) = \frac{U^-}{U^+} \cdot 100\% \quad (1)$$

where U^- is the root mean square (RMS) value of the negative sequence component and U^+ is the RMS value of the positive sequence component.

It is well-known that any three-phase system can be split into the sum of three balanced systems, namely, positive, negative and zero sequences. A balanced three-phase system will be only composed of a positive sequence system. However, in real power systems several types of disturbances may affect the grid and give rise to the appearance of a negative sequence system in addition to the positive sequence one. Zero sequence systems only appear in three-phase four-wire power systems [8] and this case is not tackled in this article, since a three-phase three-wire power system is considered.

The unbalanced three-phase voltage shown in Figure 2a has a VUF equal to 8.3%, and it has been considered as the ideal grid voltage in the simulations results of Section 6.1. It is composed of the sum of a positive sequence three-phase system with $U^+ = 0.9 \cdot 400/\sqrt{3} \approx 207.8$ V (Figure 2b) and a negative sequence three-phase system with $U^- = 0.075 \cdot 400/\sqrt{3} \approx 17.3$ V (Figure 2c). In accordance with IEC 61000-3-13, the maximum VUF during normal operation in transmission systems must not exceed 2%; therefore, the grid voltage of Figure 2a can be used to justify and test the proposed algorithm.

Figure 2. (**a**) Unbalanced ideal grid voltage in *abc*-axes, which is composed by the sum of a (**b**) positive sequence three-phase system and a (**c**) negative sequence three-phase system.



An unbalanced voltage has several negative effects. For instance, it reduces efficiency and can cause failure in induction machines [9]. It also produces negative effects on power electronic converters. The voltage unbalance can impair a Pulse-Width Modulation (PWM) converter system

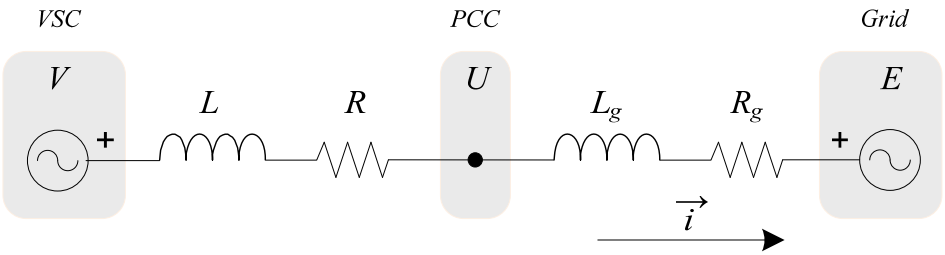
because the input active and reactive power ripples are generated by the cross products of line currents and unbalanced voltages [10]. The grid synchronization algorithm has to be sufficiently fast and accurate to extract the positive and negative voltage sequences precisely, in order to generate the output current references. A PCC voltage controller is needed to cancel these harmful effects while allowing an independent control of positive and negative sequence components.

The article is organized as follows: Section 2 analyzes the PCC voltage equations under unbalanced conditions and provides their corresponding plant models, which are focused in the grid model under a voltage unbalance. Section 3 details the control scheme that has been developed, as well as the design and tuning of the proposed PCC voltage controller. Section 4 addresses the possibility of performing an online adaptation of the DC-link reference voltage to always ensure an optimal modulation index. Section 5 investigates the sampling mode of the PCC voltage when working with an L-filter, which is of paramount importance for the correct operation of the control system in weak grids. Section 6 shows the effectiveness of the novel PCC voltage control through simulation results and, lastly, conclusions are presented in Section 7.

2. Grid Modeling Under Unbalanced Conditions

A VSC can be represented as an ideal AC voltage source (per phase). Therefore, its connection to the grid can be depicted according to the scheme of Figure 3, where L and R are the grid filter parameters, L_g and R_g are the grid impedance parameters, V is the VSC output voltage, U is the PCC voltage, E is the ideal grid voltage and $\vec{\imath}$ is the current flowing from the VSC to the grid.

Figure 3. Unifilar diagram of the connection of the VSC to the grid through an L-filter.



In order to obtain a general model of the grid, valid for both balanced and unbalanced conditions, the scheme of Figure 3 is considered. The grid model is calculated from the voltage equation between the points U (PCC) and E (ideal grid). The grid filter is not taken into account to obtain such model, since PCC voltage variations in an unbalanced system are imposed by the grid impedance and not by the grid filter.

The grid model can be expressed in time domain and in synchronous reference frame (dq-axes) as shown in Equation (2a) for positive sequence (superscript "+") and Equation (2b) for negative sequence (superscript "−"). In these equations, ω_1 is the fundamental angular frequency $\omega_1 = 2\pi 50$ rad/s. Each PCC voltage component is formed by the voltage drop across the grid impedance, a cross-coupling term between axes and the ideal grid voltage:

$$\vec{u}^{+}(t) = R_g\vec{\imath}^{+}(t) + L_g\frac{d\vec{\imath}^{+}(t)}{dt} + j\omega_1 L_g\vec{\imath}^{+}(t) + \vec{e}^{+}(t) \tag{2a}$$

$$\vec{u}^{-}(t) = R_g\vec{i}^{-}(t) + L_g\frac{d\vec{i}^{-}(t)}{dt} - j\omega_1 L_g\vec{i}^{-}(t) + \vec{e}^{-}(t) \quad (2b)$$

Each of these voltages is separated into its *d* and *q* projections: positive sequence voltages u_d^+ and u_q^+ are shown in Equation (3a) and (3b), whereas negative sequence voltages u_d^- and u_q^- are shown in Equation (4a) and (4b). These four expressions are steady-state approximations. Grid resistance R_g is considered to be very small, so that its contribution to the PCC voltage can be neglected (compared to the voltage drop across the grid filter inductance). Furthermore, the derivative of a constant signal (such as $\vec{i}$ in *dq*-axes) is zero. Note that u_d^+ is equal to zero Equation (3a) because a Phase-Locked Loop (PLL) is used to synchronize the positive sequence PCC voltage vector ($\vec{u}^+$) with the *q*-axis, hence the projection of $\vec{u}^+$ on this axis is equal to its amplitude $\left(u_q^+ \equiv |\vec{u}^+|\right)$:

$$u_d^+ = 0 \quad (3a)$$

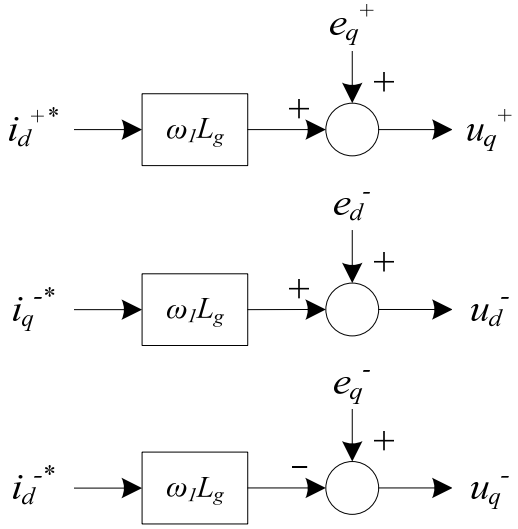
$$u_q^+ \approx \omega_1 L_g i_d^+ + e_q^+ \quad (3b)$$

$$u_d^- \approx \omega_1 L_g i_q^- + e_d^- \quad (4a)$$

$$u_q^- \approx -\omega_1 L_g i_d^- + e_q^- \quad (4b)$$

From the above equations it is straightforward to observe that each PCC voltage component is related to only one current component: u_q^+ and i_d^+; u_d^- and i_q^-; and u_q^- and i_d^-. The current component i_q^+ is related to the control of the DC-link voltage and does not influence the PCC voltage level directly. Thus, three independent voltage controllers are needed for u_q^+, u_d^- and u_q^-. Since they are constant voltages, a Proportional-Integral (PI) controller is enough to ensure zero steady-state error. The plant models needed for the design of these controllers are shown in Figure 4 for each component, based on Equation (3b) and (4).

Figure 4. Plant model of the PCC voltage control for each component in *dq*-axes.



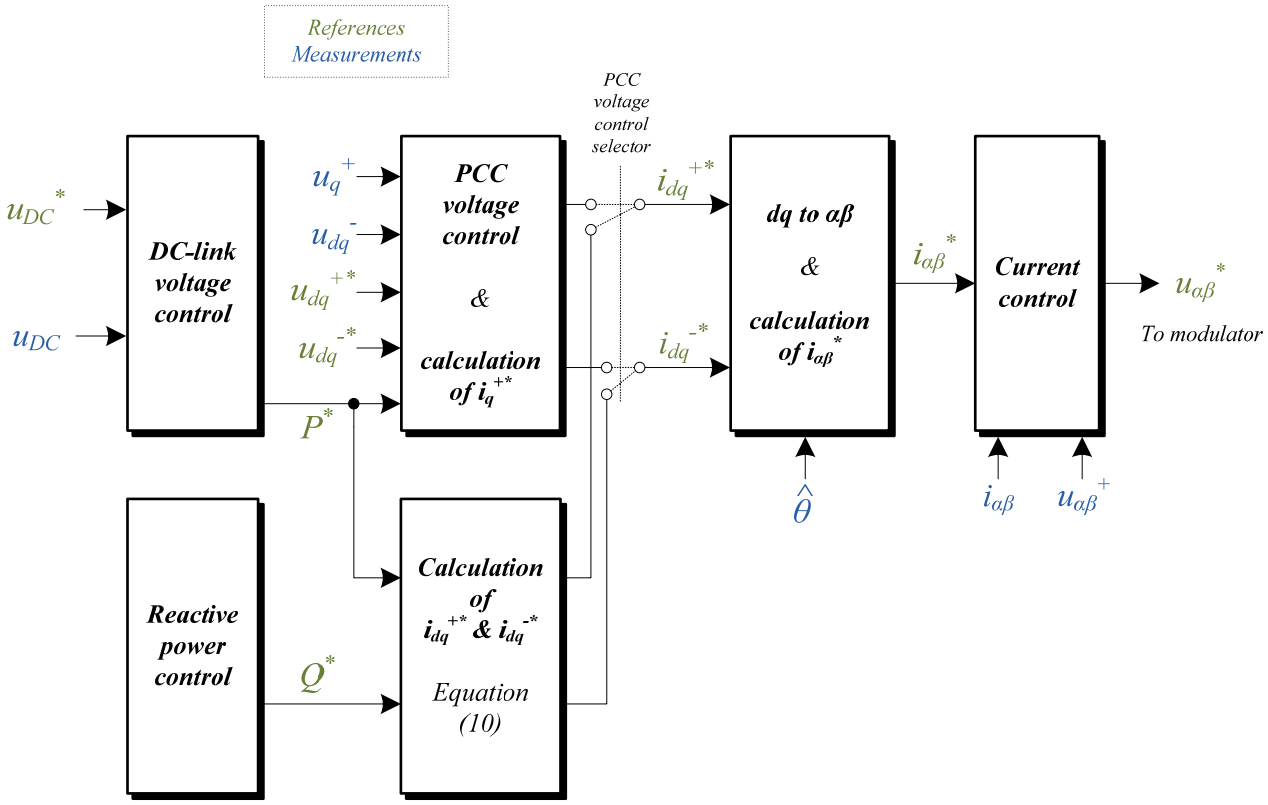
3. Control Scheme

The block diagram of the proposed control scheme is shown in Figure 5, which is composed of the following parts:

- DC-link voltage control
- Reactive power control
- PCC voltage control & calculation of i_q^{+*}
- Calculation of i_{dq}^{+*} and i_{dq}^{-*}
- Current control
- Modulation strategy

In first place, the active power reference P^* is set by the "DC-link voltage control" block. Its output constitutes an input for two possible blocks, namely, "Calculation of i_{dq}^{+*} and i_{dq}^{-*}" block or "PCC voltage control & calculation of i_q^{+*}" block. Depending on the application, one block or another will be chosen. The output of both blocks is the *dq*-axes reference current (positive and negative sequence, i_{dq}^{+*} and i_{dq}^{-*}). The following stage is the *dq* to αβ transformation plus the calculation of $i_{\alpha\beta}^*$. Finally, the low level control is performed by the "Current control" block and the modulation strategy.

Figure 5. Control scheme including the PCC voltage controller.



3.1. DC-link Voltage Control

The DC-link voltage controller is usually based on a PI controller along with an antiwindup mechanism. However, this scheme may not be sufficient in the case of weak grids. Due to the compensation of the negative sequence voltage at the PCC, an oscillation of frequency $2\omega_1$ appears in u_{DC}. If u_{DC} is not filtered, this oscillation propagates through the control system, appearing in P^* and, therefore, in the reference currents. The oscillation of frequency $2\omega_1$ in *dq*-axes is transformed into an oscillation of frequency $3\omega_1$ in the *abc*-axes.

In short, if u_{DC} is not filtered, the PCC currents will be affected by the appearance of a 3rd order harmonic (this being no zero-sequence harmonic). To eliminate this harmonic, the 2nd order oscillation is removed from the measured u_{DC} by means of a band-pass filter centered at $\omega_0 = 2\omega_1$. This filter is implemented with a Second Order Generalized Integrator for Quadrature Signal Generation (SOGI-QSG) [11], using the output in phase with the input since its transfer function behaves as a band-pass filter centered at ω_0. This way, the dynamics of the mean value of the DC-link voltage is not altered.

The block diagram of the DC-link voltage controller is shown in Figure 6, where k_{px} is the proportional gain, k_{ix} is the integral gain and k_{awx} is the antiwindup gain. The DC-link model based on the energy stored in the capacitor has been used [12]. As mentioned before, the basis of the DC-link voltage control is a PI controller and its parameters are tuned without taking into account the inner current controller. To do so, the Zero-Order Hold (ZOH) method has been applied to the plant to obtain its discrete time version, where $C_{DC} = (C_{DC1} \cdot C_{DC2})/(C_{DC1} + C_{DC2})$:

$$G_{DC}(z) = \frac{2T_s}{C_{DC}(z-1)} \tag{5}$$

The PI controller can be expressed in pole-zero form as:

$$C(z) = k_{px}\frac{z-\alpha}{z-1} \tag{6}$$

where $\alpha = 1 - \left(k_{ix}T_s/k_{px}\right)$. The open-loop transfer function has two poles placed at $z_p = 1$ and a zero placed at $z_z = \alpha$. Depending of the controller gain, the closed loop system $G_{CL}(z)$ can have two conjugate poles as shown. In this case, the general form of the denominator polynomial of $G_{CL}(z)$ is:

$$den\{G_{CL}(z)\} = \left(z - \rho e^{j\vartheta}\right)\left(z - \rho e^{-j\vartheta}\right) = z^2 - (2\rho\, cos\,\vartheta)z + \rho^2 \tag{7}$$

where $\rho = e^{-\xi\omega_n T_s}$, $\vartheta = \omega_n T_s\sqrt{1-\xi^2}$, ω_n is the natural pulsation and ξ is the damping coefficient. To avoid a large overvoltage in u_{DC}, the damping coefficient has to be chosen as $\xi \geq 1/\sqrt{2}$. From settling time and damping coefficient values, ω_n can be calculated with the expression $t_s \approx 4.6/\xi\omega_n$ for a second order system. To verify these conditions, k_{px} and α have to take the next values:

$$k_{px} = \frac{(1-\rho\, cos\,\vartheta)C_{DC}}{T_s} \tag{8}$$

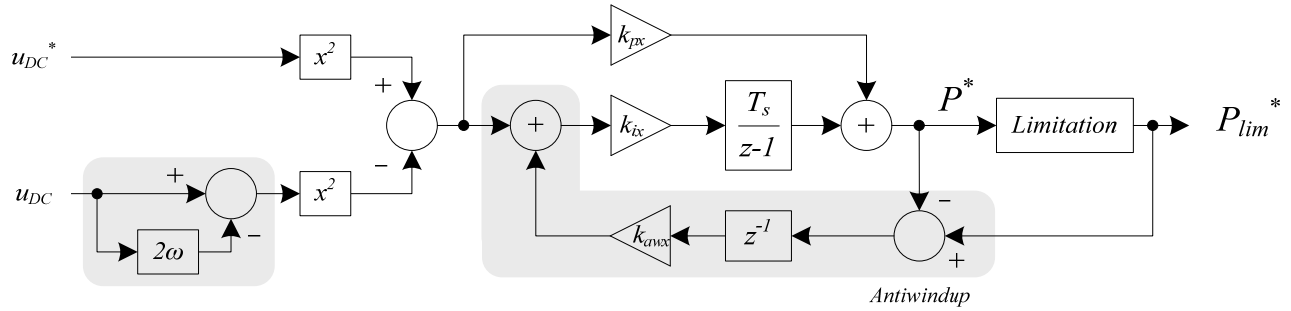
$$\alpha = \frac{1-\rho^2}{2(1-\rho\, cos\,\vartheta)} \tag{9}$$

and then $k_{ix} = (1-\alpha)k_{px}/T_s$. The antiwindup gain is chosen as $k_{awx} = 1/k_{px}$.

3.2. Reactive Power Control

This is a controller associated to variables that modify the reactive power at the PCC. In this case, this block specifies the reactive power reference Q^*, which is an output to the block "*Calculation of* i_{dq}^{+*} *&* i_{dq}^{-*}". Another variable that could be used to modify the reactive power at the PCC is the power factor.

Figure 6. Block diagram of the "*DC-link voltage control*" of Figure 5.



3.3. Calculation of i_{dq}^{+*} and i_{dq}^{-*}

This controller is regulated by the equation system in Equation (10). It relates active power, reactive power, PCC voltage and current in *dq*-axes and it is usually employed in active and reactive power control, as well as in power factor control. Active and reactive powers are divided into three parts: average power (P and Q), oscillating power with cosine terms [$P_{2\omega(c)}$ and $Q_{2\omega(c)}$] and oscillating power with sine terms [$P_{2\omega(s)}$ and $Q_{2\omega(s)}$]. If grid conditions are balanced, these four oscillating powers are zero and there are only positive sequence voltages and currents. Multiplying by the inverse matrix, the corresponding expressions for the calculation of the reference currents are obtained (i_{dq}^{+} and i_{dq}^{-}). To do so, $P_{2\omega(c)}$ and $P_{2\omega(s)}$ are set to zero to compensate the unbalance caused by negative sequence voltage and $Q_{2\omega(c)}$ and $Q_{2\omega(s)}$ are not controlled, therefore their corresponding rows are eliminated from Equation (10). Trying to control these oscillating reactive powers only deteriorates the control performance, therefore they are allowed to run freely:

$$\begin{bmatrix} P_0 \\ P_{2\omega(c)} \\ P_{2\omega(s)} \\ Q_0 \\ Q_{2\omega(c)} \\ Q_{2\omega(s)} \end{bmatrix} = \begin{bmatrix} u_d^+ & u_q^+ & u_d^- & u_q^- \\ u_d^- & u_q^- & u_d^+ & u_q^+ \\ u_q^- & -u_d^- & -u_q^+ & u_d^+ \\ u_q^+ & -u_d^+ & u_q^- & -u_d^- \\ u_q^- & -u_d^- & u_q^+ & -u_d^+ \\ -u_d^- & -u_q^- & u_d^+ & u_q^+ \end{bmatrix} \cdot \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \tag{10}$$

3.4. PCC Voltage Control

The block diagram of the PCC voltage controller is shown in Figure 7 and it is implemented in *dq*-axes. This stage is formed by three "individual voltage controllers" in parallel, whose outputs are i_d^{+*}, i_d^{-*} and i_q^{-*}, plus the calculation of i_q^{+*} by means of Equation (11). This equation is obtained from Equation (10). The minus sign that goes with u_q^+ is due to the current direction. These four outputs are the references for the current controller. In this figure, ε represents the error signal and the subscript "lim" stands for "limited". The reference voltages u_d^{-*} and u_q^{-*} are set to zero in order to eliminate the PCC voltage negative sequence, whereas the reference voltage u_q^{+*} should be equal to the PCC fundamental voltage.

The inner structure of each "individual voltage controller" is depicted in Figure 8. As mentioned, it is mainly formed by a PI controller with a forward Euler integrator. The constant δ is 1 for the voltage controllers of u_q^+ and u_d^-, and -1 for the voltage controller of u_q^- due to the minus sign in Equation (4b).

It is a first order system and, considering the cascaded system of Figure 5, the tuning goal is to achieve a settling time larger than ten times the settling time of the current controller ($t_s|_{vc} > 10 \cdot t_s|_{cc}$, where t_s is the settling time, "vc" means voltage control and "cc" means current control). This constraint affects the position of the closed-loop pole introduced by the PI controller. The integral constant (k_i) helps achieve zero steady-state error in the event of model mismatch and disturbances. Therefore, the parameter tuning is focused on settling time and controller bandwidth. The resulting parameters are $k_p = 0.05$ and $k_i = 350$.

Figure 7. Block diagram of the "*PCC voltage control & calculation of* i_q^{+*}" block of Figure 5.

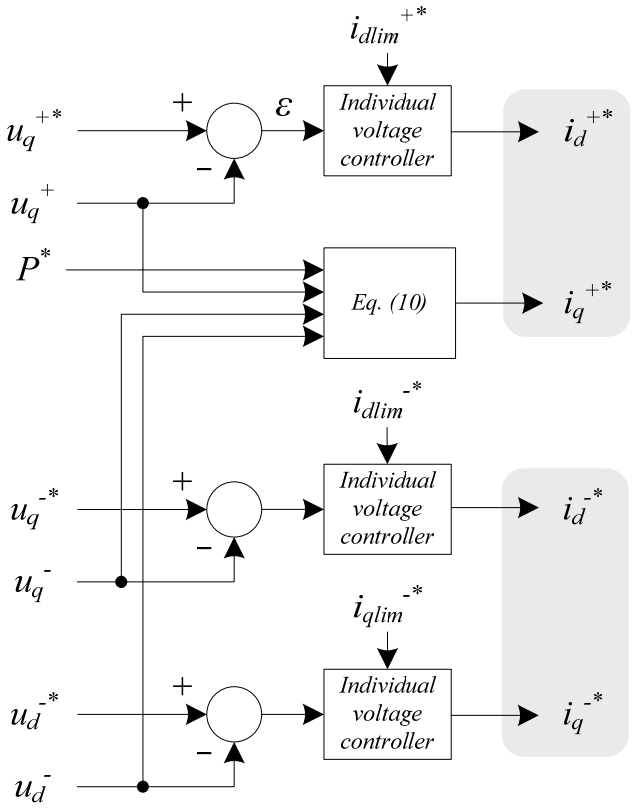
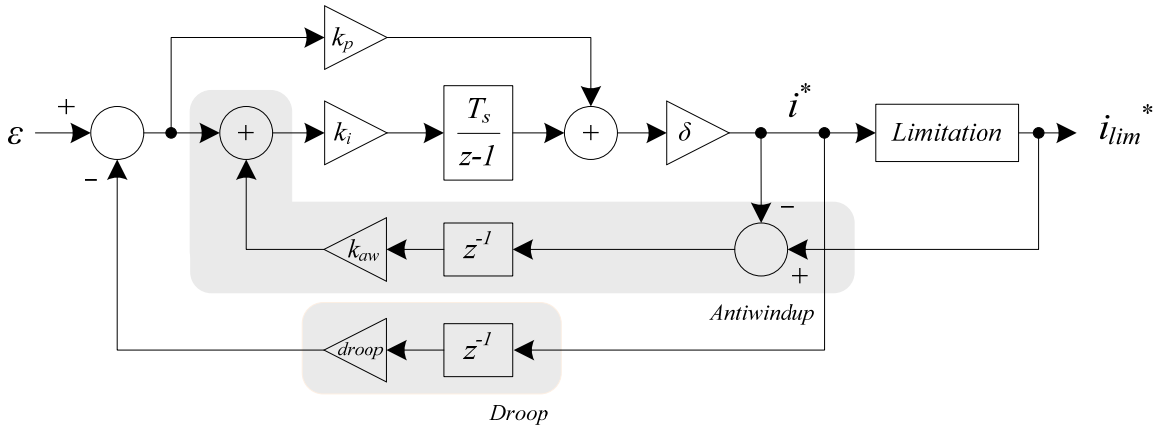


Figure 8. Block diagram of the "*individual voltage controller*" of Figure 7.



$$i_q^{+*} = \frac{P^* u_q^+}{(u_d^-)^2 + \left(u_q^-\right)^2 - \left(u_q^+\right)^2} \tag{11}$$

In order to prevent the windup of the integrator, an antiwindup mechanism has been added to each PI controller. It is characterized by the antiwindup constant, which has been set as $k_{aw} = 0.1$. High values for this parameter cause system instability. When using an antiwindup technique, an important detail to be taken into account is that its contribution should not be added to the integral branch of the PI controller until the whole control system starts. Otherwise, the control system would be forced to start with a non-zero error.

The linear operating range of a STATCOM with given maximum capacitive and inductive ratings can be extended if a regulation "droop" is allowed. Regulation "droop" means that the terminal voltage is allowed to be smaller than the nominal no-load value at full capacitive compensation and, conversely, it is allowed to be higher than the nominal value at full inductive compensation [13]. It also ensures automatic load sharing with other voltage compensators. Perfect regulation (zero droop or slope) could result in poorly defined operating point, and a tendency of oscillation, if the system impedance exhibited a "flat" region (low impedance) in the operating frequency range of interest [13]. It should be mentioned that this possible regulation makes sense in scenarios where there are several converters connected in parallel trying to control the PCC voltage. This droop control has been added to the voltage controller as shown in Figure 8, characterized by the constant $droop = 0.01$. Similarly to k_{aw}, high values for this parameter cause system instability. The expression in Equation (11) is obtained from Equation (10).

3.5. dq to αβ *Transformation and Calculation of* $i^*_{\alpha\beta}$

The outputs of the first stage of the control scheme are i^{+*}_{dq} and i^{-*}_{dq}. These current references have to be transformed to αβ-axes, since the current controller is implemented in stationary reference frame. The reason for this is that a resonant controller tuned at ω in αβ-axes is able to compensate both positive and negative sequences, whereas in *dq*-axes two controllers would be necessary, a PI controller and a resonant controller tuned at $2\omega_1$. The fact of increasing the number of controllers connected in parallel endangers the system stability and increases the settling time of the controller.

Positive and negative sequence current references in αβ-axes are calculated as shown in Equation (12a) and (12b). The estimated phase angle $\hat{\theta}$ of the positive sequence voltage vector is obtained with a PLL, whose bandwidth is 20 Hz. This results in a good tradeoff between selectivity, steady-state error and response speed. Afterwards, the final current references are calculated according to Equation (13a) and (13b):

$$\begin{bmatrix} i^{+*}_{\alpha} \\ i^{+*}_{\beta} \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & -\sin\hat{\theta} \\ \sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \cdot \begin{bmatrix} i^{+*}_{d} \\ i^{+*}_{q} \end{bmatrix} \tag{12a}$$

$$\begin{bmatrix} i^{-*}_{\alpha} \\ i^{-*}_{\beta} \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \cdot \begin{bmatrix} i^{-*}_{d} \\ i^{-*}_{q} \end{bmatrix} \tag{12b}$$

$$i^*_{\alpha} = i^{+*}_{\alpha} + i^{-*}_{\alpha} \tag{13a}$$

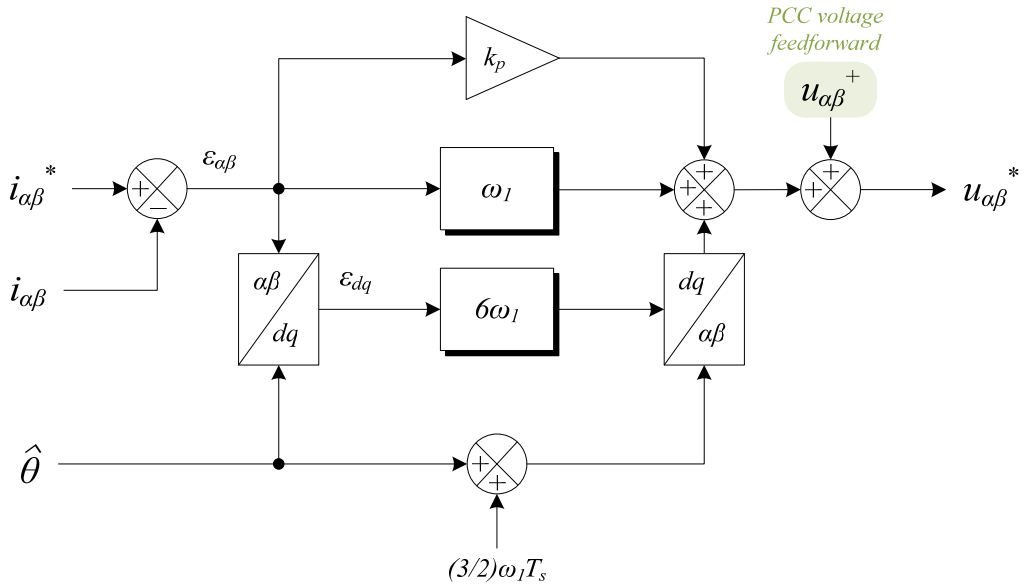
$$i^*_{\beta} = i^{+*}_{\beta} + i^{-*}_{\beta} \tag{13b}$$

3.6. Current Controller

The third stage of the control scheme is the current controller. The harmonics present in power systems are those of order $6k \pm 1$ ($k \in \mathbb{Z}$), which turn into $6k$ ($k \in \mathbb{Z}$) when changing the reference

frame from stationary (*abc* or αβ) to synchronous (*dq*). This allows halving the number of resonant controllers needed to implement the current controller [14]. Therefore, since the 5th (negative sequence) and 7th (positive sequence) harmonics are usually present in the grid, the current control scheme of Figure 9 has been used to obtain the simulation results. It consists of two resonant controllers (SOGIs) tuned at ω_1 and $6\omega_1$ (the blocks labeled as "ω_1" and "$6\omega_1$" are composed of an integral gain k_i connected in series with a SOGI), a feedforward of the positive sequence PCC voltage, and αβ to *dq* and *dq* to αβ transformations. A feedforward of the total PCC voltage (including negative sequence) would introduce non-desired harmonics in the control. The error signals in αβ-axes and *dq*-axes are $\varepsilon_{\alpha\beta}$ and ε_{dq}, respectively.

Figure 9. Block diagram of the block "*Current control*" of Figure 5.



In general, the resonant frequency of the SOGI is represented by ω_0. The discrete SOGI transfer function is given by Equation (14) and, if $\omega_0^2 T_s^2 \ll 2$, which is verified for $T_s < 1.4\ ms$ (supposing that $\omega_0^2 T_s^2 = 0.2$ is small enough, *i.e.*, a factor of 10) and if $\omega_0 = 2\pi 50\ rad/s$, Equation (14) can be approximated by Equation (15):

$$G_{SOGI}(z) = \frac{\omega_0 T_s z(z-1)}{(z-1)^2 + \omega_0^2 T_s^2 z} \tag{14}$$

$$G_{SOGI}(z) \approx \frac{\omega_0 T_s z}{z-1} \tag{15}$$

The SOGI is combined with a proportional and integral gain (k_p and k_i, respectively) to form the current controller. The resulting transfer function can be expressed as:

$$G_{P+SOGI}(z) = k_p + k_i \frac{\omega_0 T_s z}{z-1} = K_p \frac{z-\alpha}{z-1} \tag{16}$$

where $K_p = k_p + k_i \omega_0 T_s$ and $\alpha = \frac{k_p}{k_p + k_i \omega_0 T_s}$. It is important to notice that the approximation made for Equation (15), *i.e.*, if $\omega_0^2 T_s^2 \ll 2$, will not be valid for every frequency and for every sampling period. The current controller parameters take the following values:

$$K_p = \frac{1 + a - 2\rho\cos\vartheta}{b} \tag{17a}$$

$$\alpha = \frac{a - \rho^2}{bK_p} \tag{17b}$$

where $\rho = e^{-\xi\omega_n T_s}$, $\vartheta = \omega_n T_s$, ω_n is the natural pulsation, ξ is the damping factor, $a = e^{-\frac{RT_s}{L}}$ and $b = (1-a)/R$. Then, $k_p = \alpha K_p$ and $k_i = \left(K_p - k_p\right)/\omega_0 T_s$.

To help decreasing the computational burden, the trigonometric functions employed in the calculation of these transformations can be implemented by means of look-up tables if the digital platform has enough memory.

3.7. Modulation Strategy

The NPC converter, whose scheme is shown in Figure 10, has some drawbacks such as the additional clamping diodes, a more complicated PWM switching pattern design and possible deviation of neutral point (NP) voltage [15]. The capacitors can be charged or discharged by neutral current i_{NP}, causing NP voltage deviation. It might appear a ripple of frequency three times the fundamental in u_{DC1} and u_{DC2} that can destroy components if both DC-link voltages are not balanced.

To minimize this effect, a carrier-based PWM strategy with zero-sequence voltage injection [16] is applied to the three-level NPC converter. Using this technique, the locally averaged NP current is kept to zero, and consequently, the locally averaged voltages on the DC-link capacitors are constant [17].

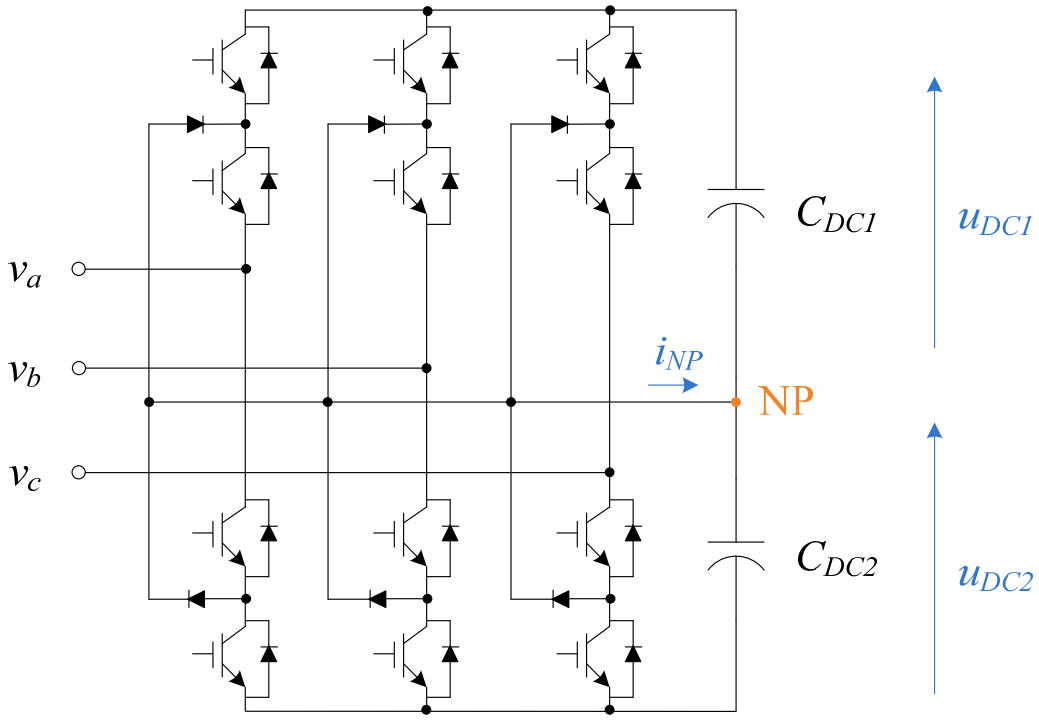
4. Online Adaptation of the DC-Link Reference Voltage

To enable the power transfer between the grid and the DC-link capacitors, u_{DC} must be greater than $\sqrt{2}\,v_{LL}$, where v_{LL} is the RMS phase-to-phase NPC output voltage. When calculating the reference DC-link voltage, a safety margin Δu_{DC} is usually given to ensure the energy transfer in case of voltage fluctuations. This margin takes values from 20 V to 50 V in weak grids. Therefore, the calculation of u_{DC}^* is shown in Equation (18):

$$u_{DC}^* \geq \sqrt{2}\,v_{LL} + \Delta u_{DC} \tag{18}$$

When the PCC voltage is expected to suffer large variations, as in the case of weak grids, u_{DC}^* should be recalculated online to adapt its value to the actual AC voltage. In this way, the modulation index is kept around its optimal value, *i.e.*, $m_a \approx 1$. Otherwise, the modulation index will be altered, which can increase the converter power losses, modify the expected harmonic content and worsen the overall system performance [15]. It is also advisable to limit the possible values of u_{DC}^* so that controllability is always ensured, as in the case of voltage dips, and limit the transition rate of u_{DC}^*.

Figure 10. Three-level NPC converter.



5. Sampling Mode When Working With an L-Filter

One of the essential parts of the converter control is the synchronization system, which allows detecting the angle of the PCC voltage vector. This angle would coincide with that of the grid voltage if it were an ideal grid. Generally, the grid impedance is neglected in terms of controller design, considering the voltage at the PCC as the system voltage [18].

Blasko *et al.* [19] established that the optimal moment to sample the currents are those in which the PWM carrier signal reaches its maximum and minimum value, since it is in those moments when the zero-crossing of the current ripple takes place. When working with an LCL-filter and a non-ideal grid, and sampling the PCC voltage at those same moments, the obtained PCC voltage in *dq*-axes corresponds to its actual value. However, this is not the same situation when working with an L-filter and a non-ideal grid. In this case, the PCC voltage presents a ripple in which two envelopes can be seen. By sampling synchronously with the sampling period of the currents, which is also the controller sampling period, the obtained PCC voltage corresponds to one of those envelopes, giving rise to incorrect projections of the PCC voltage on the *dq*-axes.

Briz *et al.* [20] posed two alternative methods to the method suggested by Blasko for sampling the currents, when the inverter is connected to a load whose natural frequency may be close to the sampling frequency. In such cases, the method based on the maximum and minimum points of the carrier signal introduces an error at the current fundamental frequency as well as aliasing problems. The methods the authors proposed were based on advancing the sampling instant and on multi-sampling per switching period.

The methods studied here for sampling the PCC voltage are similar to those shown in [20]. With the system configuration defined in Table 1, several methods for performing the PCC voltage sampling are shown in Figure 11 [21]:

(a) The previously mentioned sampling method synchronized with the current sampling, where the sampling period of the PCC voltage and the timer, T_{ss}, is equal to T_s (Figure 12a);
(b) Sampling at the midpoint of T_s, with $T_{ss} = T_s$, which obtains a PCC voltage in *dq*-axes higher than the real value (Figure 12b);
(c) Sampling shifted a time t_{ad} with respect to the sampling instants of the current, where $T_{ss} = T_s$ and where the voltage remains erroneous (Figure 12c, where $t_{ad} = T_s/4$);
(d) Oversampling of two samples, synchronized with T_s, where $T_{ss} = T_s/2$ and for which the voltage remains slightly erroneous (Figure 12d);
(e) Oversampling of three samples, synchronized with T_s, where $T_{ss} = T_s/3$ and for which the voltage still remains slightly erroneous (Figure 12e), and
(f) Oversampling of four samples, which obtains a correct PCC voltage in *dq*-axes (Figure 12f).

Table 1. System parameters with L-filter and non-ideal grid.

Parameter	Symbol	Value	Units
Base apparent power	S_{base}	100	kVA
Base voltage	U_n	$400\sqrt{2/3}$	V
Fundamental pulsation	ω_1	$2\pi 50$	rad/s
Grid-filter inductance	L	0.2209	p.u.
Grid-filter resistance	R	0.0034	p.u.
Grid-impedance inductance	L_g	0.0736	p.u.
Grid-impedance resistance	R_g	0.0005	p.u.
Switching period	T_{sw}	200	μs
Sampling period	T_s	100	μs

Figure 11. Methods for performing the PCC voltage sampling [21].

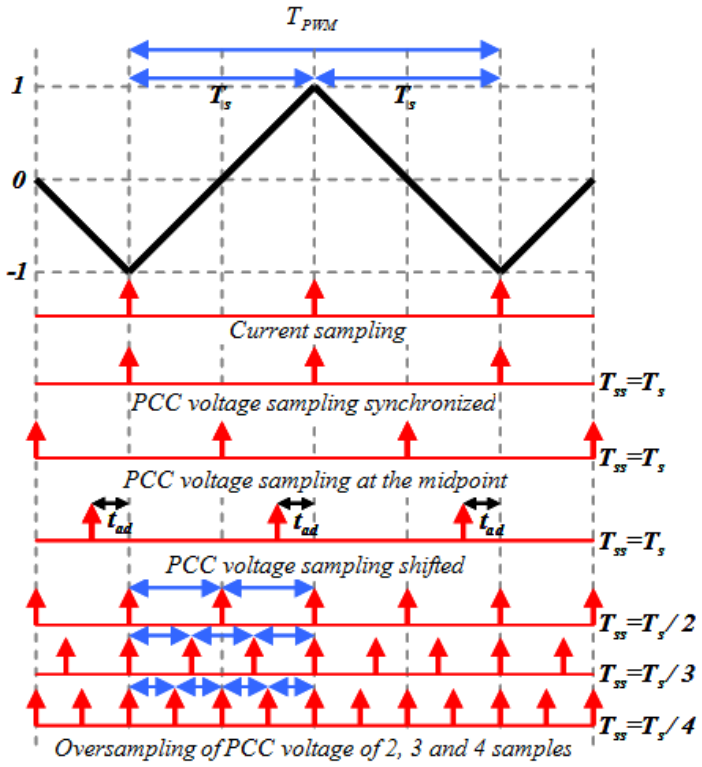
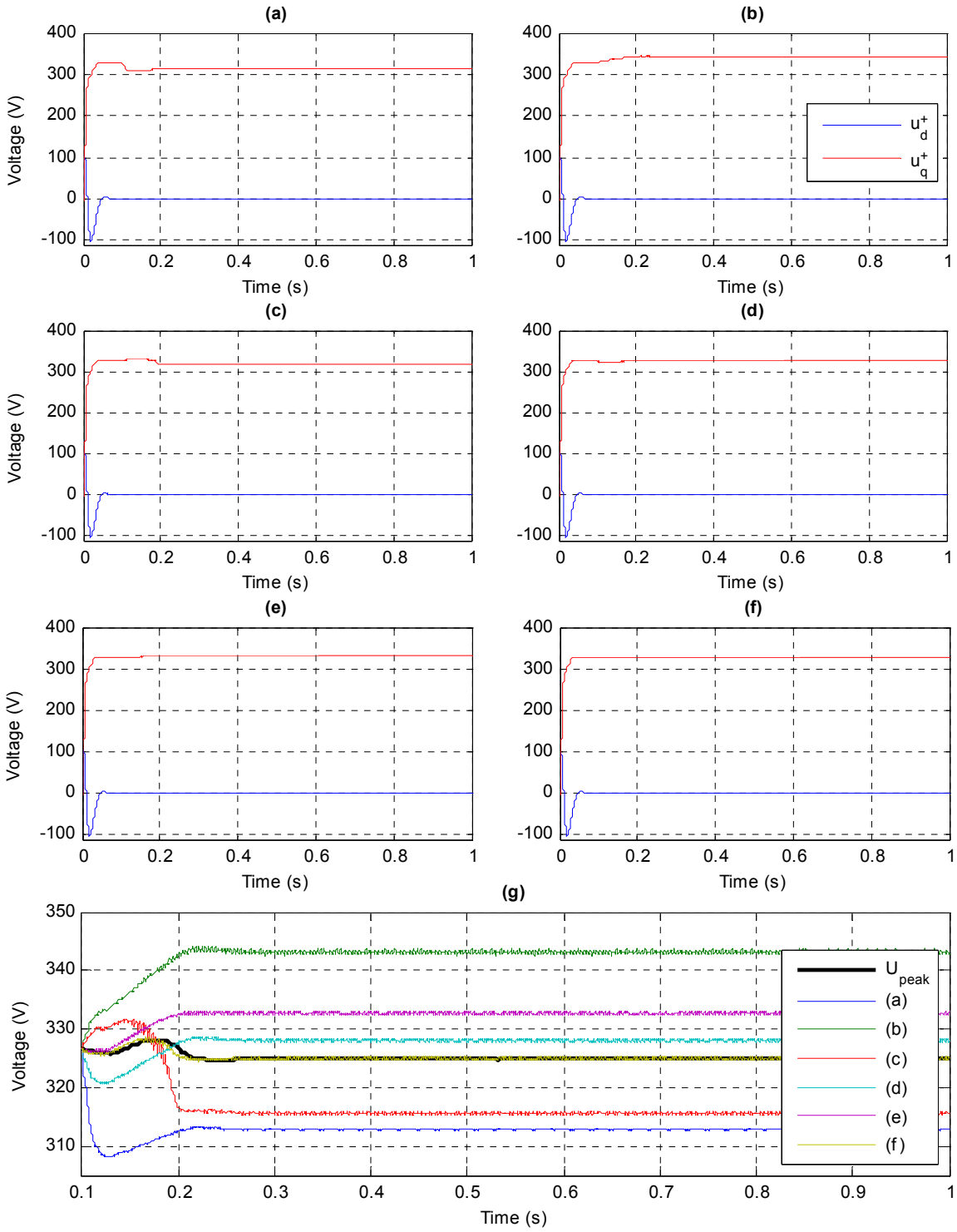


Figure 12. Estimated u_{dq}^{+} $(\tilde{u}_{q}^{+})$ with (**a**) sampling synchronized; (**b**) sampling at the midpoint; (**c**) sampling shifted; (**d**) oversampling of two samples; (**e**) oversampling of three samples; and (**f**) oversampling of four samples; (**g**) Comparison of the u_{q}^{+} obtained with the six methods after the initial transient with respect to the peak value of the fundamental PCC phase voltage (U_{peak}).



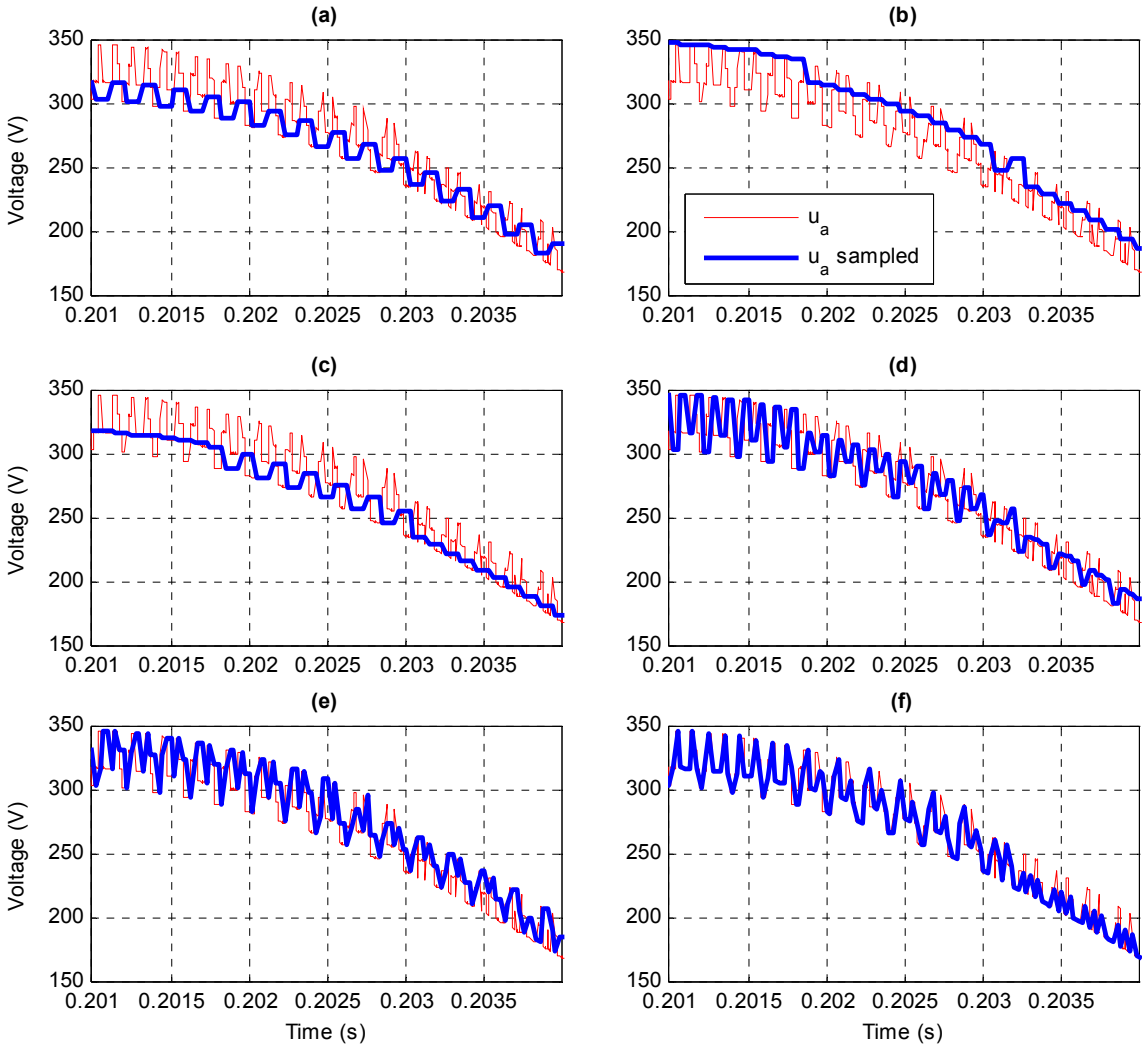
The estimated u_{q}^{+} $(\tilde{u}_{q}^{+})$ in steady-state with the six methods mentioned above are compared with the peak value of the fundamental PCC voltage in Figure 12g. Figure 13 shows the effect of applying

each sampling method on the *a*-phase of the PCC voltage. It is straightforward to see the relationship between Figures 12g and 13:

- Methods (a) and (c) detect an inner envelope of u, giving $\tilde{u}_q^+ < u_q^+$. Besides, the envelope detected with method (c) is the one closest to the fundamental voltage and, thus, $\tilde{u}_q^+\big|_{a)} < \tilde{u}_q^+\big|_{c)} < u_q^+$;
- Method (b) detects an outer envelope of u, yielding $\tilde{u}_q^+\big|_{b)} > u_q^+$;
- Methods (d) and (e) perform a more precise detection of the PCC voltage than methods (a) to (c), although there is still a small steady-state error. It is also observed that $\tilde{u}_q^+\big|_{e)} > \tilde{u}_q^+\big|_{d)} > u_q^+$ in spite of using a higher oversampling, which is due to the sampling at highly-noisy points of u;
- Method (f), *i.e.*, oversampling of four samples synchronized with T_s, is the only method that performs a precise detection of the PCC fundamental voltage: $\tilde{u}_q^+\big|_{f)} \approx u_q^+$.

The initial transient in the estimation of u_{dq}^+ (Figure 12a–f) is due to the stabilization process of the PLL. However, this transient is not significant from the viewpoint of control performance because the converter control system only starts when the PLL is stable.

Figure 13. Effect of applying each sampling method on the *a*-phase of the PCC voltage.



6. Simulation Results

6.1. Weak Grid Without Harmonics

A simulation has been carried out with MATLAB/Simulink® in order to test the performance of the proposed voltage controller. The ideal grid voltage of Figure 2 has been considered, along with the system parameters of Table 1. The NPC rated power is 100 kVA and the DC-link capacitors have a value of $C_{DC1} = C_{DC2} = 4.5$ mF. No load is connected to the PCC. The proposed voltage controller is enabled at $t = 0.5$ s.

Figure 14 shows the temporary evolution of the filtered PCC voltage in *abc*-axes. Its non-filtered waveform presents a high ripple due to the high grid impedance and, in order to appreciate the effect of the PCC voltage controller, its filtered waveform is the one represented. In the following figures, the corresponding control activation time is marked with a dashed black line. It is clear that, when the voltage control is enabled, the PCC voltage is balanced. This is corroborated by decomposing this voltage in their positive and negative sequences as shown in Figure 15. The positive sequence u_{dq}^{+} remains equal because its reference voltage corresponds to the value it had before enabling the PCC voltage control. The negative sequence u_{dq}^{-} becomes almost zero since its reference voltage is set to zero for both *d* and *q* components, as well as the VUF.

Figure 14. Filtered PCC voltage in *abc*-axes. (**a**) Representation of the waveforms in $t = [0.35, 1]$ s and (**b**) in $t = [0.35, 0.65]$ s.

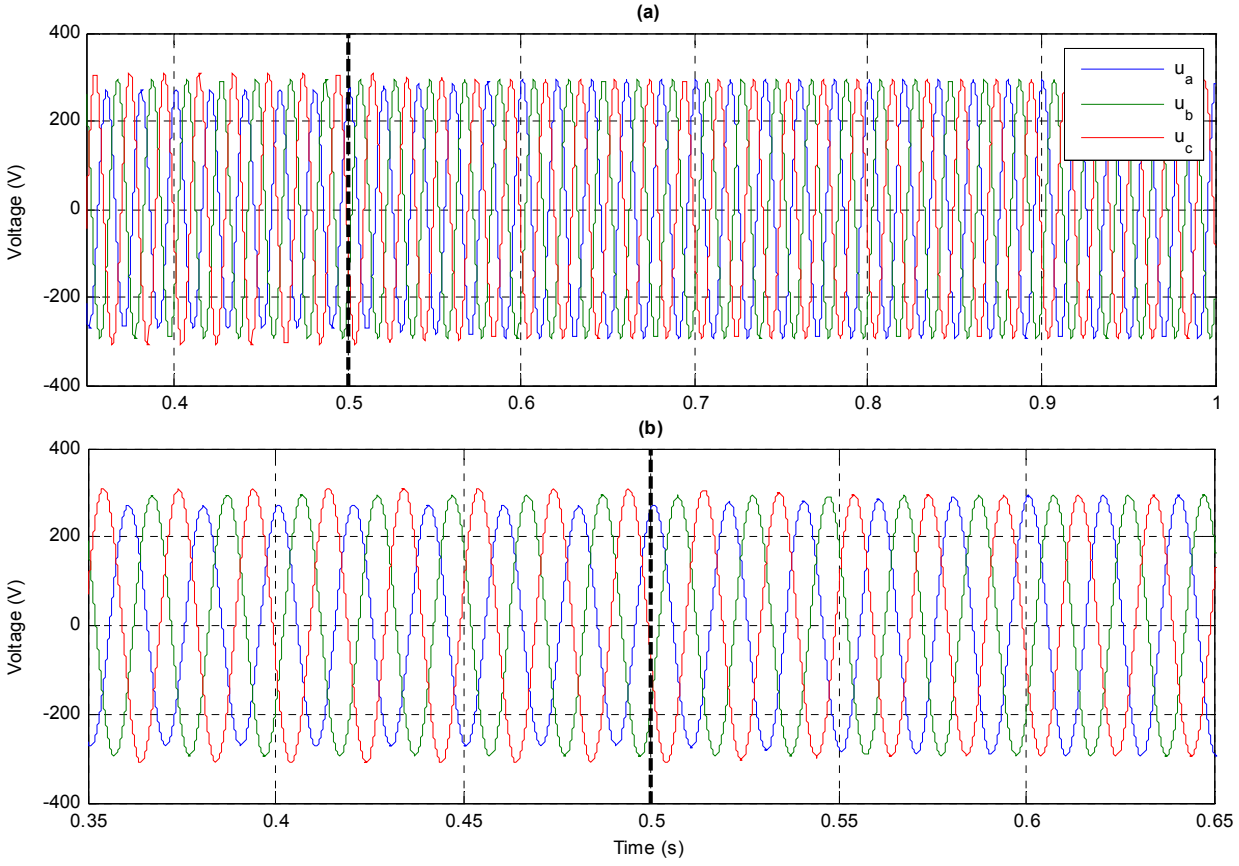
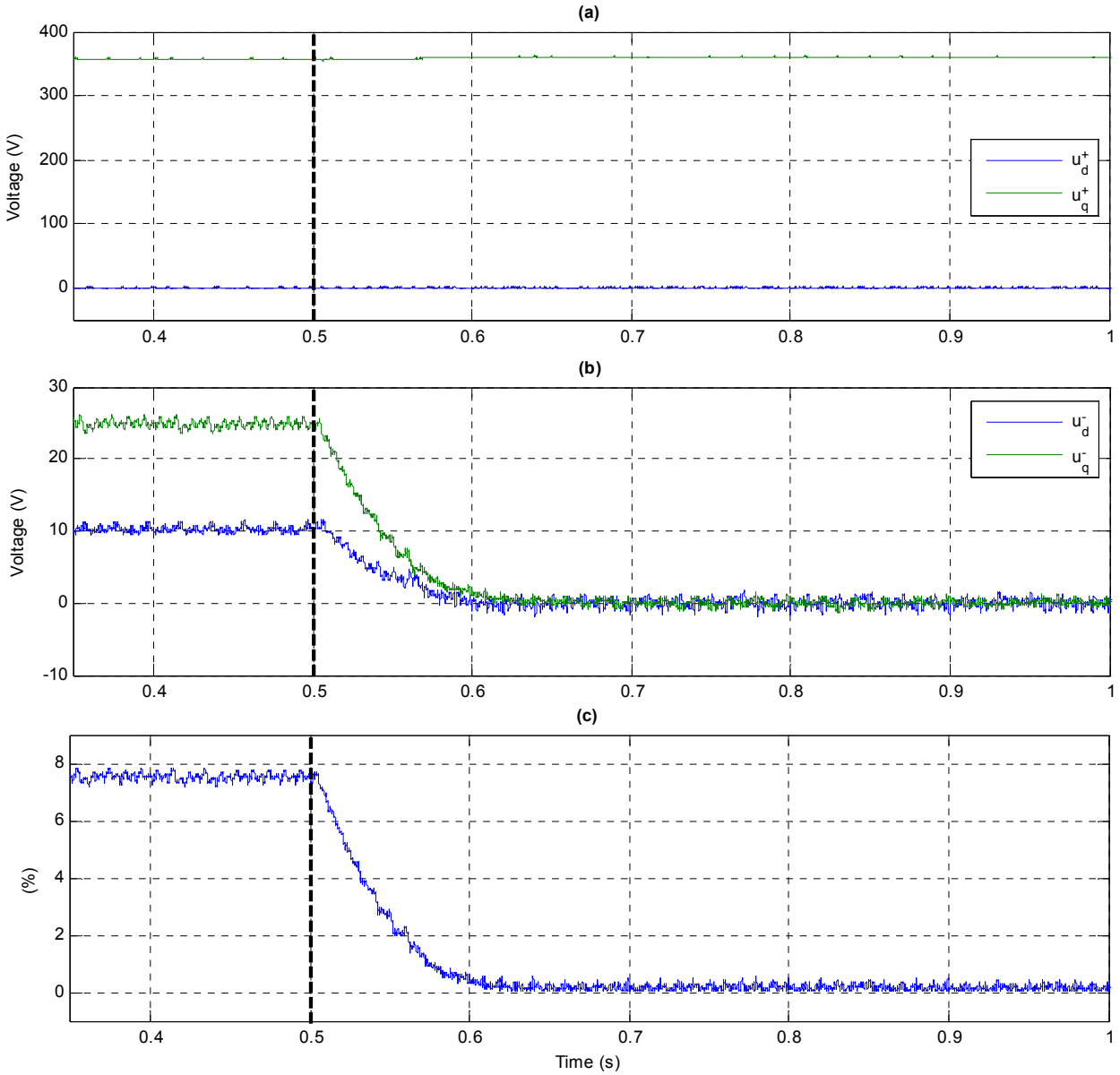
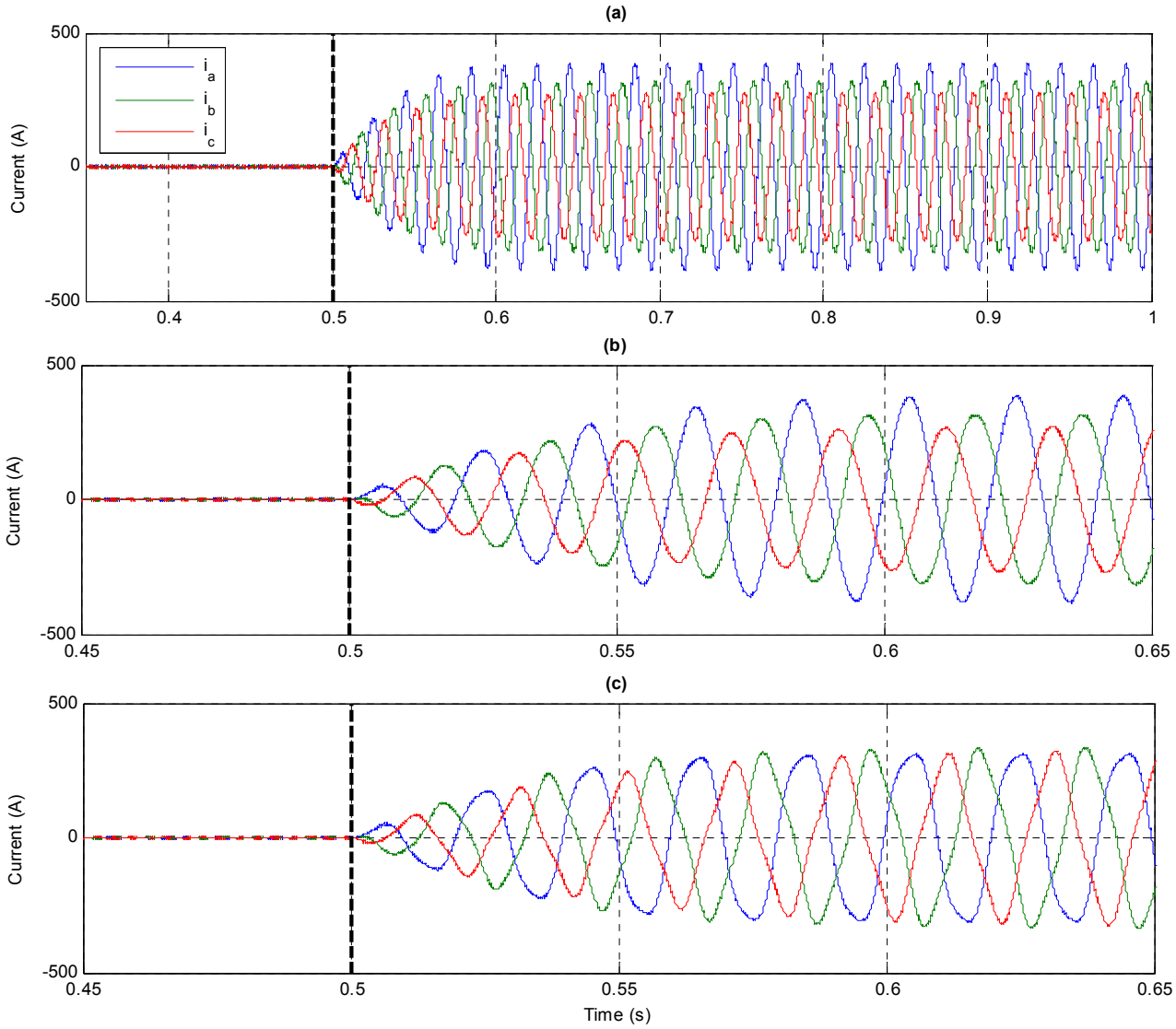


Figure 15. PCC voltage (**a**) positive and (**b**) negative sequences in *dq*-axes; (**c**) VUF (%).



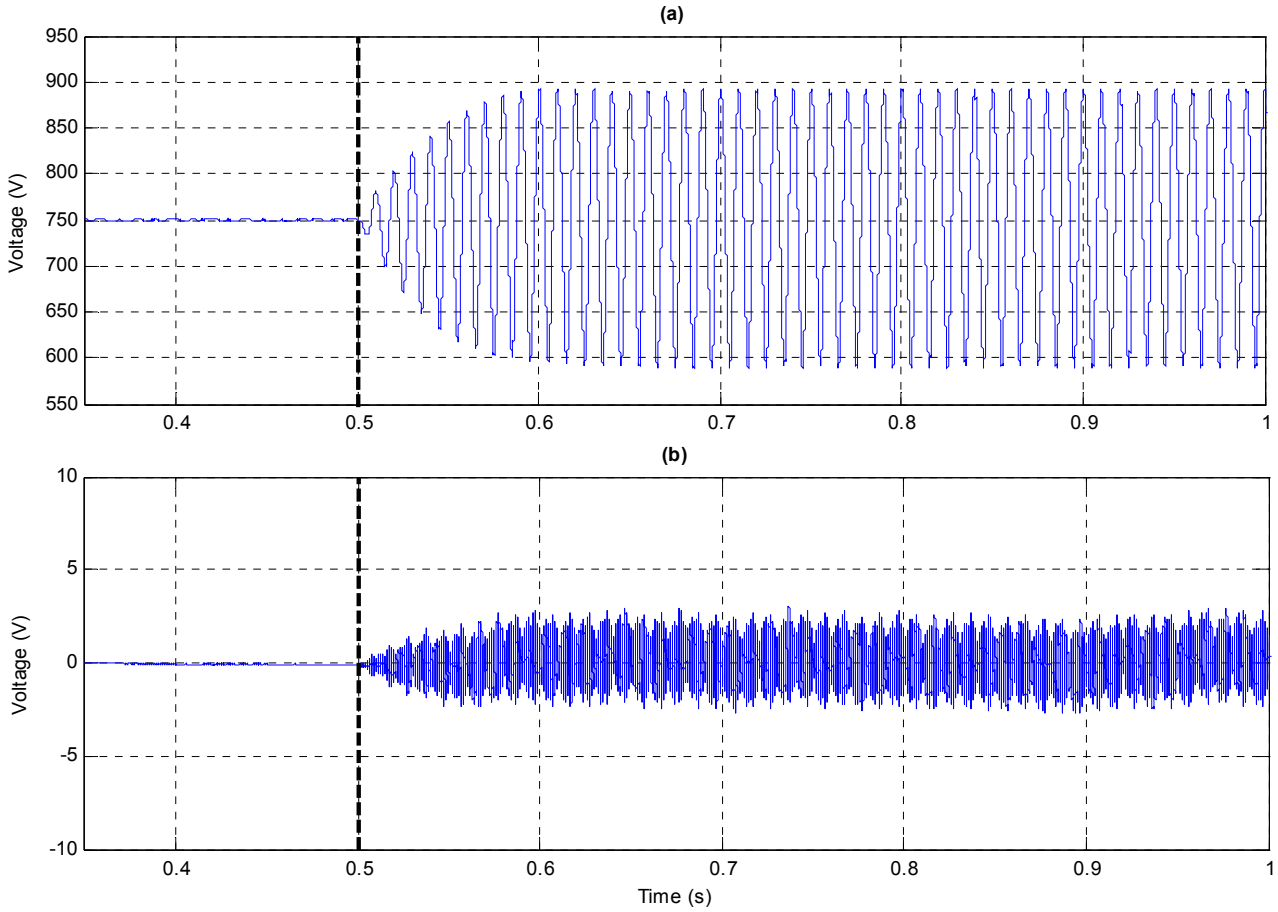
The current flowing from the VSC to the grid is represented in Figure 16a in *abc*-axes. Since no load is connected to the PCC, the current before enabling the voltage control is zero. Afterwards, the VSC provides an unbalanced current in order to compensate the negative sequence component. This is better observed in Figure 16b, which is a representation of Figure 16a between t = [0.45 0.65] s. Figure 16c is the equivalent of Figure 16b if the resonant controller 2ω is not included in the DC-link voltage controller, showing a PCC current with a 3rd order harmonic.

Figure 16. (**a**) PCC current in *abc*-axes; (**b**) Zoom of (**a**) between t = [0.45, 0.65] s; (**c**) Equivalence to (**b**) if the band-pass filter in the DC-link voltage controller is not included.



Since the PCC voltage is no longer unbalanced due to the effect of the voltage controller, the unbalance now appears in u_{DC}. Figure 17a shows that a large oscillation appears in u_{DC}, reaching nearly ±150 V. Besides, the DC-link voltage unbalance, calculated as the difference between positive and negative DC-link voltages ($u_{DC1} - u_{DC2}$), also increases. If the oscillation level is not permissible, the reference for the negative sequence voltage can be set with a value different from zero but still low enough to satisfy regulations when it comes to maximum PCC voltage unbalance. In any case, it is worth remembering that the high level of unbalance applied to carry out these tests is usually not found in a real power system, so that in practice the amplitude of the oscillation will be much smaller. According to current regulations, a VUF greater than 2% in the worst case (e.g., IEC 61000-3-13 regulation) and 3% in the best case (e.g., ENTSO-E regulation) requires the disconnection of the converter from the grid, which can be avoided with the proposed PCC voltage controller.

Figure 17. (**a**) DC-link voltage; (**b**) DC-link voltage unbalance.



6.2. Weak Grid With 5th and 7th Order Harmonics and a Higher Level of Negative Sequence

In order to test the performance of the proposed PCC voltage controller in a more realistic situation, 5th and 7th order harmonics have been included in the grid voltage with a level of $A_5 = 0.01 \cdot A_1$ and $A_7 = 0.03 \cdot A_1$, respectively. Furthermore, a higher level of negative sequence has been chosen (VUF = 10%). Figure 18 shows the temporal evolution of the PCC voltage waveform, validating as well the proper operation of the PCC voltage controller by compensating its negative sequence. The performance of the proposed controller is also observed in Figure 19, which collects the evolution of u_{dq}^{+} (Figure 19a), u_{dq}^{-} (Figure 19b) and the VUF (Figure 19c).

Figure 18. Filtered PCC voltage in *abc*-axes with 5th and 7th order harmonics. (**a**) Representation of the waveforms in t = [0.35, 1] s; and (**b**) in t = [0.35, 0.65] s.

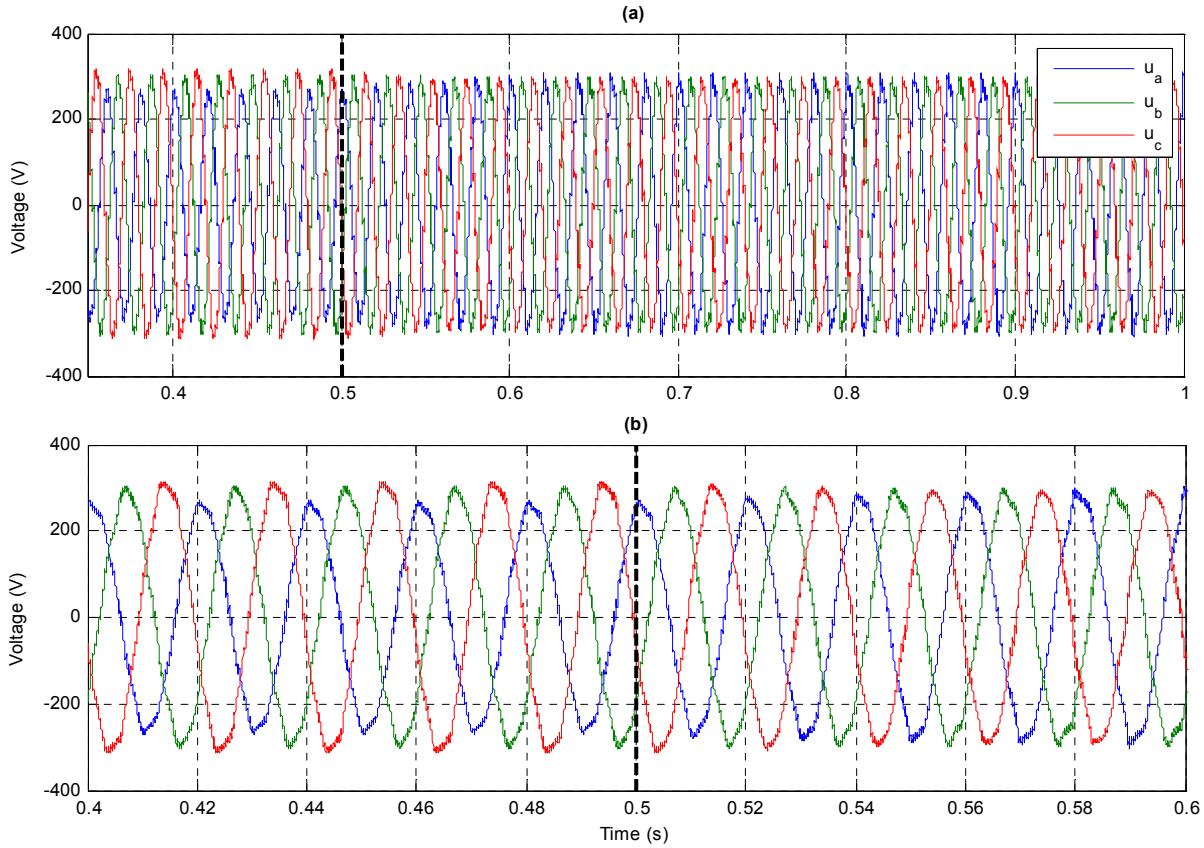


Figure 19. PCC voltage (**a**) positive and (**b**) negative sequences in *dq*-axes when the grid voltage contains 5th and 7th order harmonics. (**c**) VUF (%).

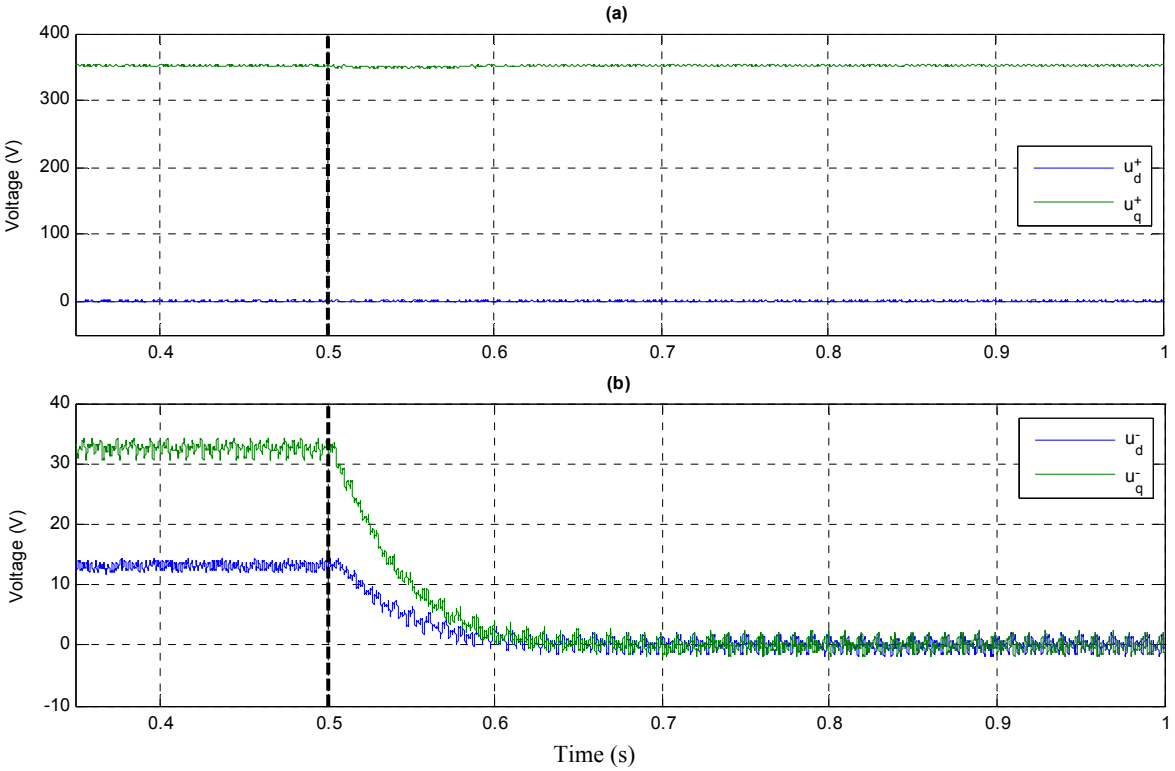
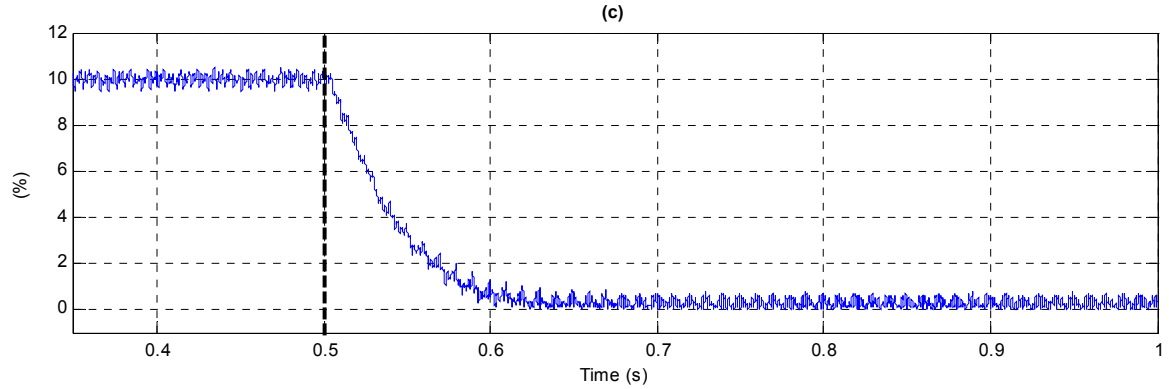


Figure 19. *Cont.*



7. Conclusions

This article has proposed a PCC voltage controller in synchronous reference frame to compensate an unbalanced PCC voltage by means of a STATCOM, allowing an independent control of both positive and negative voltage sequences. To do so, the grid model has been studied under unbalanced conditions, showing the equations that relate voltage and current.

This voltage controller has been placed inside a control scheme to evaluate its performance by means of simulation results. These results have demonstrated the efficacy of this controller, managing to significantly reduce the oscillation present in the DC-link voltage.

However, due to the compensation of the PCC voltage negative sequence, an oscillation appears on the DC-link voltage, with frequency twice the fundamental grid frequency. The magnitude of this oscillation depends on the level of negative sequence. If the level of this oscillation is not permissible, the voltage reference for negative sequence voltage can be set with a value different from zero but still low enough to satisfy regulations when it comes to maximum PCC voltage unbalance. This would result in a reduction of u_{DC} oscillation and DC-link voltage unbalance.

Experimental results have not been provided because the grid at our laboratory is not a weak grid and, even though this could be simulated by increasing the inductance in series with the VSC (thus, increasing the grid impedance), our three-level NPC converter has not been sized for compensating such unbalances.

Acknowledgments

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Conflicts of Interest

The authors declare no conflict of interest.

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