

Article

# Analysis and Performance Comparison of Different Power Conditioning Systems for SMES-Based Energy Systems in Wind Turbines

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**Abstract:** Suitability of energy systems based on Superconducting Magnetic Energy Storage (SMES) has been widely tested in the field of wind energy, being able to supply power in cases such as low wind speeds or voltage dips, and to store energy when there are surpluses. This article analyzes and compares the performance of three SMES-based systems that differ in the topology of power converter: a two-level Voltage Source Converter (VSC), a three-level VSC and a two-level Current Source Converter (CSC). Their performance has been improved by means of an appropriate modulation strategy. To obtain a high reliability and accuracy, a co-simulation between MATLAB/Simulink® (running the control system) and PSIM® (running the power system) has been executed.

**Keywords:** energy storage; superconducting magnetic energy storage; voltage source converter; current source converter

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## 1. Introduction

Energy storage systems are becoming popular in power grids due to their benefits [1]. One of the main goals of all their applications is to keep the grid active power stable in the face of any kind of disturbance that may occur in the power system, since this could spread through the grid and affect or

even damage other power devices. Within these applications, this article addresses three of the most common situations [2]:

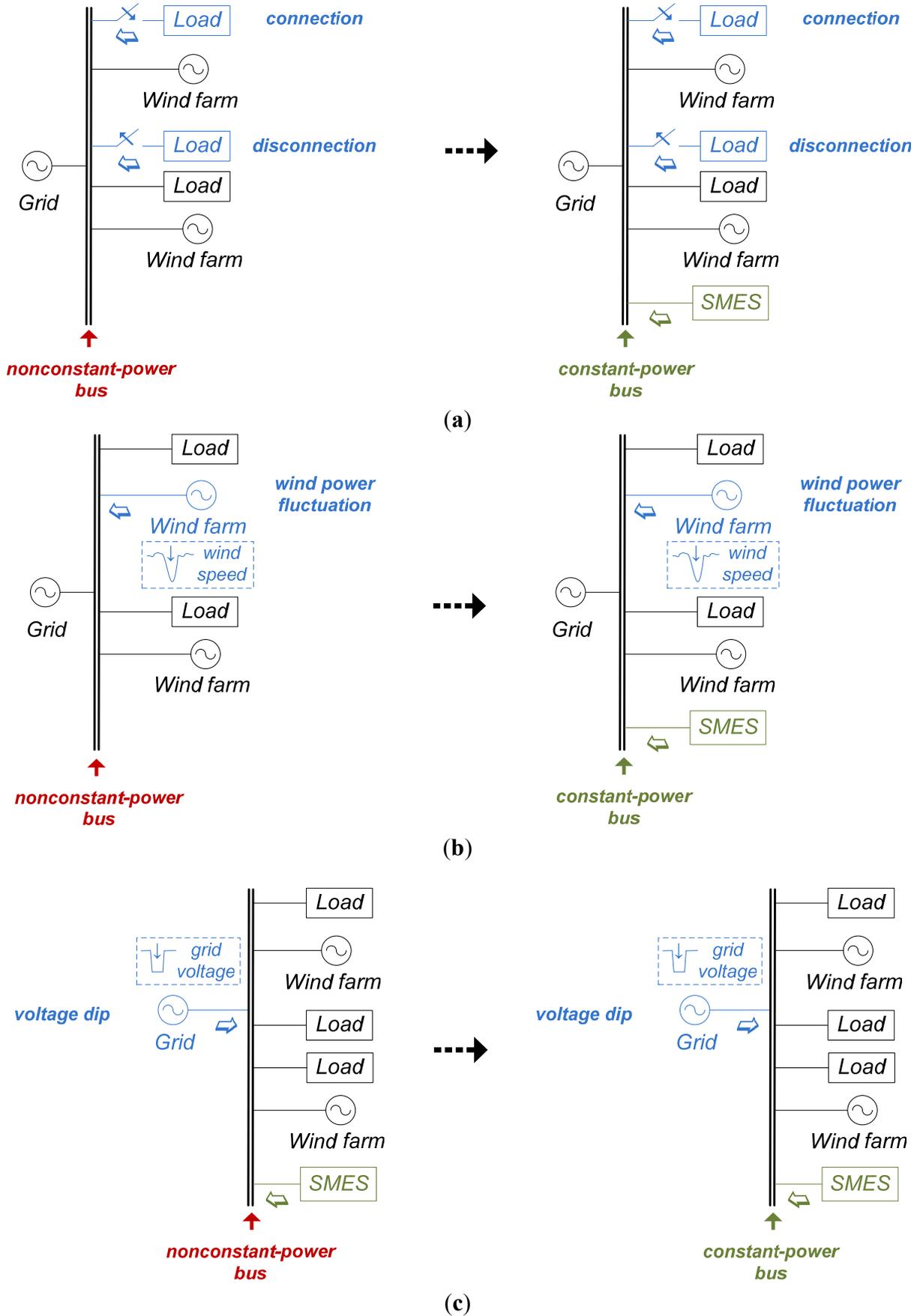
- *Load-step* (Figure 1a), in which a sudden change in the load power takes place. This may be due to critical loads, temporary connection or disconnection of loads, faults in conventional power stations, *etc.* The energy storage system must provide or absorb the energy needed to fill this gap and keep the frequency stable. Existing technology tries to maintain several conventional power stations connected to the grid, working at a low output voltage level, which wastes energy. Therefore, an energy storage system avoids this waste of energy;
- *Load-sharing* [3] (Figure 1b), in which the unpredictability of the wind power makes not possible to control the output power of a wind farm and, consequently, the power can suffer relatively large fluctuations within a short time span. The energy storage system performs the power stabilization by absorbing any fluctuation in the wind energy produced and ensures that these large variations do not reach the grid, in such a way that smooth power is delivered to consumers;
- *Grid-support* [4] (Figure 1c), wherein the voltage dips that can occur in the grid lead to a current increase to maintain the grid power constant. The energy storage system provides the extra power necessary so that the grid power and frequency are affected to a lesser extent. For instance, they can keep industrial processes operating for a given time to avoid production disturbances, which are caused by sudden transients in the power delivered by a national AC grid. Usually, the sizing of an energy storage system depends on the rated power of the wind or photovoltaic farm to which it is linked. It is chosen as a percent of this rated power to give support  $P$ - $f$  (active power–frequency).

This work deals with fast acting devices which store small amounts of energy, such as SMES. The first SMES system was proposed in [5]. The SMES is a large superconducting coil capable of storing electrical energy in the magnetic field generated by a DC current flowing through it [6]. The coil is cryogenically cooled to a temperature below its superconducting critical temperature. This means that ohmic losses during operation will be very low, close to zero.

SMES provides one of the highest densities of any power storage method [2]. An energy storage system of this type can charge and discharge very fast or, said in a different way, it has the ability to absorb or deliver high quantities of power in a very short time. In fact, its high dynamic response (that permits response time in the range of milliseconds) is one of its main advantages [2]. The active power, as well as the reactive power, can be absorbed by or released from the SMES coil according to system power requirements [7].

Another positive aspect about SMES is the life cycle. A coil of this type can withstand tens of thousands of charging cycles. This corresponds to several decades of operation and, compared to battery storage systems, the lifetime is much longer. The need for cooling is an aspect that lowers the efficiency, but the power needed for cooling is far less than the output power of the SMES. Combined with ohmic losses in the non-superconducting devices, the efficiency can exceed 90% (not including the refrigeration system, which continuously requires approximately 1.5 kW per megawatt-hour of storage capacity) [8].

**Figure 1.** Applications of SMES systems: (a) load-step; (b) load-sharing; and (c) grid-support. Left/right-side scheme shows the power system behavior without/with SMES system.



When deciding which converter topology to use to connect the SMES to the grid, aspects as harmonic distortion, usage of reactive power and on-state losses have to be considered [9]. A line-commutated converter using thyristors has low on-state losses and it can handle large amounts of power, but it has lagging power factor and high low order harmonics [10]. Even the twelve-pulse topology has too high total harmonic distortion to meet the standards regarding harmonics [11]. Because of these drawbacks, a self-commutated converter is selected in this work. Even though the on-state losses are higher than for thyristors, these have better characteristics when it comes to harmonics and their reactive power flow can be controlled.

Among self-commutated converters there are mainly two different to choose from, which are studied in this article: Current Source Converter (CSC) [10] and Voltage Source Converter (VSC) [12,13]. CSCs are only available in the market in two-level topology, whereas the VSCs are available from two-level to multi-level topologies. The CSC may seem the most suitable solution as the SMES can be viewed upon as a current source. A CSC is also more efficient when operated in square-wave mode than a PWM VSC [10]. On the other hand, a CSC is more complicated to control than a VSC, it has a high level of low order harmonics and the inductance in the DC side makes the response slower [10].

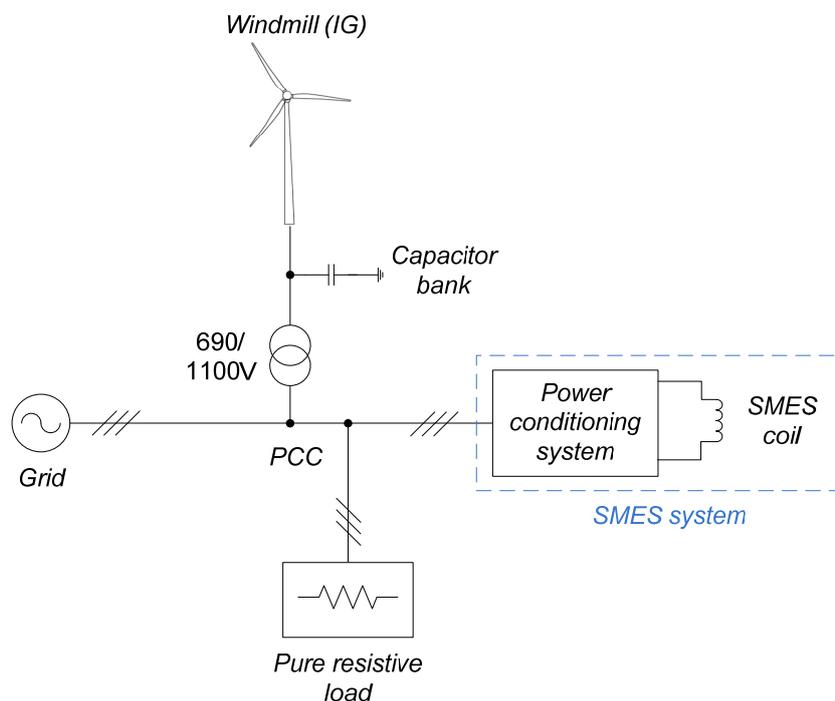
The aim of this work is to conduct a comprehensive comparison of the performance of the SMES-based system depending on the type of power conditioning system, in terms of harmonic content, switching and conduction losses, cost, complexity of control, reactive power usage, *etc.*

The article is organized as follows: Section 1 has provided a brief introduction of the energy storage systems and SMES in particular; Section 2 discusses the detailed description of the system and its components, and analyzes the three operation modes of the system through a given wind profile; Section 3 discusses the three power conditioning systems: two-level CSC, two-level VSC and three-level VSC. Their structures are analyzed, specifying their grid filters and detailing their advantages and drawbacks; the design of the control systems is carried out in Section 4, as well as the specification of the interconnection of each individual control loop and the modulation strategy for each converter; simulation results are firstly shown for an ideal wind speed profile in Section 5, and secondly the performance of each power conditioning system is compared for each of the aforementioned applications (load-step, load-sharing and grid-support); finally, conclusions are given in Section 6.

## 2. Description of the System

Figure 2 shows the general scheme of the system under investigation in this work, which consists of:

- A three-phase pure resistive load demanding a constant power of 1.5 MW connected to the grid;
- A 2 MW variable-speed Wind Turbine (WT) based on an Induction Generator (IG; the Induction Generator parameters are listed in Table 1) plus a capacitor bank connected to the Point of Common Coupling (PCC) through a 690/1100 V transformer;
- An SMES system composed by a superconducting coil and a power conditioning system. This power conditioning system consists of one of the power converters mentioned in the introduction plus a grid filter, which is an L-filter for the VSCs and a C-filter for the CSC;
- The line-to-line rms grid voltage is 1100 V and the grid frequency is 50 Hz.

**Figure 2.** Schematic representation of the system under investigation.**Table 1.** Induction generator parameters.

Parameter	Value	Units
Stator resistance	0.01379	p.u.
Stator inductance	0.04775	p.u.
Rotor resistance	0.007728	p.u.
Rotor inductance	0.04775	p.u.
Mutual inductance	2.416	p.u.
Inertia constant	5	s
Friction factor	0.008726	p.u.
Pole pairs	2	-

### 2.1. Operation Modes of the System

The SMES coil works as an active power compensator in three different operation modes:

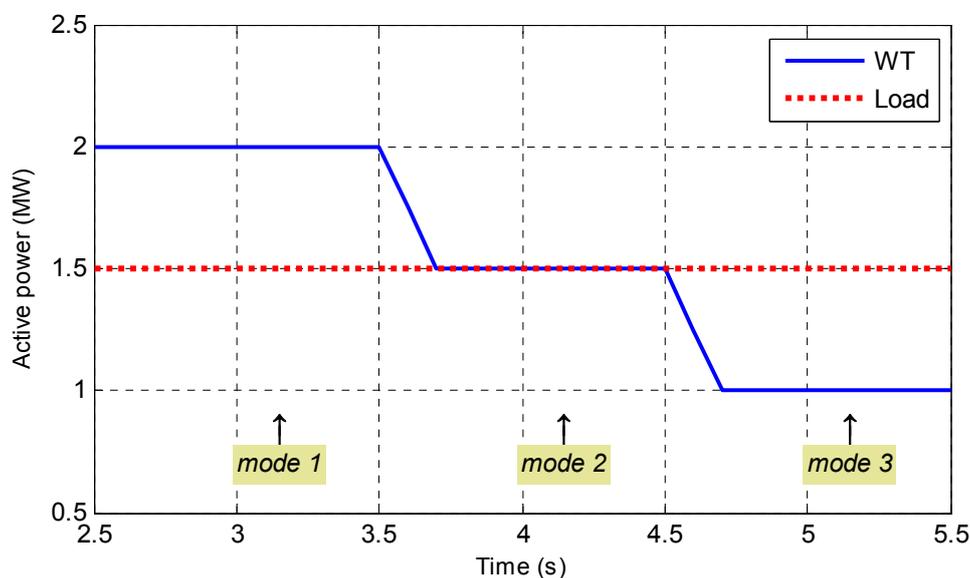
- *WT output power is higher than the reference power (mode 1):* this reference power can be the load power, calculated by means of the measured current and voltage and applying the PQ-theory [14], or any other power level specified by the grid operator. In this mode, the current through the coil increases and so does the stored energy, since it is absorbing the extra power from the IG.
- *WT output power is equal to the reference power (mode 2):* power does not flow through the SMES coil. The current remains constant at the same level that it had before both powers became equal.
- *WT output power is lower than the reference power (mode 3):* the current through the coil decreases and so does the stored energy, since the system supplies the necessary power to the grid to equal the reference power.

## 2.2. Profile of the Wind Turbine Output Power

In order to show all the different operation modes of the superconducting coil, an ideal wind speed profile that consecutively enables all of them has been applied in the simulations. The possible noise introduced by a real wind speed profile would be absorbed by the DC-link. Figure 3 shows the shape of the ideal profile of the WT output power along with the load power. The different operation modes of the SMES system are:

- In  $t = 2.5$  s the WT power is bigger than the load (or reference) power (*mode 1*).
- In  $t = 3.5$  s the WT power decreases to equal the load power (*mode 2*).
- In  $t = 4.5$  s the WT power becomes lower than the load power (*mode 3*).

**Figure 3.** Ideal profile of the WT output power and the load power.



## 3. Power Conditioning System

### 3.1. System Based on a Two-Level VSC

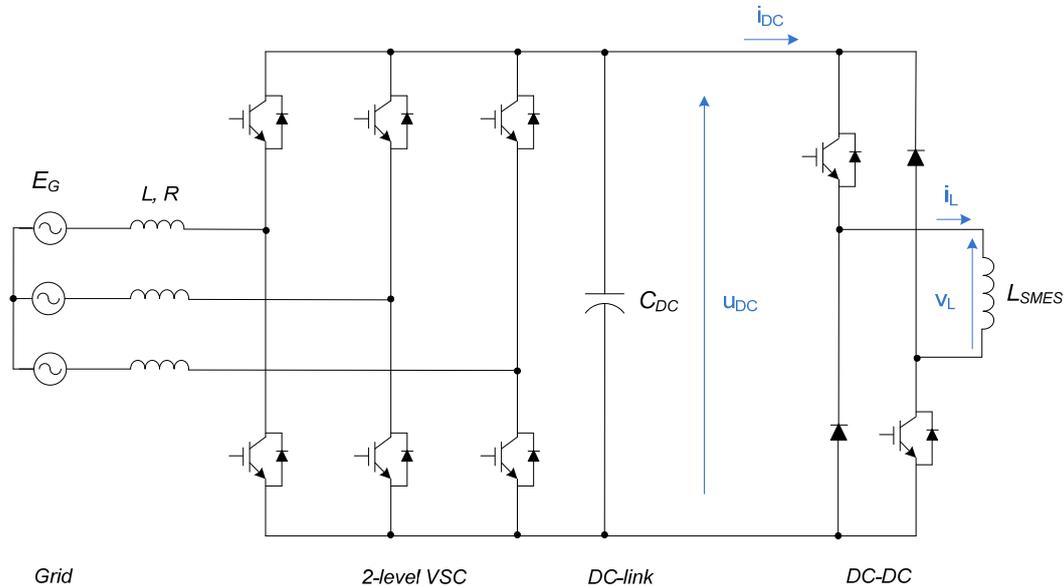
Three-phase VSCs became popular in high-power and high-performance applications because they provide constant DC-link voltage, low harmonic distortion of the utility currents, bidirectional power flow and controllable power factor [11]. Because of these features, they are becoming increasingly popular in high-power or high-performance applications. Furthermore, many well-established and widespread control strategies have been proposed for this relatively simple topology.

A DC-DC converter is needed between the VSC and the superconducting coil in order to adapt the voltage levels of the DC-link and the coil, increasing the complexity of the control structure.

Figure 4 shows an overview of the power conditioning system, where  $E_G$  is the grid voltage (1100 V);  $L$  is the sum of the L-filter inductance ( $L_F = 0.675$  mH) connected between the VSC and the PCC and the grid inductance ( $L_G = 10$   $\mu$ H);  $R$  is the sum of the equivalent resistance of the L-filter ( $R_F = 1.781$  m $\Omega$ ) and the grid resistance ( $R_G = 1$  n $\Omega$ );  $L_{SMES}$  is the SMES coil (1 H),  $i_L$  is the current through the SMES coil;  $v_L$  is the voltage in the SMES coil;  $C_{DC}$  is the DC-link capacitor (7.5 mF) and  $u_{DC}$  is the DC-link

voltage, which has been set to 1800 V. This choice has been made knowing that the natural DC-link voltage is  $u_{DC,nat} = E_G \cdot \sqrt{2} \approx 1555$  V and, therefore,  $u_{DC}$  must be higher than  $u_{DC,nat}$  to ensure a correct power transfer between the AC side and the DC side with a reasonable safety margin.

**Figure 4.** Power conditioning system based on a two-level VSC.



The two-level VSC consists of three legs of two active switches (IGBTs) with antiparallel diodes. The DC-DC converter (or chopper) consists of two legs, each of them formed by an IGBT with antiparallel diode plus a diode.

If the DC-link voltage is always positive and with value  $u_{DC}$ , the DC-DC converter is the way of controlling the sign of the voltage  $v_L$ . Its switches are both on or off at the same time. Bidirectional power flow of the converter is achieving by reversing the DC current ( $i_{DC}$ ) polarity.

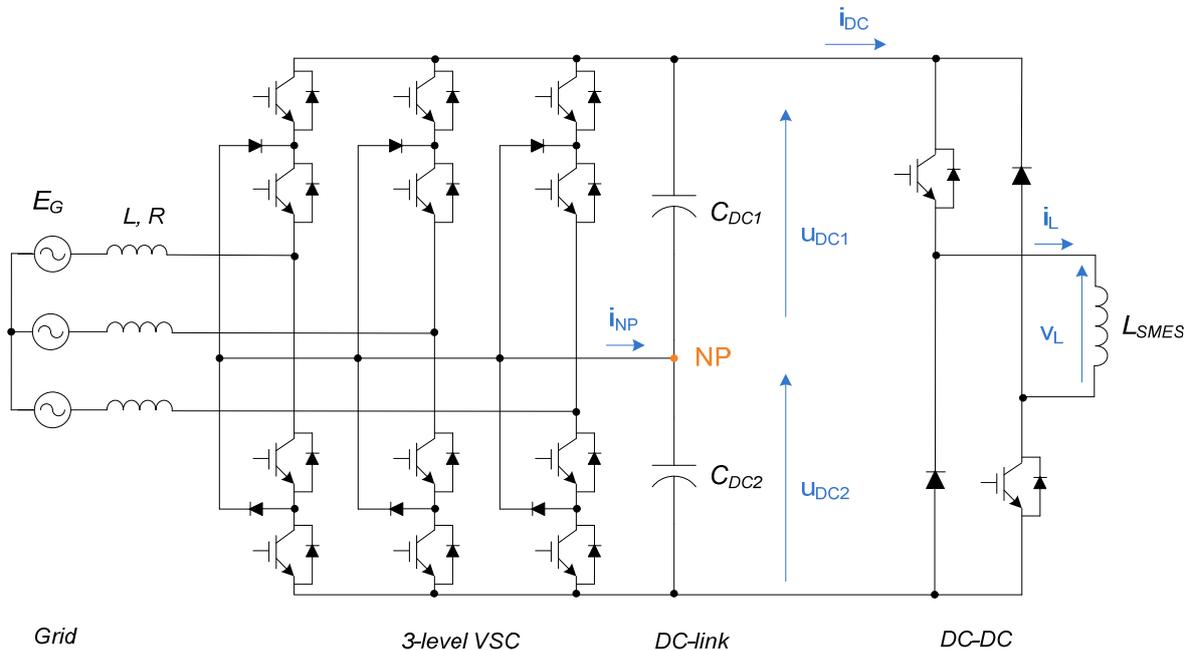
### 3.2. System Based on a Three-Level VSC

Figure 5 shows an overview of the power conditioning system, where  $E_G$  is the grid voltage (1100 V);  $L$  is the sum of the L-filter inductance ( $L_F = 0.675$  mH) connected between the VSC and the PCC and the grid inductance ( $L_G = 10$   $\mu$ H);  $R$  is the sum of the equivalent resistance of the L-filter ( $R_F = 1.781$  m $\Omega$ ) and the grid resistance ( $R_G = 1$  n $\Omega$ );  $L_{SMES}$  is the SMES coil (1H);  $i_L$  is the current through the SMES coil;  $v_L$  is the voltage in the SMES coil and  $C_{DC1}$  and  $C_{DC2}$  are the DC-link capacitors ( $C_{DC1} = C_{DC2} = 15$  mF).  $u_{DC1}$  and  $u_{DC2}$  are the voltages across each DC-link capacitor. If the VSC control is working properly, they must have the same value. The DC-link voltage is defined as:

$$u_{DC} = u_{DC1} + u_{DC2} \quad (1)$$

being set to 1800 V.

The AC-DC converter is a three-level Neutral Point Clamped (NPC) converter. Each converter leg consists of four active switches with four antiparallel diodes [12,15]. In practice, either IGBT or GCT can be employed as a switching device. On the DC side of the converter, the DC-link capacitor is split into two, providing a neutral point (NP). The diodes connected to the NP are the clamping diodes.

**Figure 5.** Power conditioning system based on a three-level VSC (NPC converter).

The three-level NPC converter has some advantages over the two-level topology: (a) No dynamic voltage sharing problem: each of the switches in the NPC converter withstands only half of the total DC voltage during commutation; (b) Static voltage equalization without using additional components: the static voltage equalization can be achieved when the leakage current of the top and bottom switches in a converter leg is selected to be lower than that of the inner switches; (c) Low THD and  $dv/dt$ : the waveform of the line-to-line voltages is composed of five voltage levels, which leads to lower THD and  $dv/dt$  in comparison to the two-level converter operating at the same voltage rating and device switching frequency.

However, the NPC converter has some drawbacks such as the additional clamping diodes, a more complicated PWM switching pattern design and possible deviation of neutral point voltage. The capacitors can be charged or discharged by neutral current  $i_{NP}$ , causing NP voltage deviation. It might appear a ripple of frequency three times the fundamental in  $u_{DC1}$  and  $u_{DC2}$  that can destroy components if both DC-link voltages are not balanced.

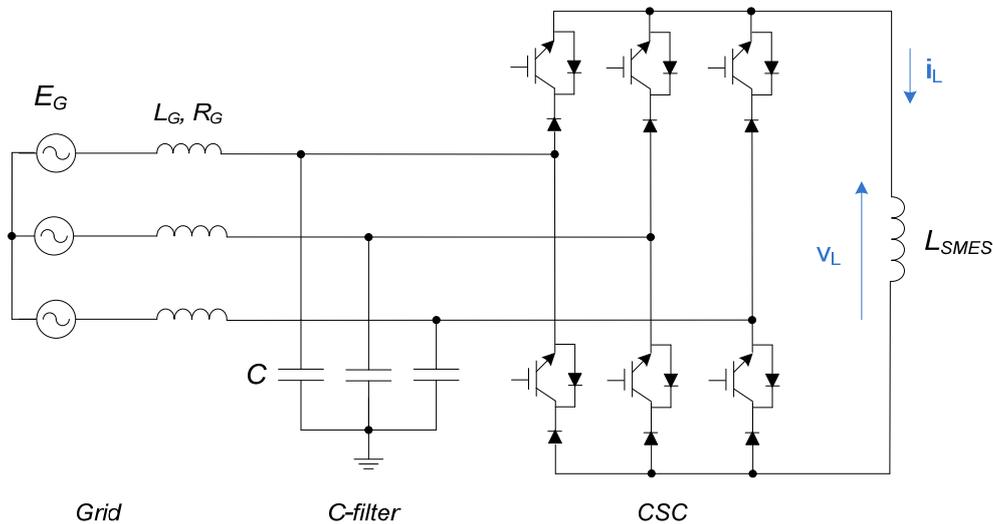
### 3.3. System Based on a Two-Level CSC

As stated earlier, CSCs may seem the most suitable solution for SMES systems as the SMES can be viewed upon as a current source. This converter has also proved to be the more suitable for delivering active and reactive power quickly into the network [16]. A CSC is also more efficient when operated in square-wave mode than a PWM VSC [17]. On the other hand, a CSC is more complicated to control than a VSC [18], it has a high level of low order harmonics and the inductance in the DC side makes the response slower.

Figure 6 shows an overview of the power conditioning system, where  $E_G$  is the grid voltage (1100 V);  $L_G$  is the grid inductance (10  $\mu$ H);  $R_G$  is the grid resistance (1 n $\Omega$ );  $L_{SMES}$  is the SMES coil (1 H);  $i_L$  is the current through the SMES coil;  $v_L$  is the voltage in the SMES coil and  $C$  is the C-filter capacitor

(6 mF). The aim of this bank of capacitors is to assist the commutation of the switching devices [10] and to provide a current path for the energy trapped in the inductance of each phase. Otherwise, a high-voltage spike would be induced, causing damages to the switching devices. It also acts as a harmonic filter, improving the load current and voltage waveforms.

**Figure 6.** Power conditioning system based on a two-level CSC.



Each leg of the CSC consists of two IGBTs and two blocking diodes. Bidirectional power flow is achieved by reversing the DC voltage polarity. Therefore, a CSC needs a blocking diode connected in series with the switching device in absence of reverse blocking capabilities in a normal IGBT. The DC side of the CSC is directly connected to the superconducting coil, and its AC side is connected to the PCC through the C-filter.

## 4. Control and Modulation Strategies

### 4.1. System Based on a Two-Level VSC

#### 4.1.1. Control System

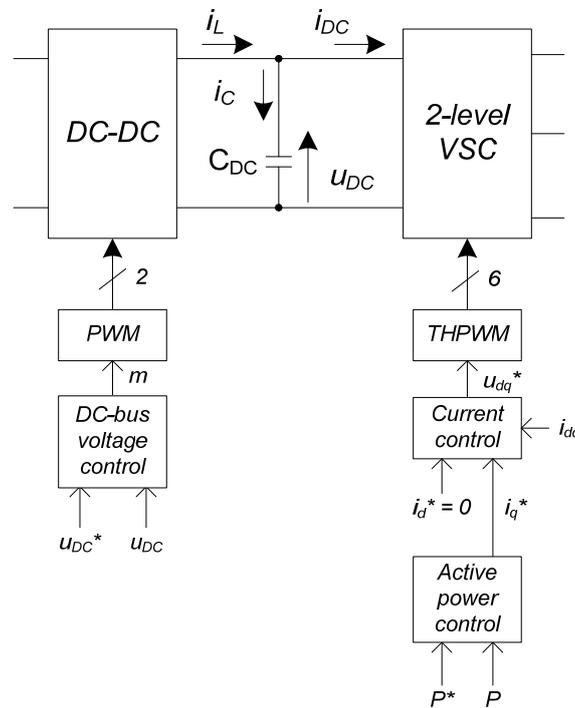
Figure 7 shows the block diagram of the control system, which consists of three controllers: DC-link voltage controller (corresponding to the DC-DC converter control system), current controller and active power controller (both corresponding to the VSC control system).

A Phase-Locked Loop (PLL) [19] performs the synchronization of the PCC voltage vector with the  $d$ -axis, so the component  $e_d$  is zero and the equations for active and reactive power become:

$$P = e_q i_q \quad Q = e_q i_d \quad (2)$$

where  $e_q = E_G = 1100$  V.

**Figure 7.** Overview of the control system of the power conditioning system based on a two-level VSC.



#### 4.1.1.1. DC-link Voltage Controller

The DC-link is an interface between the VSC and the DC-DC converter. The power equation is given by Equation (3), taking into account that the  $q$ -axis is aligned with the voltage space vector and neglecting the converter losses:

$$P = u_{DC}i_{DC} = e_q i_q \tag{3}$$

The application of Kirchoff current law to the DC-link node (see Figure 7) yields the following expression for the current in the DC-link capacitor:

$$i_c = i_L - i_{DC} \tag{4}$$

where  $i_L$  is the current in the SMES coil and  $i_{DC}$  is the current in the VSC. Combined with Equation (3) leads to a multivariable nonlinear equation, which is linearized around a steady state operating point [20]. After simplifying, the linearized expression is reduced to:

$$C \frac{d\Delta u_{DC}}{dt} = \Delta i_L \tag{5}$$

Laplace transform is applied to obtain the continuous-time transfer function, which is the plant model to the DC-link voltage controller:

$$G(s) = \frac{\Delta u_{DC}}{\Delta i_L} = \frac{1}{sC_{DC}} \tag{6}$$

A Proportional Integral (PI) controller is enough to obtain zero steady-state error, since  $u_{DC}$  is a constant voltage. This controller has directly been designed in discrete-time because it is going to be

implemented on a digital platform. Therefore, it is necessary to discretize the plant transfer function in order to design the discrete-time controller.

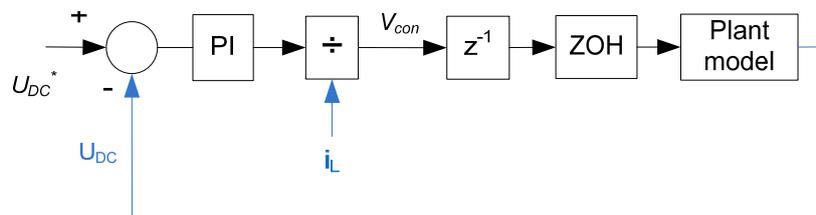
The method that has been used is Zero-Order Hold (ZOH) because the discrete-time transfer function generated with it has a behavior close to the continuous time transfer function. The discrete transfer function obtained is shown in Equation (7), where  $\mathbb{Z}$  means  $z$ -transform. The proportional and integral constants ( $K_P$  and  $K_I$ , respectively) of the controller are calculated as shown in Equation (8), thus obtaining two complex conjugate poles in the open-loop transfer function;  $T_s$  is the sampling period;  $\rho = e^{-\xi\omega_n T_s}$  and  $\theta = \omega_n T_s \sqrt{1 - \xi^2}$  ( $\xi$  is the damping factor; and  $\omega_n$  is the natural pulsation):

$$G(z) = (1 - z^{-1})\mathbb{Z}\left\{\frac{G(s)}{s}\right\} = \frac{0.0133}{z - 1} = \frac{a}{z - 1} \tag{7}$$

$$K_P = \frac{2(1 - \rho \cos \theta)}{a} \quad K_I = \frac{\rho^2 - 1 + K_P a}{aT_s} \tag{8}$$

Figure 8 shows the structure of the complete system. The blue lines represent the measurements, like the DC-link voltage and the coil current. The PI output needs to be scaled with the coil current (thus obtaining the modulation index). The block  $z^{-1}$  represents the computational delay associated to the control implementation on the digital platform.

**Figure 8.** DC-link voltage controller connected to the system.



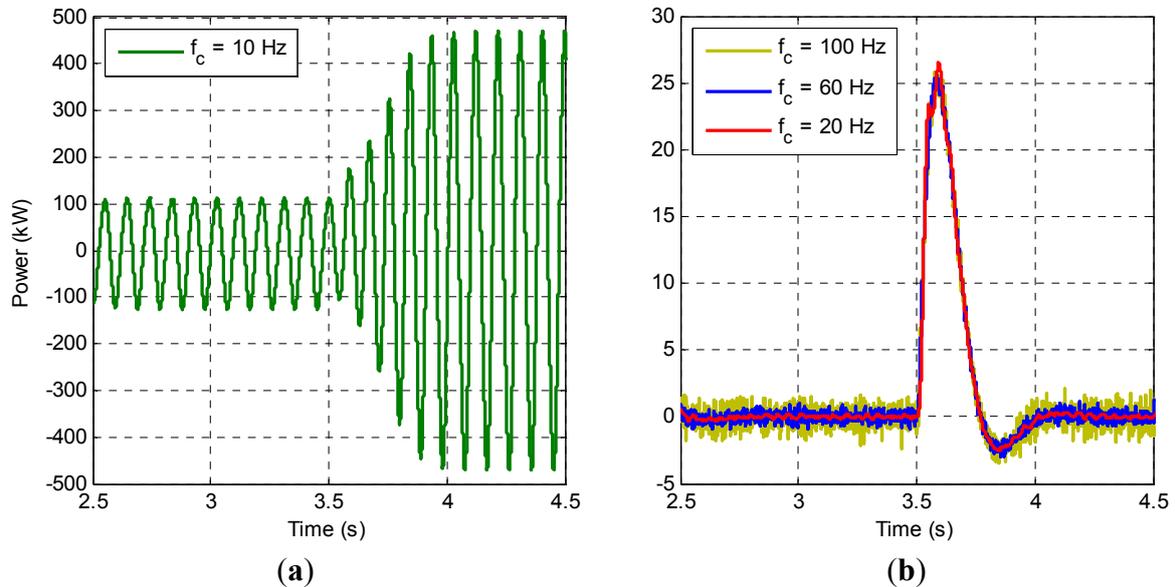
#### 4.1.1.2. Active Power Controller

The control system of the VSC consists of two cascaded linear controllers. The outer control loop is the active power control, whereas the inner control loop is the current control. The active power control regulates the magnitude and direction of the active power flux according to a specific reference. The active power reference is calculated as the difference between the load active power ( $P_{load}$ ) and the WT active power ( $P_{WT}$ ). This difference is negative if there is an energy surplus (*mode 1*), zero if the powers are balanced (*mode 2*) and positive if there is an energy demand (*mode 3*).

Knowing that the active power can be divided into two parts, one constant and another one oscillating [13], the SMES system handles only the constant power. Therefore, a low-pass filter is placed after the error calculation in order to eliminate the oscillating power, yielding  $\bar{e}$ . It is very important to choose well the value of the filter cut-off frequency because the active power reference  $P^*$  may oscillate excessively if this frequency is too low. A good filtering will be achieved if the cut-off frequency is low, but its settling time will be too high and it can affect the control dynamics. This case scenario is shown in Figure 9a, wherein an excessively low cut-off frequency (10 Hz) causes the oscillation of the active power control. Figure 9b shows that frequencies above 20 Hz lead to a stable control loop. In this figure, a ramped jump in  $P_{WT}$  has been applied at  $t = 3.5$  s to test the transient

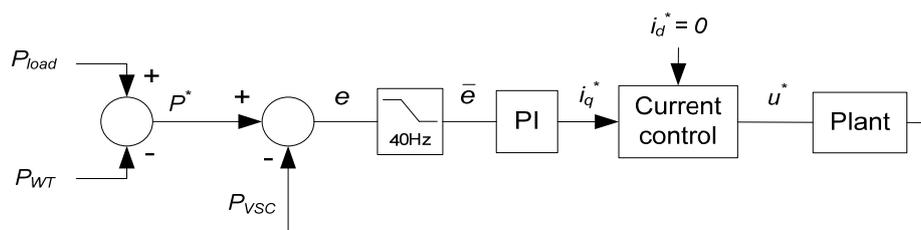
behavior of the controller. A good trade-off between settling time (speed response) and filtering capabilities is achieved with a cut-off frequency of 40 Hz. This way, the low-pass filter does not have to be taken into account in the design of the controller.

**Figure 9.** Effect of the cut-off frequency of the low-pass filter in the error of the active power control.



If the dynamics of the current controller is much faster than that of the active power controller, that is to say, if the current controller is at least 10 times faster than the power controller, this inner controller may be omitted in the design of the outer. Thus, we have two cascaded linear controllers. If we take a look at Equation (2), it is clear that the relationship between the active power and  $i_q$  is described by Equation (9). The plant model in discrete time is equal to the continuous time one, since it is only a constant. The proportional constant of the PI controller is related to the transformation of active power to active current reference, whereas the integral constant helps achieve zero steady-state error in the event of model mismatch and disturbances. Therefore, the parameter tuning is focused on settling time and controller bandwidth. Figure 10 shows the block diagram of this control. This work does not deal with reactive power compensation, therefore its current reference is set to zero ( $i_d^* = 0$ ).

**Figure 10.** Block diagram of the active power control.

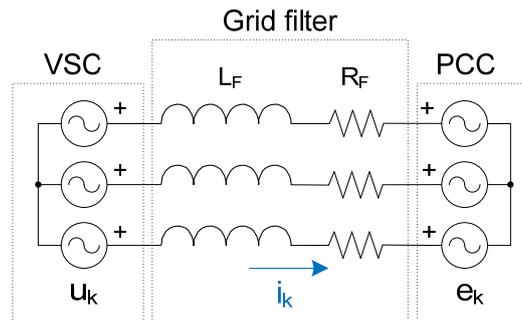


$$G(s) = \frac{P(s)}{i_q(s)} = e_q = 1100 \text{ V} \tag{9}$$

4.1.1.3. Current Controller

Given that a VSC is a controlled voltage source, Figure 11 shows the equivalent model of the system from the point of view of grid-connection, where  $u_k$  ( $k \in \{a, b, c\}$ ) is the VSC output voltage;  $e_k$  is the PCC voltage;  $L_F$  and  $R_F$  are the L-filter parameters; and  $i_k$  is the current flowing through the filter. This model is described by Equation (10) in continuous time.

Figure 11. Equivalent model of the system.



$$u_k(s) = (R_F + L_F s) i_k(s) + e_k(s) \tag{10}$$

In order to obtain the plant model for the current control, the PCC voltage is considered as a perturbation. Therefore, the relationship between the VSC output voltage and the current is given by Equation (11):

$$G(s) = \frac{i_k(s)}{u_k(s)} = \frac{1}{R_F + L_F s} \tag{11}$$

The ZOH method has been used to discretize Equation (11), giving rise to Equation (12):

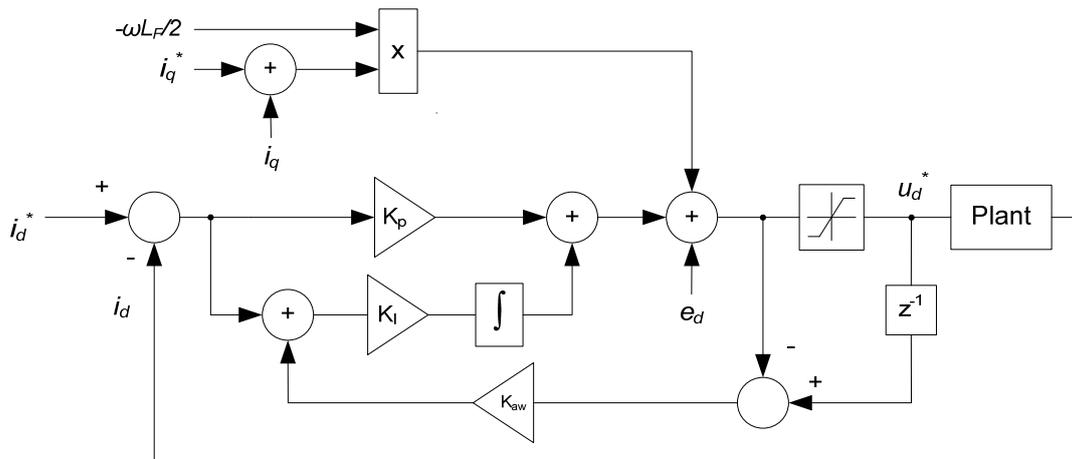
$$G(z) = (1 - z^{-1}) \mathbb{Z} \left\{ \frac{G(s)}{s} \right\} = \frac{a}{z - b} \tag{12}$$

where  $a = e^{-R_F T_s / L_F}$ ,  $b = a / R_F$ ; and  $T_s$  is the sampling period.

Figure 12 shows the  $d$ -axis current controller block diagram. The  $q$ -axis controller has the same structure. In each axis there is a PI controller with an antiwindup scheme ( $K_{aw} = 1 / K_p$ ) and a feedforward of the PCC voltage. The PI integrator has been implemented in the Euler Forward form. A cross-coupling of value  $\omega L_F$  exists between  $d$  and  $q$  axes, where  $\omega = 2\pi 50$  rad/s. This cross-coupling is small, affecting during transients, when  $\omega$  changes. This can be compensated by adding the product  $-(i_q^* + i_q) \frac{\omega L_F}{2}$  to the output of the PI controller for  $d$ -axis, and its equivalent for the  $q$ -axis [21]. The PI parameters are tuned according to Equation (13), where  $\rho = e^{-\xi \omega_n T_s}$  and  $\theta = \omega_n T_s \sqrt{1 - \xi^2}$  ( $\xi$  is the damping factor and  $\omega_n$  is the natural pulsation):

$$K_p = \frac{b + 1 - 2\rho \cos \theta}{a} \quad K_I = \frac{\rho^2 - b + K_p a}{a T_s} \tag{13}$$

Figure 12. Block diagram of the  $d$ -axis current controller.



#### 4.1.2. Modulation Strategies

The DC-DC converter modulation is accomplished by comparing a DC control voltage ( $V_{con}$ ) with a triangular voltage ( $V_{tri}$ ).  $V_{con}$  can be found in Figure 8 and it is calculated as the division between the output of the DC-link voltage controller and the coil current  $i_L$  (this division is saturated to  $\pm 1$ ).

$V_{tri}$  is defined between  $-1$  and  $+1$ . Defining the modulation index as:

$$m_a = \frac{V_{con}}{\hat{V}_{tri}} \tag{14}$$

where  $m_a$  can attain values between  $-1$  and  $+1$  [7]. The commutation frequency of the DC-DC converter is  $f_{sw\_dc} = 5$  kHz.

The three states of the coil can be described using  $m_a$ :

- $m_a > 0$ : the coil is in the charge state (*mode 1*).
- $m_a = 0$ : the coil is in steady-state (*mode 2*).
- $m_a < 0$ : the coil is in the discharge state (*mode 3*).

During the different states the current does not have a completely constant increase or decrease. But on average it increases when  $m_a$  is greater than zero and decreases when it is less than zero. In steady-state mode the charge period of the coil is equal to the discharge period, and the current fluctuates around a certain value.

The VSC modulation is a Third Harmonic injection Pulse Width Modulation (THPWM) [11]. A major limitation with the three-phase converter modulation is the reduced maximum peak fundamental output line voltage of  $\sqrt{3}u_{DC}$  that can be obtained compared to the available DC-link voltage [22]. The maximum modulation index of a three-phase converter PWM system can be increased by including a common third-harmonic term into the target reference waveform of each phase leg [23]. This third harmonic component does not affect the fundamental output voltage, since the common mode voltages cancel between the phase legs, but it does reduce the peak size of the envelope of each phase leg voltage. Hence the modulation index can be increased beyond 1 without moving into overmodulation. Overmodulation is known to produce low-frequency baseband distortion and is to be avoided if possible. A 15% increase in modulation index can be achieved by simply

including a one-sixth third-harmonic injection into the fundamental reference waveforms. The commutation frequency is  $f_{sw\_vsc} = 2.5$  kHz.

#### 4.2. System Based on a Three-Level VSC

##### 4.2.1. Control System

The control system for the three-level VSC has exactly the same structure and values as in the two-level VSC (Section 4.1.1).

##### 4.2.2. Modulation Strategy

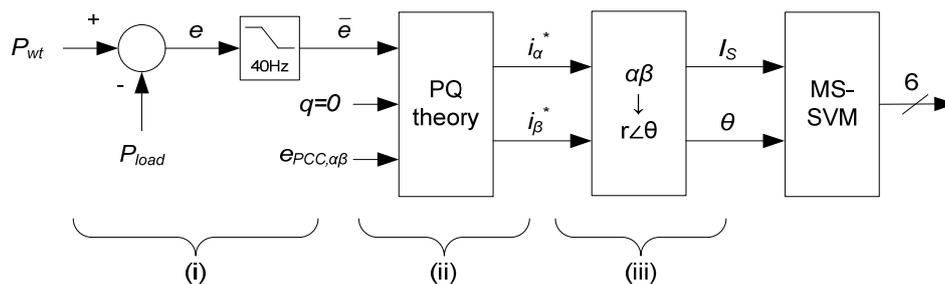
The three-level VSC modulation is accomplished in a very similar way as in the two-level VSC (Section 4.1.2). The only difference is that now there are two carriers per converter leg instead of one. One carrier is a triangular signal whose limit values are 1 and 0, and the other carrier is a triangular signal whose limit values are 0 and  $-1$ . The commutation frequency is  $f_{sw\_vsc} = 2.5$  kHz. In the case of the two-level VSC modulation, the only carrier is a triangular signal whose limit values are  $+1$  and  $-1$ .

#### 4.3. System Based on a Two-Level CSC

##### 4.3.1. Control System

Figure 13 shows the block diagram of the steps that have to be done to obtain the reference currents needed for the CSC modulation, which can be divided into three stages: (i) error calculation; (ii) calculation of current references in  $\alpha\beta$ -axes; and (iii) transformation to polar coordinates.

**Figure 13.** Block diagram of the reference current calculation and connection to the CSC modulator.



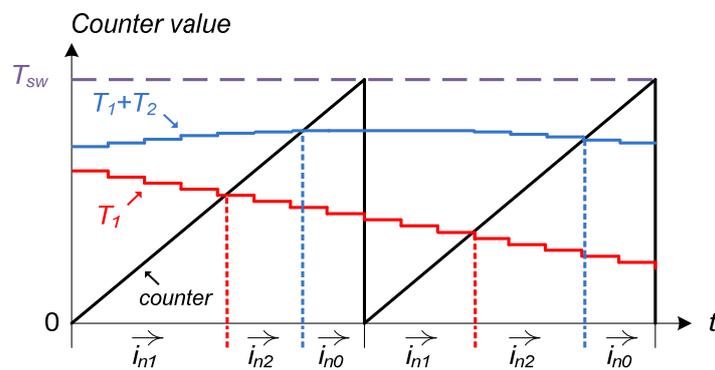
Since the average error  $\bar{e}$  only contains a DC component, a low-pass filter is enough to separate this part from the oscillating part  $\tilde{e}$ . The equation corresponding to the *PQ-theory* block is shown in Equation (15), where  $e_\alpha$  and  $e_\beta$  are the PCC voltages expressed in  $\alpha\beta$ -axes. This  $abc \rightarrow \alpha\beta$  transformation (Clarke transformation) is amplitude-invariant. It is necessary to maintain the same amplitude when changing the reference axes because afterwards the modulation index is calculated based on the current magnitude. Once the reference currents in  $\alpha\beta$ -axes are calculated, they are transformed to polar coordinates in order to separate the magnitude ( $I_s$ ) of the phase ( $\theta$ ):

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} \bar{p} \\ q \end{bmatrix} \tag{15}$$

4.3.2. Modulation Strategy

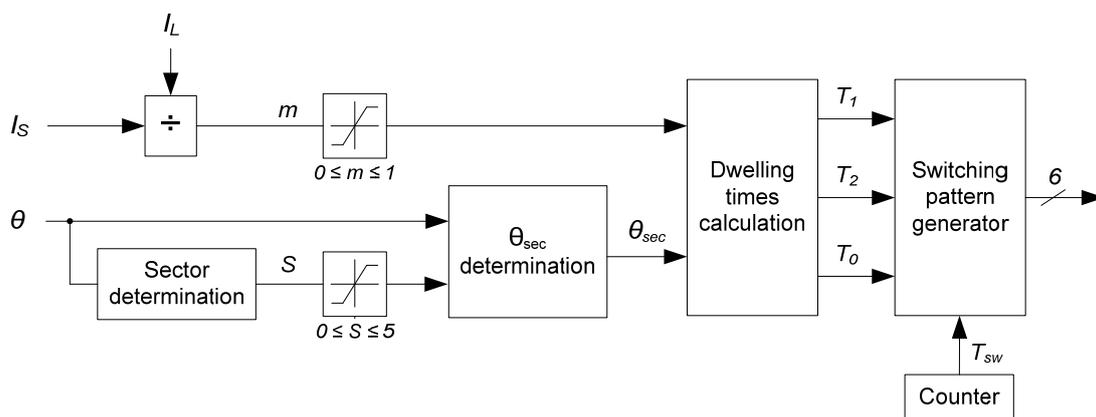
Multi Sampling-Space Vector Modulation [24] (MS-SVM) has been used in this work, which was proposed to substantially suppress the low-order harmonics in practical CSC-based drives [10]. Figure 14 illustrates the studied MS-SVM method. The basic idea is that, compared to conventional SVM [25], the vector angle sampling and the calculation of dwelling times ( $T_1$ ,  $T_2$  and  $T_0$ ) are performed more frequently. This is regulated by the sampling ratio  $SR = T_{sw}/T_s$ , where  $T_s$  is the sampling period and  $T_{sw}$  is the switching period (counter period), in a way that all the calculations are performed  $SR$  times in each counter period.

Figure 14. Vector selection in MS-SVM [24].



Similar to the conventional SVM, whose scheme is depicted in Figure 15, the number of counter periods within one sector in MS-SVM should be an integer number to eliminate nonperiodic harmonics and, moreover, it should be a multiple of six to eliminate triple harmonics. In order to verify this, the sampling ratio has been chosen as  $S_R = 8$ , being the switching frequency  $f_{sw} = 3.6$  kHz. This way, the ratio  $f_{sw}/f_0 = 3,600/50 = 72$  is an integer number and a multiple of six. The sampling frequency for the given  $SR$  is  $f_s = 28.8$  kHz ( $T_s = 34.7$   $\mu$ s), and it is considerably higher than that for the VSC. However, nowadays most digital processors are able to have these runtimes deterministically. This frequency was chosen because the fact of making a multisampling optimizes the system performance, but if the processor requirements force to handle a lower sample rate, the steady-state operation of the equipment is not penalized.

Figure 15. Scheme of the SVM modulator for a CSC.



### 5. Simulation Results and Discussion

The results shown in this Section are divided into four sets, namely, (a) basic simulation to the test the three operation modes of the system, (b) load-step, (c) load-sharing and (d) grid-support. The parameters for all of them are detailed in Table 2 (VSC-based systems) and Table 3 (CSC-based system), where  $K_P$  is the proportional gain,  $K_I$  is the integral gain and  $K_{AW}$  is the antiwindup gain.

**Table 2.** Simulation parameters of the VSC-based systems.

Grid impedance		Grid filter		Sampling & switching		DC-link control		Current control	Power control
$L_G$	0.01 mH	$L$	0.675 mH	$f_S$	2.5 kHz	$K_P$	3.4494	0.7775	0.0002
$R_G$	1 nΩ	$R$	1.781 mΩ	$f_{SW}$	5 kHz	$K_I$	775.46	0.2535	0.13
		-				$K_{AW}$	-	0.6475	-

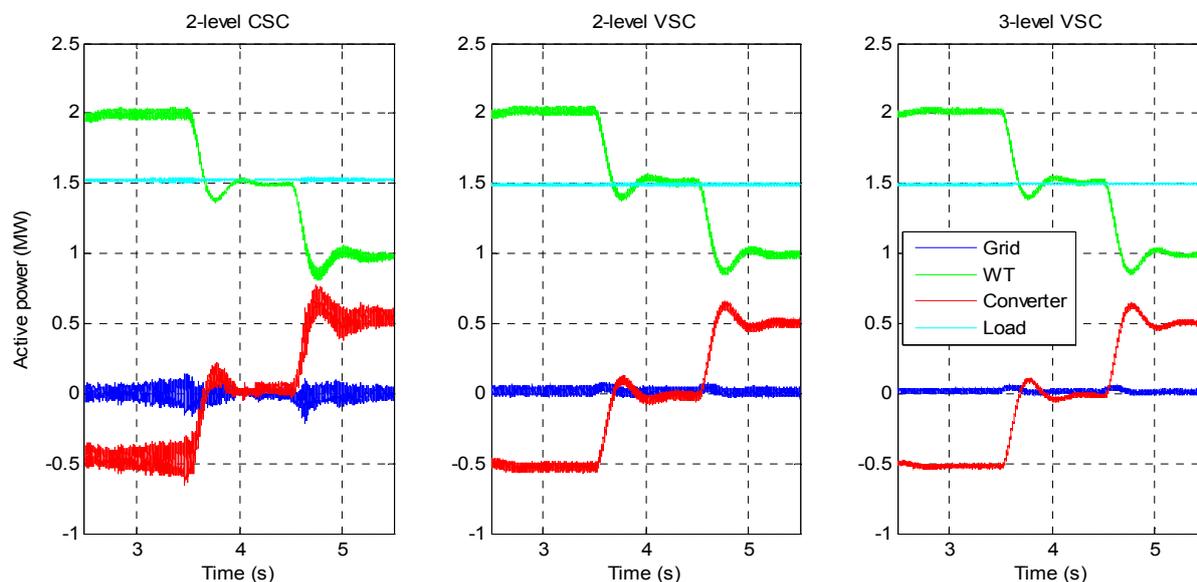
**Table 3.** Simulation parameters of the CSC-based system.

Grid impedance		Grid filter		Sampling & switching	
$L_G$	0.01 mH	$C$	10 mF	$f_S$	28.8 kHz
$R_G$	1 nΩ	-		$f_{SW}$	3.6 kHz

#### 5.1. Basic Simulation to Test the Three Operation Modes of the System

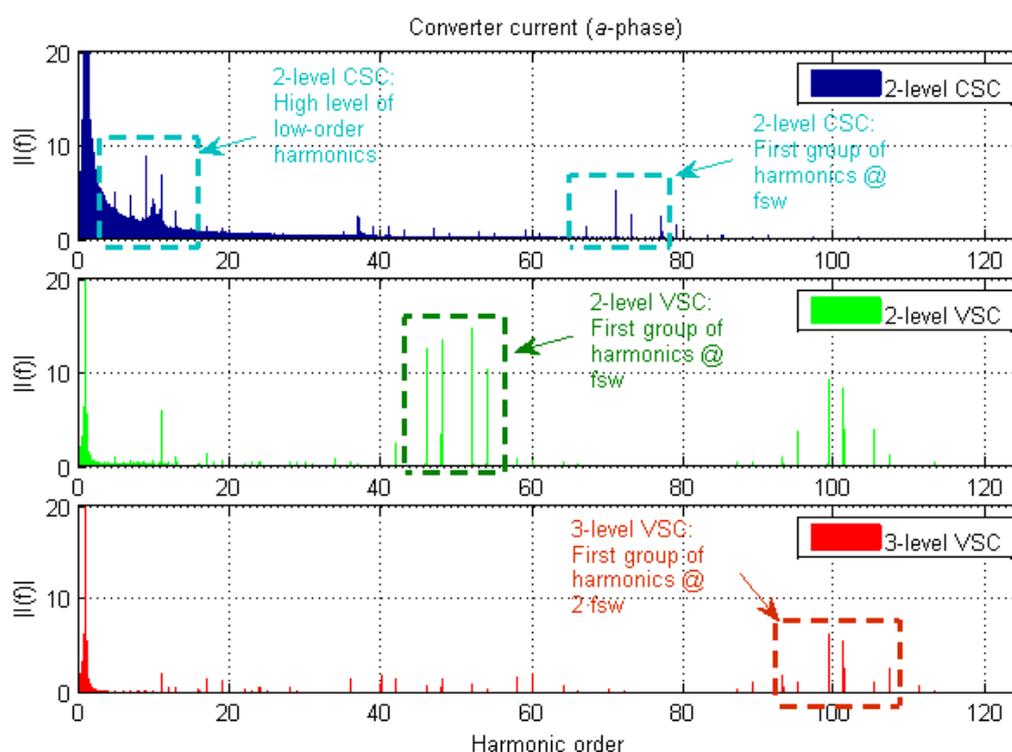
The three operation modes have been tested with a WT whose output power follows the ideal profile of Figure 2. Figure 16 shows the comparison of the different active powers (all of them without any kind of filtering) in each of the three systems, namely: grid (blue line), WT (green line), converter (red line) and load (cyan line) active powers. The converter active power compensates the difference of power between the load and the WT, thereby achieving that the grid does not have to provide or absorb active power. It is clear that the CSC-based system has a higher level of ripple than the VSC-based systems.

**Figure 16.** Grid, WT, converter and load active power in each system.

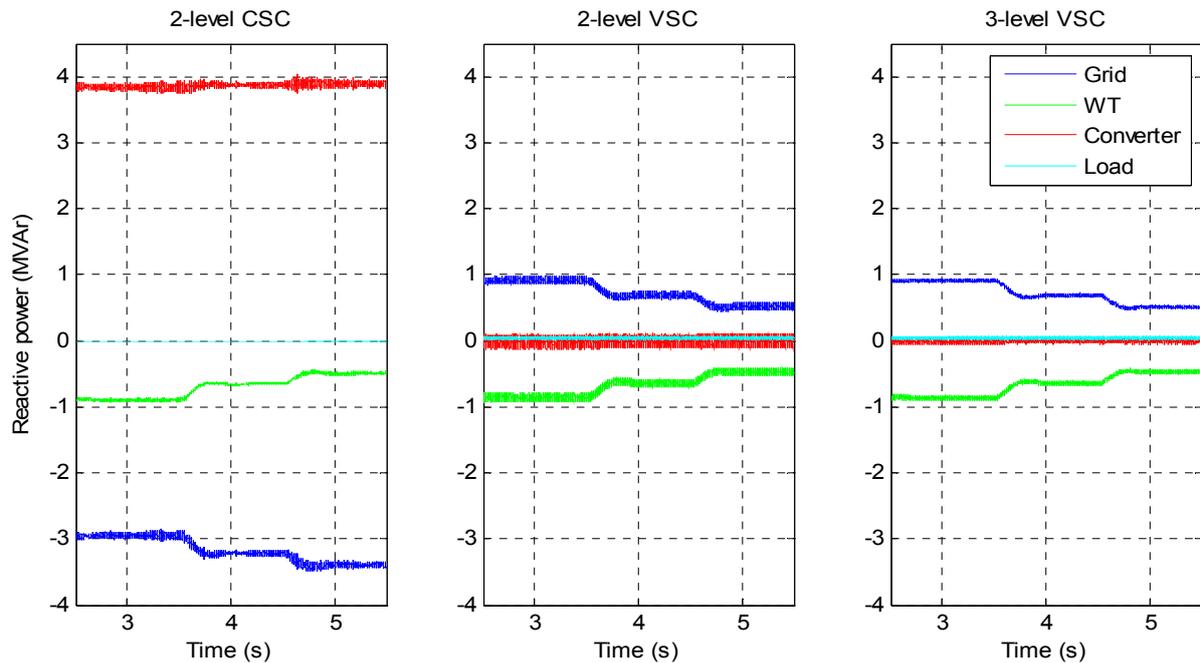


All these characteristics explained above are collected in the FFT analysis of the grid and converter current in Figure 17. The CSC current has a considerable high level of low-order harmonics. As for the VSC-based systems, the three-level VSC has a clear advantage over the two-level VSC, and it is that the first major group of harmonics after the fundamental frequency is located at two times the switching frequency instead of one. Besides, these harmonics have a lower level than in the two-level VSC. This results in a cleaner converter active power due to the reduced presence of oscillating active power. The main groups of harmonics are placed at  $h = 50, 100$  and  $72$  for the two-level VSC ( $f_{sw} = 2500$  Hz), three-level VSC ( $f_{sw} = 2500$  Hz), and two-level CSC ( $f_{sw} = 3600$  Hz), respectively. Obviously, the VSC-based systems have higher levels of high-order harmonics than the CSC-based system. In all the systems, part of the low-order harmonics is due to noise problems and PWM synchronization. The grid current follows the same pattern as the converter current, but with a reduced level of harmonics. Part of them is absorbed by the load or the WT.

**Figure 17.** FFT analysis of the converter current (*a*-phase) of each system.



Similarly to what happens with the active power, the reactive powers collected in Figure 18 show the same behavior regarding their harmonic content. The control system of the converters has not been designed to compensate reactive power and, therefore, the WT reactive power has to be compensated by the grid.

**Figure 18.** Grid, WT, converter and load reactive power in each system.

There is one difference between the CSC-based system and the VSC-based systems regarding the power levels, whose reason is the C-filter connected to the AC-side of the CSC. This C-filter is necessary in order to assist the commutation of the IGBTs and filtering the output current. Its value corresponds to a trade-off among cost, filtering capabilities, noise, *etc.* [11]. The reactive power that this capacitor introduces is described by Equation (16).

$$Q = V^2 \omega C = 1100^2 \cdot 2\pi \cdot 50 \cdot 10^{-2} \cong 3.8 \text{ MVar} \quad (16)$$

The result obtained from Equation (12) corresponds to the CSC reactive power shown in Figure 18. This figure shows that the reactive power generated by the C-filter is greater than the reactive power that the WT absorbs, so that the surplus is absorbed by the grid.

A major drawback of the CSC-based system is derived from this high level of reactive power. Since the active power is already set, the higher the reactive power, the higher the apparent power, hence higher current flow through the system. Moreover, the whole power conditioning system cannot achieve unity power factor. In the case at hand, the grid current amplitude difference between the CSC-based system and the VSC-based systems, all of them represented in Figure 19, is up to 6 times in the worst case (*mode 3*), whereas in the converter currents (after the grid filter) this difference increases to around 40 times in the worst case (*mode 2*). Needless to say that thicker and costlier cables will be necessary to withstand such level of current.

Special care has to be taken when computing the current references, since there is a maximum realizable current depending on the converter sizing.

The value of the superconducting coil determines the velocity of charge and discharge of the current through it and the level of noise in the system. Knowing that the voltage across an inductance is described by Equation (17), the current growth rate  $di_L(t)/dt$  is higher for small values of  $L$  ( $v_L(t)$  is set by the converter), but it also leads to a noisier system. A tradeoff between noise levels and dis/charge levels has to be carried out:

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \tag{17}$$

**Figure 19.** Grid current and converter current after the grid filter in each system.

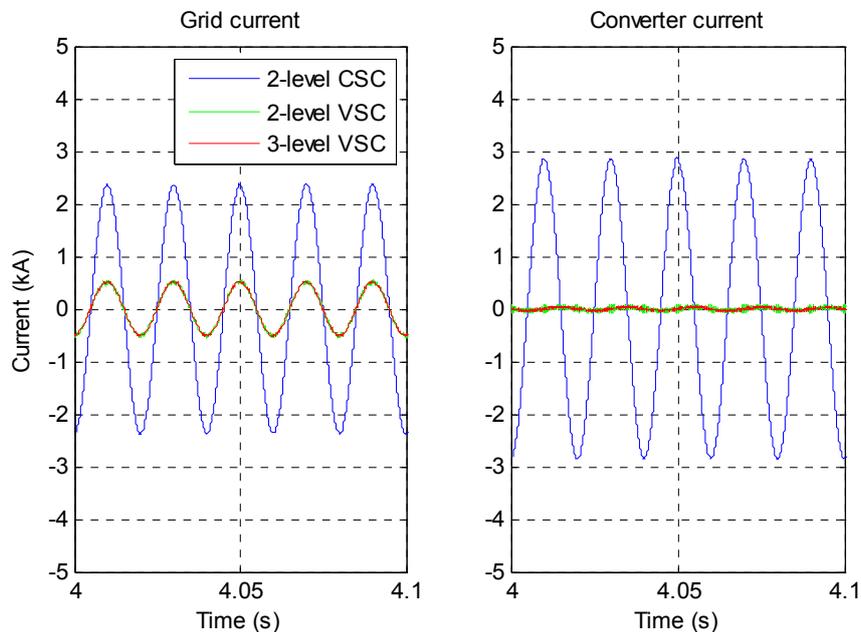
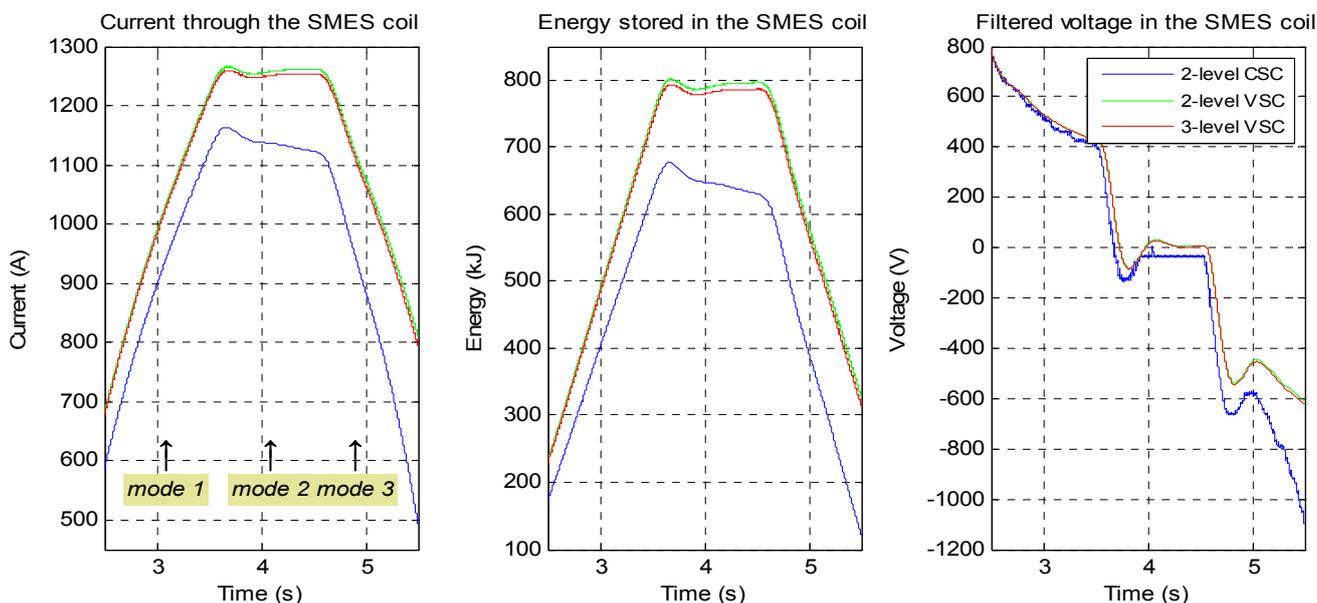


Figure 20 shows the current and filtered voltage in the SMES coil. Taking into account that the initial values of the current are different due to the start-up of the systems, it can be concluded that the three power conditioning systems have the same velocity of charge. In equal conditions, the three of them would reach the same level of stored energy when the operation mode 2 is reached. The higher value of the current in the VSC-based systems is owing to the initial load of the DC-link capacitor/s, which is carried out before the control starts.

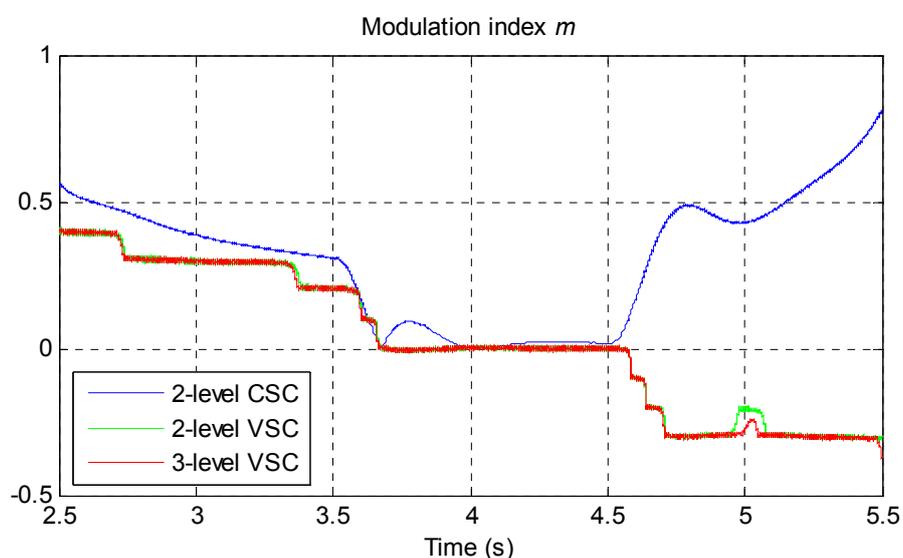
**Figure 20.** Current and voltage in the superconducting coil in each system.



Regarding *mode 2*, the current in the VSC-based systems remains more or less constant (remember that the superconducting coil has ideally zero impedance), unlike the CSC-based system. This is because the CSC-based system does not have a power control system itself, and the reference currents present higher oscillations when changing the operating mode, so it takes longer to reach the steady state. These reference currents are calculated in  $\alpha\beta$ -axes, and together with the coil current the amplitude modulation index needed for the MS-SVM is calculated.

Regarding the operation mode 3, the CSC-based system is discharged slightly faster than the VSC-based systems. This is due to the DC-DC converter control of the VSC-based systems, which keeps the modulation index more constant as compared in Figure 21.

**Figure 21.** Comparison of the modulation indices in each system.



Lastly, the power losses of the converters have been calculated by means of a co-simulation between MATLAB<sup>®</sup>/Simulink (running the control system) and PSIM (running the power system). The software PSIM has the option to include IGBTs and diodes with the desired technical features, making it easier to include commercial devices in the simulation thanks to the manufacturers' datasheets. Table 4 collects the commercial devices from the manufacturer Infineon that have been employed in each power conditioning system. They have been chosen according to their nominal current, nominal voltage and power losses.

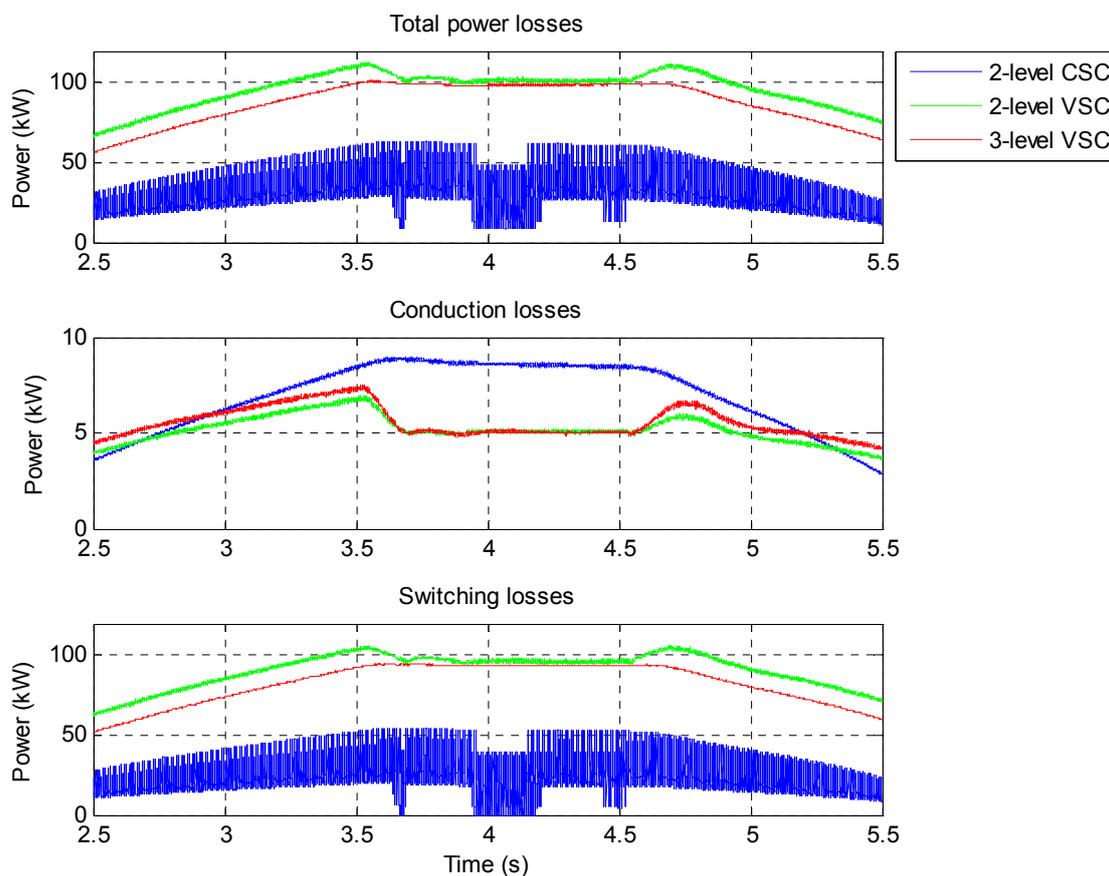
**Table 4.** Commercial IGBTs and diodes used in each power conditioning system.

Title	Two-level CSC	Two-level VSC		Three-level VSC	
		VSC	DC-DC	VSC	DC-DC
IGBT	FZ1200R33KL2C	FZ800R33KL2C	FZ1200R33KL2C	FZ600R17KE3	FZ1200R33KL2C
Diode	D3501N	—	D3501N	D4201N	D3501N

The total power losses are represented in Figure 22, calculated as the sum of the conduction and switching losses, which are also represented. Remember that *mode 1* corresponds to  $t = (2.5,3.5]$  s, *mode 2* corresponds to  $t = (3.5,4.5]$  s and *mode 3* corresponds to  $t = (4.5,5.5]$  s, and the power conditions in which these losses have been obtained are in Figure 16. The aim of this simulation is to

compare the power losses according to the operation modes of the system. If power would increase or decrease, the losses pattern would follow the same relation, hence more emphasis is given to the loss analysis depending on the operation mode. As for the load power level, this also leads to similar results. Note that power losses are different if the converter is compensating active or reactive power, but the SMES system is viewed only as an active power compensator in this work.

**Figure 22.** Comparison of the power losses in each system.



Obviously, an increase in the current handled by the power conditioning system is accompanied by an increase in its losses, both conduction and switching. This is observed during *mode 1*, and the opposite situation during *mode 3*. While the current keeps constant, the losses keep constant as well (*mode 2*). The system with the lowest total power losses is the CSC-based system thanks to its minimum switching losses, followed by the three-level VSC and the two-level VSC. It is worth noting that the reduction in the losses of the three-level VSC is due to its remarkable decrease in the switching losses, since the IGBTs are less stressed from that standpoint. Since there are now two IGBTs driving in each switching period instead of one as in the two-level VSC, conduction losses are higher in the three-level VSC, but these levels are not comparable with the switching losses.

## 5.2. Load-Step

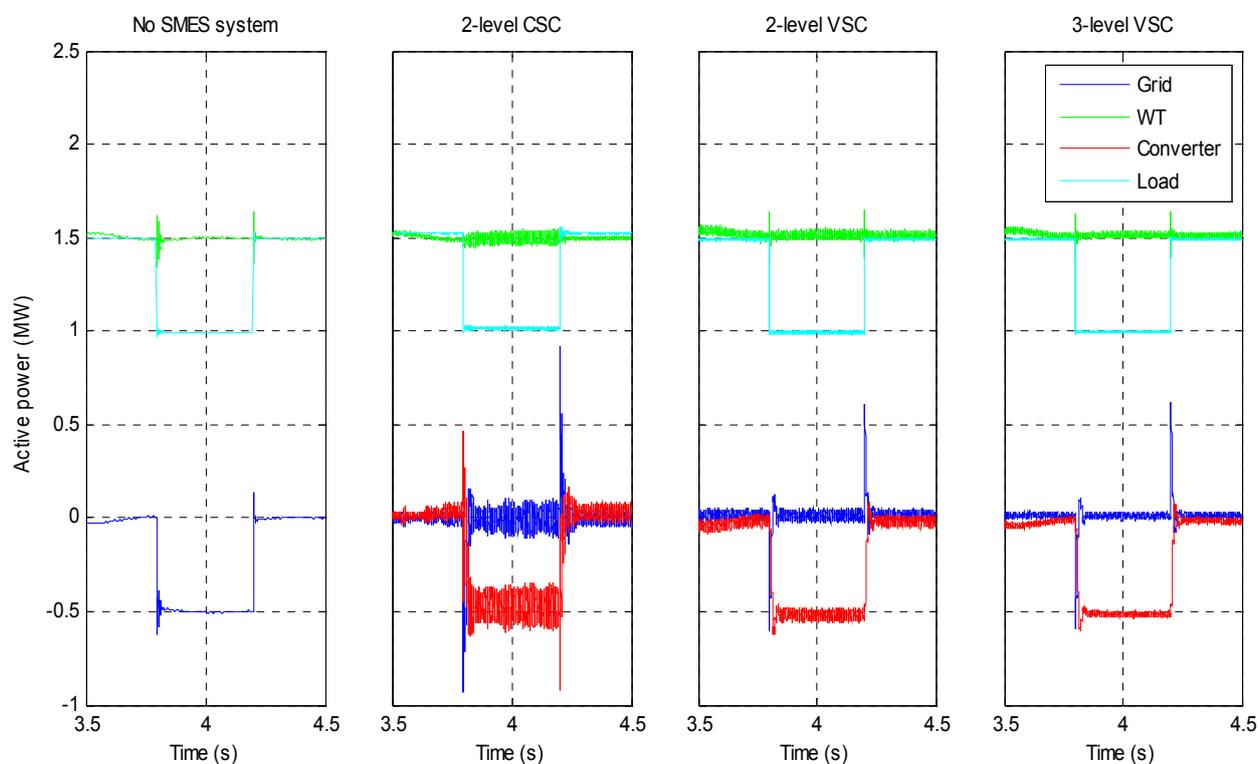
Figure 23 shows in first place the consequence of a load-step of  $-0.5$  MW in the system when no energy storage system is connected to the PCC. The grid active power has to change its value from 0 W to absorb the extra power from the WT, which is 0.5 MW in this case, and the grid current is

forced to increase its amplitude. This same situation would happen if the load-step would be of +0.5 MW, in which the grid would have to supply 0.5 MW to the load.

The remaining graphics in Figure 23 show the results of adding an SMES system, according to the power conditioning system used. The SMES system stores the extra power from the WT in the superconducting coil, thus leaving the grid active power around its previous value after a short stabilization period. In this simulation, this period occurs at  $t = 3.8$  s (when the load power decreases) and at  $t = 4.2$  s (when the load power returns to its former value).

It is noteworthy that if the load-step would be of +0.5 MW, the stored energy in the SMES system would need to reach a certain level before the load-step in order to provide the exact amount of power to the load.

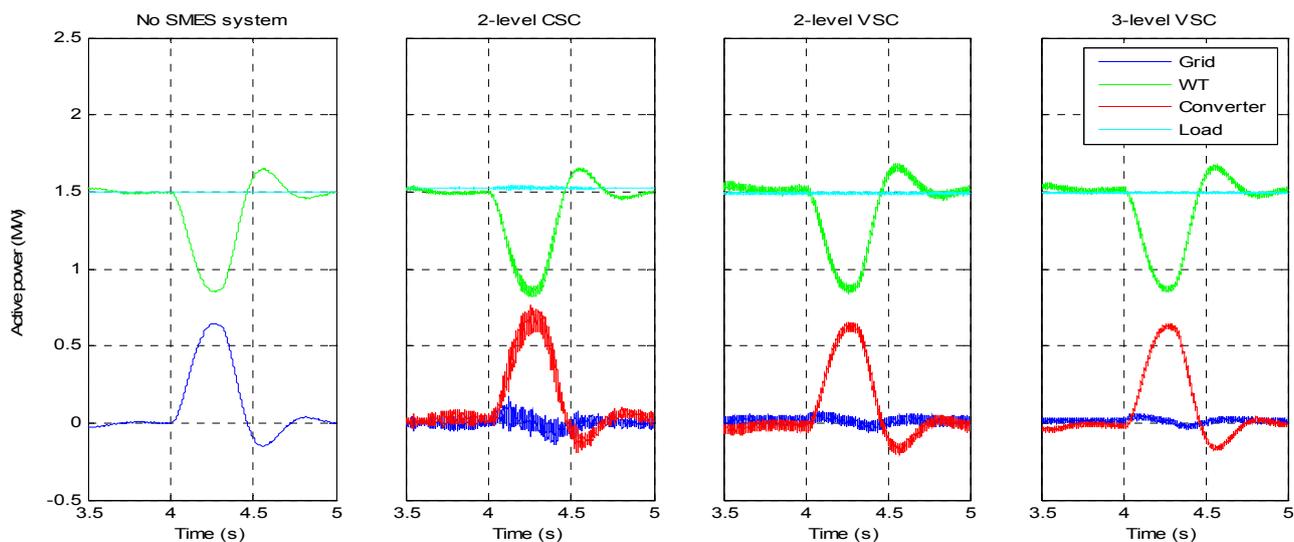
**Figure 23.** Operation with and without SMES system for load-step application.



### 5.3. Load-Sharing

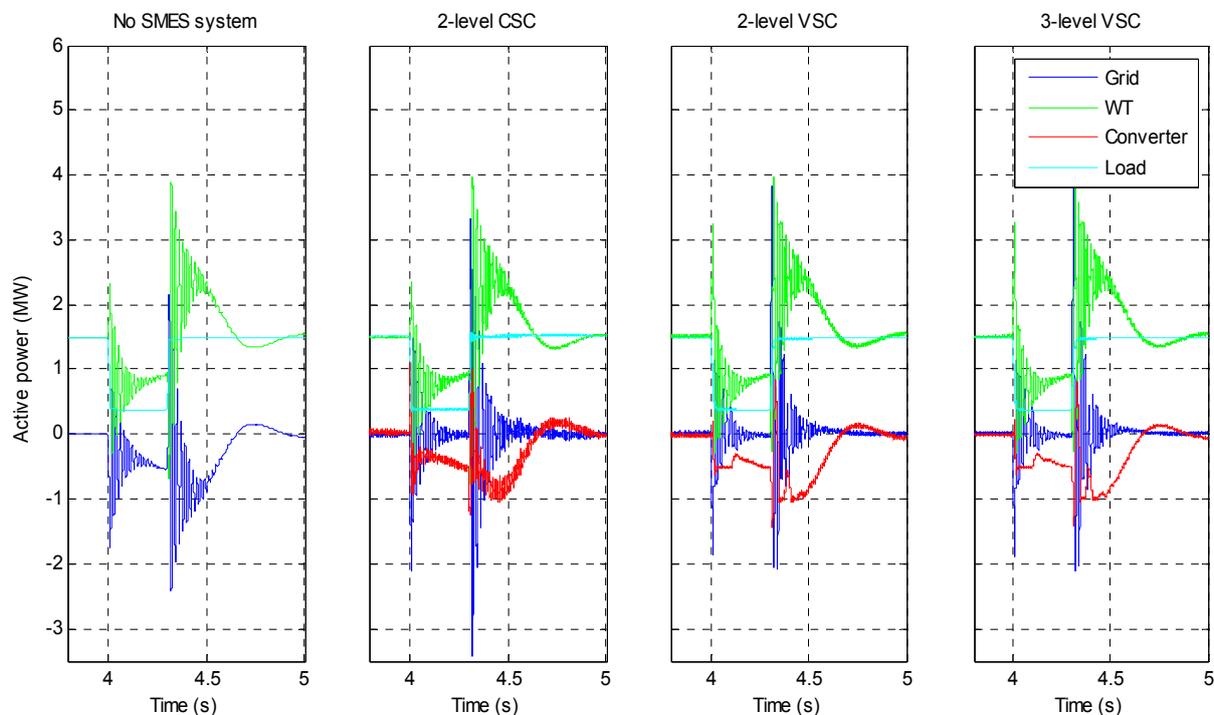
Figure 24 shows in first place the consequence of a 0.7 MW-peak fluctuation in the WT output power when no energy storage system is connected to the PCC. This power fluctuation is transferred to the grid and can bring serious consequences to the rest of grid-connected systems.

The remaining graphics in Figure 24 correspond to the performance of each power conditioning system, showing their capabilities to stabilize the grid active power.

**Figure 24.** Operation with and without SMES system for load-sharing application.

#### 5.4. Grid-Support

It is widely known that voltage dips are one of the most common disturbances in the grid nowadays. Therefore, several techniques have been studied and developed to compensate their harmful effects. Figure 25 shows how the SMES system is able to operate under these circumstances.

**Figure 25.** Operation with and without SMES system for grid-support application.

With no energy storage system operating, the grid active power decreases as well as the load active power. When connecting the SMES system, the grid active power is stabilized around 0 W thanks to the power that the SMES system is supplying in the PCC.

Table 5 gives an overview of the three power conditioning systems. Each system has its own advantages and disadvantages depending on the criterion, but it is clear the three-level VSC (multi-level NPC's in general) is gaining ground to its competitors. It has a good overall performance in terms of harmonics, power losses, *etc.*

**Table 5.** Comparison table of the three systems.

Item	Two-level CSC	Two-level VSC + DC-DC	Three-level VSC + DC-DC
Active power compensation	Medium-good	Good	Good
Reactive power usage (Figure 18)	Yes, due to the C-filter	No	No
Grid-filter (Figures 4–6)	C-filter	L-filter	L-filter
Modulation strategy	MS-SVM	THPWM + PWM	THPWM + PWM
Harmonic content (Figure 17)	High	Medium	Low
Low-order harmonics	High	Low	Low
High-order harmonics	Medium	Medium-high	Low
Number of devices (Figures 4–6)	12	10	22
IGBTs	6	8	14
Diodes	6	2	8
Total power losses (Figure 22)	Low	High	Medium
Switching losses	Low	High	Medium
Conducting losses	Low	Very low	Very low
Max./Min. DC-voltage	$\pm 1555$ V	$\pm 1800$ V	$\pm 1800$ V
Complexity of control	Low	Medium	Medium
Reaction time	No major differences		

## 6. Conclusions

Many and various are the applications of SMES systems. Among them, this paper has analyzed the behavior and suitability of these systems for three of them: load-step, load-sharing and grid-support. In all of them there are circumstances whereby the active power grid is affected to a greater or lesser extent, emphasizing the character of grid active power stabilization of these energy storage systems. Thus, they are able to reduce the harmful effects that these transients cause to other devices connected to the grid.

From the viewpoint of cost, the system that means the highest investment is the three-level VSC, given that the use of a three-level converter and the need for a DC-DC converter increases the number of devices. On the other hand, the same fact of working with three levels reduces the stress on each switch and reduces the power losses compared to two-level VSC, which is the option that presents greater losses. The two-level CSC is presented as an intermediate option in terms of cost, and as a good option in terms of losses since it is the system with fewer devices.

From the viewpoint of the harmonic content, the two-level CSC is characterized by introducing low-order harmonics. This worsens the quality of the power handled by the SMES system and can excite undesired resonances. The way to reduce these harmonics is through the C-filter, but as we increase its value, the reactive power consumed increases as well as the magnitude of the currents. A future study is to improve the grid filter for CSC converters to solve these problems. The three-level

VSC is the opposite case, which gives a better power quality due to the displacement of the first fundamental harmonic group to twice the switching frequency. From the viewpoint of the complexity of control, none of them has a high computational load.

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### Conflict of Interest

The authors declare no conflict of interest.

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