Energies **2013**, *6*, 1068-1100; doi:10.3390/en6021068

OPEN ACCESS

energies

ISSN 1996-1073

www.mdpi.com/journal/energies

Article

A Photovoltaic Power System Using a High Step-up Converter for DC Load Applications

Sheng-Yu Tseng * and Hung-Yuan Wang

Department of Electrical Engineering, Chang-Gung University Kwei-Shan Tao-Yuan, Taiwan; E-Mail: ice_rap1105@hotmail.com

* Author to whom correspondence should be addressed; E-Mail: sytseng@mail.cgu.edu.tw; Tel.: +886-3-2118800 (ext. 5706); Fax: +886-3-2118026.

Received: 26 December 2012; in revised form: 7 February 2013 / Accepted: 8 February 2013 / Published: 21 February 2013

Abstract: This paper presents a power system using a high step-up converter for dc load applications. The high step-up converter adopts a boost converter with interleaved mode and a coupled inductor to raise its powering ability and increase its step-up voltage ratio, respectively. In order to increase conversion efficiency, an active clamp circuit is introduced into the proposed one to provide soft-switching features to reduce switching losses. Moreover, switches in the converter and active clamp circuit are integrated with a synchronous switching technique to reduce circuit complexity and component counts, resulting in a lower cost and smaller volume. A perturb and observe method is adopted to extract the maximum power from photovoltaic (PV) arrays. Furthermore, a microchip associated with PWM IC is used to implement maximum power point tracking operation, voltage regulation and power management. Finally, a prototype PV power system with 400 V/6 A has been implemented for verifying the feasibility of the proposed PV power system. It is shown to be suitable for PV energy conversion applications when the duty ratios of switches in the dc/dc converter are less than 0.5.

Keywords: photovoltaic power system; high step-up converter; boost converter; perturb and observe method

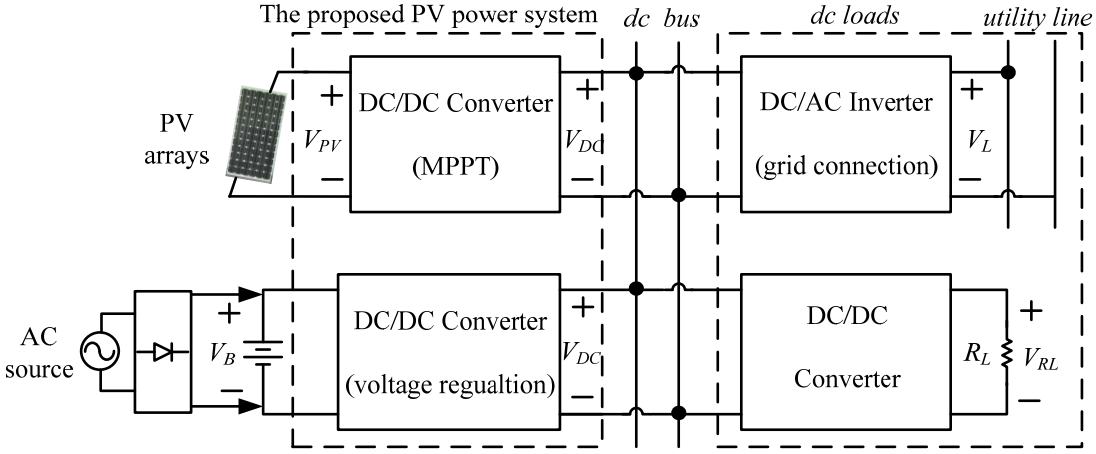
---

1. Introduction

Limited fossil energy and increased air pollution have spurred researchers to develop clean energy sources. One of these sources is the photovoltaic (PV) power generation system, which is a clean, quiet and an efficient method for generating electricity. In practical applications, PV arrays can be used in battery charging, water pumping, PV vehicles, satellite power systems, grid-connected power systems, standalone power systems, and so on. Due to the low conversion efficiency of PV arrays, on way to reduce the cost of the overall system is by using high efficiency power processors. The power processor usually adopts a dc/dc converter as its energy processing system.

When a dc/dc converter is used in a PV array power system, it is operated at the maximum power point (MPP) of the PV arrays to extract the maximum possible power for increasing the utilization rate of the PV arrays. As a result, its output voltage does not remain at the desired constant dc voltage. Therefore, a dc/dc converter with voltage regulation is used to connect with PV power systems in parallel to keep the output voltage in the desired constant dc voltage range, as shown in Figure 1.

Figure 1. Block diagram of PV power generation system for DC load applications.



In Figure 1, the dc bus voltage can supply a dc/ac inverter for a grid-connected power system [1–5], a dc/dc converter for dc load [6–10], and so on. The dc/ac inverter and dc/dc converter are regarded as dc loads. In this paper, the proposed power supply includes a dc/dc converter as the maximum power point tracking (MPPT) point of the PV arrays and a dc/dc converter as the load voltage regulator.

To increase the utility rate of PV arrays, power systems using PV arrays must track MPP to extract as much power as possible from the arrays. Several MPPT algorithms have been proposed [11–20]. Some of the more popular MPPT algorithms are the constant voltage method [11,12], β method [13], system oscillation method [14,15], ripple correlation method [16], incremental conductance method [17] and perturb and observe method [18–20]. Due to its simplicity and ease of implementation, the perturb and observe method is often used. Therefore, the perturb and observe method was adopted to implement the MPPT of the proposed power system.

In order to increase the conversion efficiency of a PV power system, switching power converters are widely used as dc/dc converters. Since the proposed PV power system requires a high step-up dc/dc converter, a transformer or coupled inductor is usually introduced into switching power

converters [21,22]. Compared with the converter using an isolation transformer, the one using a coupled inductor has a simpler winding structure and a higher coupling coefficient. It can reduce inductor currents to ensure lower conduction losses and decrease leakage inductance to attain a lower switching loss, respectively. As a result, the one can use a lower value of the input filter capacitor to obtain a good regulation of the output voltage. Therefore, a system using a coupled inductor is relatively attractive. However, since the energy is trapped in the leakage inductor of the coupled inductor, it will not only increase voltage stresses, but induce significant switching losses of the switches in the converter. In order to solve these problems, several methods have been proposed [23–25]. In [23], a resistor-capacitor-diode (R-C-D) snubber is used to alleviate switch voltage stresses, but the energy trapped in the leakage inductor is dissipated by the resistor, resulting in a lower conversion efficiency of the converter. Therefore, a passive losses circuit [24] is adopted to recover the energy and reduce voltage spikes across switches, but active switches are still operated in hard switching mode. Its conversion efficiency does not increase significantly. In [25], an active clamp circuit is introduced into the converter for recovering the energy of the leakage inductor and limit voltage spike across switches. Moreover, the one can also achieve zero-voltage switching (ZVS) in converter switches to increase their conversion efficiency. As mentioned above, a boost converter associated with a coupled inductor is adopted in this research as the dc/dc converter, as shown in Figure 2. In order to further increase the powering capability of the converter, boost converters with interleaved manner have been proposed by several authors [26–29], as shown in Figure 3.

Figure 2. Schematic diagram of a boost converter with coupled inductor.

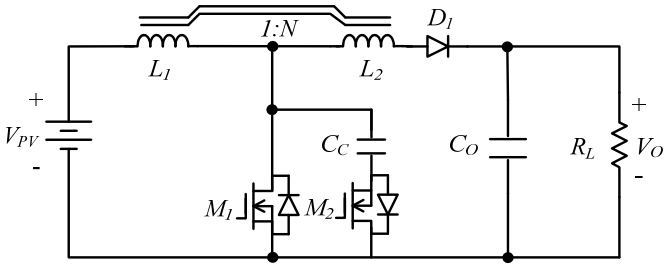
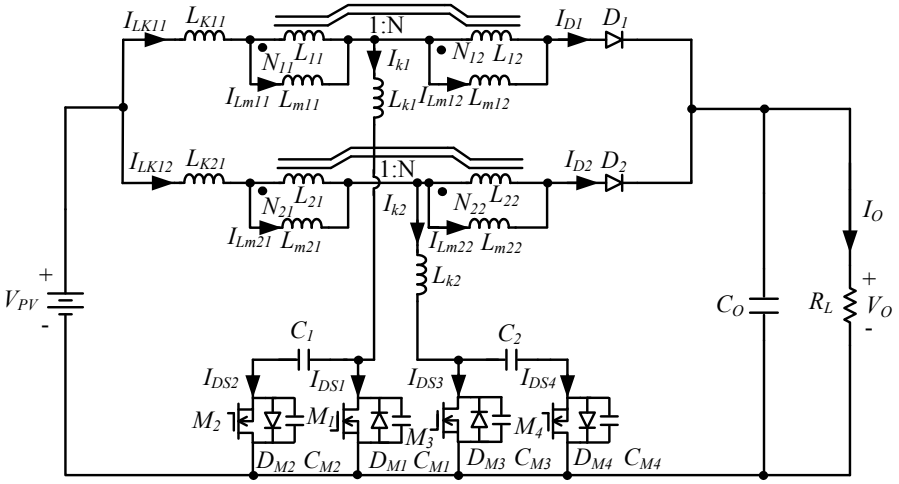
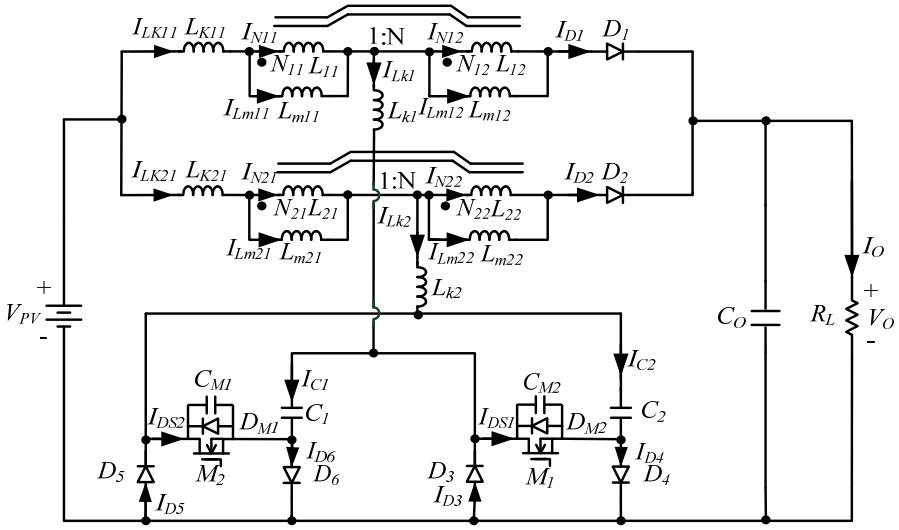


Figure 3. Schematic diagram of interleaved active clamp boost converter with coupled inductor.



Due to the complexity of the circuit structure, the proposed dc/dc converter can be simplified however, as shown in Figure 4. From Figure 4, it can be seen that the proposed interleaved active clamp boost converter can use less component counts to achieve a high step-up voltage ratio and similar conversion efficiency for reducing the costs.

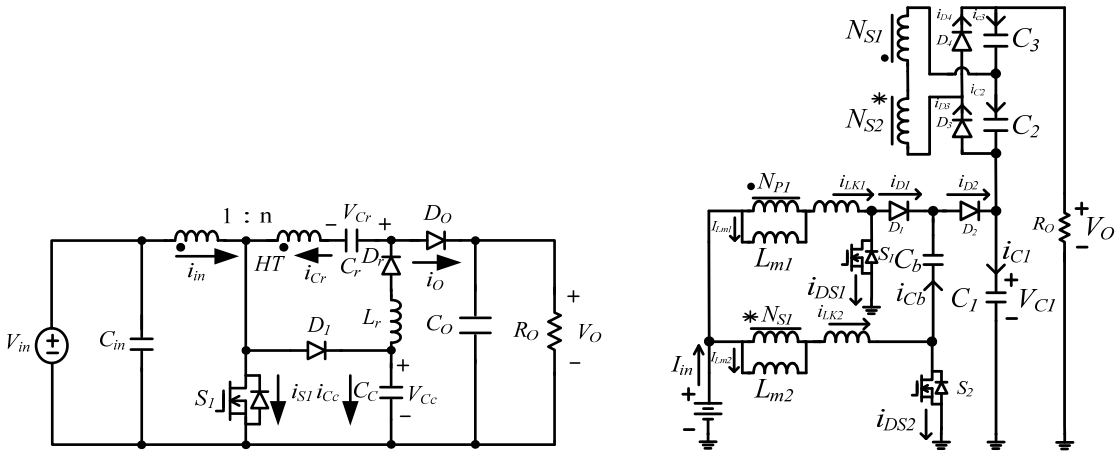
Figure 4. Schematic diagram of the proposed interleaved active clamp boost converter with coupled inductor.



In particular, a general half-bridge converter, push-pull converter and full-bridge converter need pulse-width modulation (PWM) IC with two gate signals to drive their switches. Since the input sources of the converters adopt the voltage fed type, the duty ratios of their control PWM ICs are limited to within 0.5. If the dc/dc converter adopts a special PWM IC, which has a higher duty ratio (≥0.5), these are difficult to obtain and the cost will be increased.

In [28], as shown in Figure 5a, the duty ratios of switches in the proposed converters require that the duty ratios of the PWM ICs must be greater than 0.5, resulting in a higher cost. Moreover, its resonant capacitor has a higher current ripple rating (CRR), and it will need a special capacitor, which has a low ESR, high CRR and high operational bandwidth. Therefore, it is suitable for a low power level application. In [29] a voltage multiplier module to implement a high step-up voltage ratio was proposed, as shown in Figure 5b. Its voltage doubler capacitors also require a higher CRR. In particular, its controller adopts a DSP to implement its control method. Its cost is increased and its powering capability will be limited. In order to reduce the limitations of PWM ICs and capacitors for a voltage regulator, the proposed dc/dc converter can use a general PWM IC with two gate signals to achieve a high step-up voltage ratio and a high conversion efficiency with less component counts. As mentioned above, the proposed converter can reduce cost and further decrease its size, weight and volume. It is suitable for PV arrays applications when the PWM IC duty ratios are less than 0.5.

Figure 5. Schematic diagram of the conventional high step-up converters (**a**) proposed in [28]; and (**b**) proposed in [29].



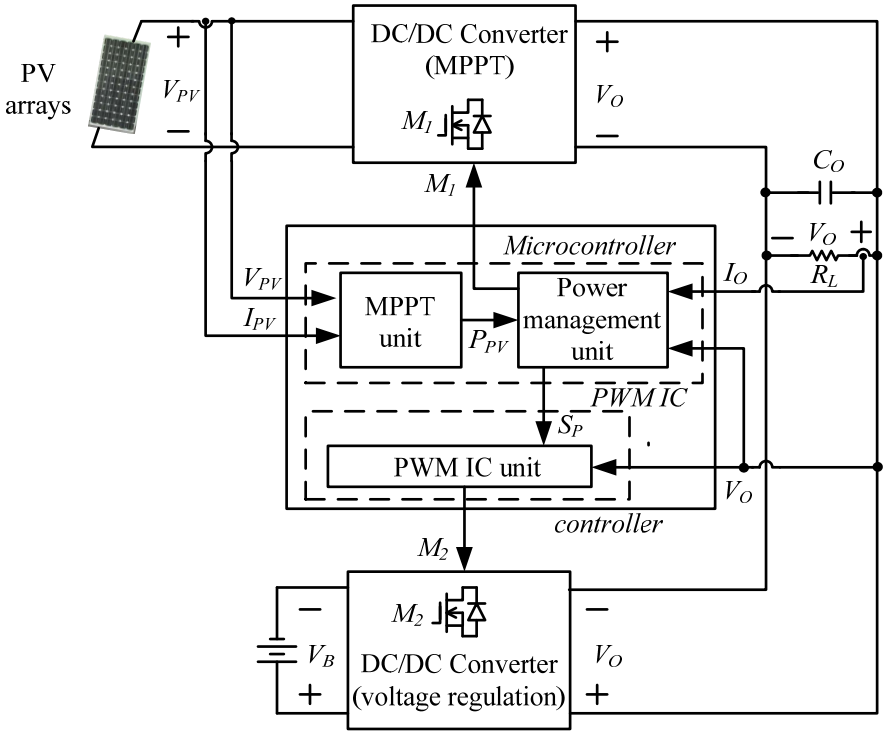
2. Control Algorithm of the Proposed PV Power System

In order to achieve a proper power management of the PV power system, the topology of the PV power system and power management are described in the following sections.

2.1. Circuit Topology of the Proposed PV Power System

The proposed PV power system consists of a dc/dc converter with MPPT, and a dc/dc converter with voltage regulation and controller, as shown in Figure 6.

Figure 6. Derivation of the proposed interleaved boost converter with coupled inductor.



Two dc/dc converters adopt an interleaved active clamp boost converter with coupled inductor, respectively, as shown in Figure 4. The one with MPPT control algorithm is used to extract the maximum power from the PV arrays. The other one, equipped with a voltage regulation control method, is required to regulate the power between the PV arrays and loads and to generate a constant output voltage for supplying power to the dc loads. Since the one with the MPPT control algorithm uses PV arrays as its power source, its controller, which is a microcontroller, is divided into two control units: MPPT unit and power management unit. The MPPT one can track the maximum power point (MPP) of the PV arrays. Its control method adopts the perturb and observe method, which is described in [18–20]. The power management one can separately regulate the output voltage of dc/dc converters with MPPT control algorithm and with the voltage regulation control method, according to the relationships between the maximum power $P_{PV(max)}$ of the PV arrays and the load power P_L by signals M_1 and S_P. Moreover, the PWM IC unit is adopted to control the dc/dc converter by the voltage regulation control method to obtain a constant output voltage. Regulation of the output power by control signal S_p is also required. All of the protections are implemented by the microcontroller. The protections include over-current and -temperature protections of two dc/dc converters and battery undercharge. Therefore, the proposed PV power system can achieve the optimal utility rate of PV arrays.

2.2. Power Management

The proposed PV power system includes two dc/dc converters connected in parallel to supply power to the load. Its operational modes can be divided into eight modes. Note that P_{PV} is the output power of the PV arrays, P_{VB} is that of the battery and P_L is the load power. Moreover, "1" represents the power which is generated by PV arrays or is dissipated by load, while "0" is the power which is not generated or is not dissipated. According to the power management flow chart of the proposed PV power system shown in Figure 7, all operational modes are shut down, except for operational modes IV, VI and VIII. In the following, operational modes IV, VI and VIII are described.

2.2.1. Operational Mode IV

In the operational mode, the dc/dc converter with battery is adopted to supply power to the load. When the load power $P_L > P_{VB(max)}$, the proposed PV power system is shut down. When the load power $P_L < P_{VB(max)}$, the power curve of the PV arrays follows the load power, as shown in Figure 8, until energy stored in battery is completely discharged. The PV power system is then shut down.

2.2.2. Operational Mode VI

In operational mode VI, the dc/dc converter with PV arrays as its power source is used to supply power to the load, as shown in Figure 9. From Figure 9, it can be seen that when the maximum power $P_{PV(max)} \geq P_L$, power curve of the PV arrays follows that of load power. If $P_{PV(max)} < P_L$, the proposed PV power system is shut down.

Figure 7. Flow chart of power management of the proposed PV power system.

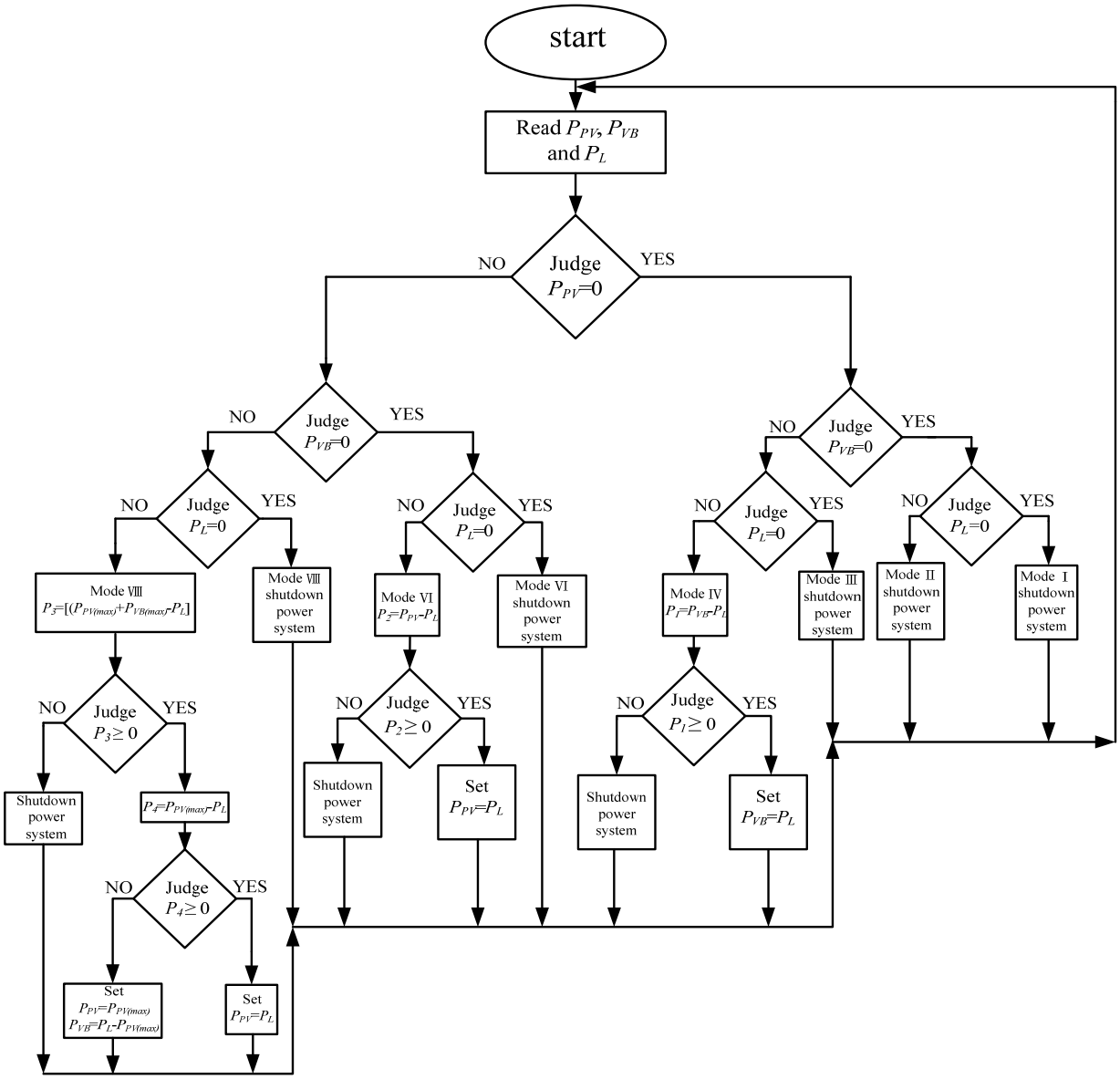


Figure 8. Plot of power curve of the proposed PV power system under operational mode IV.

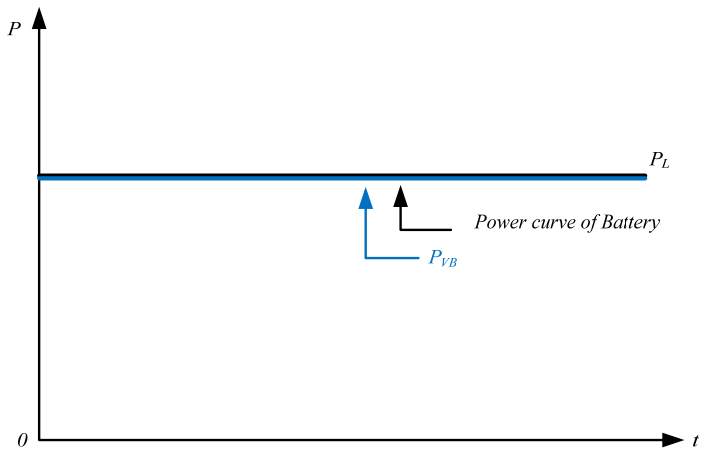
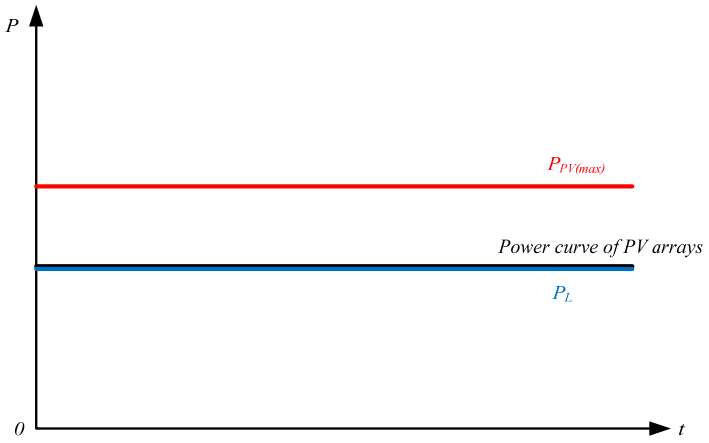


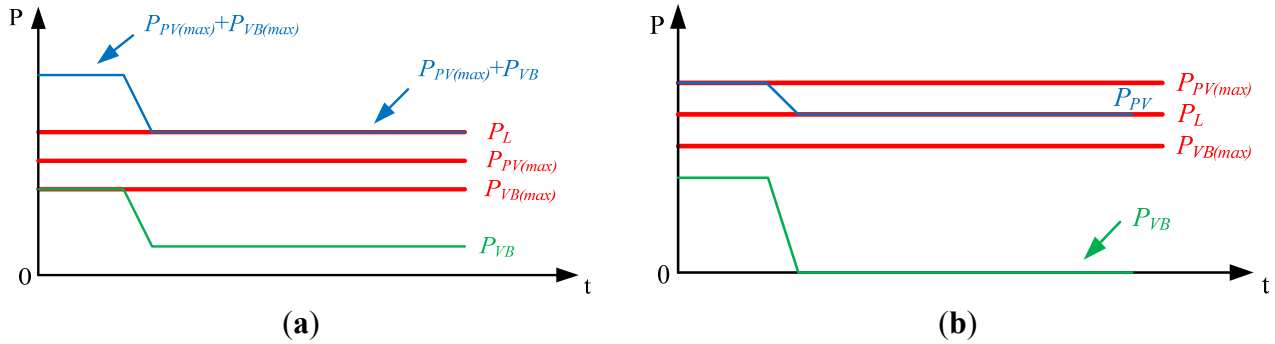
Figure 9. Plot of power curve of the proposed PV power system under operational mode VI.



2.2.3. Operational Mode VIII

In operational mode VIII, two dc/dc converters using PV arrays and battery as their power sources are adopted to supply power to the load, respectively, as shown in Figure 10. When the total maximum output power of the two dc/dc converters is equal to or greater than P_L, the PV power system can be working. Under the other operational conditions within this operational mode, one is shut down. When the total maximum output power ($P_{PV(max)} + P_{VB(max)}$) > P_L, the dc/dc converter with PV arrays as its power source is operated at MPP of the PV arrays and the one with battery as its power source is operated under the output power of ($P_L - P_{PV(max)}$), as shown in Figure 10a. Moreover, when $P_{PV(max)} > P_L$, the one with battery as its power source is shut down and the output power P_{PV} of the PV arrays is equal to P_L, as shown in Figure 10b. According to the energy conservation of the PV power system, P_L is the sum of P_{PV} and P_{VB} and P_L extracts as much power as possible from the PV arrays to increase utilization rate of the PV array.

Figure 10. Plot of power curves P_{PV}, P_{VB} and P_L (**a**) under $P_{PV(max)} + P_{VB(max)} \geq P_L$ and (**b**) under $P_{PV(max)} + P_{VB(max)} \geq P_L$ and $P_{PV(max)} \geq P_L$.



3. Operational Principle of the Proposed DC/DC Converter

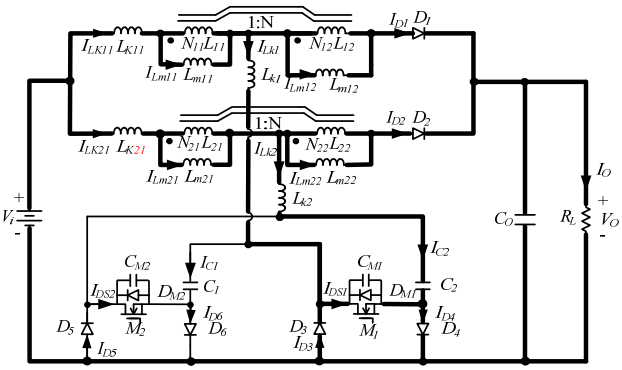
When $P_{PV(max)} < P_L$, the dc/dc converter using PV arrays as its power source is operated at current regulation to extract the maximum power from the PV arrays. When $P_{PV(max)} \geq P_L$, the one is operated at voltage regulation to supply power to the load. Its function is the same as the one using battery as its

power source. Therefore, two dc/dc converters can adopt the same circuit structure. In the following, the operational principle of the proposed dc/dc converter is briefly described.

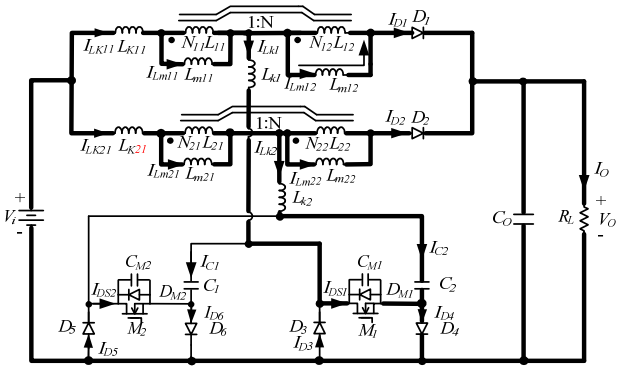
Operational Principle of the Proposed Converter

The dc/dc converter of the proposed PV power system using interleaved active clamp boost converter with coupled inductor is shown in Figure 4. According to the circuit operational principle of the proposed boost converter, its operational modes are divided into 12 modes, as show in Figure 11, and their key waveforms are illustrated in Figure 12. Since the operational modes between $t_0 \sim t_6$ are similar to those waveforms between $t_6 \sim t_{12}$, except that the operational switch changes from M_1 to M_2, each operational mode during half one switching cycle is briefly described in the following.

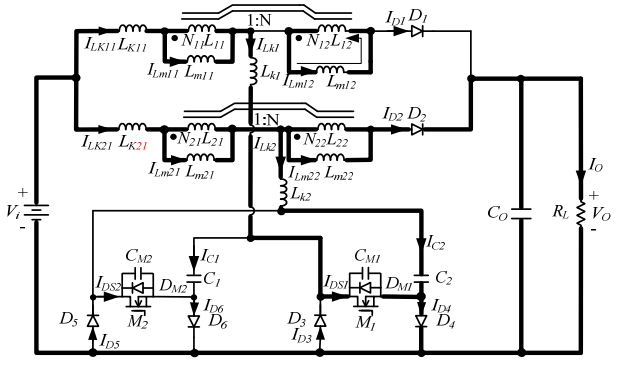
Figure 11. Equivalent circuit of each operational mode in the proposed interleaved active clamp boost converter with coupled inductor over half of one switching cycle.



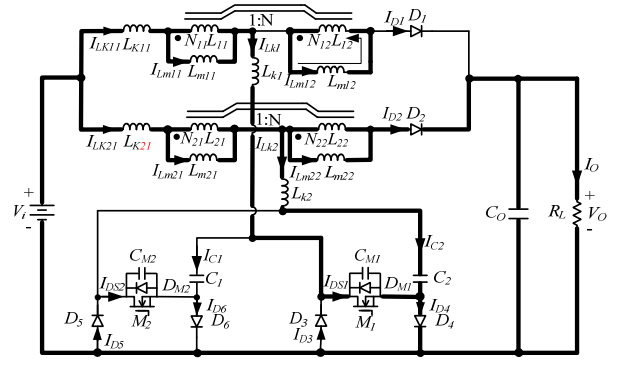
Mode 1 ($t_o \le t < t_1$)



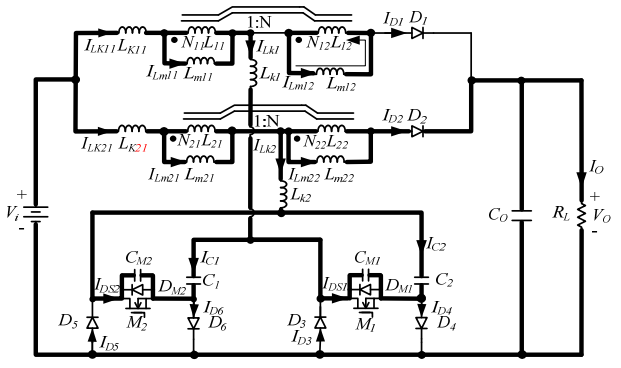
Mode 2 ($t_1 \le t < t_2$)



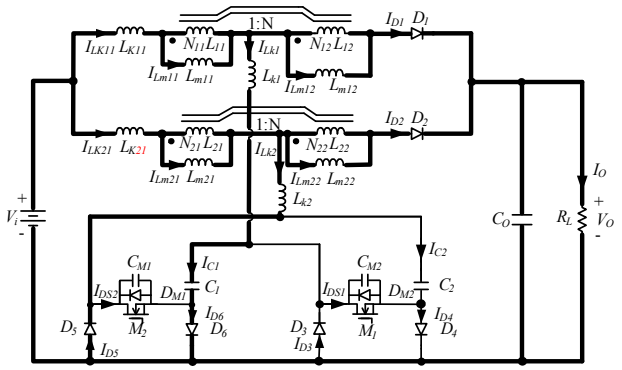
Mode 3 ($t_2 \le t < t_3$)



Mode 4 ($t_3 \le t < t_4$)

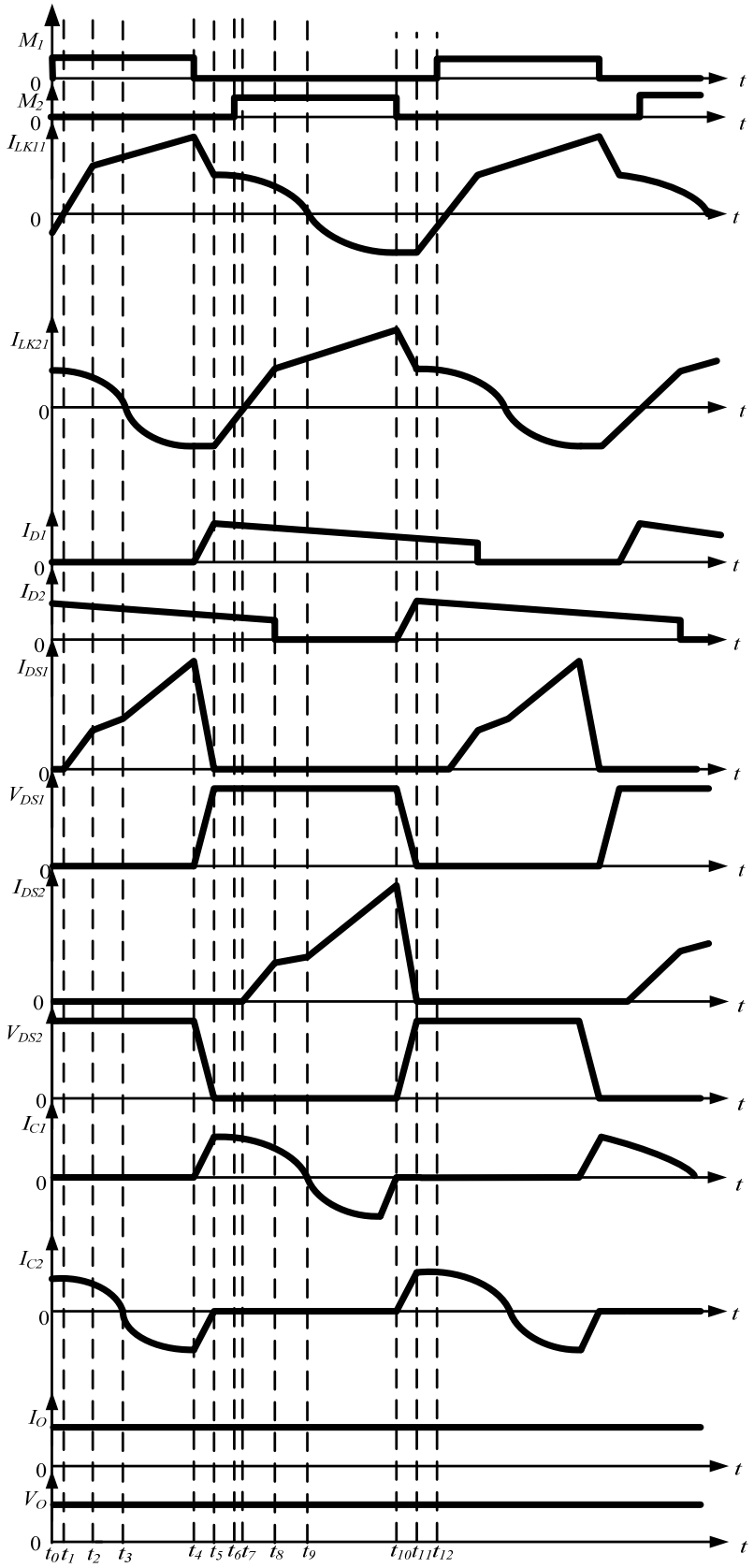


Mode 5 ($t_4 \le t < t_5$)



Mode 6 ($t_5 \le t < t_6$)

Figure 12. Key waveforms of the proposed converter operating over one switching cycle.



Mode 1 (Figure 11a: $t_o \leq t < t_1$): before t_0, switches M_1 and M_2 are in the off state. Diodes D_3 and D_4 are forwardly biased, therefore, voltage V_{DS1} across switch M_1 is equal to 0. When $t = t_0$, switch M_1 is

turned on. Since diodes D_3 and D_4 are forwardly biased before switch M_1 is turned on, switch M_1 is operated with ZVS at turn-on transition. During this time interval, leakage inductor L_{K21}, external inductor L_{K2} and capacitor C_2 form a resonant network and they start to resonate. Moreover, since current I_{LK11} is a negative value, diode D_3 is set as freewheeling by inductors L_{K1} and L_{K11}. Therefore, current I_{DS1} of switch M_1 is equal to 0.

Mode 2 (Figure 11b: $t_1 \le t < t_2$): at t_1, current I_{LK11} is equal to 0. Within this time interval, current I_{LK11} ranges from 0 to a positive value, therefore, diode D_3 is reversely biased. Current I_{DS1} ranges from 0 to a positive value and its value is equal to I_{LK11}. Diode D_4 is kept in the forwardly conduction state and its current I_{D4} is the sum of I_{LK11} and I_{C2}. The resonant network formed by L_{K21}, L_{K2} and C_2 is still in the resonant state. Diodes D_1 and D_2 are set in freewheeling mode, respectively, by inductors L_{m11}, L_{m12}, L_{m21} and L_{m22}.

Mode 3 (Figure 11c; $t_2 \le t < t_3$): when $t = t_2$, current I_{LK11} reaches the initial value which is the initial current value of the coupled inductor when the proposed converter is operated in continuous conduction mode (CCM). At that moment, diode D_1 is in the reversely bias state. The voltage V_{PV} is approximately applied to inductor L_{m11} because L_{m11} is much greater than L_{K11}. Within this time interval, current I_{LK11} is equal to I_{DS1} and its value increases linearly. Moreover, current I_{LK2} is equal to I_{C2} and its value ranges from a positive value to 0 with the resonant manner. Current I_{D4} is still sum of I_{DS1} and I_{C2}. Diode D_2 is kept in freewheeling state by inductors L_{m21} and L_{m22}.

Mode 4 (Figure 11d; $t_3 \le t < t_4$): at t_3, current I_{LK21} (= I_{C2}) is equal to 0. Within this time interval, current I_{LK21} ranges from 0 to a negative value with the resonant manner. Since current I_{DS1} is greater than I_{C2}, diode D_4 is still kept in the forwardly biased state. Operational conditions of the other components are the same conditions of Mode 3. As a result, current I_{LK11} (= I_{DS1}) increases linearly and current I_{D2} decreases linearly.

Mode 5 (Figure 11e, $t_4 \le t < t_5$): at t_5, switch M_1 is turned off. At that moment, current I_{DS1} is approximately equal to I_{C2}, therefore, diode D_4 is reversely biased. Within this time interval, energies stored in inductors L_{K11}, L_{K1}, L_{K21} and L_{K2} are released to the charge capacitor C_{M1} and discharge capacitor C_{M2}. Voltage V_{DS1} across capacitor C_{M1} ranges from 0 to $[V_{C2} + (NV_{PV} + V_O)/(N + 1)]$, while V_{DS2} across capacitor C_{M2} ranges from $[V_{C1} + (NV_{PV} + V_O)/(N + 1)]$ to 0. Diodes D_1, D_3, D_5 and D_6 are still kept in the reversely bias state, while diode D_2 is kept in freewheeling mode by inductors L_{m21} and L_{m22}.

Mode 6 (Figure 11f; $t_5 \le t < t_6$): when $t = t_5$, the voltage V_{DS2} across switch M_2 is equal to 0. At the same time, diodes D_5 and D_6 are in the forwardly bias state, while diode D_1 is in freewheeling mode due to inductors L_{m11} and L_{m12}. Inductor L_{K11}, L_{K1} and capacitor C_1 form a resonant network and they start to resonate. Moreover, diode D_2 is still kept in freewheeling mode by inductors L_{m21} and L_{m22}. When switch M_2 is turned on at the end of mode 6, the other half of one switching cycle will start.

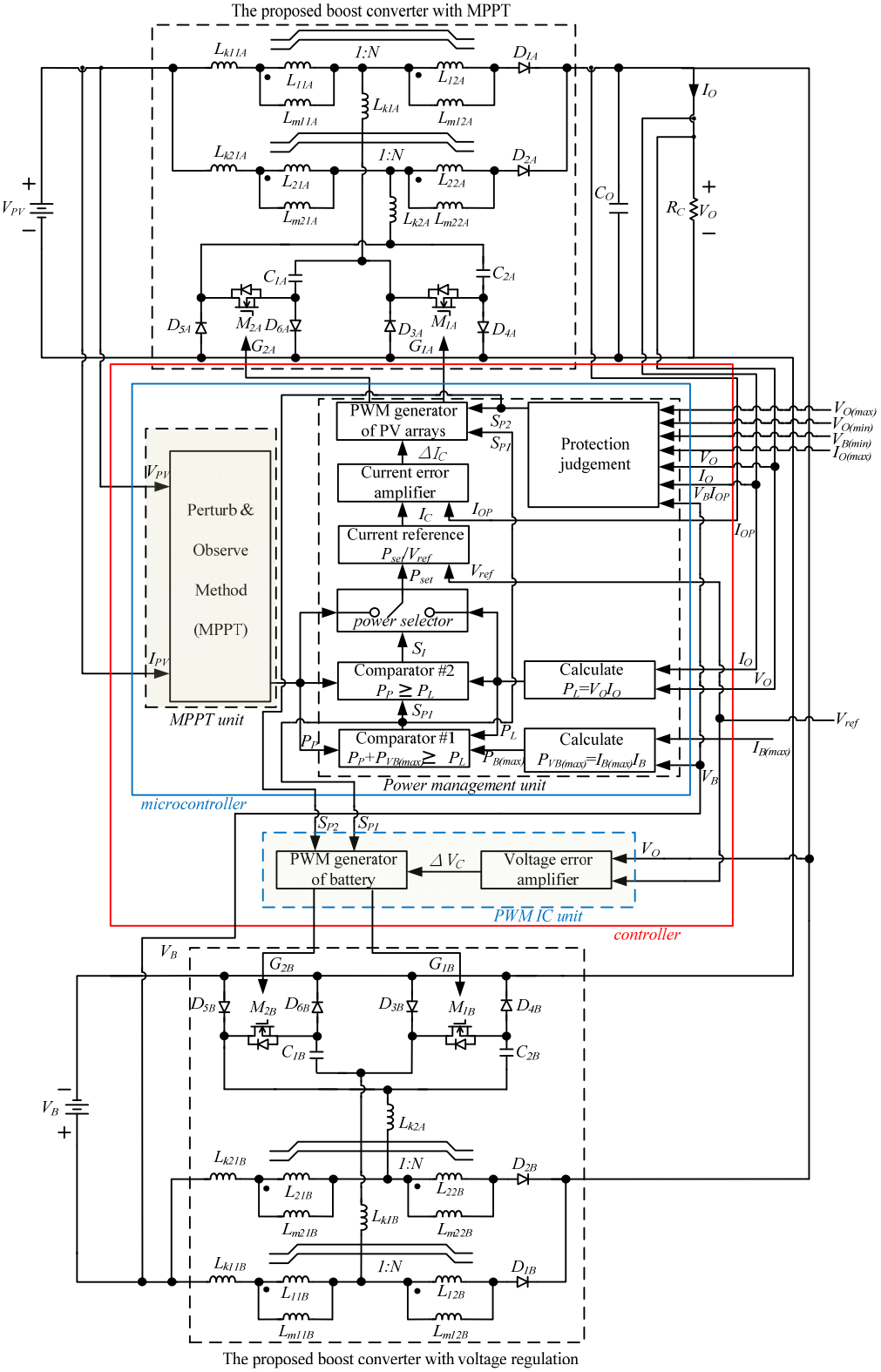
4. Control and Design of the Proposed PV Power System

In design considerations, the proposed one must match the operation conditions of MPPT for PV arrays and regulate the power between PV arrays and load by battery. In the following, control and design of the proposed PV power system are described.

4.1. Control of the Proposed PV Power System

The proposed PV power system consists of two boost converters and controller. The controller adopts a microcontroller and PWM IC. A block diagram of the proposed PV power system is shown in Figure 13.

Figure 13. Block diagram of the proposed PV power system.



In Figure 13, microcontroller is divided into two units: MPPT and power management units. In the MPPT unit, the perturb and observe method is adopted to track MPP of the PV arrays. The maximum power P_p of PV arrays can be decided by the MPPT unit. In the power management unit, the maximum discharging current $I_{B(max)}$ of the battery is set for obtaining the maximum battery charging power $P_{B(max)}$, which is equal to $V_B I_{B(max)}$. Output voltage V_O and current I_O are sent to the power management unit for attaining load power P_L. Power $P_{B(max)}$ and P_L are calculated by the multiplexer inside microcontroller, respectively. Three powers P_p, $P_{VB(max)}$ and P_L are sent to comparator #1 to judge the relationship of $(P_p + P_{VB(max)})$ and P_L. When $(P_p + P_{VB(max)}) \geq P_L$, signal S_{p1} is kept at a low level. PWM generators of PV arrays and battery are operated in a normal operational mode. In this operational condition, signals G_{1A}, G_{2A}, G_{1B} and G_{2B} are generated by two PWM generators to drive switches M_{1A}, M_{2A}, M_{1B}, and M_{2B}. As a result, the proposed boost converter depends on the MPPT control algorithm to extract the maximum power of the PV arrays to load, while the proposed one follows the voltage regulation control method to regulate the power between the PV arrays and load, and sustain a desired constant voltage across the load.

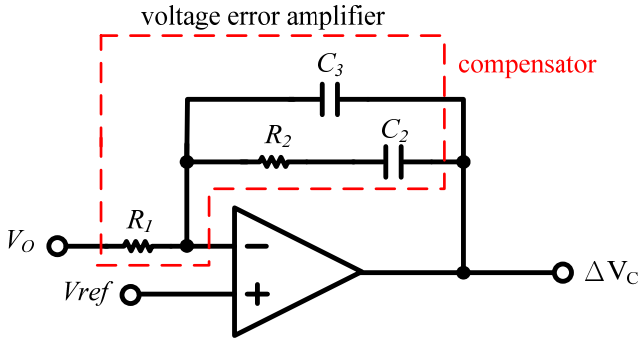
When $(P_p + P_{VB(max)}) < P_L$, signal S_{p1} reaches a high level. Two PWM generators are shut down. That is, the proposed PV power system is also shut down. When $(P_P + P_{B(max)}) \geq P_L$, comparator #2 is enabled by signal S_{P1} when S_{P1} is in a low level state. It is used to judge the power relationship of P_p and P_L. When P_p is equal to or greater than P_L, signal S_1 attains a high level. The output signal P_{set} of the power selector controlled by signal S_1 is set to be equal to P_L. When $P_p < P_L$, signal S_1 is in a low level state. The signal P_{set} is specified by P_P. The next step is to determine the current reference I_C. The P_{set} and V_{ref} are sent to the current reference unit. I_C can be obtained and it is equal to (P_{set}/V_{ref}). Note that V_{ref} is the reference voltage of the output voltage V_O. When current reference I_C is sent to the current error amplifier, it can be compared with I_{OP}, which is output current of the proposed boost converter with the MPPT control method to attain the current error value ΔI_C. When the PWM generator of the PV arrays receives ΔI_C, duty ratios of the PWM signals G_{1A} and G_{2A} can be determined by the value of ΔI_C. Signals G_{1A} and G_{2A} can drive switches M_{1A} and M_{2A} to generate power for supplying power to the load. Moreover, protection judgment receives signals of the practical values V_O, I_O and V_B, and those signals of the set values $V_{O(max)}$, $V_{O(min)}$, $I_{O(max)}$ and $V_{B(min)}$, which are determined by the operational conditions of the load and undercharge of the battery, respectively. When output voltage $V_O \geq V_{O(max)}$, the proposed PV power system is operated in over-voltage condition. Signal S_{P2} becomes a high level signal to shut down two PWM generators. When $V_O < V_{O(min)}$, the proposed one is operated in under-voltage condition. Therefore, signal S_{p2} is in the high level state and two PWM generators are shut down. If output current $I_O \geq I_{O(max)}$, the proposed system enters over-current condition. Two PWM generators are shut down. Moreover, when battery voltage $V_B \leq V_{B(min)}$, the battery enters the undercharge condition. The proposed one is also shut down. As mentioned above, protections of the proposed PV power system include over-voltage, over-current, undervoltage and undercharge protections.

The proposed boost converter with voltage regulation uses a lead-acid battery as its power source. Its main objectives are to regulate the power between PV arrays and load, and to sustain a constant output voltage for supplying power to the load. In order to implement power balance among PV arrays, battery and load, and sustain a constant output voltage, a PWM IC is adopted to control the proposed boost converter. Its control unit includes a voltage error amplifier and battery PWM generator. The

voltage error amplifier receives V_O and V_{ref}, which are determined by the voltage requirement of the load, to obtain the voltage error value ΔV_C, which is equal to ($V_{ref} - V_O$). The ΔVc is sent to the PWM generator of the battery to produce PWM signals G_{1B} and G_{2B}. Signals G_{1B} and G_{2B} can control switches M_{1B} and M_{2B} to regulate the power between the PV arrays and the load. Moreover, PWM IC can be shut down by signals S_{P1} and S_{P2} when signals S_{P1} or S_{P2} are in the high level state.

Figure 13 shows the block diagram of the proposed PV power system. The MPPT algorithm is implemented by a microcontroller. Since the power variation of PV arrays is slow, the compensator of the current error amplifier inside the microcontroller adopts proportional (P) control to implement MPPT control. In the proposed boost converter with voltage regulation, its compensator is set in the voltage error amplifier of PWM IC unit. According to the application note suggestions of the PWM IC datasheet supplied by the manufacturer, the compensator of the voltage error amplifier controller with two poles and one zero, as shown in Figure 14, is used to achieve a stable converter system.

Figure 14. Schematic diagram of voltage error amplifier in PWM IC unit.



In order to design a stable system for the proposed converter, a small signal model for the proposed one is derived. Since the proposed converter with active clamp circuit only helps switches achieve soft-switching features, it can be neglected in the derived converter. Moreover, the proposed one consists of two boost converters with interleaving manner to supply power to the load. In order to simplify the derivation of the small signal model, a single boost with coupled inductor is adopted to describe the control system design of the proposed one. In the proposed system, we assume that all the components are ideal and that the converter operates in a continuous conduction mode (CCM). Its equivalent circuit is shown in Figure 15. Figure 15a shows the corresponding equivalent circuit and Figure 15b illustrates the simple equivalent circuit. In Figure 15a, we can define the switching function as:

$$f = \begin{Bmatrix} 1, & S & ON \\ 0, & S & OFF \end{Bmatrix} \tag{1}$$

According to Equation (1), we can get:

$$\begin{cases} i_{L2} = (1-f)i_{L1} \\ V_{ab} = (1-f)\dfrac{V_O + NV_{PV}}{1+N} \end{cases} \tag{2}$$

When the parameter *f* is represented with duty ratio *d*, the average model is given by Figure 15c. The state space average equation of the equivalent circuit with state variables i_{L1} and V_C is depicted by where:

$$\begin{cases} \dot{X} = AX + BU, \\ Y = CX + DU, \end{cases}$$
$$\begin{cases} X = \begin{bmatrix} i_{L1} & v_c \end{bmatrix}^T, \\ A = \begin{bmatrix} -\dfrac{r_1}{L_1} & \dfrac{d-1}{L_1(1+N)} \\ \dfrac{1-d}{C_O} & -\dfrac{1}{R_L C_O} \end{bmatrix}, \\ B = \begin{bmatrix} \dfrac{1+Nd}{L_1(1+N)} & 0 \end{bmatrix}^T, \\ C = \begin{bmatrix} 0 & 1 \end{bmatrix}, and \\ D = 0. \end{cases} \tag{3}$$

By substituting $I_{L1} + \hat{i}_{L2}, D + \hat{d}$ (I_{L1}, I_{L2} and D are the steady components, while $\hat{i}_{L1}, \hat{i}_{L2}$ and $\hat{d}$ are the small disturbance quantities), and $i_{L2} = (1 - d)i_{L1}$ in Equations (2) and (3), they can be rewritten by Laplace transformation and be expressed by:

$$\begin{aligned} G(s) &= \frac{\hat{V}_O(s)}{\hat{d}(S)} = \frac{V_O}{(1-D)} \frac{((1-D)R_L)/(1+ND)L_1) - s)(s + (1/(R_L C_O)))}{s^2 + ((1/R_L C_O)s) + ((1-D)^2 / L_1 C_O(1+N))} \\ &= K \frac{((1/Tz_1) - s)(s + (1/Tz_2))}{(s + (Tp_1))(s + (1/Tp_2))} \end{aligned} \tag{4}$$

where:

$$\begin{cases} K = \dfrac{V_O}{(1-D)}, \\ T_{Z1} = \dfrac{(1+ND)L_1}{(1-D)R_L}, \\ T_{Z2} = R_L C_O, \\ T_{P1} = \dfrac{4}{(1/R_L C_O) + \sqrt{(1/R_L C_O)^2 - 4(1-D)^2/(L_1 C_O(1+N))}}, \\ T_{P2} = \dfrac{4}{(1/R_L C_O) - \sqrt{(1/R_L C_O)^2 - 4(1-D)^2/(L_1 C_O(1+N))}}. \end{cases}$$

Its detailed analysis is proposed in [30]. The open-loop control of the proposed converter is shown in Figure 15c. Its block diagram of the closed-loop control system is illustrated in Figure 16. In Figure 16, $H(s)$ (= $1/K_f$) represents the sensor gain, $G(s)$ (= $(1 + sC_2R_2)/[sR_1(C_2 + C_3)][1 + sR_2(C_2//C_3)]$) is the transfer ratio of the compensator, $P(s)$ (= $1/V_M$) depicts that of the pulse-width modulator and $G(s)$ expresses that of the converter. Its closed-loop transfer function from V_{ref} to V_O is expressed by:

$$\frac{\hat{V}_O(s)}{\hat{V}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \tag{5}$$

where $T(s)$ (= $[H(s)G_C(s)G(s)]/V_M$) is the loop gain.

Figure 15. Equivalent circuit based on (**a**) ideal switch; (**b**) switching function; and (**c**) average equivalent circuit.

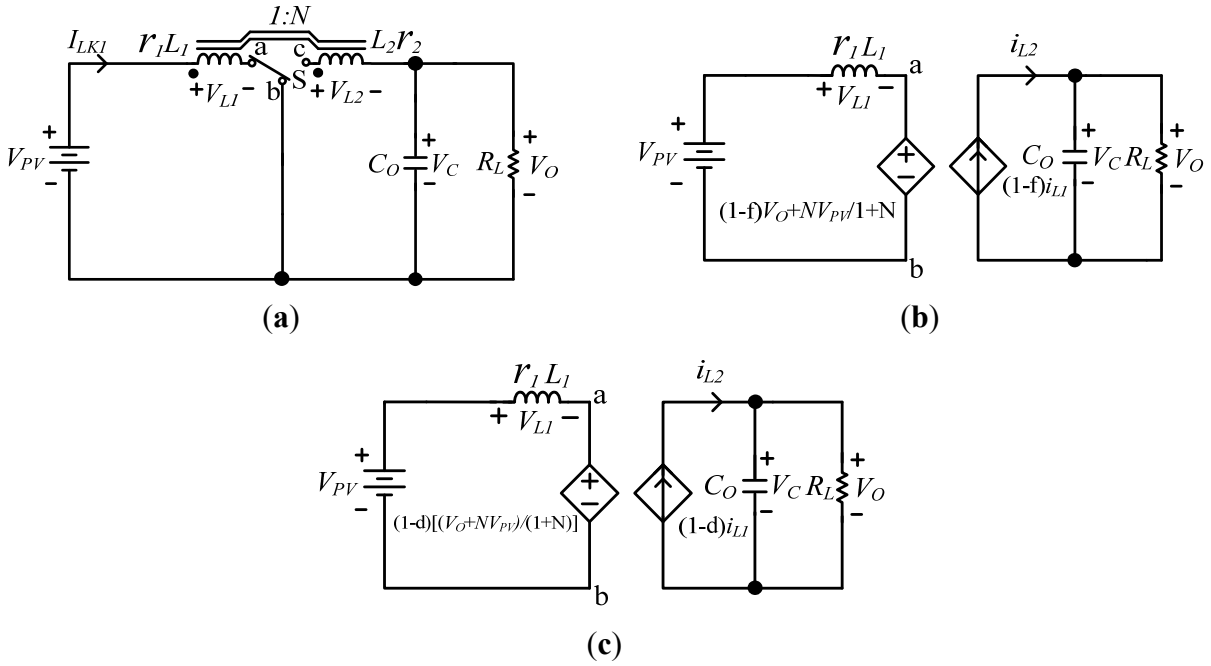
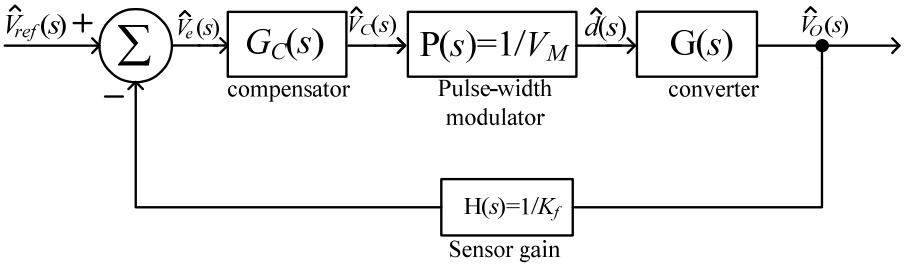


Figure 16. Block diagram of the closed-loop control system of the proposed converter.



4.2. Design of the Proposed Interleaved Boost Converter

Since the dc/dc converter using PV arrays as its power source, as shown in Figure 14, can be operated under current and voltage regulation, respectively, according to the different operational conditions, the components of the two dc/dc converters have the same design values. Due to the fact the switches in the two boost converters use the synchronous switch technique to simplify them, the ratios are limited to 0.5. In the design of the interleaved active clamp boost converter, determination of duty ratio D, coupled inductances (L_{m11} and L_{m12}) and (L_{m21} and L_{m22}), active clamp capacitors C_1 and C_2, and output filter are important. In the following, their designs are analyzed briefly.

4.2.1. Duty Ratio D

To determine the duty ratio D, we must first establish the input to output voltage transfer ratio M. Since the active clamp circuit helps switches M_1 and M_2 to achieve soft-switching features, transfer ratio M of boost converter has a slightly different value compared with the one without active clamp circuit. As a result, transfer ratio M of the proposed one is regarded as that of the conventional one. According to the volt-second balance principle of a coupled inductor L_{m11}, the following equation can be obtained:

$$V_{PV}DT_s + [\frac{-(V_D - V_{PV})}{N+1}(1-D)T_S] = 0 \tag{6}$$

where N is turns ratio of couple inductor (L_{m11} and L_{m12}) or (L_{m21} and L_{m22}) and T_s is period switch M_1. From Equation (1), transfer ratio M can be expressed by:

$$M = \frac{V_o}{V_{PV}} = \frac{(1+ND)}{(1-D)} \tag{7}$$

Based on the operational condition of the proposed boost converter with switch integration, duty ratio D of switch M_1 or M_2 is limited to 0.5 and they are operated in complementary fashion. According to Equation (7), a large duty ratio D corresponds to a smaller turns ratio N of the coupled inductor, which results in a lower current stress being imposed on switches M_1 and M_2, as well as voltage stresses on diodes D_1 and D_2. However, in order to accommodate variations of load, line voltage, component values and duty loss, it is better to select an operating range D = 0.35~0.4.

4.2.2. Coupled Inductors (L_{m11} and L_{m12}) or (L_{m21} and L_{m22})

Once the duty ratio D is selected, the turns ratio N of coupled inductors L_{m11} and L_{m12} can be determined using Equation (7), which yields

$$N = \frac{(1-D)V_o - V_{PV}}{DV_{PV}} \tag{8}$$

By applying Faraday's law, N_{11} of coupled inductor can be given by:

$$N_{11} = \frac{DV_{PV}T_s}{A_c \Delta B} \tag{9}$$

where A_c is the effective cross-section area of the coupled inductor core and ΔB is the working flux density. According to Equations (8) and (9), N_{12} can therefore be determined.

To achieve a *ZVS* feature, the energy stored in the leakage inductor L_{K11} (or L_{k21}) and external inductor L_{k1} (or L_{k2}) must satisfy the following inequality:

$$\frac{1}{2}(L_{K11} + L_{K1})(I_{LK11(tv10)} - I_{LK11(tv11)})^2 \geq \frac{1}{2}C_T V_{DS1}{}^2{}_{(\max)} \tag{10}$$

where L_{k1} is the external inductor to increase operational ranges of the soft-switching circuit, $I_{LK11(tv11)}$ is the current of L_{k11} at time t_{11}, $I_{Lk11(tv10)}$ is that at time t_{10}, C_T is the total capacitor which is the sum of C_{M1} and C_{M2}, and $V_{DS1(max)}$ represents the maximum voltage across switch M_1 and its value is equal to

$[V_{PV} + (V_O - V_{PV})/(N + 1)]$. According to the circuit operational principle, the voltage V_{C1} across capacitor C_1 can be approximately expressed by:

$$V_{C1} = \frac{NV_{PV} + V_O}{N+1} \tag{11}$$

Once C_T, and $I_{LK11(tv10)}$ and $I_{LK11(tv11)}$ are specified, the inequality of inductor L_T (= L_{K1} + L_{K11}) can determined as:

$$L_T \geq \frac{C_T(NV_{pv} + V_O)^2}{(N+1)^2(I_{LK11(tv10)} - I_{LK11(tv11)})^2} \tag{12}$$

Since the proposed converter is operated in continuous conduction mode (CCM), inductances L_{m11} and L_{m12} must be greater than L_{m11B} and L_{m12B}, respectively, which are the inductances at the boundary of CCM and discontinuous conduction mode (DCM). Its boundary current waveforms are shown in Figure 17. From Figure 17, it can be seen that when switch M_1 is turned on, inductor current I_{LK11} is the sum of I_{Lm11} and I_{N11}, which is the equivalent reflected current from the secondary winding N_{12} to the primary winding N_{11}. Therefore, current I_{LK11} can be expressed by:

$$I_{LK11} = I_{Lm11} + I_{N11} \tag{13}$$

where I_{N11} is equal to NI_{N12} (= NI_{Lm12}). Therefore, $I_{LK11(1)}$ can be determined as:

$$I_{LK11(1)} = \frac{V_{PV}}{L_{m11B}}DT_S + \frac{N^2V_{PV}}{L_{m12B}}DT_S \tag{14}$$

where L_{m11} is the magnetizing inductor of primary winding of coupled inductor and L_{m12} is its secondary winding inductor. According to Equation (14), $I_{LK11(1)}$ can be rewritten by:

$$I_{LK11(1)} = \frac{2V_{PV}}{L_{m11B}}DT_S \tag{15}$$

Moreover, $I_{LK11(2)}$ can be given by:

$$I_{LK11(2)} = \frac{I_{LK11(1)}}{(1+N)} = \frac{2V_{PV}}{(1+N)L_{m11B}}DT_s \tag{16}$$

Since current $I_{D1(1)}$ is equal to $I_{LK11(2)}$ and average current $I_{D1(av)}$ equals half of output current I_O, the average current $I_{D1(av)}$ can be expressed as follows :

$$I_{D1(av)} = \frac{I_o}{2} = \frac{V_{PV}}{(1+N)L_{m11B}}D(1-D)T_s \tag{17}$$

According to Equation (17), the boundary inductance L_{m11B} can be determined as:

$$L_{m11B} = \frac{2V_{PV}}{(1+N)I_o}D(1-D)T_{s.} \tag{18}$$

Based on the magnetic principle of coupled inductor, the relationship between inductances L_{m11B} and L_{m12B} can be expressed as follows:

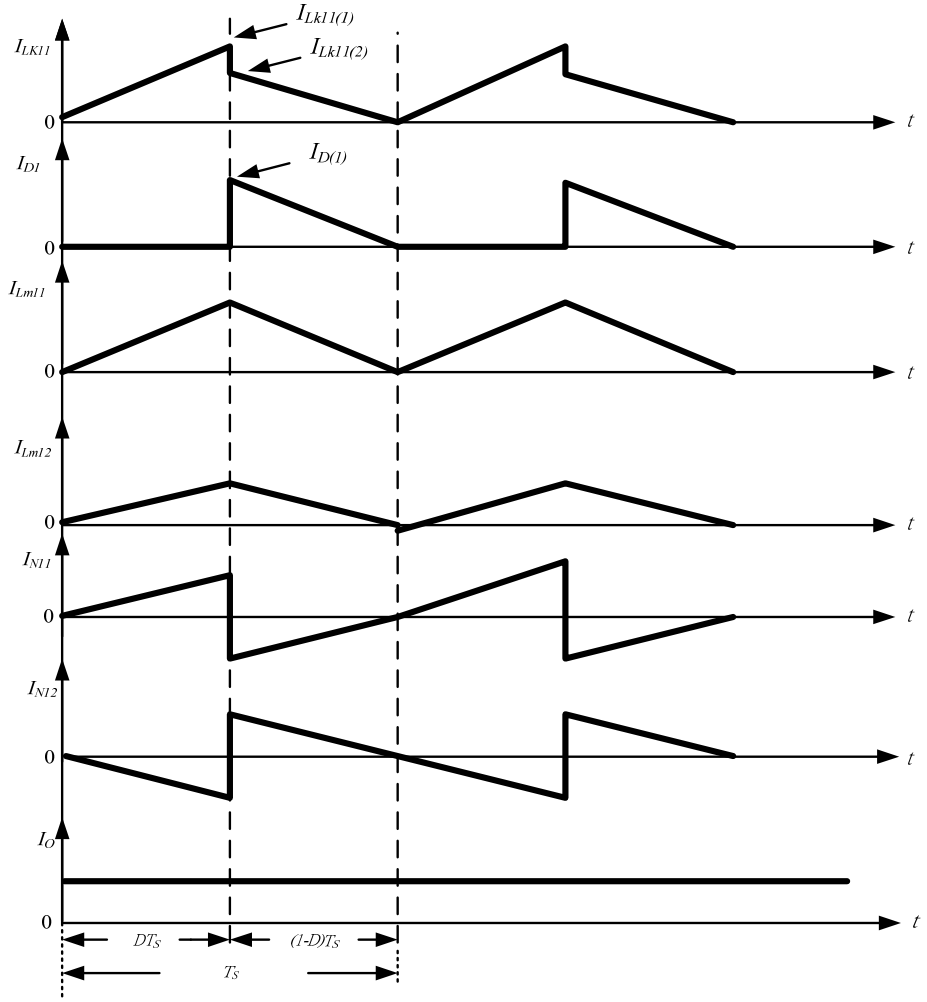
$$L_{m12B} = N^2L_{m11B} \tag{19}$$

Substituting Equations (18) in (19), inductor L_{m12B} can be determined as:

$$L_{m12B} = \frac{2N^2 V_{PV}}{(1+N)I_o} D(1-D)T_s \tag{20}$$

According to the operational requirements of the proposed boost convertor which is operated in CCM, inductors L_{m11} and L_{m12} must be greater than L_{m11B} and L_{m12B}, respectively. Since $L_{m21} = L_{m11}$ and $L_{m22} = L_{m12}$, inductors L_{m21} and L_{m22} are also separately greater than L_{m11B} and L_{m12B}.

Figure 17. Conceptual current waveforms of inductor currents and output current in the proposed converter operated at the boundary of CCM and DCM.



4.2.3. Active Clamp Capacitor C_1 or C_2

The active clamp Capacitors C_1 and C_2 are used to achieve soft-switching features. In order to achieve ZVS features, one half of the resonant period formed by L_T and C_1 or L_T and C_2 should be equal to or greater than the maximum off time of switches M_1 or M_2. Therefore, capacitor C_1 (or C_2) must satisfy the following inequality:

$$\pi\sqrt{L_T C_1} \geq t_{off} = (1-D)T_s \tag{21}$$

From Equations (12) and (21), when L_T is specified, the capacitance ranges of C_1 (or C_2) can be determined as:

$$C_1 \geq \frac{(1-D)^2 T_s^2}{\pi^2 L_T} \tag{22}$$

4.2.4. Output Capacitor C_o

The output capacitor C_o is primarily designed for reducing ripple voltage. The ripple voltage ΔV_{rco} across output capacitor C_o is determined by:

$$\Delta V_{rco} = \frac{\Delta Q_{co}}{2C_o} = \frac{1}{2C_o}(I_{o(\max)} D T_s) \tag{23}$$

where $I_{O(max)}$ is the maximum output current.

5. Experimental Results

The proposed PV power system is shown in Figure 13. To verify the performance of the proposed PV power system, two dc/dc converters using an interleaved active clamp boost converter with coupled inductor to generate dc voltage of 400 V for dc load applications with the following specifications were implemented:

A. The proposed boost converter with MPPT

- Input voltage V_{PV}: 34~42 V_{dc} (PV arrays);
- Output voltage V_O: 400 V_{dc};
- Output maximum current $I_{OP(max)}$: 3 A; and
- Output maximum power $P_{PV(max)}$: 1.2 kW.

B. The proposed boost converter with voltage regulation

- Input voltage V_B: 40~54 V_{dc} (four sets of 12 V batteries connected in series);
- Output voltage V_O: 400 V_{dc};
- Output maximum current $I_{OB(max)}$: 3 A; and
- Output maximum power $P_{B(max)}$: 1.2 kW.

According to designs and specifications of the proposed boost converters, components of power stages in the proposed two boost converters are determined as follows:

- Switches M_{1A}, M_{2A}, M_{1B}, M_{2B}: IRFP260N×2 (connected in parallel);
- Diodes D_{1A}, D_{2A}, D_{1B}, D_{2B}: DSSK60-02A;
- Diodes D_{3A}, D_{4A}, D_{5A}, D_{6A}: DSSK60-02A;
- Diodes D_{3B}, D_{4B}, D_{5B}, D_{6A}: DSSK60-02A;
- Coupled inductors L_{m11}, L_{m21}: 28 μH;
- Leakage inductors of coupled inductor (L_{m11}, L_{m12}) and (L_{m21}, L_{m22}): 0.8 μH and 0.81 μH;
- Cores of coupled inductors (L_{m11}, L_{m12}) and (L_{m21}, L_{m22}): EE-55;
- Turns ratio N: 15; and

- Extera inductors L_{k1}, L_{k2}: 1.2 μH.

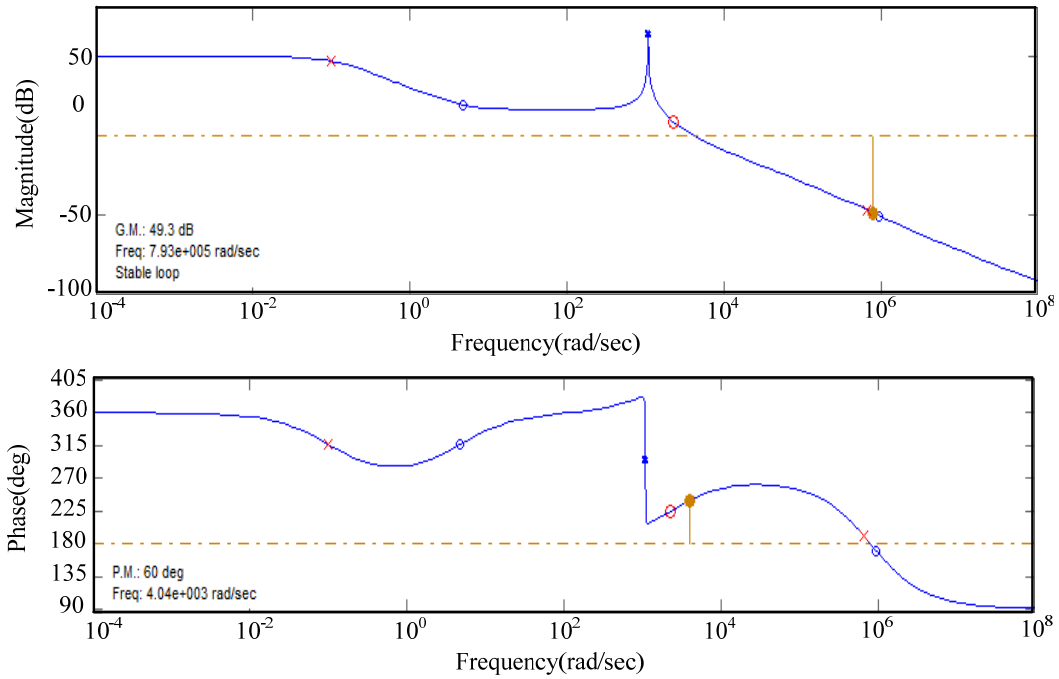
According to the previous specifications and the compensator of the proposed converter, parameter values of the small signal model in the proposed system (as shown in Figure 16) are listed in Table 1.

Table 1. Parameter values of small signal model of the proposed converter.

symbol	parameter value
V_O	400
D	0.36
L_1	28 μH
N	15
C_O	780 μF
R_L	266.66 Ω
R_1	10 kΩ
R_2	220 Ω
C_2	2 μF
C_3	6.8 nF
V_M	2.5
K_f	160

We can use the Matlab simulation tool to obtain Bode plots of the proposed converter under the closed loop condition. They are shown in Figure 18. From Figure 18, it can be seen that P.M. of the proposed one is 60°. Therefore, this can prove that the proposed converter is a stable system.

Figure 18. Bode plots of the proposed converter under the closed loop condition.



Since the proposed interleaved PV power system uses PV arrays and batteries as its input sources, the maximum output power of the proposed PV power system can supply 2.4 kW. In order to extend battery discharge time, the maximum output power of the battery module is suggested to be 1.2 kW. In

our research, four sets of lead-acid batteries (12 V/75 Ah) connected in series are adopted in the proposed converter. According to discharge times supplied by the battery manufacturer, a sustained discharge time of 2 hours is possible when the output power of battery is 1.2 kW, while the discharge time can extend to 8 hours when it is 500 W. The curve of output power *versus* discharge time of batteries as supplied by the battery manufacturer is shown in Figure 19, while the curve of discharge time *versus* discharge current (CA) of the batteries is depicted in Figure 20.

Figure 19. Plot of output power *versus* discharge time of the batteries supplied by battery manufacturer.

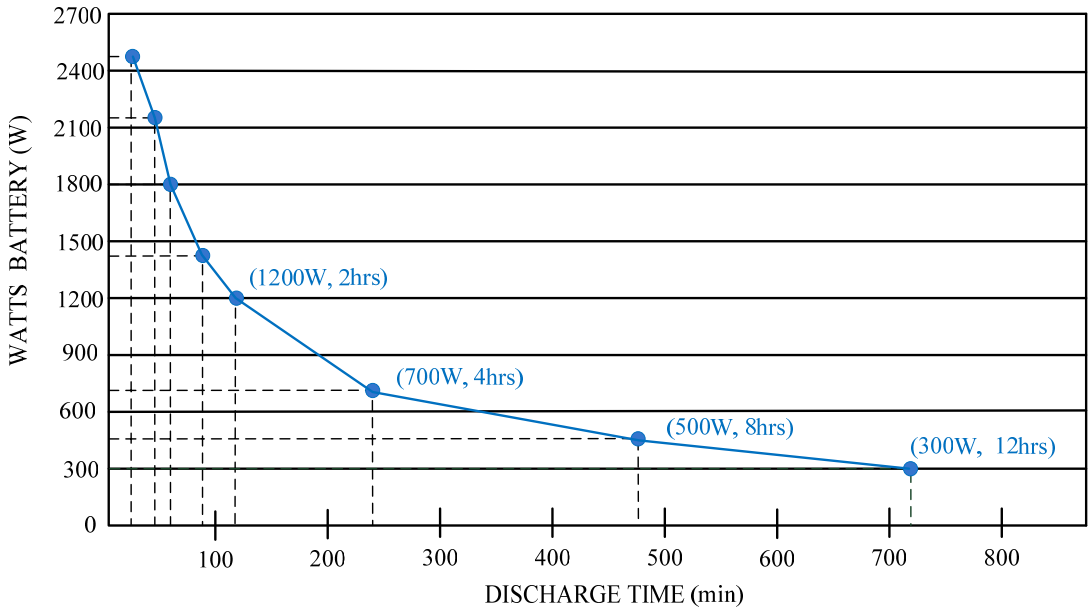
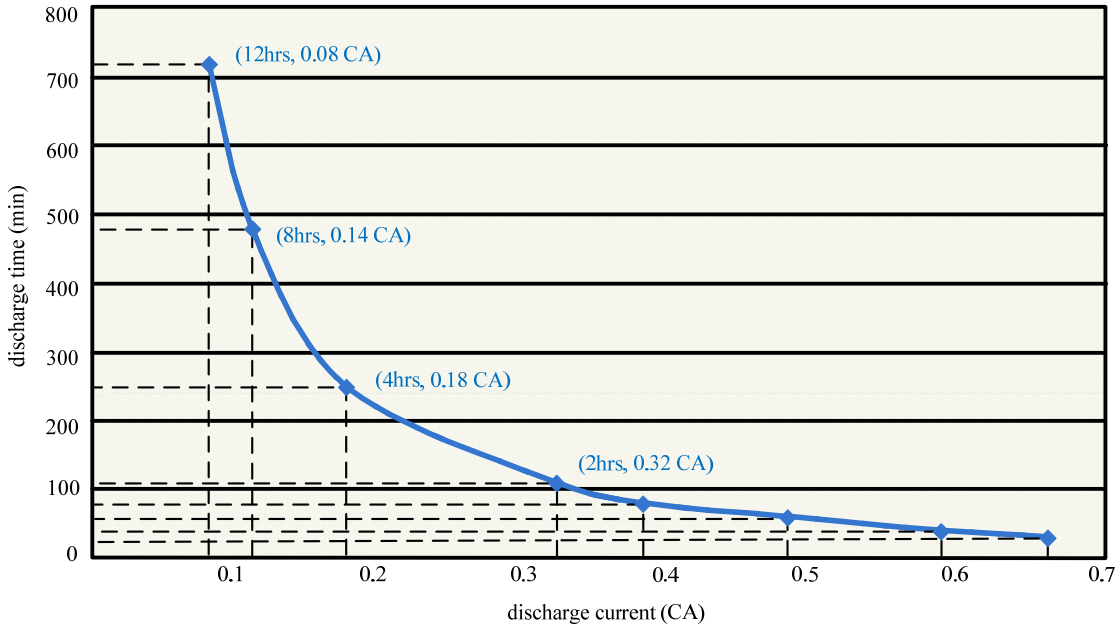


Figure 20. Plot of discharge time *versus* discharge current (CA) of batteries supplied by the battery manufacturer.



From Figure 20, it can be seen that when output power of battery is 1.2 kW, its discharge current is 0.32 CA. When the battery is completely discharged, a battery charger is adopted. The block diagram of the proposed PV power system and battery charger is shown in Figure 21. When the battery is in the charging state during the night, switch S_1 is turned on and a battery charger using a buck converter is adopted to charge the battery. On the other hand, when the battery in the discharging state during the day, switch S_2 is turned on and battery uses the proposed converter to supply power to the load. A photograph of the hardware is shown in Figure 22.

Figure 21. Block diagram of the proposed PV power system and battery charger.

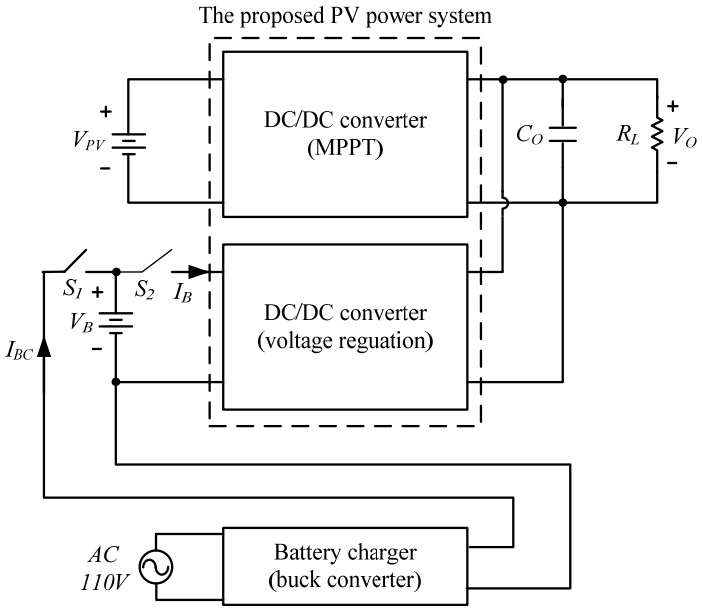


Figure 22. Photograph of the hardware for the proposed PV power system and battery charger.

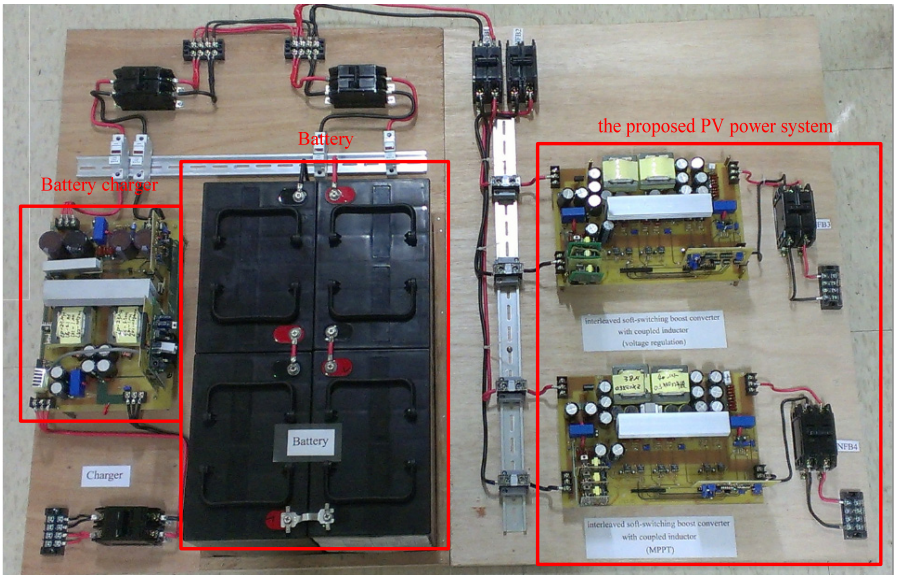
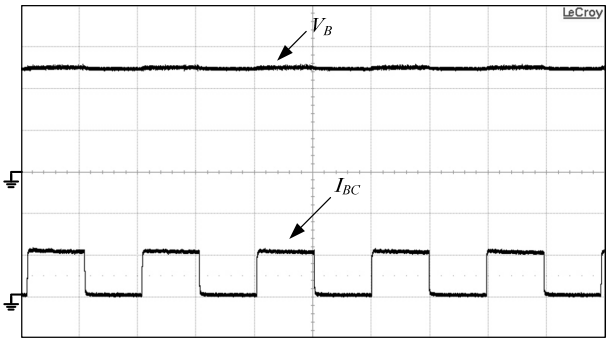


Figure 23 shows measured charging voltage V_B and current I_{BC} waveforms of the battery, illustrating that the charging current I_{BC} uses the pulse current charging method and its charging current I_{BC} is under the repeat period of 200 ms, duty ratio of 0.5 and peak charging current of 20 A.

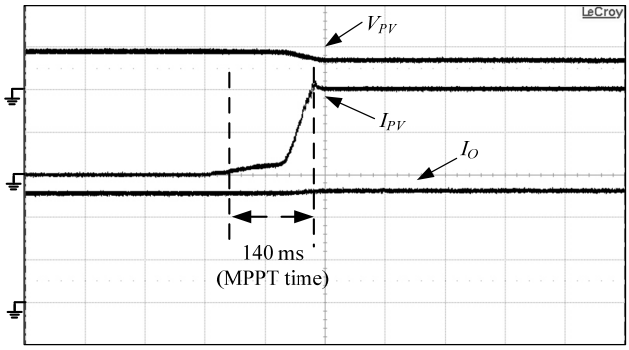
When the battery voltage V_B reaches its end of charge voltage V_{FV} (about 54 V), the battery charger is shut down. Figure 24 shows measured voltages and currents waveforms of the proposed PV power system under output power P_O of 1 kW and PV arrays maximum output power $P_{PV(max)}$ of 700W. Figure 24a shows measured PV arrays voltage V_{PV}, current I_{PV} and output current I_O waveforms, while Figure 24b depicts measured battery voltage V_B, current I_B and output current I_O waveforms.

Figure 23. Measured charge voltage V_B and charge current I_{BC} waveforms of battery under the repeat period of 200 ms, duty ratio of 0.5 and peak charging current of 20 A.



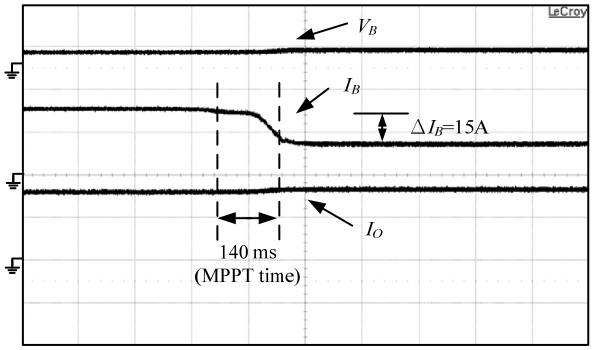
(V_B: 20 V/div, I_{BC}: 20 A/div, time: 100 ms/div)

Figure 24. Measured voltage and currents waveforms of the proposed PV power system under output power P_O of 1 kW and PV arrays maximum power $P_{PV(max)}$ of 700 W: (**a**) P_V arrays voltage V_{PV}, current I_{PV} and output current I_O waveforms; and (**b**) battery voltage V_B, current I_B and output current I_O waveforms.



(V_{PV}: 50 V/div, I_{PV}: 10 A/div, I_O: 1 A/div, time: 100 ms/div)

(**a**)



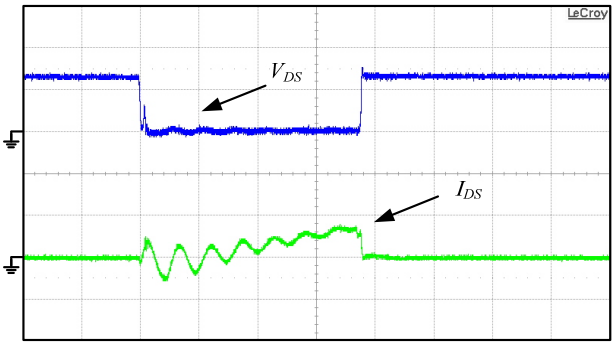
(V_B: 50 V/div, I_B: 20 A/div, I_O: 1 A/div, time: 100 ms/div)

(**b**)

From Figure 24, it can be seen that MPPT time of PV arrays is about 140 ms from 0 to 700 W and battery discharging current I_B varies from 30 A to 15 A. This proves that the proposed PV power system can regulate the output powers of the battery and PV arrays to supply power to the load.

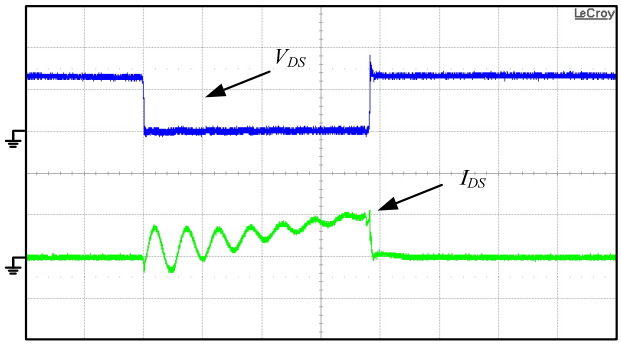
In order to verify the feasibility of the proposed interleaved active clamp boost converter with voltage regulation, measured voltage V_{DS} and I_{DS} waveforms of switches M_{1B} and M_{2B} are shown in Figures 25 and 26, respectively. Figure 27 shows those waveforms under 10% of full load condition, while Figure 26 depicts those waveforms under full load condition. From Figure 25, it can be found that when load is at 10% of full load condition, switches M_{1B} and M_{2B} are in the hard switching and soft switching boundary, respectively.

Figure 25. Measured voltage V_{DS} and current I_{DS} waveforms of (**a**) switch M_{1B} and (**b**) switch M_{2B} of the proposed converter 10% of full load.



(V_{DS}: 50 V/div, I_{DS}: 10 A/div, time: 2 μs/div)

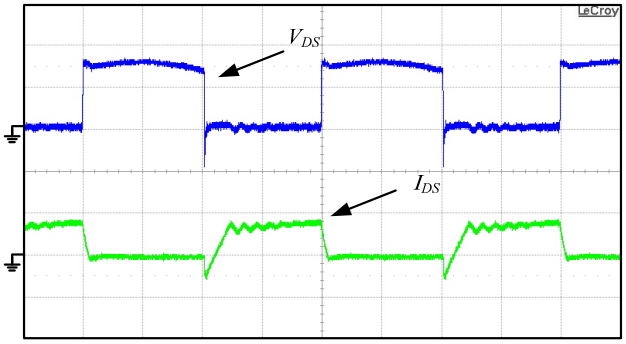
(**a**)



(V_{DS}: 50 V/div, I_{DS}: 10 A/div, time: 2 μs/div)

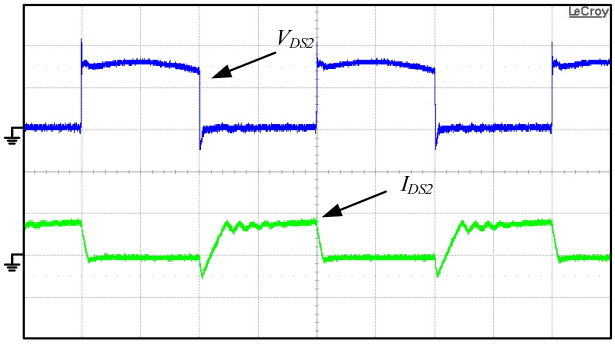
(**b**)

Figure 26. Measured voltage V_{DS} and current I_{DS} waveforms of (**a**) switch M_{1B} and (**b**) switch M_{2B} of the proposed converter under full load.



(V_{DS}: 50 V/div, I_{DS}: 50 A/div, time: 5 μs/div)

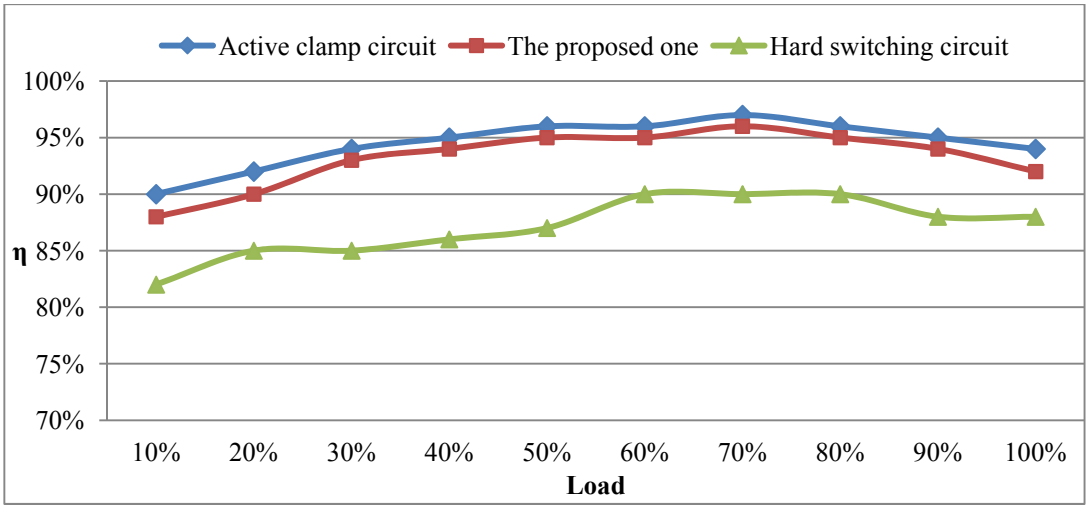
(**a**)



(V_{DS}: 50 V/div, I_{DS}: 50 A/div, time: 5 μs/div)

(**b**)

Figure 27. Comparison conversion efficiency among the interleaved active clamp boost converter with hard-switching circuit, active clamp circuit and the proposed one.



When the load is greater than 10% of full load, switches M_{1B} and M_{2B} can be operated with ZVS at turn on. Comparison of the conversion efficiency among the interleaved boost converter with hard-switching circuit, the active clamp circuit (as shown in Figure 3) and the proposed one is shown in Figure 27. It reveals that the efficiencies of the boost converter with the active clamp circuit and the proposed one are always higher than that with a hard-switching circuit from light load to heavy load. Moreover, efficiency of the boost with the proposed circuit is approximately the same as that with the active clamp circuit (as shown in Figure 3) from light load to heavy load. The reason for this is that although currents flowing through diodes D_{4B} and D_{6B} have larger losses, compared with the boost converter with the active clamp circuit shown in Figure 3, the diode current I_{D6B}, which flows through diode D_{6B} shown in Figure 13, is the sum of current I_{M2B} and resonant current I_{C1B}. Since current I_{C1B} is a resonant current, the negative resonant current I_{C1B}, which is shown in Figure 12 during t_9~t_{10} interval, does not flow through diode D_{6B}. Therefore, this can partially reduce the forward conduction losses of diode D_{6B}. Similarly, the forward conduction losses of diode D_{4B} can also be reduced. As mentioned above, the boost converter with the proposed circuit can also keep it at a high conversion efficiency from light load to heavy load. Its maximum efficiency is 96% under 70% of full load conditions and its full load efficiency is about 92%. According to the efficiency curve of the proposed interleaved boost converter shown Figure 27 and the circuit structure, its performance can compare with the results in [28] and [29]. The performance comparison results are listed in Table 2. Note that the special capacitor is required to possess a lower ESR and a higher CRR and the special PWM IC possesses a larger duty ratio, greater than 0.5.

Table 2. Performance comparison of interleaved high step-up converters.

High step-up interleaved converter	**Converter in [28]**	**Converter in [29]**	**The proposed converter**
Voltage gain	$\frac{N+2}{1-D}$	$\frac{2(N+1)}{1-D}$	$\frac{N+2}{1-D}$
Voltage stress on switch	$\frac{N+2}{1-D}$	$\frac{V_O}{N+2}$	$\frac{V_O+NV_{PV}}{N+1}$
Voltage stress on diodes	$\frac{N+2}{1-D}$	$\frac{NV_O}{N+1}$	V_O+NV_{PV}
Quantities of switches	2	2	2
Quantities of diodes	6	4	4
Quantities of cores	4	2	$4\,(\frac{\text{2 main cores}}{\text{2 resonant cores}})$
Quantities of capacitors	4 (special capacitors)	(special capacitors)	3
Maximum duty ratio	>0.5	>0.5	<0.5
Controller	Complex (special PWM IC)	Complex (DSP)	Simple
Cost	High	Middle	Low
Efficiency	Higher	Higher	High
Power level	Small power	Small or middle power	Middle or high power

In order to simply analyze the CRR_S of the proposed one and the conventional one proposed in [29], we assume that values of output capacitors C_1, C_2 and C_3 of the conventional one are equal to that of output capacitor C_O, and their voltages V_{C1}, V_{C2} and V_{C3} are the same value. Each output capacitor of the proposed one and the conventional one adopt the same current I_{D1} to charge them, as shown in

Figure 28. According to the previously assumed conditions, the equivalent circuit of the output terminals is shown in Figure 29.

Figure 28. Conceptual current waveforms of inductor current, diode current, output capacitor current and output current in the proposed converter operated converter operated in the boundary of CCM and DCM.

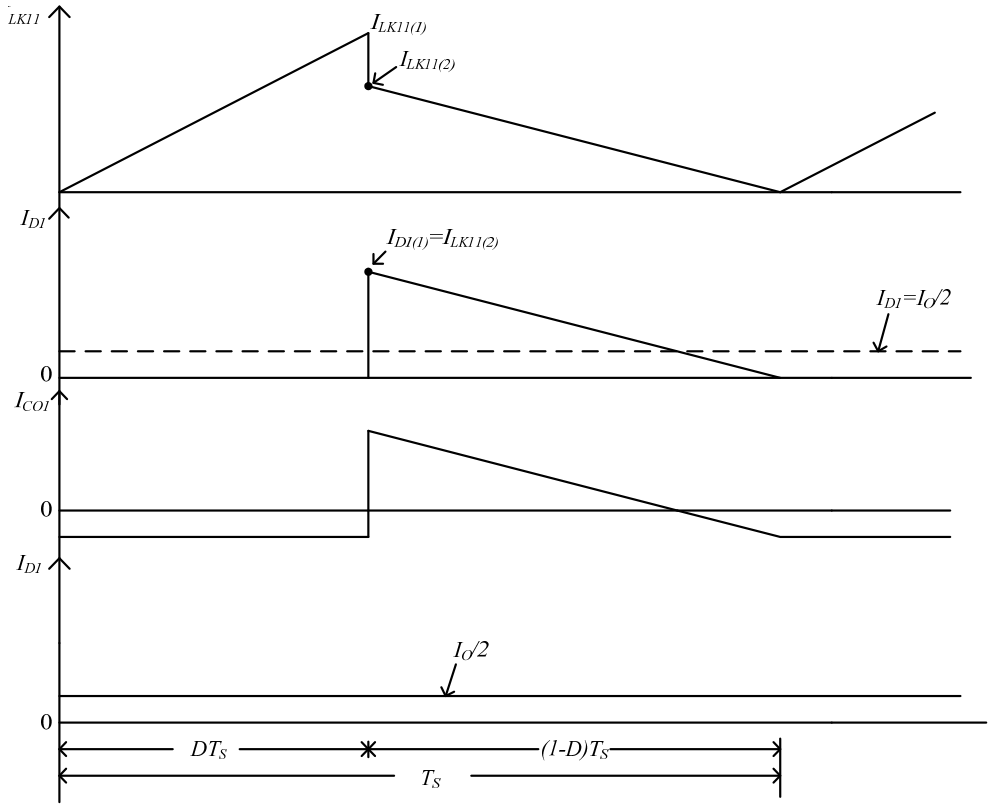


Figure 29. Equivalent circuit of output terminals: (**a**) the proposed converter; (**b**) the conventional converter proposed in [29]; and (**c**) the simplified conventional converter proposed in [29].

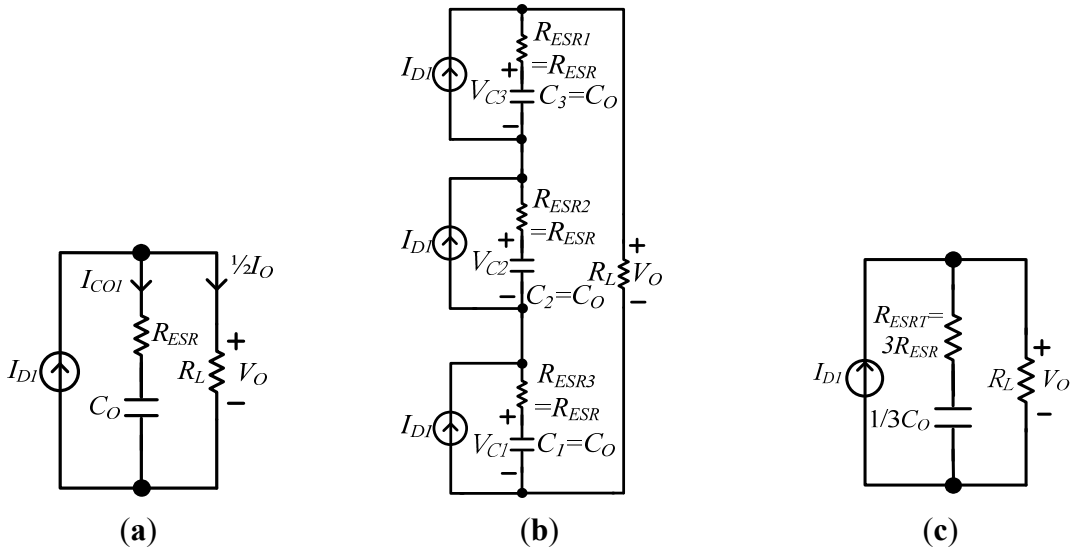
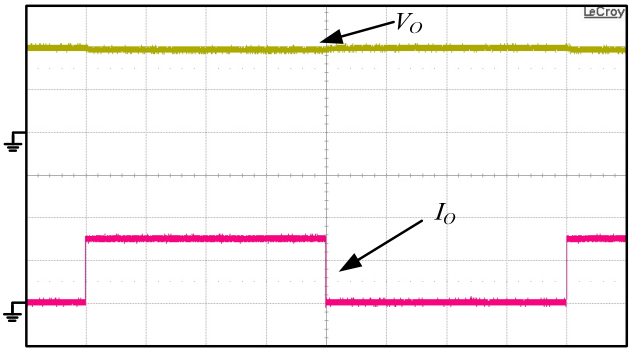


Figure 29a shows the one of the proposed converter, while Figure 29b illustrates the one of the conventional one. Its simplified equivalent circuit is shown in Figure 29c. From Figure 29, it can be found that the equivalent ESR R_{ESRT} (= $3R_{ESR}$) of the conventional one is greater than that of the proposed one. That is, output capacitors of the conventional one must have a higher CRR, which is proportional to the ESR of the capacitor. Therefore, the system reported in [28] is suitable for low power level applications. The system in [29] is applied to low or middle power level applications. The proposed PV power system can be applied to a middle or high power level application. Figure 30 illustrates the step-load change be between 0% and 100% of full load, from which it can be observed that voltage regulation of output voltage V_O has been limited with in ±1% to prove a good dynamic response.

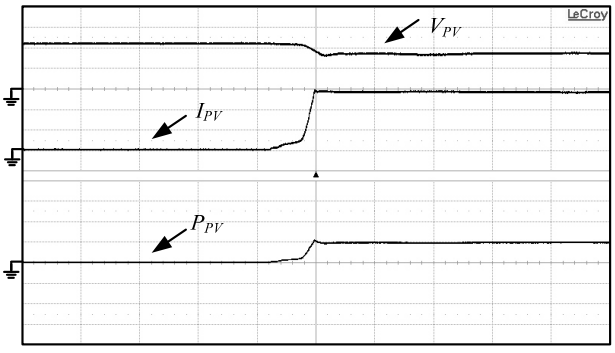
Figure 30. Output voltage V_O and output current I_O under step-load changes between 0% and 100% of the full load condition of the active clamp interleaved boost converter.



(V_O: 200 V/div, I_O: 2 A/div, time: 50 ms/div)

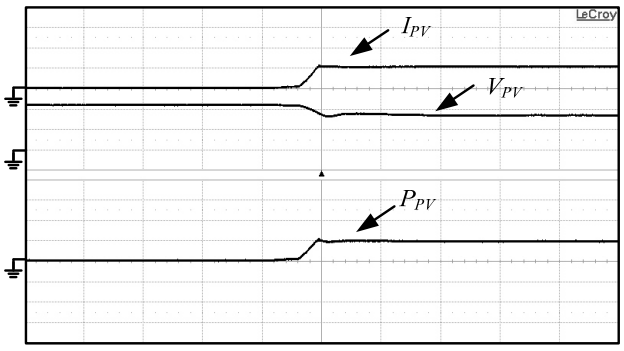
The MPPT waveforms of the proposed interleaved active clamp boost converter with MPPT are shown in Figure 31. Figure 31a shows those waveforms under the maximum PV arrays power of 500 W, while Figure 31b illustrates those waveforms under the maximum power of 750 W. From Figure 31, it can be found that the tracking time of MPPT is about 70 ms from 0 to the maximum power of PV arrays.

Figure 31. Measured voltage V_{PV}, current I_{PV} and power P_{PV} waveforms of PV arrays (**a**) under $P_{PV(max)}$ = 500 W; and (**b**) under $P_{PV(max)}$ = 750 W.



(V_{PV}: 20 V/div, I_{PV}: 5 A/div, P_{PV}: 500 W/div, time: 200 ms/div)

(a)

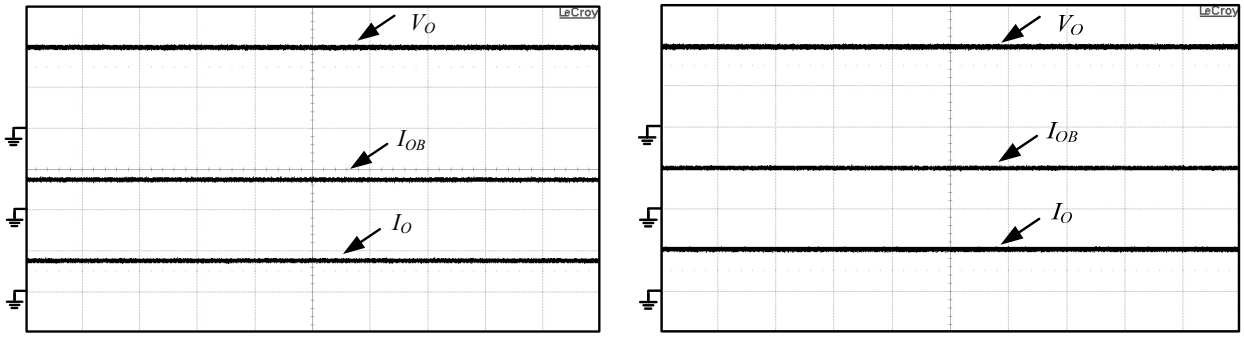


(V_{PV}: 20 V/div, I_{PV}: 20 A/div, P_{PV}: 750 W/div, time: 200 ms/div)

(b)

Measured output voltage V_O and current I_{OB} and I_O when the operational mode is within mode IV and $P_{VB(max)} \geq P_L$ in power management of the proposed PV system is shown in Figure 32. Figure 32a depicts those waveforms under $P_L = 320$ W, while Figure 32b shows those waveforms under $P_L = 800$ W. From Figure 32, it can be seen that output voltage V_O is sustained at 400 V and current I_{OB} is equal to I_L.

Figure 32. Measured voltage V_O, current I_{OB} and I_O waveforms of the proposed PV power system operated in mode IV (**a**) under $P_L = 320$ W; and (**b**) under $P_L = 800$ W.



(V_O: 200 V/div, I_{OB}: 1 A/div, I_O: 1A/div, time: 500 μs/div)

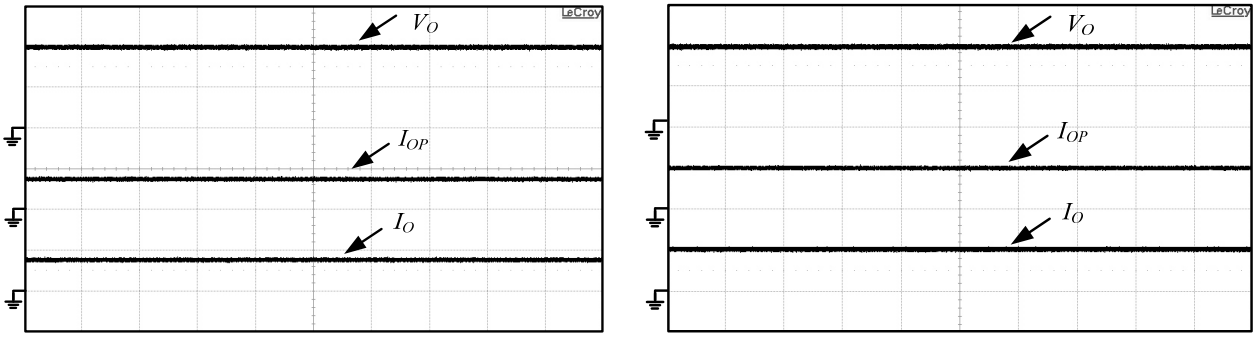
(**a**)

(V_O: 200 V/div, I_{OB}: 2 A/div, I_O: 2 A/div, time: 500 μs/div)

(**b**)

When the operational mode of the proposed PV power system is mode VI and $P_{PV(max)} \geq P_L$, its measured output voltage V_O and current I_{OP} and I_L waveforms under $P_{PV(max)} = 800$ W and $P_L = 320$ W are shown in Figure 33a, illustrating that output voltage V_O is clamped at 400 V, current I_{OP} is equal to I_L and $P_{PV} = 320$ W. Figure 33b shows those waveforms under $P_L = 800$ W. When $P_L = 800$ W, output power P_{PV} is also equal to 800 W and it is operated at its MPP. As mentioned above, operational modes of the proposed PV power system are respectively in the mode IV and VI states, the proposed one can regulate power between PV arrays, battery and load.

Figure 33. Measured voltage V_O, current I_{OP} and I_O waveforms of the proposed PV power system operated in mode VI (**a**) under $P_L = 320$ W; and (**b**) under $P_L = 800$ W.



(V_O: 200 V/div, I_{OP}: 1 A/div, I_O: 1 A/div, time: 200 μs/div)

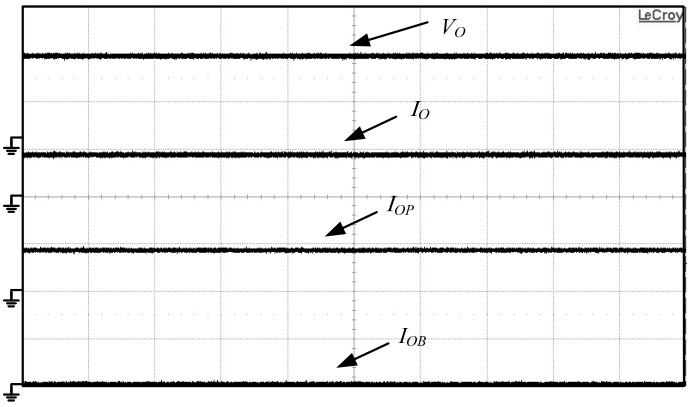
(**a**)

(V_O: 200 V/div, I_{OP}: 2 A/div, I_O: 2 A/div, time: 200 μs/div)

(**b**)

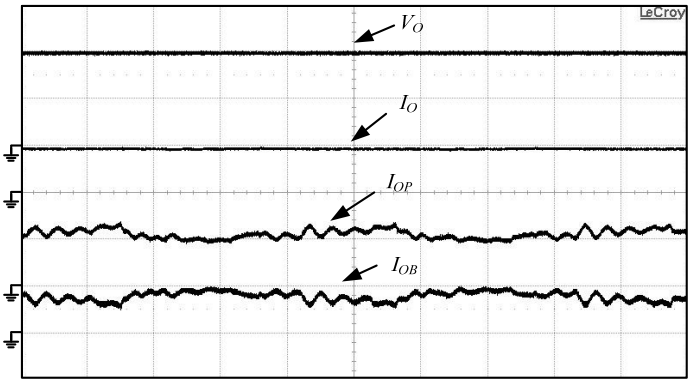
When the operational mode of the proposed one is mode VIII and $(P_{PV(max)} + P_{VB(max)}) \geq P_L$, its operational conditions are divided into two conditions. One is $P_{PV(max)} \geq P_L$ and the other is $P_{PV(max)} < P_L$. When $P_{PV(max)} \geq P_L$, its measured output voltage V_O, and currents I_{OP}, I_{OB} and I_L waveforms under $P_{PV(max)}$ = 750 W and P_L = 375 W are shown in Figure 34. Under this operational condition, current I_{OP} is equal to I_O and I_{OB} is equal to 0. That is, the proposed boost converter with MPPT is used to supply power to the load and the PV arrays are not operated at MPP, while the proposed boost one with voltage regulation is shut down. When $P_{PV(max)} < P_L$, its measured output voltage V_O, and currents I_{OP}, I_{OB} and I_O under $P_{PV(max)}$ = 375 W and P_L = 750 W is shown in Figure 35, illustrating that output voltage V_O is still lamped at 400 V and $I_O = I_{OP} + I_{OB}$. That is, the PV arrays can be operated at the maximum power point of 375 W and the battery can supply power to the load for balancing the power between the PV arrays and load. From experimental results, it can be seen that the proposed PV power system can use its power management circuit to achieve power balance between PV arrays, batteries and loads.

Figure 34. Measured voltage V_O, current I_{OB}, I_{OP} and I_O waveforms of the proposed PV power system operated in mode VIII under $(P_{P(max)} + P_{VB(max)}) \geq P_L$ and $P_{PV(max)} \geq P_L$.



(V_O: 200 V/div, I_O: 1 A/div, I_{OP}: 1 A/div, I_{OB}: 1 A/div, time: 200 μs/div)

Figure 35. Measured voltage V_O, current I_{OB}, I_{OP} and I_O waveforms of the proposed PV power system operated in mode VIII under $(P_{P(max)} + P_{VB(max)}) \geq P_L$ and $P_{PV(max)} < P_L$.



(V_O: 200 V/div, I_O: 1 A/div, I_{OP}: 1 A/div, I_{OB}: 2 A/div, time: 200 μs/div)

6. Conclusions

In this paper, two interleaved active clamp boost converters with coupled inductor are adopted to form a PV power system for dc load applications. The two proposed interleaved active boost converters using PV arrays and batteries as their power source, respectively, have been proposed to implement MPPT and power management. Moreover, their operational principle, derivation and design have been also described in detail. From experimental results, it can be seen that the proposed converter can yield higher efficiency than the one equipped with a hard-switching circuit. An experimental prototype for dc load applications [$P_{PV(max)}$ = 1.2 kW, $P_{VB(max)}$ = 1.2 kW] has been built and evaluated, achieving the efficiency of 91% under full load conditions and verifying the feasibility of the proposed active clamp circuit. Moreover, power management and MPPT with the perturb and observe method have also been implemented.

References

1. Yu, Y.; Zhang, Q.; Liang, B.; Liu, X.; Cui, S. Analysis of a single-phase Z-Source inverter for battery discharging in vehicle to grid applications. *Energies* **2011**, *4*, 2224–2235.
2. Pérez, P.J.; Almonacid, G.; Aguilera, J.; de la Casa, J. RMS Current of a photovoltaic generator in grid-connected PV systems: definition and application. *Int. J. Photoenergy* **2008**, *2008*, 356261:1–356261:7.
3. Yoo, J.; Park, B.; An, K.; Al-Ammar, A.E.; Khan, Y.; Hur, K.; Kim, J.H. Look-Ahead Energy Management of a Grid-Connected residential PV system with energy storage under time-based rate programs. *Energies* **2012**, *5*, 1116–1134.
4. Gerlando, A.D.; Foglia, G.; Iacchetti, M.F.; Perini, R. Analysis and test of diode rectifier solutions in grid-connected wind energy conversion systems employing modular permanent-magnet synchronous generators. *IEEE Trans. Ind. Electron.* **2012**, *59*, 2135–2146.
5. Ramirez, F.A.; Arjona, M.A. Development of a grid-connected wind generation system with a modified PLL structure. *IEEE Trans. Sust. Energy* **2012**, *3*, 474–481.
6. Van Breussegem, T.M.; Steyaert, M.S.J. Monolithic capacitive DC-DC converter with single boundary—Multiphase control and voltage domain stacking in 90 nm CMOS. *IEEE J. Solid State Circuit.* **2009**, *46*, 1715–1727.
7. Galigekere, V.P.; Kazimierczuk, M.K. Analysis of PWM Z-Source DC-DC converter in CCM for steady state. *IEEE Trans. Circuit Syst.* **2012**, *59*, 854–863.
8. Wang, Z.; Li, H. A Soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wide input voltage range. *IEEE Trans. Power Electron.* **2012**, *27*, 669–684.
9. Do, H.-L. Improved ZVS DC-DC converter with a high voltage gain and a ripple-free input current. *IEEE Trans. Circuit Syst.* **2012**, *59*, 846–853.
10. Qian, W.; Cha, H.; Peng, F.Z.; Tolbert, L.M. 55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles. *IEEE Trans. Power Electron.* **2012**, *27*, 1668–1678.
11. Brunton, S.L.; Rowley, C.W.; Kulkarni, S.R.; Clarkson, C. Maximum power point tracking for photovoltaic optimization using ripple-based extremum seeking control. *IEEE Trans. Power Electron.* **2010**, *25*, 2531–2540.

12. Agarwal, V.; Aggarl, R.K.; Patidar, P.; Patki, C. A novel scheme for rapid tracking of maximum power point in wind energy generation systems. *IEEE Trans. Power Electron.* **2010**, *25*, 228–236.
13. Subiyanto; Mohamed, A.; Shareef, H. Hopfield neural network optimized fuzzy logic controller for maximumpower point tracking in a photovoltaic system. *Int. J. Photoenergy* **2012**, *2012*, 798361:1–798361:13.
14. Taherbaneh, M.; Rezaie, A.; Ghafoorifard, H. H.; Rahimi, K.; Menhaj, M. B. Maximizing output power of a solar panel via combination of sun tracking and maximum power point tracking by fuzzy controllers. *Int. J. Photoenergy* **2010**, *2010*, 312580:1–312580:13.
15. Weidong, X.; Dunford, W.G. A Modified Adaptive Hill Climbing MPPT Method for Photovoltaic Power Systems. In *Proceedings of 35th Annual IEEE Power Electrons Specialists Conference* (*PESC*), Aachen, Germany, 20–25 June 2004; pp. 1957–1963.
16. Kobayashi, K.; Matsu, H.; Sekine, Y. An excellent operating point tracker of the solar-cell power supply system. *IEEE Trans. Ind. Electron.* **2006**, *53*, 495–499.
17. Jain, S.; Agarwa, V. A new algorithm for rapid tracking of approximate maximum power point in photovoltaic systems. *IEEE Power Electron. Lett.* **2004**, *2*, 16–19.
18. Chung, H.S.-H.; Tse, K.K.; Ron Hui, S.Y.; Mok, C.M.; Ho, M.T. A novel maximum power point tracking technique for solar panels using a sepic or cuk converter. *IEEE Trans. Power Electron.* **2003**, *18*, 717–724.
19. Billy, M.T.H.; Henry, S.H.C.; Hui, S.Y.R. An integrated inverter with maximum power tracking for grid-connected PV systems. *IEEE Trans. Power Electron.* **2004**, *20*, 953–962.
20. Casadei, D.; Grandi, G.; Rossi, C. Single-phase single-stage photovoltaic generation system based on a ripple correlation control maximum power point tracking. *IEEE Trans. Energy Convers.* **2006**, *21*, 562–568.
21. Mousavi, A.; Das, P.; Moschopoulos, G. A comparative study of a new ZCS DC–DC full-bridge boost converter with a ZVS active-clamp converter. *IEEE Trans. Power Electron.* **2012**, *27*, 1347–1358.
22. Yang, F.; Ruan, X.; Yang, Y.; Ye, Z. Interleaved critical current mode boost pfc converter with coupled inductor. *IEEE Trans. Power Electron.* **2011**, *26*, 2404–2413.
23. Meng, P.; Chen, H.; Zheng, S.; Wu, X.; Qian, Z. Optimal design for the damping resistor in RCD-R snubber to suppress common-mode noise. In *Proceedings of Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, USA, 21–25 February 2010; pp. 691–695.
24. River, T.H.L.; Henry, S-H.C.; Anson, K.T.S. Passive lossless snubber for boost PFC with minimum voltage and current stress. *IEEE Trans. Power Electron.* **2010**, *25*, 602–613.
25. Bongseong, K.; Ju, H.-J.; Ko, K.-C.; Hotta, E. Active clamping circuit to suppress switching stress on a MOS-gate-structure-based power semiconductor for pulsed-power applications. *IEEE Trans. Plasma Sci.* **2011**, *39*, 1295–1304.
26. Ku, C-P.; Chen, D.; Huang, C-S.; Liu, C-Y. A novel SFVM-M3 control scheme for interleaved CCM/DCM boundary-mode boost converter in PFC applications. *IEEE Trans. Power Electron.* **2011**, *26*, 2295–2303.
27. Genc, N.; Iskender, I. DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter. *IET Power Electron.* **2011**, *4*, 1016–1022.

28. Bin, G.; Jason, D.; Lai, J.-S.; Zheng, Z.; Chung, L. High boost ratio hybrid transformer DC-DC converter for photovoltaic module applications. *IEEE Trans. Power Electron.* **2013**, *28*, 2048–2058.
29. Tseng, K.-C.; Huang, C.-C.; Shih, W.-Y. A high step-up converter with a voltage multiplier module for a photovoltaic system. *IEEE Trans. Power Electron.* **2013**, *28*, 3047–3057.
30. Fang, Y.; Ma, X. A novel PV microinverter with coupled inductors and double-boost topology. *IEEE Trans. Power Electron*. **2010**, *25*, 3139–3147.