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Optimal Switching Table-Based Sliding Mode Control of an Energy Recovery Li-Ion Power Accumulator Battery Pack Testing System

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Abstract: The main objective of the present work is to apply a sliding mode controller (SMC) to medium voltage and high power output energy recovery Li-ion power accumulator battery pack testing systems (ERLPABTSs), which are composed of a three-level neutral-point-clamped (NPC) three-phase voltage source inverter (VSI) and a two-level buck-boost converter without an isolating transformer. An inner current decoupled control scheme for the aforementioned system is proposed and two sliding mode planes for active and reactive current control are designed based on the control scheme. An optimized switching table for current convergence is used according to the error sign of the equivalent input voltage and feedback voltage. The proposed ERLPABTS could be used to integrate discharging energy into the power grid when performing high accuracy current testing. The active and reactive power references for the grid-connected inverter are determined based on the discharging energy from the DC-DC converter. Simulations and experiments on a laboratory hardware platform using a 175 kW insulated gate bipolar transistor (IGBT)-based ERLPABTS have been implemented and verified, and the performance is found satisfactory and superior to conventional ERLPABPTS.

1. Introduction

Energy has become one of the most important parts of our lives and, due to its widespread use and effects, there is a need to create methods of conserving it, particularly to prevent further air pollution. Many countries have invested heavily in developing electric vehicles (EVs), which usually contain three parts: a driving motor, a power transmission system, and a power supply system. The first two technologies have been heavily investigated and are becoming increasingly reliable. However, the power battery pack, which influences the driving mileage, requires further optimization before electric vehicles can be commercialized successfully. The power battery pack testing system is used to evaluate the performance of power accumulator batteries, and it plays an important role in choosing and comparing batteries for EVs. There has been considerable research on battery pack testing systems [1–10]. A bi-directional energy flow power circuit topology combined with the control scheme used for power accumulator battery pack testing system (PABPTS) was designed to reduce the energy required for discharge test experiments and was described in [11]. This technology can integrate discharging energy of Li-ion battery with the power grid, and is called an energy recovery power accumulator battery pack testing system (ERPABPTS).

Most conventional ERLPABTSs featuring bi-directional two-level voltage source converters for DC-AC transformation have suffered from large switching stress and wastage. This is because conventional ERLPABTSs have the drawbacks of high total harmonic distortion, power transistors in the two-level converter when used for medium voltage (e.g., 900–1000 V), and high power output (e.g., 250 kW). Voltage rating requirements are much higher for two-level voltage source converters. The neutral-point-clamped (NPC) PWM inverter, which was first described by Nabae and Akira [12] in 1981, has emerged as a solution for working with higher voltage levels. The commutation of the switches permits the addition of capacitor voltages, which can reach high voltages at the output, while the power semiconductors only need to withstand reduced voltages [13]. The following attractive features could be achieved if NPC-based three-level converters could be integrated into the power circuit topology of ERPBTSs: (1) extremely low distortion and low dv/dt of the output voltage; (2) low distortion input current draw with structure-type filters (such as LCL filters) simplified to L filters; (3) low switching frequencies that would significantly reduce switching loss; (4) smaller common-mode (CM) voltage to reduce the stress in motor bearings. In addition, the CM voltage could be eliminated by using proper methods [14].

A great deal of work related to the multi-level converter topology, control schemes, and their applications has been done in the last ten years [15–17]. Mondal *et al*. [18] extended the space voltage pulse width modulation (SVPWM) of the three-level inverter into the over-modulation region. Busquets-Monge *et al*. [19] presented a new modulation approach for the complete control of the neutral-point voltage in a three-level three-phase NPC voltage source inverter. The modulation approach

was based on the virtual space vector concept, which guarantees the balancing of the neutral-point voltages for any load (whether linear or nonlinear) over the full range of converter output voltage and for all load power factors, with the only requirement being that the sum of the three-phase output currents is zero. Implementing the modulation was simple based on the phase duty-ratio expressions. A hybrid PWM modulation scheme [20] that uses both SVPWM and virtual SVPWM (VSVPWM) was presented, and allowed for complete control of the neutral point voltage in NPC three-level inverters, the performance of which was verified through simulation and experiment. In addition to the advanced modulation scheme, Verveckken *et al*. [21] developed a direct power control (DPC) method based on instantaneous power theory to apply the full potential of a power converter to a grid-connected system. Another typical application of multi-level converters is in AC motor driving systems where direct torque control (DTC) of induction motors using NPC three-level converters was described in [22–24].

The aim of this paper is to further extend sliding mode control to ERLPBTS using a three-level NPC converter. This is based on the work done in [25,26], but differs from previous research in that, for the first time, the inner current decoupling control method combined with sliding mode control is illustrated, along with an optimal switching table for the convergence of an equivalent input voltage for an NPC-based voltage source converter. The surface derivation and the principle of decoupling between phases are presented. Specifically, comparisons between the proposed scheme (sliding mode control) and the conventional proportional integral (PI) control scheme in the discharging current test of the PBPTS are presented. Another contribution of this paper is the elimination of the need for an isolation transformer, which makes the system more efficient as well as being lighter and smaller in volume.

This paper is arranged as follows: in Section 2, we explain the configuration and operation principles of the ERLPBPTS when it works in discharging mode. In Section 3, the saturation-restrained inner sliding model controlled current decoupling control scheme which is combined with an optimal switching table, are designed to integrate the three-level inverter to an AC-grid. We also design a fast dynamic time response current controller for discharging tests with minimum overshoot by establishing the dynamic equation of the small signal average model. In Section 4, simulations are performed to demonstrate the feasibility and correctness of the recommended scheme. The hardware setup and experimental results to verify the proposed scheme are given in Section 5. Finally, conclusions and suggested future works are presented in Section 6.

2. Configuration, Operation Principle, and Mathematical Model of NPC-Based Transformerless Three-Level ERPBPTS

2.1. Composite Power Circuit Description

The diagram of the improved ERLPABTS is shown in Figure 1. It is used for the two-channel ERPBPTS. Compared with conventional two-level ERLPABTS system in [11], it is easily seen that there is no isolation transformer in the power circuit. The three-phase AC-DC rectifier/inverter and the DC-DC buck-boost chopper are composed of a three-level diode-clamped NPC-VSC converter. Hence, the configuration of the whole system contains the following parts:

(a) A three-phase breaker on grid-side for short circuit protection;
(b) Three *L*-type filters for higher-order current harmonic elimination;

(c) A three-phase, three-line, three-level NPC-VSC inverter/rectifier on the inverter side;

(d) A dual-channel DC-DC buck-boost chopper for charging and discharging control of the power accumulator battery pack;

(e) Two large value DC current filter inductors in channels A and B are used to minimize the current ripple while performing current test experiments;

(f) The DC-DC buck and boost chopper shares the same dc-link voltage. Large value and volume DC-bus capacitors are needed to keep the dc-link voltage constant;

(g) Dual channel power battery packs for load testing, which can be a lead-acid battery, lithium-ion battery, or super-capacity battery.

Figure 1. Block diagram of the ERLPABTS using an improved NPC-VSC converter.
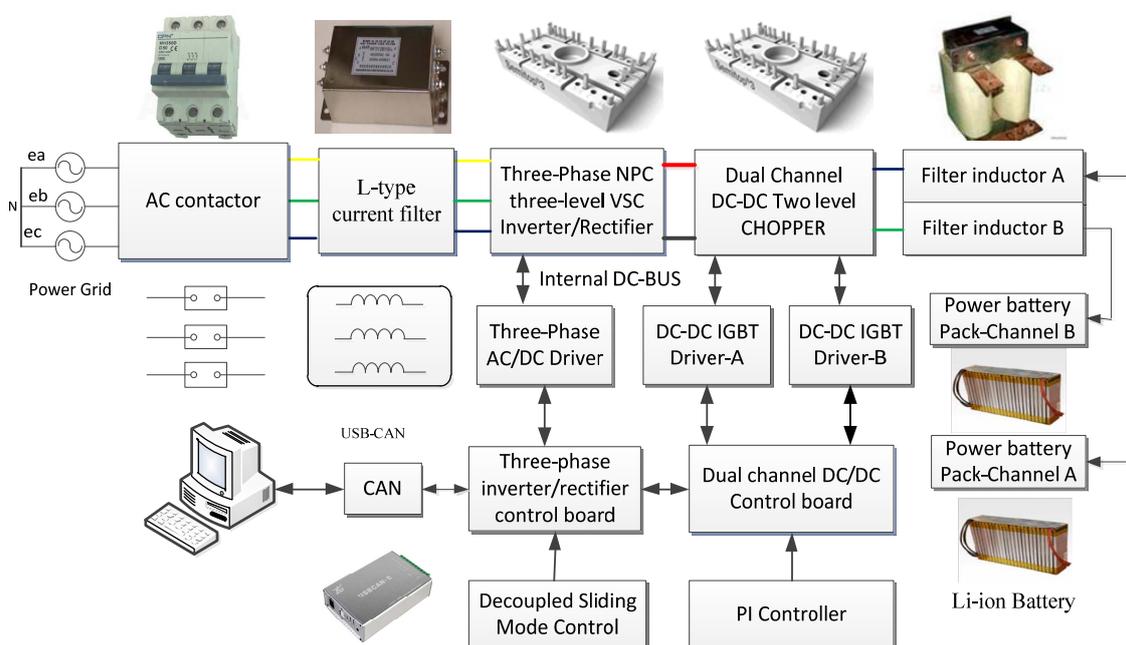
The detailed parameters of the above components for the simulation and experiments are provided in Tables A1 and A2. In our previous work [11], a fundamental frequency transformer has to be used to match the voltage between the grid-side and the converter side. In order to reduce the total output current harmonic, an LCL type filter is usually used to reduce the current harmonic distortion, but, this creates the problems because of the complicated control algorithm and the resonance, which is usually addressed through active damping control [27]. However, the present system does not have these drawbacks since the output voltage of the NPC-VSC converter is closer to sinusoidal. Furthermore, an *L* filter might be used for a simplified implementation of a three-level converter.

Besides the current filter, in the proposed scheme, two digital signal processing (DSP) control boards are needed to control the AC-DC converter and the DC-DC converter, respectively. The controller for the AC-DC converter is responsible for the unity power factor grid-connected control, while, in Figure 2, the DC-DC converter utilizes T5 in the buck chopper for charging control and T6 in the boost chopper for discharging control.

Figure 2. Power circuit topology of the ERLPABTS using the NPC-VSC converter.
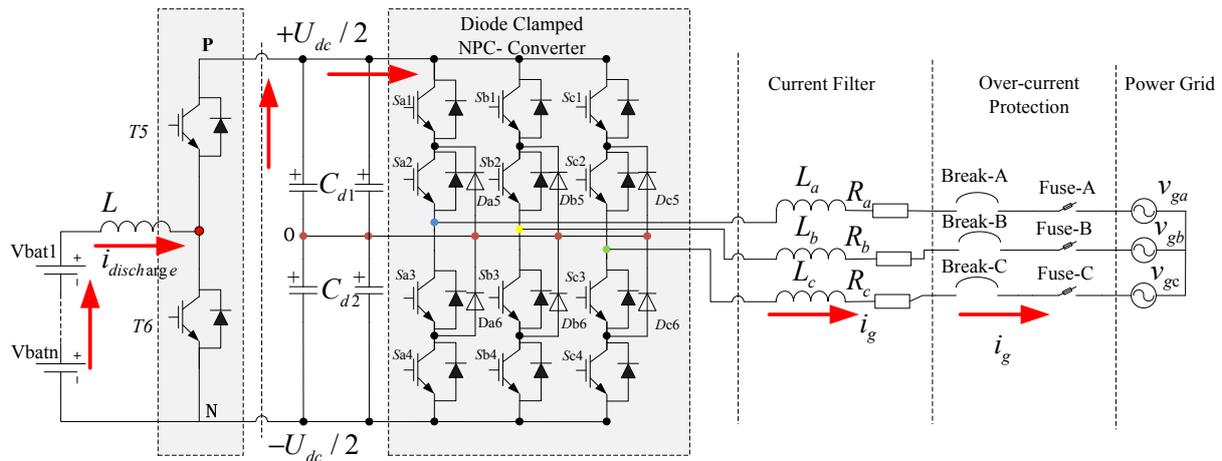
In summary, the key advantages of the proposed three-level converter in ERLPABTS are: it can handle higher and multi-level voltages with low total harmonic distortion (THD), it has a, low power transistor voltage rating requirement, and it eliminates the need for complicated filters or bulky and low efficiency isolation transformers. All of these features make the improved power circuit topology superior to that of the conventional system.

2.2. Operation Principle

The detailed schematic power circuit topology of the improved NPC-based three-level grid-connected system for ERPBPTS is shown in Figure 2, It is different from the conventional two-level converter in [11], because there are a total of twelve additional power transistors, and six additional voltage clamped power diodes. The ERLPABTS, therefore, has three output voltage levels: $+U_{DC}/2$, 0, and $-U_{DC}/2$. Due to the merits of a three-level converter, a simplified L type interface filter might be adopted for current filtering. A bi-directional buck and boost chopper is used for the charging and discharging current control of the power battery pack.

The operating principle of the proposed power circuit is described as follows: when the discharging current test experiment is performed, the DC-DC converter functions as a boost chopper and $T6$ is switched ON and OFF with the PWM. A constant charging current is obtained via the bypass diode of $T5$, which causes an increase in the DC-link voltage. The power transistor would be damaged through the high-voltage break down if it were not properly controlled. This energy is released to the power grid through a three-level NPC converter system. An energy balanced control strategy between the DC-DC converter and the DC-AC converter would be the most important consideration. In this way, the discharging energy could be recovered effectively, which could realize a high resolution discharging current test at the same time. A current filter, over-current protection devices, and fast-acting fuses are also used for protection. In summary, the control part of the system includes two branches: the first is the controller design for the non-isolating DC-DC boost chopper, and the second is the controller design for the energy recovery control of the ERLPABTS.

Considering the time response requirement of ERLPABTS, the instantaneous charging and discharging current control capability of the power battery pack must be evaluated. The traditional

proportional and integral (PI) controller in PABPTS cannot satisfy the dynamic parameter requirements of the battery testing system. Sliding mode control (SMC) has the advantages due to its insensitivity to modeling error, variation on the parameters, and external disturbance. Moreover, sliding mode control can provide much faster dynamic response, especially in the unfixed structure and time-variant of a grid connected inverter. Therefore sliding mode control could obtain better performance than a conventional PI controller in this application.

3. Sliding Mode Controller Design for ERLPABTS under Discharge Mode

3.1. Decoupled Sliding Mode Controller Design for the NPC VSI Based Grid-Connected System

Since the mathematical mode of the three-phase NPC VSI converter for ERPABPTS has already been elaborated in our aforementioned word in [25,26], the decoupled sliding mode controller for the system would be discussed in detail in this paper. Sliding mode control is a variable structure control that selects the suitable switching configuration of the converter to drive the trajectory toward a predefined switching surface. When a system governed by sliding mode control reaches the control surface, it is forced to constrain its dynamic evolution on this surface for all subsequent time. The system dynamics restricted to this surface represent the controlled system behavior. The previous step for the controller design consists of choosing a suitable sliding surface. The controller will be designed in order to force the output function to track a reference signal. Assuming that the error between reference active and reactive current ($i_d{}^*$, $i_q{}^*$) and feedback current (i_d, i_q) could be expressed as: $s_d = i_d{}^* - i_d$, $s_q = i_q{}^* - i_q$. The sliding mode controller for the active and reactive current component could be represented as $G_d\ (s_d,\ ds_d/dt)$ and $G_d\ (s_q,\ ds_q/dt)$, respectively, and the duty cycle (D_d, D_q) under synchronous rotating reference frame can be revised as:

$$\begin{cases} D_d = 2 \cdot \left(G_d\left(s_d, \dot{s}_d\right) \cdot (s_d + \dfrac{ds_d}{dt}) - \omega L \cdot i_q + e_d \right) / v_{dc} \\ D_q = 2 \cdot \left(G_q\left(s_q, \dot{s}_q\right) \cdot \left(s_q + \dfrac{ds_q}{dt} \right) + \omega L \cdot i_d + e_q \right) / v_{dc} \end{cases} \tag{1}$$

According to the requirement of the sliding mode control method, the selection of the control input components u_{eqd} and u_{eqq} must satisfy the arriving condition which means:

$$s_d \cdot \dot{s}_d < 0 \quad s_q \cdot \dot{s}_q < 0 \tag{2}$$

When $s_d = s_q = 0$, the equivalent control input voltage components u_{eqd} and u_{eqq} can be shown as:

$$\begin{cases} \dfrac{di_d^*}{dt} = \dfrac{di_d}{dt} = -\dfrac{R}{L} \cdot i_d + \omega \cdot i_q + \dfrac{1}{L} \cdot v_{eqd} - \dfrac{1}{L} \cdot e_d \\ \dfrac{di_q^*}{dt} = \dfrac{di_q}{dt} = -\omega \cdot i_d - \dfrac{R}{L} \cdot i_q + \dfrac{1}{L} \cdot v_{eqq} - \dfrac{1}{L} \cdot e_q \end{cases} \tag{3}$$

In Equation (3), v_{eqd} and v_{eqq} represent the input equivalent voltage components. Combining Equation (3) with Equation (2), we can derive the differential equations of the components s_d and s_q as:

$$
\begin{cases}
\dfrac{di_d}{dt} - \dfrac{di_d^*}{dt} = \dfrac{v_{dc}}{L}\left(v_d - v_{eqd}\right) = \dfrac{ds_d}{dt} \\[3mm]
\dfrac{di_q}{dt} - \dfrac{di_q^*}{dt} = \dfrac{v_{dc}}{L}\left(v_q - v_{eqq}\right) = \dfrac{ds_q}{dt}
\end{cases}
\tag{4}
$$

Considering Equations (2) and (4) with respect to the arriving condition, then

$$
\begin{cases}
s_d \cdot \left(v_d - v_{eqd}\right) < 0 \\[2mm]
s_q \cdot \left(v_q - v_{eqq}\right) < 0
\end{cases}
\tag{5}
$$

Therefore, the equivalent control input must satisfy the following condition (6) to force the movement trajectory to be convergent to pre-defined sliding mode plane:

$$
\begin{cases}
\mathrm{sgn}\left(v_d - v_{eqd}\right) = \mathrm{sgn}(s_d) \\[2mm]
\mathrm{sgn}\left(v_q - v_{eqq}\right) = \mathrm{sgn}(s_q)
\end{cases}
\tag{6}
$$

The sliding mode current controller must be designed to satisfy Equation (6), where v_d and v_q are the voltage components needed to be composited. Space vector pulse width modulation could be used the composite the needed voltage, this has been illustrated in reference [16,28,29]. Yet, this need complicated mathematic computation for Clark and Park transformations, due to this, faster and higher micro-controller is needed. In this paper, to simply the control algorithm, an optimized switching table is put forward and used. It is shown in Table 1, the optimized switching table can avoid duplicate cross zone power transistor switching. From Equation (6), we may conclude that the error signal between input voltage v_d and equivalent input voltage v_{eqd} for active power component decides the output signal of switch S_p, and the error between input voltage v_q and equivalent input voltage v_{eqq} for reactive power control decides the output signal of switch S_q. In order to acquire the current location of which the grid voltage vector, the angle information of grid-connected voltage θ can be calculated by e_α and e_β which is shown as: $\theta = e_\beta / e_\alpha$, twelve sectors are divided in one cycle, θ is the current location of grid-side voltage vector and it can be calculated as:

$$
(n-2) \cdot \frac{\pi}{6} \leq \theta_n \leq (n-1) \cdot \frac{\pi}{6}
\tag{7}
$$

In Equation (7), the section number $n = (1, 2, \ldots, 12)$.

Table 1. Optimized switching table for the proposed scheme.

S_p	S_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	101	111	100	000	110	111	010	000	011	111	001	000
	1	111	111	000	000	111	111	000	000	111	111	000	000
0	0	101	100	100	110	110	010	010	011	011	001	001	101
	1	100	110	110	010	010	011	011	001	001	101	101	100

3.2. Active and Reactive Current Component Generation

It should be noted that unlike conventional VSI converters, there is no constant power source voltage in the DC-bus. The voltage is decided by the discharging current and the battery pack's terminal voltage on the boost converter side, which charges the electrolytic capacitors on the DC-bus and results in fast dc-link voltage climbing rates. Thus, a reference current for integrating the grid is used to maintain a constant DC-link voltage, and a switch is needed to control whether it is integrated to the power grid. As the discharging energy is temporarily stored in the dc-bus capacitors, the active power component that needs to be recovered could be determined by multiplying the DC-link voltage (v_{DC}) and the DC-link current (i_{DC}) as:

$$p_{ref} = v_{dc} \cdot i_{dc} \tag{8}$$

Based on the active and reactive current component references by [11], we may conclude that the active and reactive current component reference ($i_d{}^*$, $i_q{}^*$) can be represented as:

$$\begin{cases} i_d^* = \dfrac{2}{3} \cdot \dfrac{\left(v_{dc} \cdot i_{dc} \cdot v_d + q_{ref} \cdot v_q\right)}{v_d^2 + v_q^2} \\[4mm] i_q^* = \dfrac{2}{3} \cdot \dfrac{\left(v_{dc} \cdot i_{dc} \cdot v_q - q_{ref} \cdot v_d\right)}{v_d^2 + v_q^2} \end{cases} \tag{9}$$

When under a synchronous rotating frame and assuming that the reference reactive power component and voltage component are $q_{ref} = 0$ and $v_d = 0$, respectively, Equation (9) can be rewritten as:

$$i_d^* = 0 \quad i_q^* = \frac{2}{3} \cdot \frac{v_{dc} \cdot i_{dc}}{v_q} \tag{10}$$

Considering the decoupled control scheme proposed in [11] and the optimal switching table for output voltage vector, the control diagram of the whole system would be illustrated in Figure 3 as:

Figure 3. Control block diagram of the composite power converter system for ERLPABTS.
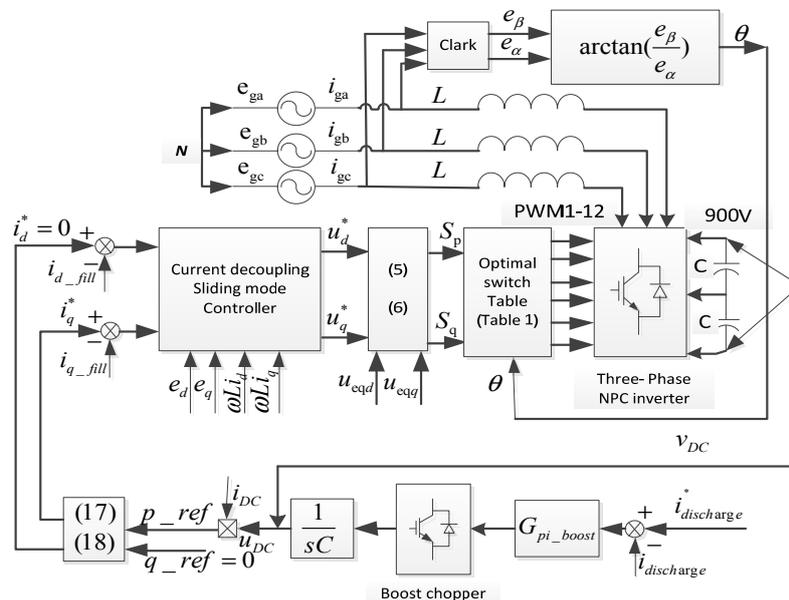
3.3. Dynamic Model of the DC-DC Boost Chopper for Discharging Current Control of ERPBTS

The boosting chopper is used for a constant current discharging test experiment of a power accumulator battery pack testing system. The reason that a switching mode DC-DC power converter is used instead of a linear mode controlled power transistor which works in a linear area is that it has the ability to process a large discharging testing current with much a higher DC-bus voltage and minimum switching loss. However, the switching mode DC-DC converter has a shortcoming because of the current ripple on each switching point and thus a large amount of electronic noise might occur in this case. A mathematical model and its related non-linear control of the boost chopper were given in [11], while an optimal minimum time response current control scheme under the maximum and minimum voltages and the current limitation for ERPBTS was previously proposed in [25]. Therefore this paper focuses on the combination of two power circuits, which include a DC-DC buck and boost chopper and an NPC three-level converter, the latter of which is used for integration into a power grid with high voltage and low total harmonic distortion.

4. Simulation Results and Discussion

Simulations for integrating the three-phase NPC inverter with the distribution grid using an *L* filter interface in a Powersim 9.0 environment are carried out in order to describe and validate the capability of the proposed control scheme. The improved composite power circuit for ERPBTSs is verified through these simulations. The model is co-simulated using Matlab/Simulink and PSIM9.0 via a simcoupler block. The power circuit is established in Psim 9.0 environment and the control algorithm is realized in Simulink. The configuration and control block diagram of the system are shown in Figure 3, and the electrical parameters used for the simulation can be found in Tables A1 and A2 in the Appendix. The simulation study is performed with three main objectives in mind:

(1) To demonstrate the feasibility of the proposed control scheme for the composite power circuit.
(2) To verify the merits of reduced total harmonic distortion of a grid-connected current by using the proposed scheme and an optimized switching table in a three-level VSC converter.
(3) To realize the performance of the current decoupling scheme and the proposed sliding mode controller provided in Equation (6).

Figure 4 shows a PI control diagram of the composite power circuit for ERPBTS. The gain (*k*) and time constant (*T* in seconds) of the PI controller in a discharging control test are set to ($k_p = 0.04$, $T = 0.012$). The transfer function of the PI controller used for i_d and i_q control is shown in Equation (11). The PWM duty cycle is calculated using Equation (9). Two signal generators are needed to obtain the positive and negative output sinusoidal waveform. The space vector voltage to be synthesized is realized by selecting a particular voltage vector depending on the composite voltage vector's present location:

$$G_{pi} = 0.04 \cdot \frac{(1+0.012 \cdot s)}{0.012 \cdot s} \tag{11}$$

In this section, in order to verify the performance of a different controller, we will show the simulation results for the improved composite power circuit for ERLPABTS using sliding mode control and the PI controller method, respectively.

Figure 4. Inner active and reactive current component control using PI method.
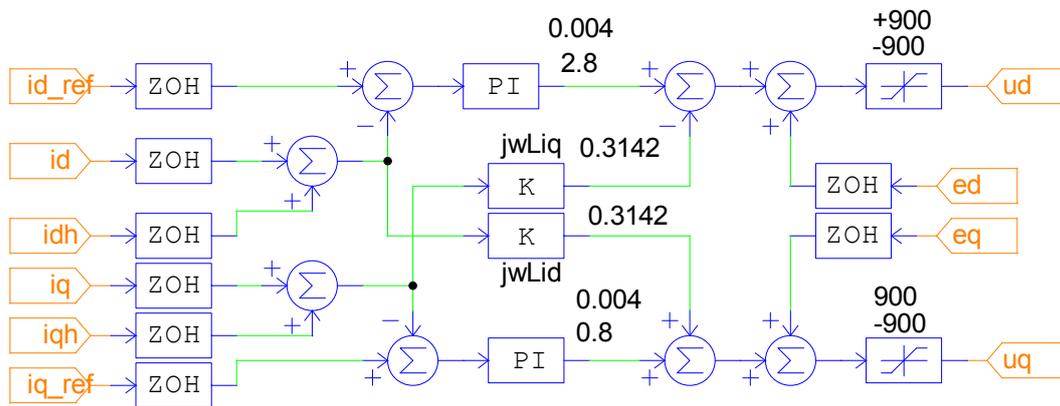
Figure 5a shows the waveform of the reference discharging current and feedback current. A step-forward reference current of 400 A is given at 0.03 s and the feedback current keeps track of its reference current with a peak value of 10 A overshot 20 ms later. This demonstrates the feasibility of the proposed scheme.

Figure 5b gives the waveform of a dc-link voltage v_{dc} that is set to 900 V using a switch that enables and disables PWM modulation to keep the dc-link voltage constant. The initial dc-link capacitor voltage is pre-charged to 800 V to prevent an instantaneous charging current when powered on. It can be clearly seen that the dc-link voltage remains steady and stable.

Figure 5c shows the waveform of the active and reactive powers (P_ref, Q_ref) reference where the active power (P_ref) is given by Equation (8) and the reference reactive power (Q_ref) is set to 0 to realize unity power factor control.

It can be seen that there is a time difference between the reference active power and the feedback active power which is due to the dc-link voltage. The simulation test showed that the grid-connected NPC-inverter starts to work only when the voltage reaches 900 V, and it takes 10 ms to charge from 800 V to 900 V. The reference active power is 96 kW, and the feedback active power can effectively keep track of its reference value.

Figure 5d provides the time response of the grid-connected phase current (i_{ga}) and the grid voltage (v_{ga}). It can be seen that the phase-current is almost in phase with the phase voltage, and that a unity power factor control is realized in the three-phase NPC inverter.

Figure 5e shows the time response of the active and reactive currents (i_d, i_q) when using a sliding mode controller and PI controller (Figure 5f). The active and reactive current references are given by Equation (9) and it is found that the feedback current could track the reference current very well. However, there is steady state error (~5 A) in this situation. The peak-to-peak active current value (i_{p-p}) is about 50 A. In order to compare the result when using different controllers, an extra inductor of 0.5 mH is added to the system at 80 ms, and is used to simulate the un-modeled parameter variations. It can be clearly seen that the active and reactive current components (i_d, i_q) are influenced from 0 A to 50 A. The active and reactive current components when using the sliding mode controller vary from 0 A to −25 A, which is half of the variation when using the PI controller. This demonstrates that the proposed controller is insensitive to parameter variations, and is superior to the conventional PI controller.

Figure 5. Simulation results of the proposed scheme. (**a**) Time response of reference discharging current and feedback current; (**b**) Time response of dc-link voltage; (**c**) Time response of reference active and reactive power; (**d**) Time response of the grid-connected phase current (i_{ga}) and grid voltage (v_{ga}); (**e**) Time response of the active and reactive currents (i_d, i_q) using a sliding mode controller; (**f**) Time response of the active and reactive currents (i_d, i_q) using PI controller.
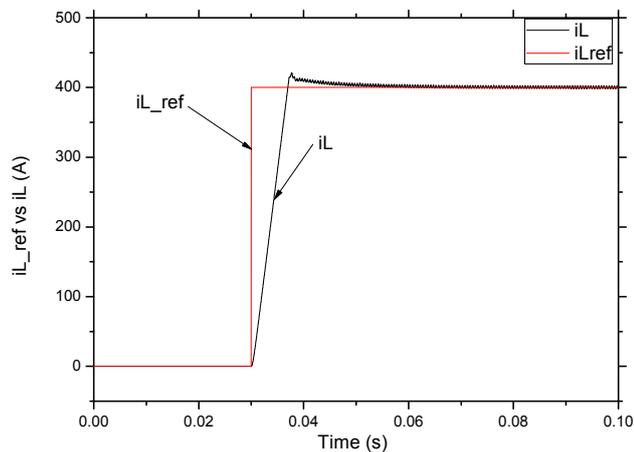
(**a**)
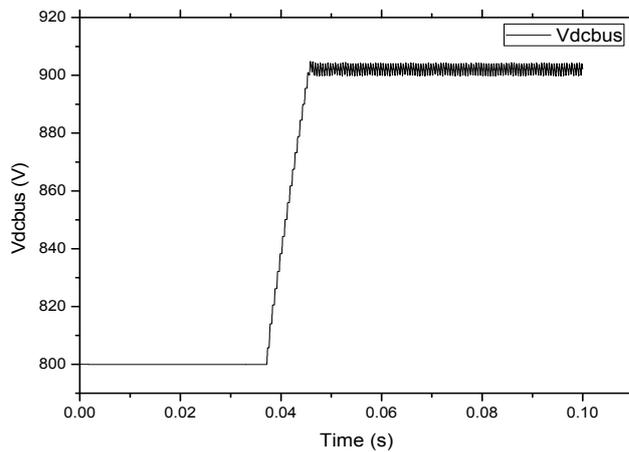
(**b**)
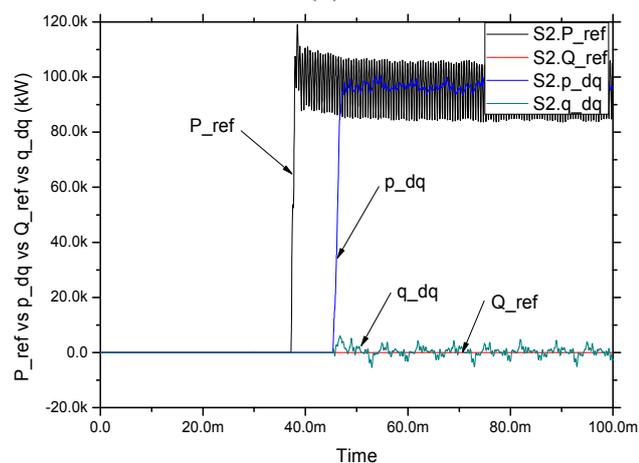
(**c**)
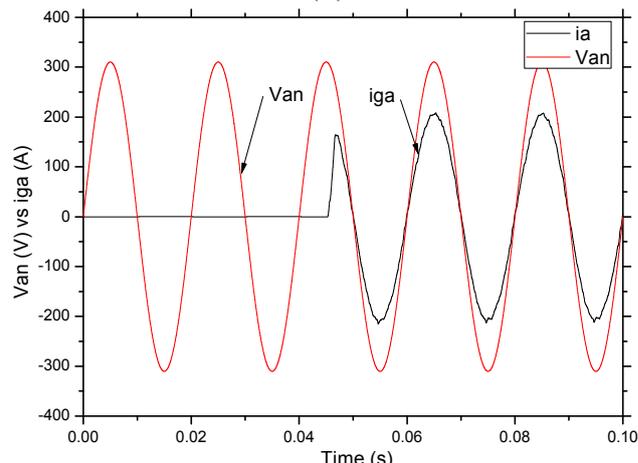
(**d**)
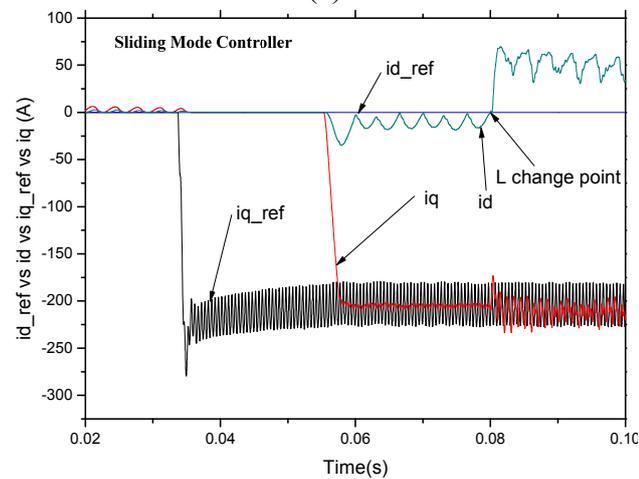
(**e**)
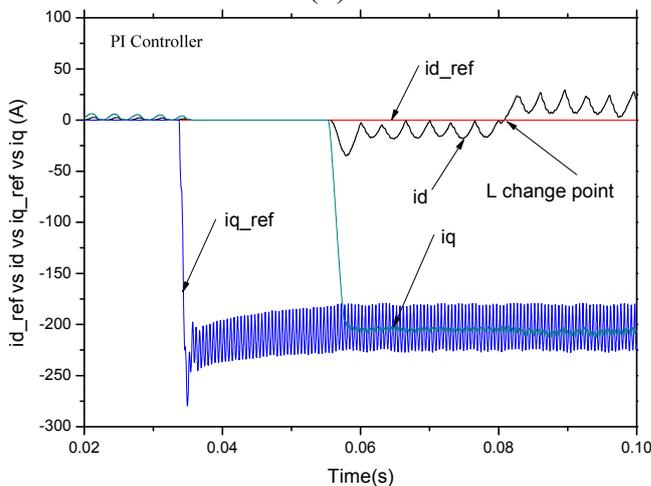
(**f**)

Figure 6a shows the time response of the line-to-line voltage using a three-level converter without a transformer, while Figure 6b gives the time response of the line-to-line voltage using a two-level converter. We can see that the voltage in Figure 6a is more sinusoidal due to its multiple output levels. Figure 7a illustrates the harmonic distribution of the phase current using a conventional two-level inverter, and Figure 7b shows the NPC based three-level power converter. The conventional two-level converter has more harmonics since its total harmonic distortion is 16% while that of an NPC-based three-level VSC converter is only 2.11%.

Figure 6. Line-to-line output voltage of the (**a**) three-level NPC-VSC converter and (**b**) two-level converter.


(**a**)

(**b**)
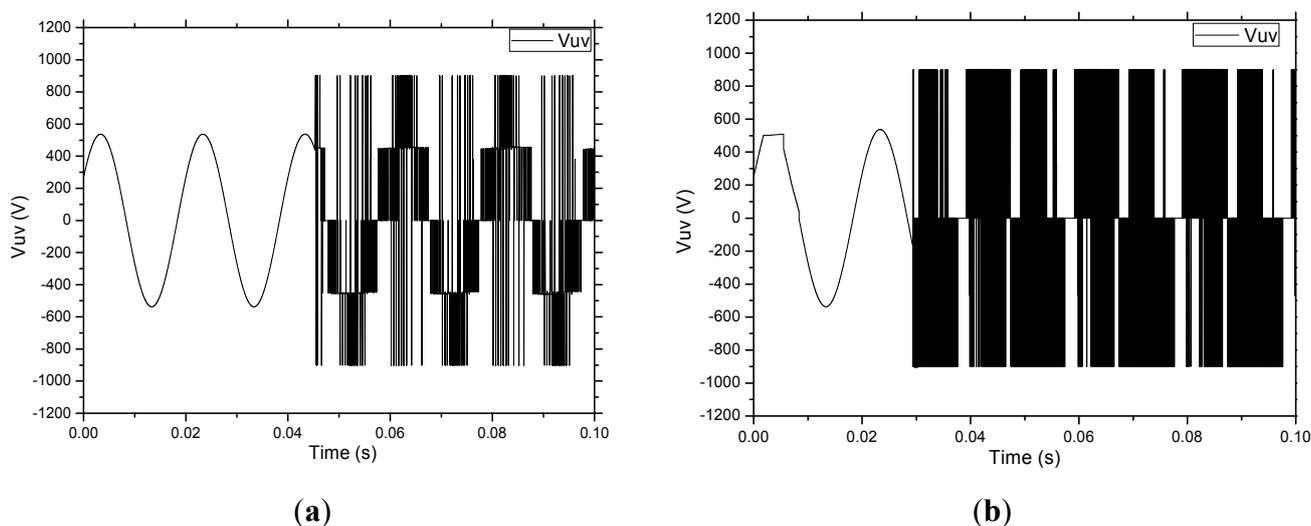
Figure 7. Harmonic distribution of the (**a**) three-level NPC-VSC converter and (**b**) two-level converter.


(**a**)

(**b**)
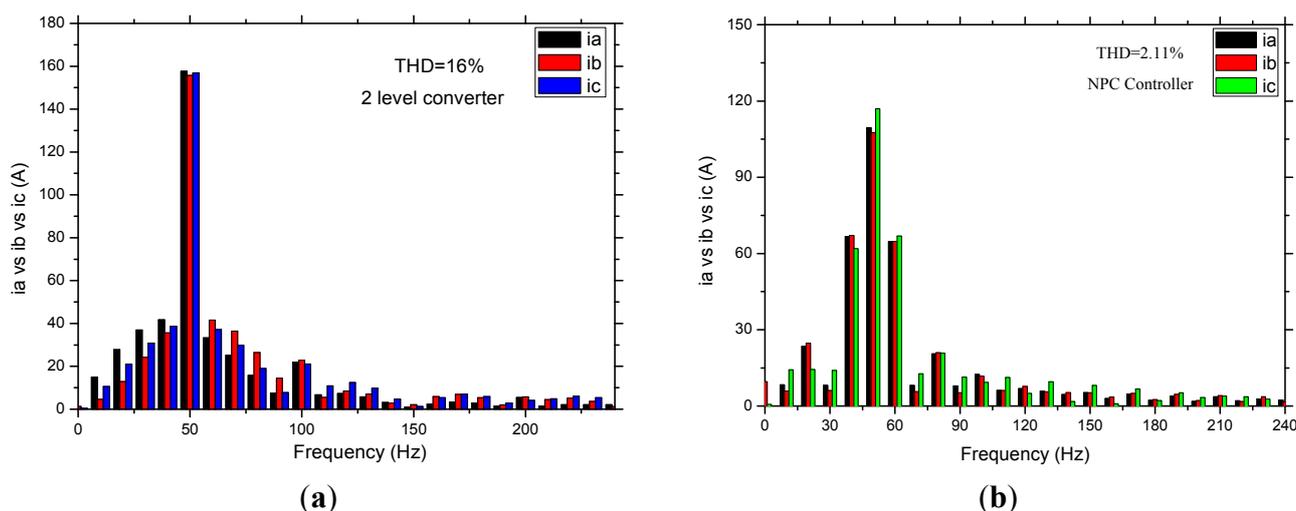
5. Experimental Section

A three-level NPC-VSC inverter, which is used for a grid-connected energy recovery Li-ion type power battery testing system experimental platform based on the DSP-TMS320LF2808, is setup to verify the proposed design. The hardware setup of the power circuit configuration of the system is shown in Figure 8a, while the IGBT driving, protection and core control board is shown in Figure 8b.

The power input part of the two-channel ERLPABTS is presented in Figure 8c. The Li-ion battery used for experiment is presented in Figure 8d. System configuration of the experimental setup was illustrated in earlier sections via a block diagram, and the power transistor parameters are listed in Table A1 and Table A2 in the Appendix. The control scheme can be referenced in the simulation section.

Figure 8. The three-phase NPC inverter based ERLPABTS for the experiment. (**a**) Power circuit of the system; (**b**) IGBT driving, protection and core control board; (**c**) Power input of the two-channel ERLPABTS; (**d**) Li-ion battery used for experiment.

(**a**)

(**b**)

(**c**)

(**d**)
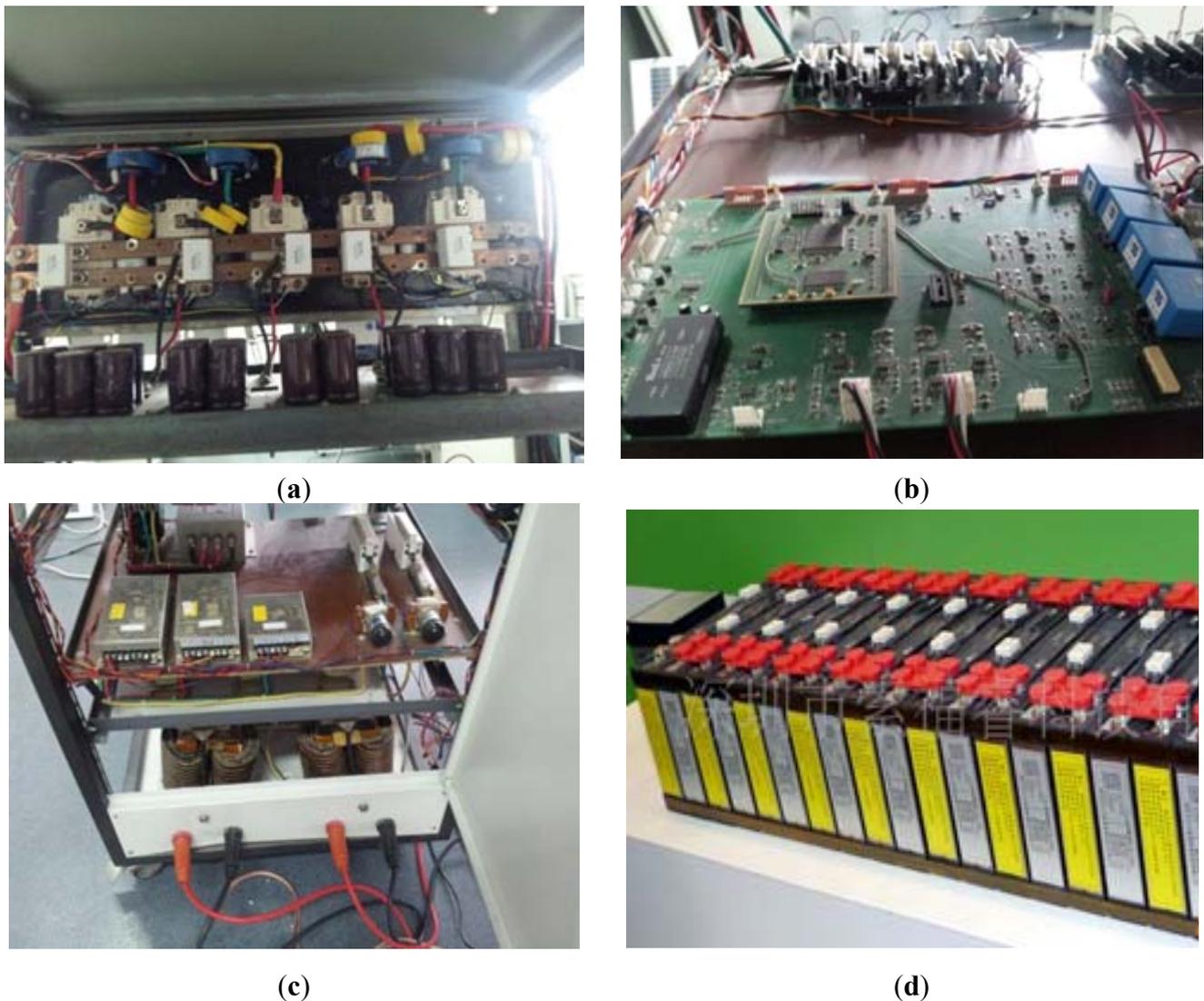
The power circuit of the PWM converter consists of six IGBT where each of the IGBT modules has two integrated IGBT blocks inside. This forms a three-phase NPC full-bridge inverter circuit and a half-bridge circuit, the electrical parameters of which are shown in Table 1 of the Appendix. Two Hall-effect LEM sensors (LT108-S7) and four isolation voltage sensors are used for the line currents and the DC-bus voltage detection. One high-resolution LEM sensor is employed to detect the charging and discharging currents in the DC-DC power circuit. A total of fourteen PWM output signals are required in the proposed scheme of which twelve are used for the three-phase NPC converter, while the others are used for the buck-boost chopping DC-DC converter. An optimized switch table for

PWM generation is used for the attenuation of the active and reactive current components on the grid side, while the phase lock loop (PLL) control algorithm is used to obtain the precise angular information of the synthesized voltage vectors.

The experiments are implemented by changing the reference discharging current of the power battery pack. A step forward discharging current of 200 A is supplied at 20 ms, which is then increased to 100 A at 60 ms. The DC-bus voltage (V_{dc}) is set to 900 V, and the DC-bus capacities are charged by the energy released from the boosting chopper control component which gives rise to its terminal voltage. The three-phase NPC converter stops working when the DC-link voltage falls below 900 V and it restarts when the DC-link voltage is higher than 900 V. A small band could be used to keep the DC-bus voltage stable without using a high switching frequency. The reference of the active and reactive power varies according to the discharging current and the DC-bus voltage which keeps the energy balanced both in the boost chopper and inverter sides. The discharge energy of the battery power testing is therefore restored to the power grid with high efficiency.

The discharging current response of the power battery pack is shown in Figure 9a. The feedback current initially peaks at 225 A and then keeps track of the reference current after 10 ms when given a reference current of 200 A at $t = 20$ ms. The feedback current initially drops to less than 100 A and then converges back to the command value 10 ms later when a step-down discharge current of 100 A is given at $t = 60$ ms. An instantaneous inrush current is caused by the pure inductor load on the boost chopper side. A smaller filter inductance has drawbacks due to the large current ripples, but a large filter inductance results in a short time response and a large volume. An inductance of 4 mH is adopted for this experiment.

The time response of the DC-bus voltage is shown in Figure 9b. The initial DC-bus voltage is set to 500 V which starts to increase at $t = 20$ ms and reaches 900 V about 2.5 ms later. The DC-bus voltage starts to increase again at $t = 60$ ms when a step-down current reference is given which is due to the reduced load on the DC-bus.

Figures 9c and 9d illustrates the experimental results of the active and reactive current components (i_d and i_q) when the grid-connected interface inductor changes under the PI and SMC control methods, respectively. Compared with Figure 9c, the active and reactive current components in Figure 9d are influenced less by the grid-connected inductance variations (± 10 A in PI and ± 6 A) when the inverter side inductor (i_g) changes from 1 mH to 0.67 mH at 120 ms and from 0.67 mH to 1 mH at 250 ms, This demonstrates that by using the sliding mode controller, the system is insensitive to the parameter variations in the system. The improved control method could offer better robustness than the conventional method.

Figure 9e illustrates the time response of the active and reactive current components in the three-phase NPC converter. It shows that the reactive current component (i_d) converges to zero, and that the active current feedback (i_q) follows its reference component (i_{qref}) very well when the DC-bus voltage increases to 900 V.

To summarize, the experimental results confirm that the proposed scheme is not only feasible, but also valid and applicable. The proposed scheme could greatly improve conventional composite power circuits since the proposed novel system is more compatible, lighter, and less total grid current harmonic distortion.

Figure 9. (**a**) Experimental results of time response *vs.* discharging current (i_L); (**b**) Experimental results of time response *vs.* dc-bus voltage (V_{dcbus}); (**c**) Experimental results of active and reactive current components (i_d and i_q) when the grid connected interface inductor changes by using the PI method; (**d**) Experimental results of active and reactive current components (i_d and i_q) when the grid-connected interface inductor changes from 0.67 mH to 1 mH by using SMC method; (**e**) Experimental results for grid-connected current (i_a) and grid voltage of the system (v_{an}).
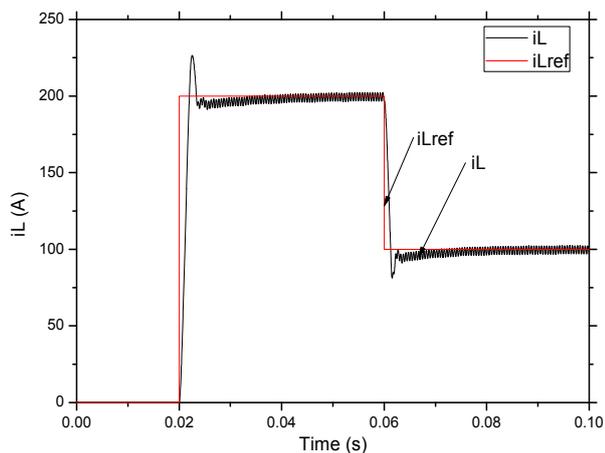
(**a**)
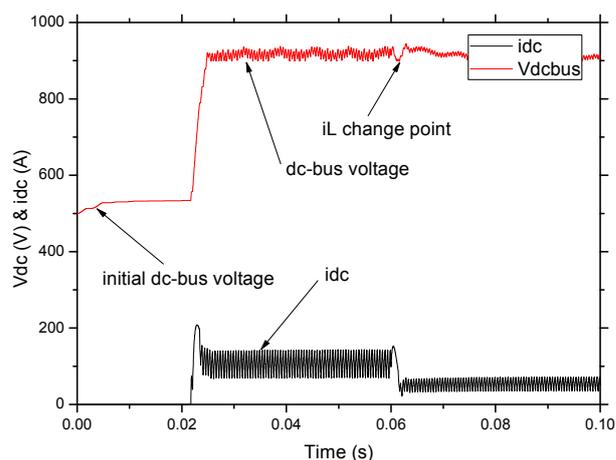
(**b**)
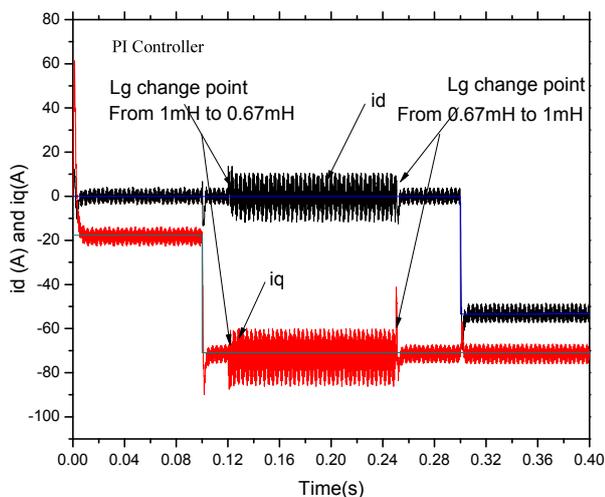
(**c**)
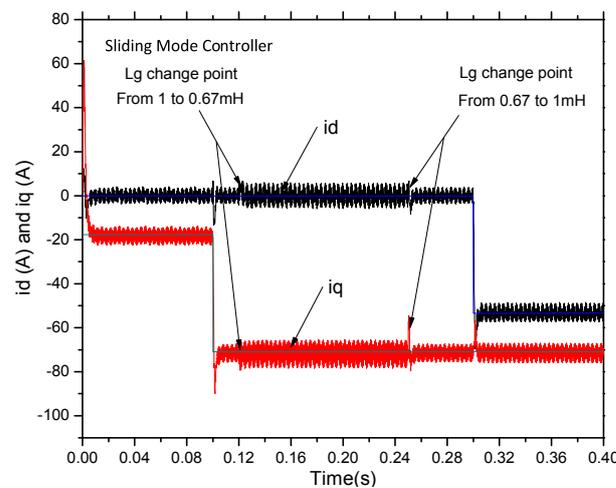
(**d**)
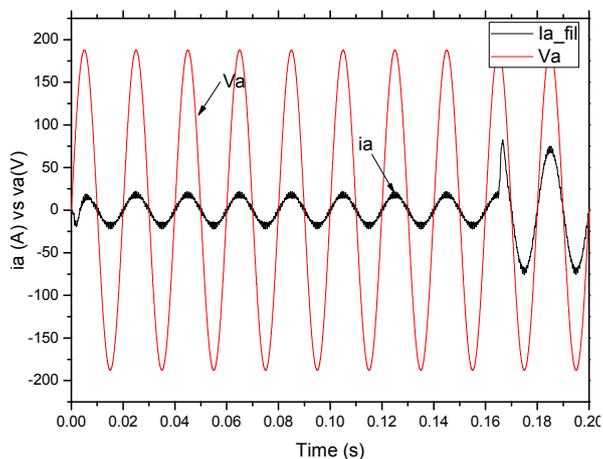
(**e**)

6. Conclusions

This paper applies a three-level NPC-VSC power inverter to grid-connected ERLPABTSs. A sliding mode based current decoupling controller under a synchronous rotating reference frame is designed, and s-functions for the active current component i_d and the reactive current component i_q are proposed. Moreover, the performance of the proposed inner current decoupling control scheme with sliding mode control is proven to be better than that of a conventional PI controller. The simulation and experimental results confirm the feasibility and validity of the proposed scheme. The simulation results also showed that the proposed decoupling scheme can successfully control the active and reactive parts independently with the given active and reactive current reference components.

The advantages of using a three-level NPC VSC inverter are: it offer lower total current harmonic distortion; lower switching frequency and the minimum power transistor rated voltage and current capability requirements; no need for an isolation transformer; and a simplified *L*-type interface filter. These advantages make the suggested composite power circuit topology and the control strategy more suitable for high voltage and large current applications , especially in ERPBTSs.It is suggested that future works might focus on anti-islanding and overload protection since a large number of ERLPABTS instruments shares the same power-bus in the factory.

Appendix

Table A1. Power transistor specifications adopted for the three-phase NPC-VSC inverter.

Components	Part name/Manufacturer	Rating values
IGBT	SKM400GB128D/ SEMIKRON	1200 V–400 A
Fast DIODE	SKKD75F12/SEMIKRON	1200 V–75 A
Capacitor	YDK	450 V–5000 μF

Table A2. Specifications adopted for the proposed ERLPABTS under discharging mode.

Elements	Parameters	Values
Power Battery Pack	Battery terminal voltage V_{bat}	240 V
	Battery type	Li-ion
AC Power grid	Grid voltage (line to line rms) V_g	380 V
	Line frequency f_n	50 Hz
	Grid impedance L_g	1 mH
L filter	Converter side inductor L	1 mH
DC-DC Converter	Nominal power	175 kW
	Inductor for boost chopping L	4 mH
	Switching frequency f_s	5000 Hz
	Dead time t_d	2 us
DC-AC Converter	Nominal power P_e	175 kW
	Two series DC-link capacitor C_{dc}	16,000 uF
	Initial dc-link capacitor voltage V_{c0}	500 V
	DC-link voltage reference V_{dc_ref}	900 V
	IGBT switching frequency f_{inv}	2000 Hz
	Dead time t_d	2 us

Conflicts of Interest

The authors declare no conflict of interest.

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