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Article

Asymmetrical Interleaved DC/DC Switching Converters for Photovoltaic and Fuel Cell Applications—Part 1: Circuit Generation, Analysis and Design

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Abstract: A novel asymmetrical interleaved dc/dc switching converters family intended for photovoltaic and fuel cell applications is presented in this paper. The main requirements on such applications are small ripples in the generator and load, as well as high voltage conversion ratio. Therefore, interleaved structures and voltage multiplier cells have been asymmetrically combined to generate new converters, which inherently operate in discontinuous conduction mode. The novel family is derived from boost, buck-boost and flyback-based structures. This converter family is analyzed to obtain the design equations and synthesize a design process based on the typical requirements of photovoltaic and fuel cell applications. Finally, the experimental results validate the characteristics and usefulness of the asymmetrical interleaved converter family.

Keywords: dc/dc switching converters; photovoltaic; fuel cell; interleaved topologies; asymmetrical interleaved; discontinuous conduction mode

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1. Introduction

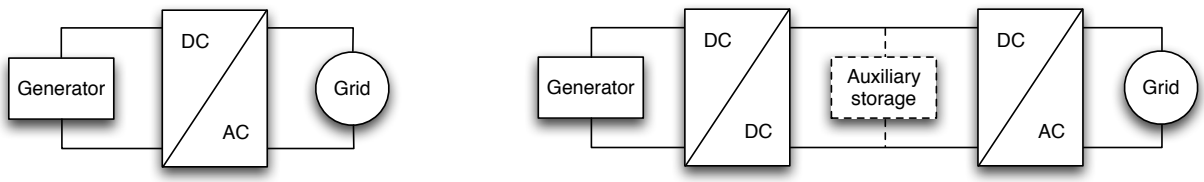
Photovoltaic and fuel cells systems are efficient alternatives to provide electrical power to distributed generation systems (DGS) since they introduce grid flexibility, redundancy for critical applications,

in situ energy generation, mitigation of transmission costs [1,2] and reduction of traditional energy generation that impact the environment. Similarly, photovoltaic and fuel cells generators have been intensively used in residential applications [3,4], electric vehicle power supply [5,6] and autonomous and portable applications [7,8].

Photovoltaic and fuel cell systems require a power electronics interface to be connected to the grid. This can be solved by using a single stage structure based on an inverter [9], as depicted in Figure 1(a), or by using a double stage structure based on dc/dc and dc/ac converters [10], as depicted in Figure 1(b). The single stage solution requires an inverter with specific features depending on the power source, *i.e.*, Maximum Power Point Tracking (MPPT) controller for photovoltaic applications. The double stage approach allows to use commercial grid-connection inverters without special features, and also to use a single inverter for a distributed generation system based on multiple fuel cells and photovoltaic generators [11]. In addition, several stand-alone applications require DC power, where a single dc/dc converter is required [5,12].

The double stage power electronics interface for photovoltaic and fuel cell systems in residential and general grid-connected applications is commonly based on a boosting converter that feeds an inverter. This is due to the requirement of increasing the voltage given by the source to the grid-connected inverter operating conditions. The most commonly used dc/dc converter in the first stage of this grid-connection and residential systems is a boost converter [6,7,12], which provides an acceptable voltage conversion ratio and also requests a continuous current from the power source. Similarly, in vehicular and stand-alone applications the boost converter is also widely adopted [5].

Figure 1. Photovoltaic and fuel cell systems grid-connection structure.



(a) Single stage. (b) Double stage.

Other characteristics required in photovoltaic and fuel cell applications are low current ripple injected to the power source and high conversion efficiency [5,13]. The current ripple magnitude is an additional factor in the selection of power converters for fuel cells and photovoltaic applications because high current ripples degrade the fuel cell stack, reducing its power production and life time [14]. In the photovoltaic case, the current ripple impacts the power generation since it produces an oscillation around the Maximum Power Point (MPP) [13,15], reducing the energy extracted from the photovoltaic generator. Those characteristics make the boost converter a good candidate to interface the photovoltaic and fuel cells systems. Instead, traditional buck or buck-boost converters will require an additional filter to interact with the power source due to the discontinuous input current of those topologies.

Using a boost converter, the current ripples in fuel cell and photovoltaic generators depend on the inductor size, switching frequency, input capacitor and power source high frequency impedance [16], and therefore to reduce the current ripple it is necessary to increase the converter inductance or input

capacitance, modifying the dynamics of the system. This can be addressed by using an additional filter between the power generator and the power converter [5], increasing also the power losses, size, weight, cost and order of the system.

Another possibility to reduce the converter's input current ripple is given by the interleaving structures [17]. The interleaving technique connects dc/dc converters in parallel to share the power flow between two or more conversion chains. This implies a reduction in the size, weight and volume of the inductors and capacitors [13,18]. Also, a proper control of the parallel converters increases the ripple frequency and reduces the ripple waveforms at the input and output of the power conversion system, which leads to a significant reduction of the current and voltage ripples [17,18]. The interleaving solution has been successfully used in fuel cell and photovoltaic applications [5,19,20], but the traditional interleaving structures require an internal current control loop in each phase to ensure the desired current and power sharing among the parallelized converters, since the different impedances in the parallel phases due to component tolerances can cause unbalances [5,19,20].

To achieve high voltage conversion ratio in photovoltaic and fuel cell applications, new dc/dc converters have been designed [21], but such converters are not easily interleaved as traditional ones. For example, Li *et al.* [22] and Kjaer *et al.* [23] review several power conversion structures dedicated to photovoltaic generators, where several dc/dc and dc/ac converters have been analyzed. Such works put in evidence the large amount of transformer-based solutions available in literature, but no interleaved structures are discussed.

Another option to increase the voltage conversion ratio of traditionally dc/dc converters consists in using voltage multiplier cells [24]. This solution affects the behavior of the original power converter, therefore it must be analyzed in detail, and continuous (CCM) or discontinuous (DCM) conduction modes are available for circuit operation. Another option to increase the dc/dc voltage conversion ratio providing high efficiency is to use asymmetrical structures [25].

This paper proposes the new asymmetrical interleaved converters (AIC) family as a significant contribution for fuel cell and photovoltaic power conversion systems. The AIC family was developed from traditional boost and buck-boost interleaved converters complemented with voltage multiplier cells, which provide higher conversion ratios compared with the respective traditional interleaved converters, but preserving the small input current and output voltage ripples characteristic of the interleaved structures, even in the buck-boost case. Similarly, the AIC family does not require an inner current control loops commonly used in traditional interleaved structures, reducing the complexity of the system.

Another characteristic of the proposed AIC family is its inherent DCM operation, which in traditional dc/dc converters [26], and even in its interleaved versions [27], implies a dependency of the voltage conversion ratio from the circuit parameters and load impedance, making it difficult to design non-constant load conditions. In the AIC family, despite its DCM operating conditions, conversion ratios do not depend on the circuit or load parameters, making it possible to adopt the traditional design procedures [26]. Finally, the AIC family includes isolated and non-isolated converters: boost and buck-boost derived topologies allow to interface fuel cells and photovoltaic systems with a wide range of high and low voltage applications. Also, the flyback structures of the AIC family provide higher voltage conversion ratios and additional galvanic isolation.

The remaining of the paper is organized as follows: the next section presents the interleaving concept through a classical configuration based on boost converters and the adoption of classical voltage multiplier cells to derive the new interleaved converters. Section 3 introduces the AIC family by means of an interleaved boost derived converter, named Asymmetrical interleaved dual boost, whose circuital analysis is performed. The AIC family design process is also introduced in Section 3 by means of a design example verified experimentally. Section 4 presents the second member of the AIC family, the Asymmetrical interleaved dual buck-boost, whose circuital analysis and design equations are described. Then, Section 5 introduces the AIC family members based on flyback transformers, named Asymmetrical interleaved dual flyback converters, where the isolated and non-isolated versions are developed and analyzed. Finally, conclusions are given in Section 6, where the particular features of each AIC family member are discussed and a simple selection criterion is given.

2. Interleaved Structures and Voltage Multiplier Cells

The interleaving technique consists in the parallel interconnection of a determined number of identical converter cells (N canonical cells), whose control signals are strategically phase-shifted in each switching period. This arrangement reduces the net ripple amplitude through harmonic cancellation and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses, at the time that divides the input power between the N canonical cells. An interleaved system reduces the ripple filtering requirements, the conduction losses, and prototype size without sacrificing conversion efficiency [18].

The interleaved interconnection of two switching cells requires the individual switching instants of the two cells to be sequentially phased over equal fractions of a switching period. To reduce the converter ripples, two configurations are optimal: when one switch is ON at the same time the other one is OFF. In these optimal configurations, the inductor current of one cell is increasing while the other one is decreasing, therefore the inductor current waveforms of the two switching cells have slopes with opposite signs. For this reason, their sum, which is the slope of the total interleaved input current, is reduced as well as its ripple. Consequently, if the aim is to obtain low input and output ripples, the interleaved circuit has to be controlled to turn on the switches in a complementary way. This complementary interleaving offers more simplicity in the control design than other kinds of interleaving, because one activation signal is the opposite of the other activation signal [28].

2.1. Interleaved Dual Boost (IDB)

The application of the complementary interleaving technique to the parallel connection of two boost converters was analyzed in [28]. The circuit was named IDB (Interleaved Dual Boost) and its scheme is depicted in Figure 2. To obtain the desired ripple reduction, both IDB boost converters must be operated in CCM [28]. This condition can be ensured by fulfilling the boost CCM conversion ratio in each branch:

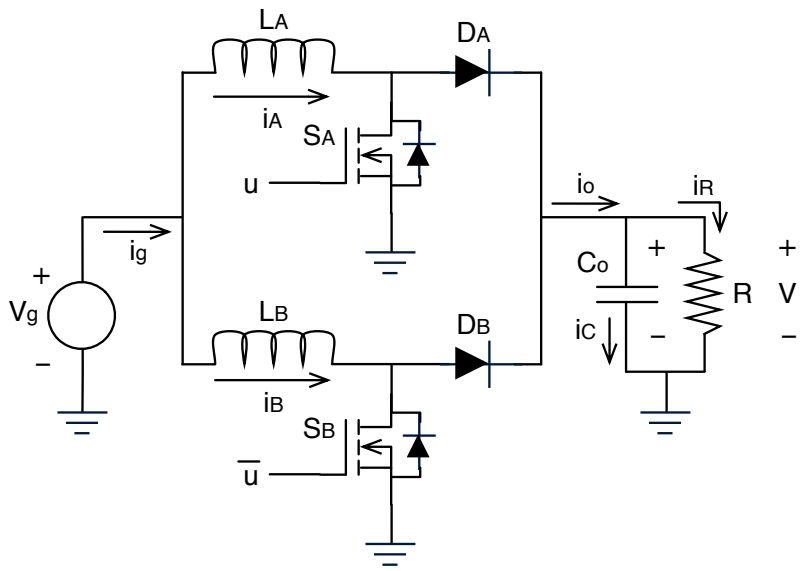
$$V = \frac{V_g}{1 - D_A} = \frac{V_g}{1 - D_B} \tag{1}$$

where V is the IDB output voltage, V_g its input voltage, and D_A and D_B are the first and second branches duty cycles, respectively. Equation (1) leads to

$$D_A = D_B = 0.5 \tag{2}$$

From Equations (1) and (2), the IDB CCM operation can be ensured only for a steady state duty cycle of 50%, or 0.5. Consequently, the usefulness of the circuit in complementary interleaving is restricted to a 50% duty cycle, which makes impossible to regulate its output voltage.

Figure 2. Interleaved dual boost (IDB) converter.

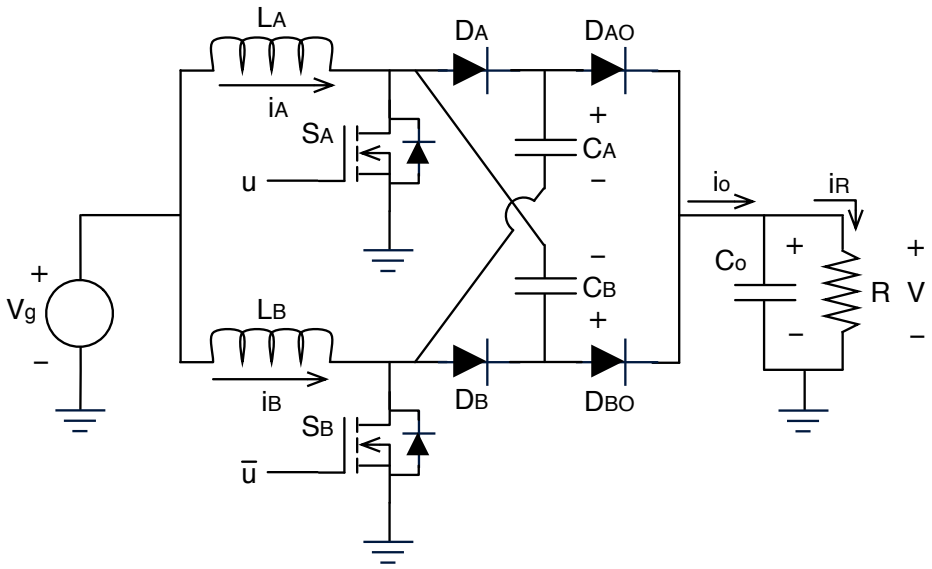


2.2. *Switched Capacitor Interleaved Dual Boost (SCIDB)*

The SCIDB [28] is obtained from the interconnection of the IDB converter with one classical switched capacitor-based voltage multiplier cell, deriving the circuit depicted in Figure 3. Such a circuit is a four-order step-up converter, where the switches are controlled in a complementary way, providing conversion ratios higher than four for duty cycles different from 0.5, but in such conditions the input ripple cancelation is not optimal. Also, the capacitors C_A and C_B are interconnected in parallel for particular duty cycle conditions, generating current spikes to balance the capacitors voltages, degrading the output voltage ripple quality.

However, the SCIDB converter has controllability problems for duty cycle equal to 0.5 resulting from the cancellation of the global variables in its small signal transfer functions [28]. In this converter, the proximity of the open loop poles to the imaginary axis depends on the elements' parasitic resistances, and the voltage transfer functions exhibit zeros on the right-hand side of the Laplace plane. Finally, the optimal input current and output voltage ripples cancelation is achieved in an operating point where the SCIDB behavior is strongly dependent on the elements' parasitic resistances. Therefore, Section 3 describes the generation of the AIC family from circuital modification to the SCIDB converter to overcome its natural disadvantages without degrading the desired ripple harmonics cancelation and high voltage conversion ratio characteristics.

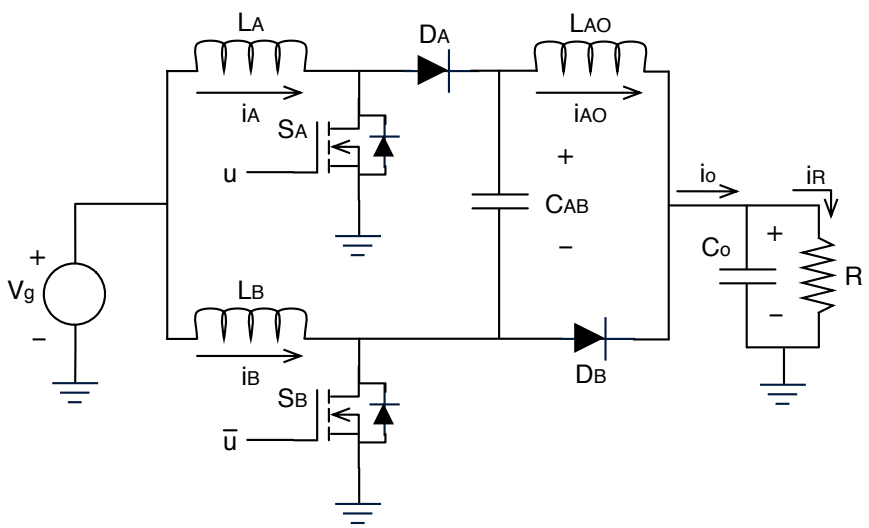
Figure 3. Switched capacitor interleaved dual boost (SCIDB) converter.



3. Asymmetrical Interleaved Dual Boost (AIDB)

The Asymmetrical interleaved dual boost (AIDB) was obtained from the SCIDB converter by performing circuital modifications. The first objective was the improvement of the output voltage ripple by increasing the order of the output filter. In this way, inductive filters were placed at the branch outputs in order to avoid the current spikes caused by capacitors C_A and C_B. The structure obtained exhibit a similar behavior to the IDB [28], where the CCM operating condition is constrained to duty cycles near to 0.5, therefore it is not possible to regulate. This is because each branch of the SCIDB structure with high-order output filter behaves as a voltage source as in the IDB case. To avoid this limitation, the symmetry of the structure is broken by removing a voltage multiplier cell from one branch of the converter, obtaining the asymmetrical circuit of Figure 4.

Figure 4. Asymmetrical interleaved dual boost (AIDB) converter.



The AIDB converter is a parallel interconnection between a boost with an output filter (branch A) and a boost simple cell (branch B), in which the first capacitor of the A-branch output filter is connected to the intermediate node of the boost of the B-branch. This method follows the concept of switching capacitors-based voltage multiplier cells. The MOSFETs S_A and S_B are activated in a complementary way to obtain the desired input current ripple reduction.

3.1. Circuital Analysis

The sequences of operation intervals, which have the duration d_1T, d_2T and d_3T, respectively, are obtained from circuital analysis. In order to illustrate the circuit topologies and the transitions among them, the waveforms of the AIDB currents have been obtained following the analytical method based on initial simulations described in [29], which has been extensively used in the analysis of dc/dc switching converters [30,31]. Without loss of generality, Figure 5 shows the DCM current waveforms of the AIDB circuit for a duty cycle equal to 0.5. Since the analysis considers a non-regenerative load (it only consumes energy), the i_O current is always positive and Figure 5 has not cross over zero current. Then, from the intervals definition, the following relationships are obtained:

$$d_1 + d_2 + d_3 = 1 \tag{3}$$

$$d_1 = d' \quad \wedge \quad d_2 + d_3 = d \tag{4}$$

Figure 5. AIDB operation intervals: d_1T, d_2T and d_3T.

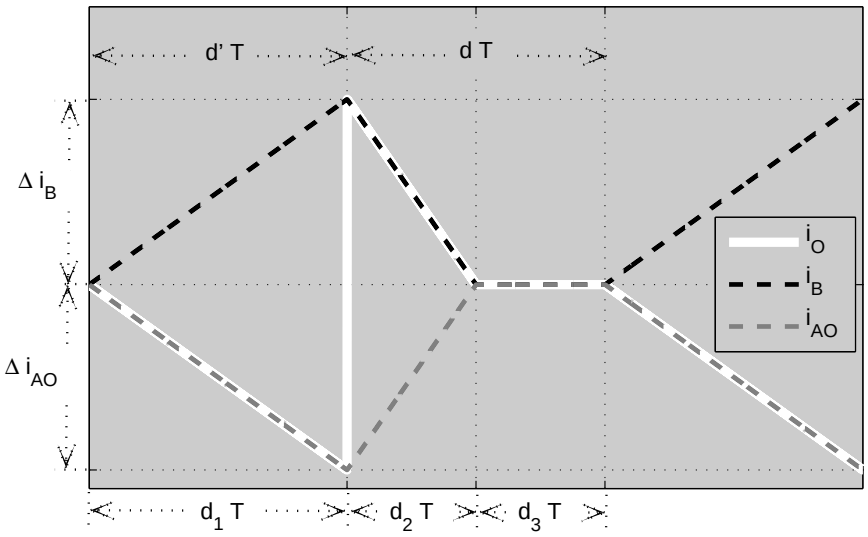


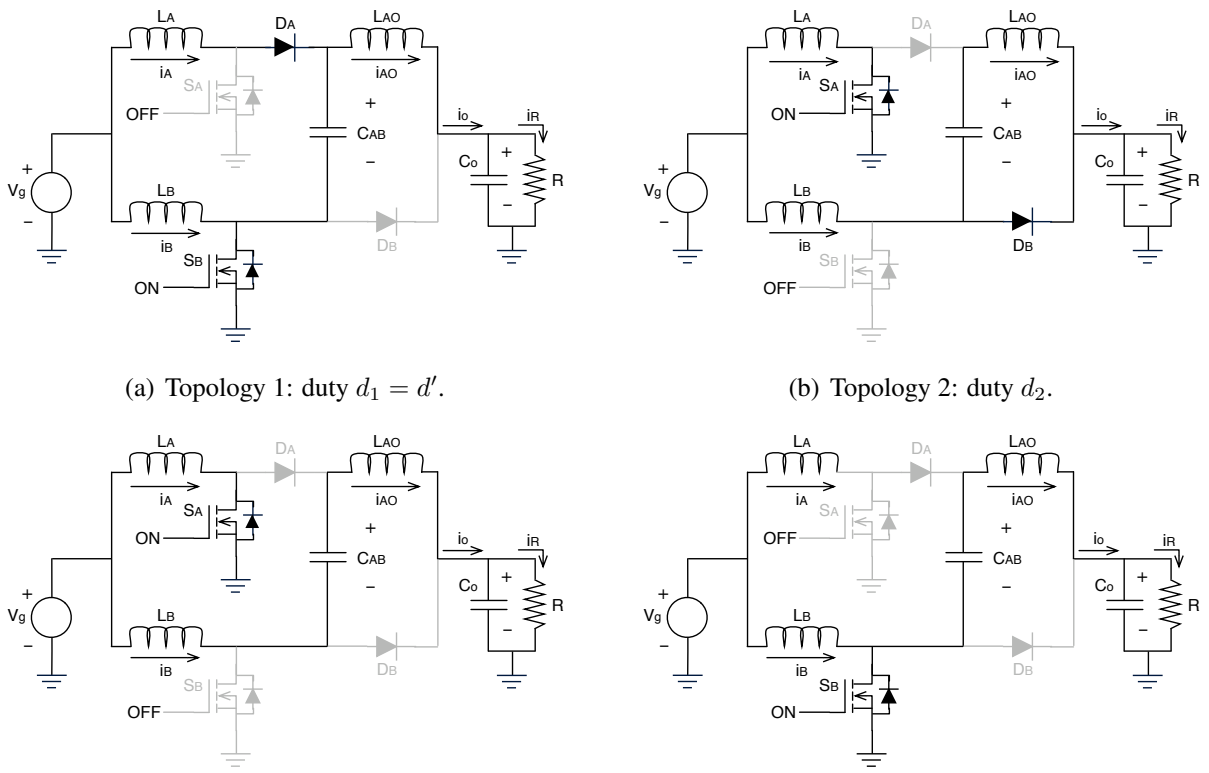
Figure 6 shows the four topologies of the converter in each operation interval:

- topology 1: S_B and D_A ON; S_A and D_B OFF.
- topology 2: S_A and D_B ON; S_B and D_A OFF.
- topology 3: S_A ON; S_B, D_A and D_B OFF; D_B OFF because i_B and i_{AO} are in DCM.
- topology 4: S_B ON; S_A, D_A and D_B OFF; D_A OFF because i_A is in DCM.

Two different topology sequences take place depending on the duty cycle as will be demonstrated afterwards: for duty cycles greater than 0.382, the converter structure changes into topologies 1, 2 and 3. Similarly, for duty cycles lower than 0.382, the converter structure changes into topologies 1, 4 and 2. In the first sequence, named *designed sequence*, the transition from topology 1 to topology 2 is driven by the change of the MOSFET states. The transition from topology 2 to topology 3 occurs when i_B and i_{AO} currents are equal, and therefore the diode D_B current becomes zero. Finally, the transition from topology 3 to topology 1 is driven by the change of the MOSFET states. In the second sequence, named *undesired sequence*, the transition from topology 1 to topology 4 occurs when the i_A current falls to zero. The transition from topology 4 to topology 2 is driven by the change of the MOSFET states. Finally, the transition from topology 2 to topology 1 is driven by the change of the MOSFET states.

The designed sequence provides the low input current and output voltage ripples characteristic required for photovoltaic and fuel cell applications. This is because the L_A inductor current is continuous and hence produces a low harmonic content. In contrast, the undesired sequence exhibits both L_A and L_B discontinuous inductor currents producing high harmonic content, making it not useful for the intended applications. Therefore, the circuital equations are analyzed to obtain the conditions that ensure the operation in the desired sequence.

Figure 6. AIDB topologies.



(a) Topology 1: duty $d_1 = d'$.

(b) Topology 2: duty d_2.

(c) Topology 3: duty d_3.

(d) Topology 4: duty d_3.

Considering the small-ripple approximation in the state variables of the converter [26], therefore the operation in the designed sequence, the steady-state operation intervals can be described in terms of the converter duty cycle D and the topologies transitions: the AIDB converter remains on topology 1 meanwhile MOSFET S_A is OFF and MOSFET S_B is ON, which corresponds to $D_1 \cdot T = D' \cdot T$, leading

to Equation (5), as shown in Figure 6(a). Similarly, since the transition from topology 2 to topology 3 is caused by the dynamics of the circuit, and the AIDB remains on topology 3 while MOSFET S_A is ON and MOSFET S_B is OFF, the combined duration of topologies 2 and 3 is equal to $D \cdot T$. Also, defining the interval durations of topologies 2 and 3 as $D_2 \cdot T$ and $D_3 \cdot T$, respectively, Equations (6) and (7) are obtained.

$$D_1 = D' \tag{5}$$

$$D_2 + D_3 = D \tag{6}$$

$$D_1 + D_2 + D_3 = 1 \tag{7}$$

From the AIDB topologies depicted in Figure 6, a permanent loop is formed by the voltage source V_g, the inductors L_B and L_{AO}, and the capacitors C_{AB} and C_O, is constantly interconnected. Considering the converter in steady-state, the average values of the inductor voltages are equal to zero due to the volt-second balance [26], and the permanent loop leads to:

$$V_g + V_{AB} = V_o \tag{8}$$

where V_{AB} and V_O represents the C_{AB} capacitor and output voltages, respectively. The steady state condition allows to calculate the L_A inductor current ripple magnitude from the first topology, left side of Equation (9), and from the second or third topology, right side of Equation (9), where T is the switching period.

$$\left| \frac{V_g - V_{AB}}{L_A} \cdot D' \cdot T \right| = \left| \frac{V_g}{L_A} \cdot D \cdot T \right| \tag{9}$$

From (9) it is obtained the expression for V_{AB} as:

$$V_{AB} = \frac{V_g}{D'} \tag{10}$$

Similarly, the average value of V_O can be obtained as:

$$V_O = V_g \cdot \left(1 + \frac{1}{D'} \right) \tag{11}$$

where the AIDB voltage conversion ratio is given by (12), which is higher than the one provided by the boost converter (13) [26] for the same duty cycle.

$$M(D)_{AIDB} = 1 + \frac{1}{1 - D} \tag{12}$$

$$M(D)_{Boost} = \frac{1}{1 - D} \tag{13}$$

Analyzing the permanent loop in topology 3, the inductors L_B and L_{AO} voltages are related by:

$$-V_g + V_B - V_{AB} + V_{AO} + V_o = 0 \tag{14}$$

where V_B and V_{AO} correspond to the inductor L_B and L_{AO} voltages, respectively. Introducing Equations (10) and (11) into (14), the following relationship is obtained:

$$V_B = -V_{AO} \tag{15}$$

In the permanent loop of topology 3 the inductors L_B and L_{AO} are in series, therefore its currents must be equal:

$$i_B = i_{AO} \tag{16}$$

Deriving Equation (16), the following relation is obtained:

$$L_{AO} \cdot V_B = L_B \cdot V_{AO} \tag{17}$$

The solution of the system described by Equations (15), (16) and (17) is given by $V_B = V_{AO} = 0$, which implies that i_B and i_{AO} are equal and constant in the interval $D_3 \cdot T$. Also, from the charge balance in the output capacitor C_o for topology 3, the following relation is given:

$$i_B = i_{AO} = I_o \ , \quad \forall \ (D_1 + D_2) \cdot T \leq t \leq T \tag{18}$$

where I_o represents the average value of the output current in the switching period.

The ripple amplitude of the L_B current can be obtained from the first and second topologies as given in (19), because in the third topology there is no ripple (18) and the converter is in steady state.

$$\left| \frac{V_g}{L_B} \cdot D' \cdot T \right| = \left| \frac{V_g - V_o}{L_B} \cdot (D - D_3) \cdot T \right| \tag{19}$$

From (11) and (19), the duty D_3 of the third operation interval can be calculated as:

$$D_3 = 1 - D' - (D')^2 \tag{20}$$

Moreover, the duty D_2 is calculated from (6) and (20):

$$D_2 = (D')^2 \tag{21}$$

The AIDB average capacitor voltages Equation (10), voltage conversion ratio Equation (12), and duty of the operation intervals Equation (5,21,20), do not depend on the converter parameters despite its DCM operation in topology 3. This is an useful characteristic since it is possible to adopt traditional CCM design procedures [26], which are not easily applied to traditional DCM operating conditions.

Equation (20) defines a boundary in the duty cycle at $D = 0.382$. When $0 < D < 0.382$, $D_3 < 0$ implies that the AIDB converter is not operating in the designed sequence, therefore it is operating in the undesired one. In the particular case of $D = 0.382$, since $D_3 = 0$, the AIDB converter only operates in topologies 1 and 2, working in CCM. This operation sequence is defined as *limit sequence*.

The average current in the C_{AB} capacitor in the first, second and third topologies is given by $I_A - I_{AO}$, $-I_{AO}$ and $-I_{AO} = -I_B$, respectively, where I_A is the steady state current in L_A, I_{AO} is the steady state current in L_{AO}, and I_B is the steady state current in L_B. From the charge balance on C_{AB} capacitor Equation (22), and from Equation (6), the relation between I_A and I_{AO} presented in Equation (23) is obtained.

$$(I_A - I_{AO}) \cdot D' \cdot T - I_{AO} \cdot D_2 \cdot T - I_{AO} \cdot D_3 \cdot T = 0 \tag{22}$$

$$I_A = \frac{I_{AO}}{D'} \tag{23}$$

Similarly, the charge balance on the output capacitor C_O can be analyzed in two different approaches. The first one, given in Equation (24), takes into account that in topologies 2 and 3 the output current is supplied by L_B. The second approach, given in Equation (25), is based on the series connection of L_B and L_{AO} in the third topology. Moreover, from Equation (20) and Equation (21), the relation between I_{AO} and I_B is given in Equation (26).

$$I_{AO} \cdot D' \cdot T + I_B \cdot D \cdot T = \frac{V_O}{R} \tag{24}$$

$$I_{AO} \cdot D' \cdot T + I_B \cdot D_2 \cdot T + I_{AO} \cdot D_3 \cdot T = \frac{V_O}{R} \tag{25}$$

$$I_{AO} = I_B \tag{26}$$

From Equations (11,23,24,26), the steady state values of the inductor currents are:

$$I_{AO} = I_B = \frac{V_g}{R} \cdot \left(1 + \frac{1}{D'}\right) \tag{27}$$

$$I_A = \frac{I_B}{D'} = \frac{I_{AO}}{D'} \tag{28}$$

Since the input node of the AIDB converter consist in the parallel connection of both L_A and L_B inductors, Equation (28) gives information about the current sharing in a particular operating point. Therefore, an additional control loop to ensure the current sharing among branches is not required. Moreover, both Equations (27) and (28) define the inductor current ratings, where I_B and I_{AO} have the same current rating while I_A has a higher one. As consequence, L_A inductor will be heavier and bulkier than L_{AO} and L_B.

3.2. Design Process

The design process of the AIDB converter must be defined in terms of the typical requirements in photovoltaic and fuel cell applications. The first condition imposed will be the voltage conversion ratio because fuel cell and photovoltaic generators define the converter input voltage, while the load specifications define the converter output voltage. From Equation (12), the duty cycle for a given input and output voltages is:

$$D = \frac{V_O - 2V_g}{V_O - V_g} \tag{29}$$

A second important requirement concerns the input current ripple amplitude as described in Section 1. In this way, the input current ripple magnitude of the AIDB converter, which corresponds to the difference between L_A and L_B current ripples in the first, second, and third topologies, is given by Equation (30–32), respectively.

$$\Delta i_{g1} = Vg \cdot T \cdot \left(\frac{-D}{L_A} + \frac{D'}{L_B}\right) \tag{30}$$

$$\Delta i_{g2} = Vg \cdot T \cdot (D')^2 \cdot \left(\frac{1}{L_A} - \frac{1}{D' \cdot L_B}\right) \tag{31}$$

$$\Delta i_{g3} = \frac{Vg \cdot T}{L_A} \cdot \left(1 - D' - (D')^2\right) \tag{32}$$

The input current ripple magnitudes of the three topologies represent the input current ripple evolution in the switching period. Considering steady state behavior:

$$\Delta i_{g1} + \Delta i_{g2} + \Delta i_{g3} = 0 \tag{33}$$

Therefore, the magnitude of the larger ripple section must be equal to the sum of the magnitudes of the other ones, and corresponds to the magnitude of the input current ripple Δi_g:

$$\Delta i_g = \max\left(\left|\Delta i_{g1}\right|, \left|\Delta i_{g2}\right|, \left|\Delta i_{g3}\right|\right) \tag{34}$$

Adopting the design condition $L_A = L_B = L$, the expressions for Δi_{g1}, Δi_{g2} and Δi_{g3} are simplified to Equations (35–37) and related by Equations (38–40).

$$\Delta i_{g1} = \frac{V_g \cdot T}{L} \cdot (2D' - 1) \tag{35}$$

$$\Delta i_{g2} = -\frac{V_g \cdot T}{L} \cdot (D \cdot D') \tag{36}$$

$$\Delta i_{g3} = \frac{V_g \cdot T}{L} \cdot \left(1 - D' - (D')^2\right) \tag{37}$$

$$\Delta i_{g1} < \Delta i_{g2}\ ,\ \forall\ D \in [0.382, 1] \tag{38}$$

$$\Delta i_{g1} < \Delta i_{g3}\ ,\ \forall\ D \in [0.439, 1] \tag{39}$$

$$\Delta i_{g2} < \Delta i_{g3}\ ,\ \forall\ D \in [0.500, 1] \tag{40}$$

Therefore, Equation (34) is modified to design L_A and L_B for a given Δi_g adopting $L_A = L_B = L$, where

$$L = \begin{cases} \dfrac{V_g \cdot T}{\Delta i_g} \cdot D \cdot D' & ,\ 0.382 \leq D \leq 0.5 \\ \dfrac{V_g \cdot T}{\Delta i_g} \cdot \left(1 - D' - (D')^2\right) & ,\ 0.5 < D \leq 1.0 \end{cases} \tag{41}$$

When the condition $L_A = L_B$ is not adopted, L_A and L_B can be designed in terms of the inductor current ripples as given in Equations (42) and (43), respectively.

$$L_A = \frac{V_g}{\Delta i_A} \cdot D \cdot T \tag{42}$$

$$L_B = \frac{V_g}{\Delta i_B} \cdot D' \cdot T \tag{43}$$

Similarly, L_{AO} inductor can be designed in agreement with the desired inductor current ripple Δi_{AO} as given in Equation (44).

$$L_{AO} = \frac{V_g - V_O \cdot D'}{\Delta i_{AO}} \cdot T \tag{44}$$

But considering that current in C_{AB} is defined by the difference between L_B and L_{AO} currents, the condition that provides the best approximation to a triangular waveform of the C_{AB} voltage is given by Equation (45), since this simplifies the capacitor design in terms of voltage ripple by following the criteria given in [26].

$$\left|\Delta i_{AO}\right| = \left|\Delta i_B\right| \tag{45}$$

From Equations (43–45), and taking into account that L_{AO} and L_B currents have opposite slopes Equation (15), the additional design criterion given in Equation (46) is proposed.

$$L_{AO} = L_B \tag{46}$$

The design of the C_{AB} capacitor can be also based on the capacitor voltage ripple as described in Equation (47),

$$C_{AB} = \frac{V_g}{R \cdot \Delta v_{AB}} \cdot \left(1 + \frac{1}{D'}\right) \cdot D \cdot T \tag{47}$$

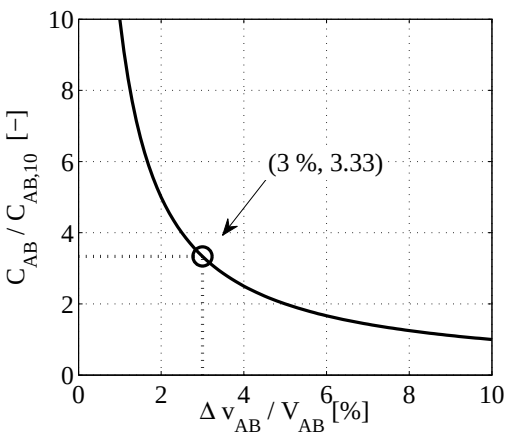
but triangular current waveforms on L_A, L_B and L_{AO} are also desirable to simplify the inductor analysis following the small-ripple approximation [26]. Such a condition is obtained by minimizing the C_{AB} voltage ripple, generating inductors voltage close to square waveforms, which is an additional design criterion. The relative C_{AB} voltage ripple is given by Equation (48), and the C_{AB} capacitance for $\Delta v_{AB}/V_{AB} = 10\%$ is given by Equation (49).

$$\frac{\Delta v_{AB}}{V_{AB}}\,[\%] = \frac{T \cdot D \cdot (2 - D)}{R \cdot C_{AB}} \tag{48}$$

$$C_{AB,10} = 10 \cdot \frac{T \cdot D \cdot (2 - D)}{R} \tag{49}$$

To illustrate the C_{AB} selection criterion, Figure 7 shows the C_{AB} capacitor value in comparison with $C_{AB,10}$ for relative C_{AB} voltage ripples lower than 10%. It is noted that a $\Delta v_{AB}/V_{AB} = 5\%$ is obtained by using a $C_{AB} = 2 \cdot C_{AB,10}$, while a $\Delta v_{AB}/V_{AB} = 3\%$ is obtained by using a $C_{AB} = 3.33 \cdot C_{AB,10}$. The required C_{AB} capacitance grows proportionally to the inverse of Δv_{AB} ripple magnitude. Finally, it is necessary to define a tradeoff between capacitance and voltage ripple magnitude.

Figure 7. C_{AB} relative size for different voltage ripples.



The design of the output capacitor C_O is performed to fulfill a given output voltage ripple requirement. Based on Equations (18) and (27), and on the circuital analysis of the topologies of Figure 6, the output current ripple in the first topology is given by Δi_{AO} Equation (44). Using the approximation given

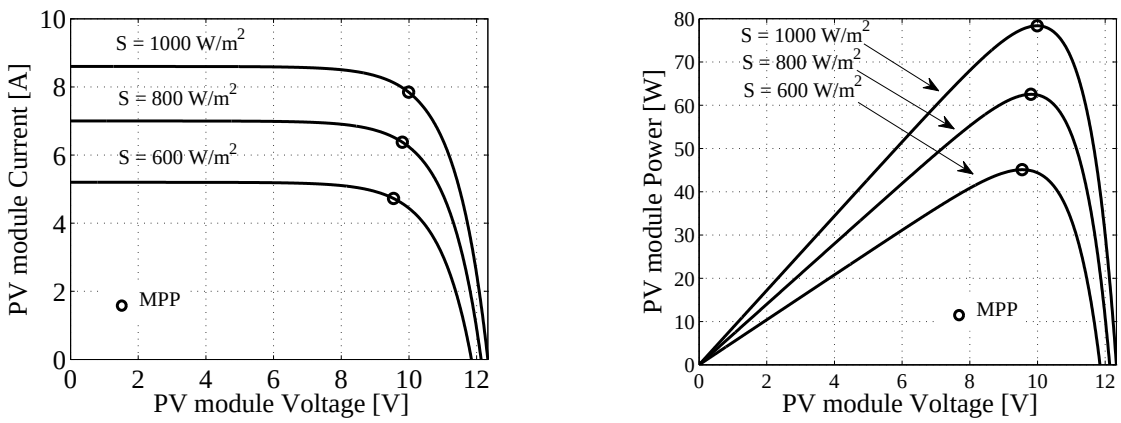
by [26] to calculate the capacitor voltage ripple in triangular current waveforms, the C_O capacitance to obtain an output voltage ripple Δv_O is:

$$C_O = \frac{(D' \cdot T)^2 \cdot V_g}{2 \cdot L_{AO} \cdot \Delta v_O} \tag{50}$$

3.3. Design Example and Experimental Results

The design of the AIDB converter is illustrated considering a grid connected photovoltaic application, which requires a step-up dc/dc converter to meet the inverter input voltage level [32]. In particular, the Distributed Maximum Power Point Tracking technique (DMPPT) uses a dedicated dc/dc converter for each PV module, which can be defined as the basic unit of the PV panel that can be subjected to the mismatching phenomena [32]. The DMPPT solution allows to overcome shadowing and mismatching conditions that degrade the power production of the PV panel. Without loss of generality, this example considers the PV panel Sharp NU-U235F1: it consists of three cell-strings in series, each one of them equipped with a by-pass diode. Consequently, the NU-U235F1 is composed by three PV modules, each one of them exhibiting a maximum power P_{mpp} = 78 W, voltage at maximum power V_{mpp} = 10 V, current at maximum power I_{mpp} = 7.84 A, open circuit voltage V_{oc} = 12.33 V, and short circuit current I_{sc} = 8.60 A, all of those parameters measured in Standard Test Conditions (STC). Figure 8 shows the current-voltage (I-V) and power-voltage (P-V) characteristic curves for a single PV module under three different irradiance conditions (S): 1000 W/m^2, 800 W/m^2, and 600 W/m^2.

Figure 8. Sharp NU-U235F1 single module characteristics.



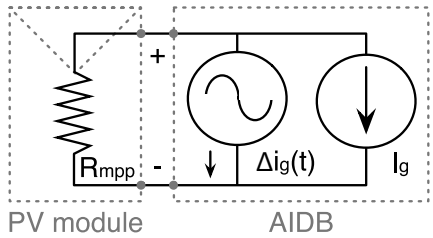
(a) I-V curve. (b) P-V curve.

Considering a 500 W and 120 VAC grid connected full bridge inverter, where the MPPT is performed by AIDB converters, the application uses two NU-U235F1 PV panels, which corresponds to the 95% of the maximum power allowed in the inverter. Since each PV panel consists of three PV modules, this DMPPT example requires six AIDB converters with series connected output ports.

The full bridge inverter requires 170 V to meet the grid voltage. To provide an additional 5% safety margin to compensate parasitic losses, the input voltage for the inverter has been set to 180 V. Such a condition defines the AIDB input and output voltages $V_g = 10$ V and $V_O = 30$ V, respectively, therefore the duty cycle in the MPPT conditions is $D = 0.5$ as described in Equation (29).

The input inductors must be designed to ensure the required input current ripple magnitude. In this photovoltaic example, such a ripple magnitude affects the power produced by the PV module since it generates an undesired oscillation around the optimal operating point. To analyze this effect, the small signal equivalent circuit of the PV module-AIDB converter given in Figure 9 is used.

Figure 9. PV module and AIDB small signal equivalent circuit.



The AIDB input current $i_g(t)$, in steady-state, can be modeled by

$$i_g(t) = I_g + \Delta i_g(t) \tag{51}$$

where I_g correspond to the DC component of the input current, and $\Delta i_g(t)$ represents the current ripple with a peak-to-peak magnitude of Δi_g. In the same model $R_{mpp} = V_{mpp}/I_{mpp}$ represents the small signal behavior of the PV module [32], named PV module differential resistance. Since a properly designed MPPT controller provides a MPPT efficiency higher than 99% [33], the oscillation on the power due to the AIDB input current ripple is selected to be 0.1%, Equation (52). The current ripple magnitude that generates such a power oscillation is:

$$\frac{\Delta P_{max}}{P_{mpp}} = 0.1\% \tag{52}$$

$$\Delta P_{max} = R_{mpp} \cdot \Delta i_g^2 \tag{53}$$

For the considered NU-U235F1 PV modules, $R_{mpp} = 1.276\ \Omega$, ΔP_{max} = 78 mW, and Δi_g = 247.3 mA. Using Equation (41), and adopting a switching frequency $f_{sw} = 50$ kHz, the input inductors are calculated equal to 202.18 μH, where near commercial inductors $L_A = L_B = 200\ \mu$H were selected. Similarly, following the design criteria given in Equation (46), $L_{AO} = 200\ \mu$H was designed.

In fuel cell applications, the input current ripple constraint for the AIDB converter design can be extracted from the fuel cell manufacturer specification for the maximum current ripple allowed, as well as from experimental results reported in the literature [5].

The C_{AB} capacitor is designed to obtain inductor currents triangular waveforms. In this way, a tradeoff between the C_{AB} capacitance and the Δv_{AB} voltage ripple is achieved by using Figure 7, selecting $C_{AB} = 50\ \mu$F that generates an acceptable $\Delta v_{AB}/V_{AB} = 3\%$ condition. Also, to obtain a small series resistance, five 10 μF capacitors have been parallelized to construct C_{AB}.

The design of C_O can be performed by using Equation (50). In practical applications, the output voltage ripple is defined by the load requirements. To illustrate the design procedure, this example adopts an output voltage ripple magnitude equal to 0.4% of the nominal output voltage as proposed in [34] for traditional dual interleaved boost converters. To obtain such a Δv_O condition, an output capacitance

equal to 20.83 μF is required, where five 4.7 μF commercially available capacitors were parallelized to achieve a $C_O = 23.5$ μF.

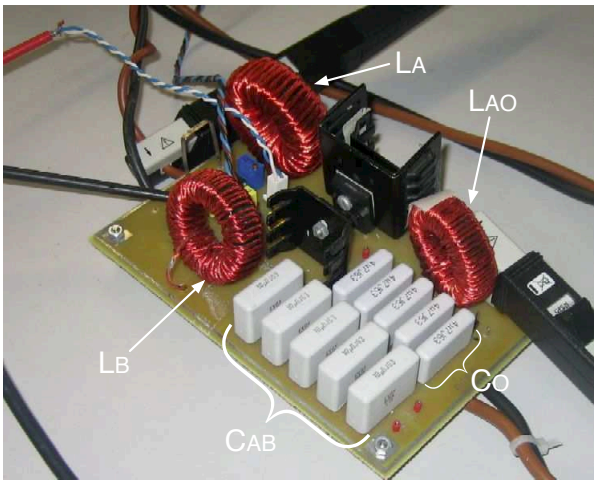
In PV applications it is common to place a capacitor between the PV module and the dc/dc converter [33] to reduce the current ripple injected into the module. Using the model of Figure 9, and considering a capacitor C_{PV} between the PV module and the dc/dc converter, and a maximum allowed ripple magnitude Δi_{PV} propagated into the PV module, the value of C_{PV} is given by:

$$C_{PV} = \frac{[\Delta i_g/\Delta i_{PV}] - 1}{2\pi \cdot f_{sw} \cdot R_{mpp}} \quad , \quad 0 < \Delta i_{PV} \leq \Delta i_g \tag{54}$$

Equation (54) makes evident that the AIDB small input current ripple requires a small C_{PV}, or even allows to remove it depending on the AIDB design. This can be contrasted with the traditional PV applications using boost converters [32,33] where a significant capacitor C_{PV} is required, which also introduces dynamics that affect the MPPT algorithm design as described in [33].

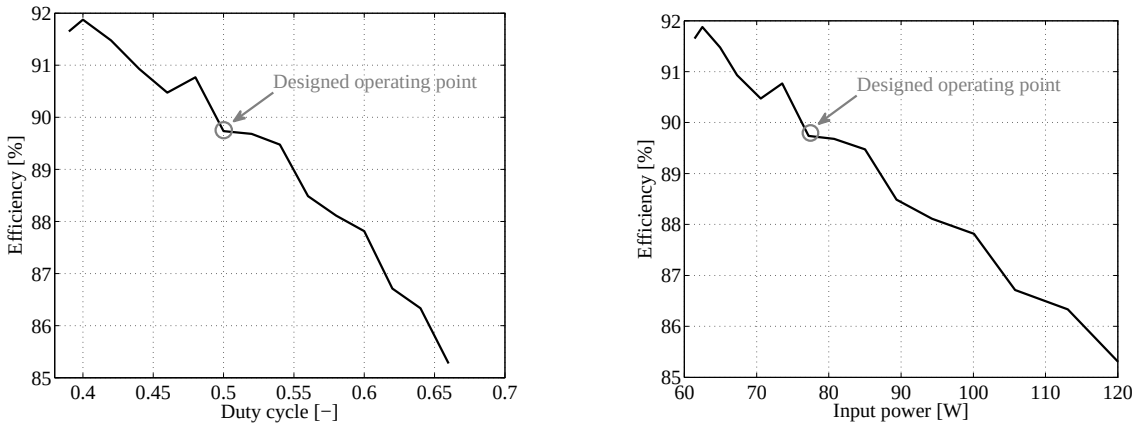
An AIDB experimental prototype is depicted in Figure 10. As expected, the inductor L_A is bulkier than L_{AO} and L_B since it must to conduct higher currents. Moreover, in the electronic devices the following parasitic resistances were measured: resistance in L_A, L_B and L_{AO} were $R_{L_A} = 34$ $m\Omega$ and $R_{L_B} = R_{L_{AO}} = 66$ $m\Omega$, respectively. Resistance in C_{AB} and C_O were $R_{C_{AB}} = R_{C_O} = 81$ $\mu\Omega$, and the MOSFETs and DIODEs used were IRFP054 and MBR1045, respectively, and a single IR4428 driver was required since it provides complementary outputs to drive both MOSFETs.

Figure 10. AIDB experimental prototype.



The efficiency of the experimental prototype at the designed operating point is 89.74% as observed in Figure 11, where different duty cycle and input power (P_i) conditions have been evaluated: $0.382 < D < 0.660$ and $62\ W < P_i < 120\ W$. Such an operating range has been constrained in the left by the duty cycle boundary that guarantees the operation in the designed sequence and in the right by limitations in the equipment used for the tests.

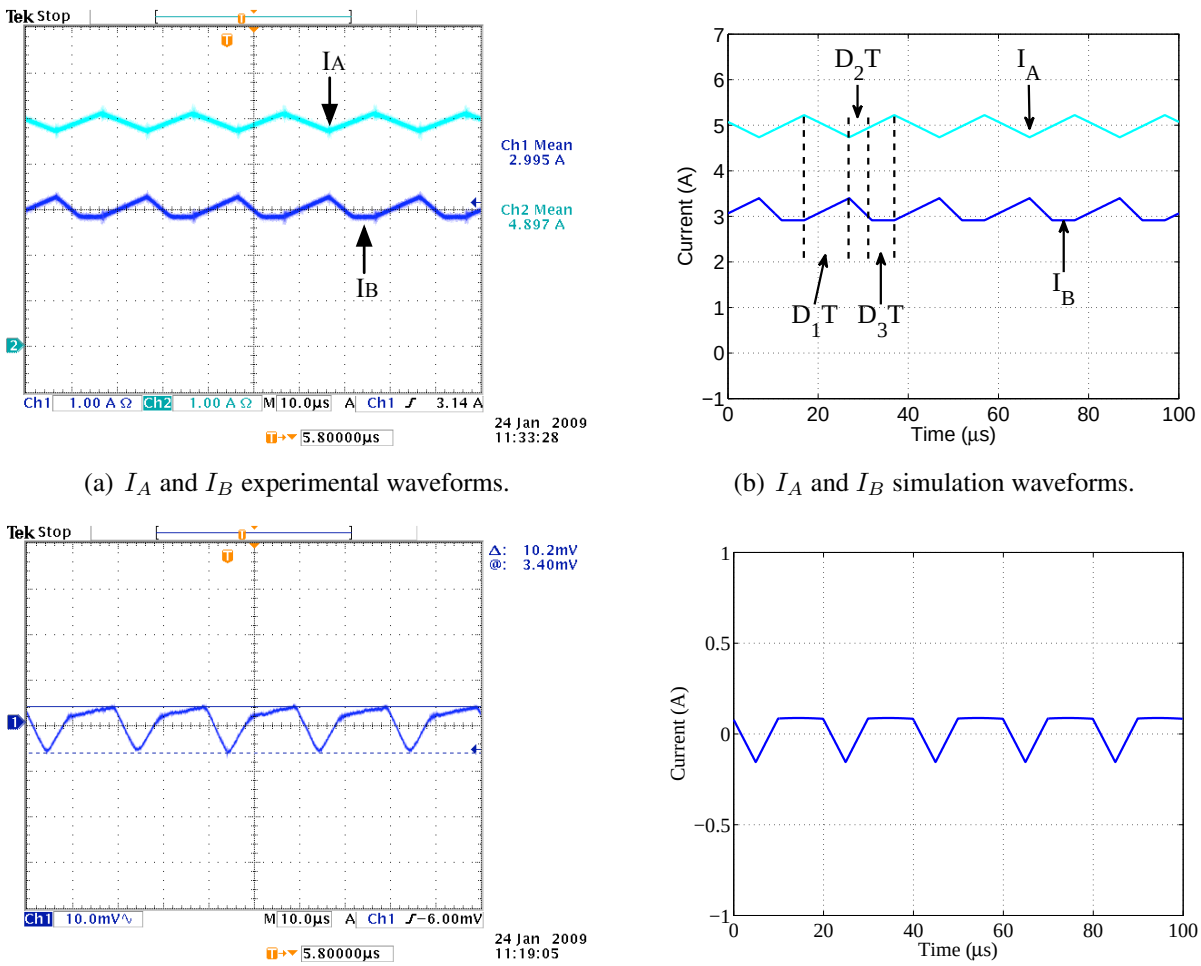
Figure 11. Experimental efficiency of the AIDB prototype.



(a) Different duty cycle conditions. (b) Different input power conditions.

To illustrate the AIDB converter behavior, a simulation model of the converter and the experimental prototype has been tested considering the design example conditions. In this way, Figure 12 shows the input inductor currents and the overall AIDB input current.

Figure 12. AIDB input current waveforms for $D = 0.5$.



(a) I_A and I_B experimental waveforms. (b) I_A and I_B simulation waveforms.

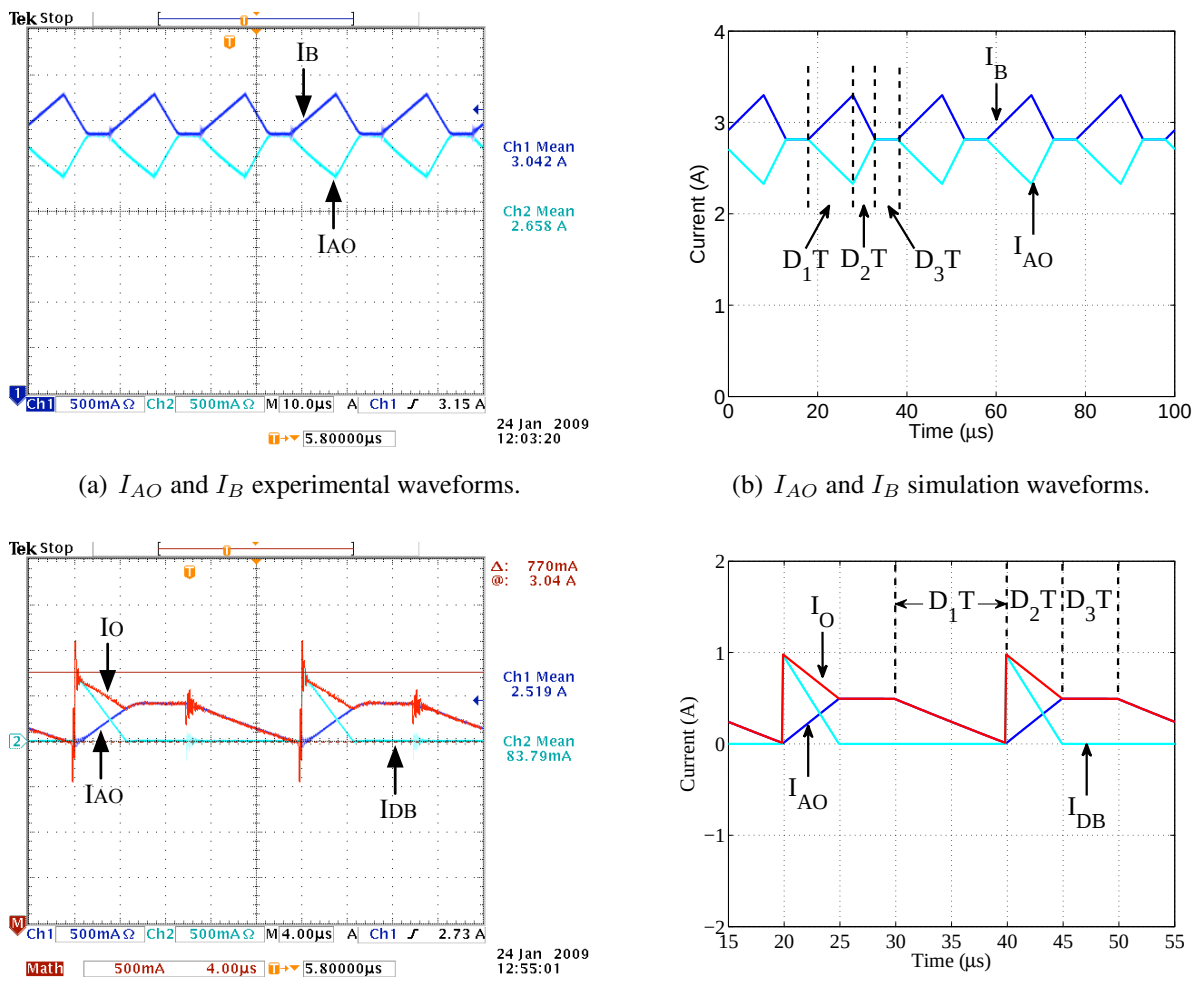
(c) I_g experimental waveform. (d) I_g simulation waveform.

In particular, Figures 12(a) and 12(b) depict the L_A and L_B currents, named I_A and I_B, where it is observed that I_A current is in CCM as previously described in (9). Similarly, I_B operates in DCM exhibiting the three operating intervals $D_1 \cdot T$, $D_2 \cdot T$ and $D_3 \cdot T$, where the AIDB converter follows the designed sequence topology 1–topology 2–topology 3.

Figures 12(c) and 12(d) show the experimental and simulated AIDB input current waveform, where the small input current ripple condition imposed in the design process is observed. Such an input current ripple has been measured by using a current-to-voltage sensor with a gain K_g = 25 mV/mA, obtaining a Δi_g = 255 mA, which represents an error of 3% over the designed input current ripple. Also, the experimental L_A and L_B current ripples were measured by using a current probe obtaining $\Delta i_A = 518\ mA$ and $\Delta i_B = 483\ mA$, which show an error of 4% in comparison with the theoretical calculations performed with Equations (42) and (43).

Figure 13 shows the discontinuous and output current waveforms obtained in the design example conditions. Figures 13(a) and 13(b) verify the analysis from Figure 5, where the three operating intervals are observed. Also, the operation condition for the third topology, where the inductors L_B and L_{AO} are in series and have equal currents according to Equation (18), is experimentally verified.

Figure 13. AIDB discontinuous and output current waveforms for $D = 0.5$.



(a) I_{AO} and I_B experimental waveforms.

(b) I_{AO} and I_B simulation waveforms.

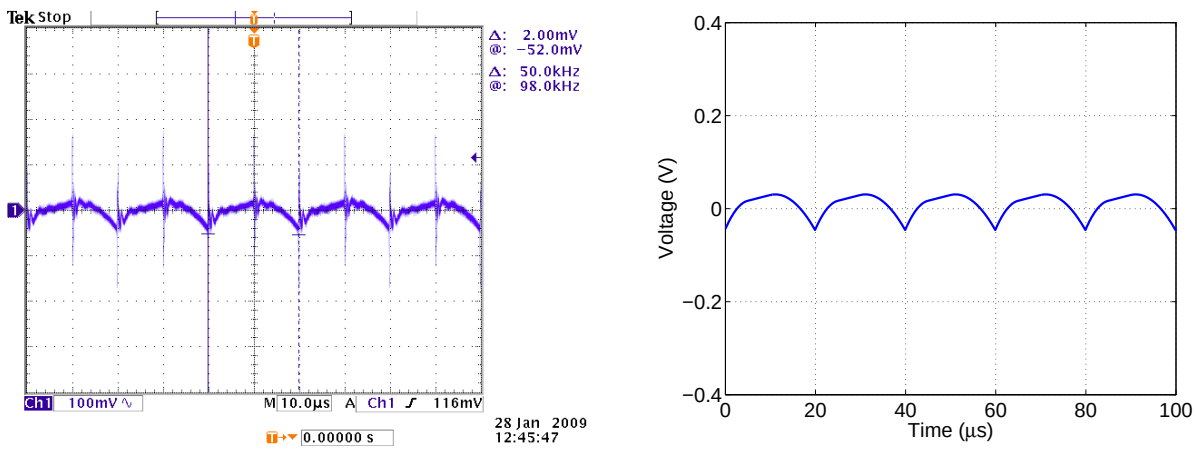
(c) I_O, I_{DB} and I_{AO} experimental waveforms.

(d) I_O, I_{DB} and I_{AO} simulation waveforms.

Similarly, Figures 13(c) and 13(d) verify the designed sequence and the diode D_B operation as described in the topologies of Figure 6. It is observed that D_B is active only in the second interval as defined in the designed sequence. The experimental results also verify that the output current is equal to L_{AO} current in the first and third topologies and equal to L_{AO} and D_B aggregated currents in the second topology, which makes evident the converter operation in the designed sequence.

Figure 14 shows the experimental and simulated output voltage waveforms, which are in agreement with the design example previously presented. The experimental output voltage ripple magnitude exhibits a 6% error over the theoretical calculations given by Equation (50).

Figure 14. AIDB output voltage waveform for $D = 0.5$.

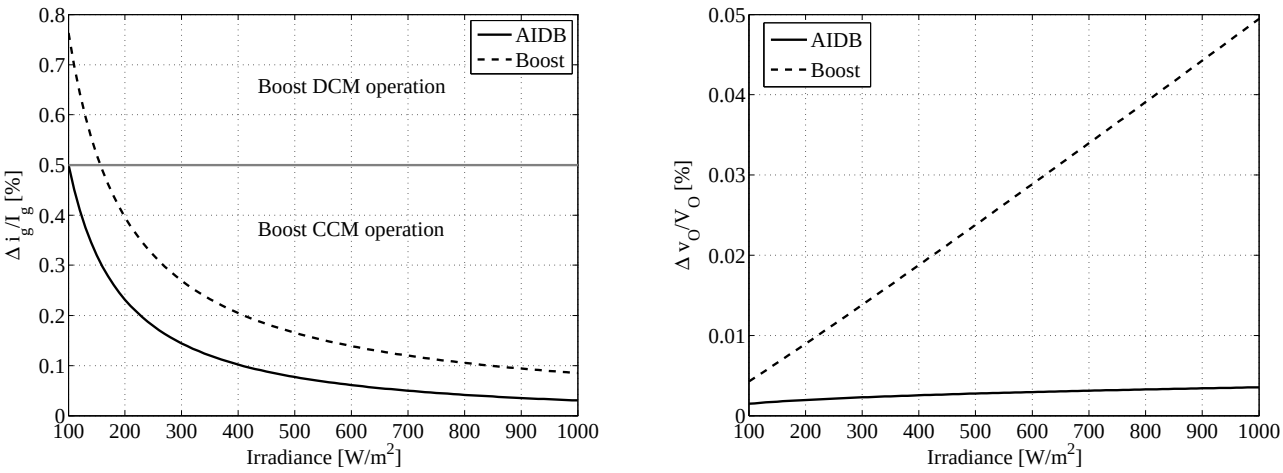


(a) V_O experimental waveform. (b) V_O simulation waveform.

The results presented in Figures 12–14, show a good correlation between experimental and simulated waveforms. In addition, the experimental results exhibit a satisfactory agreement with the design calculations, validating the design process proposed in this section.

Finally, to provide a comparison with a classical solution in the example conditions, the designed AIDB converter was contrasted with a Boost converter by means of simulations. To ensure a fair comparison, the Boost converter considers the same inductance and operating point used to design the AIDB converter. Figure 15 shows the relative ripples in contrast with I_{mpp} and V_O, *i.e.*, input current and output voltage DC components, for multiple irradiance conditions. The results confirm that the AIDB solution provides smaller ripples, which produces lower harmonic contents injected into the PV array and the load. Therefore, the proposed AIDB solution requires smaller (and cheaper) capacitors. In addition, if the irradiance decreases enough, the Boost converter enters DCM (Δi_g is peak-to-peak, hence DCM occurs for $I_g < \Delta i_g/2$) where classical predictions are not valid. Therefore, the design process proposed for the AIDB solution is more reliable than classical design procedures for a Boost solution: the AIDB design equations are valid for the whole operating range, instead the behavior of the Boost converter in DCM changes depending on the load variations, which could be difficult to predict.

Figure 15. Ripple magnitudes of AIDB and Boost converters.

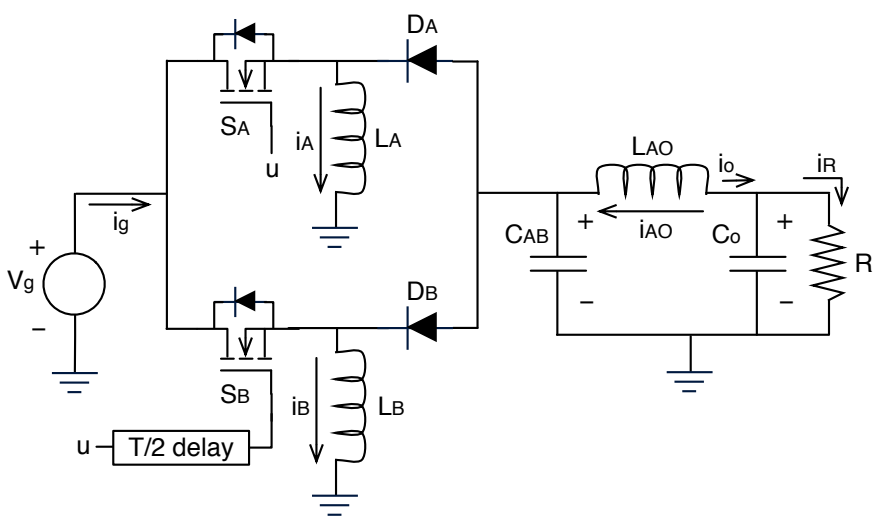


(a) Input current ripple. (b) Output voltage ripple.

4. Asymmetrical Interleaved Dual Buck-Boost (AIDBB) Converter

The application of complementary interleaving and the converter structure modifications to improve characteristics can be extended to different elementary converters to generate the AIC family, exhibiting the same AIDB characteristics: low ripple in global variables and two sequences of operation. In this way, the same circuital modification was applied to the Interleaved dual buck-boost (IDBB) converter reported in Figure 16 [35], which also considers a third-order output filter to mitigate the output voltage ripple. From such a procedure is derived the Asymmetrical interleaved dual buck-boost (AIDBB) converter, depicted in Figure 17.

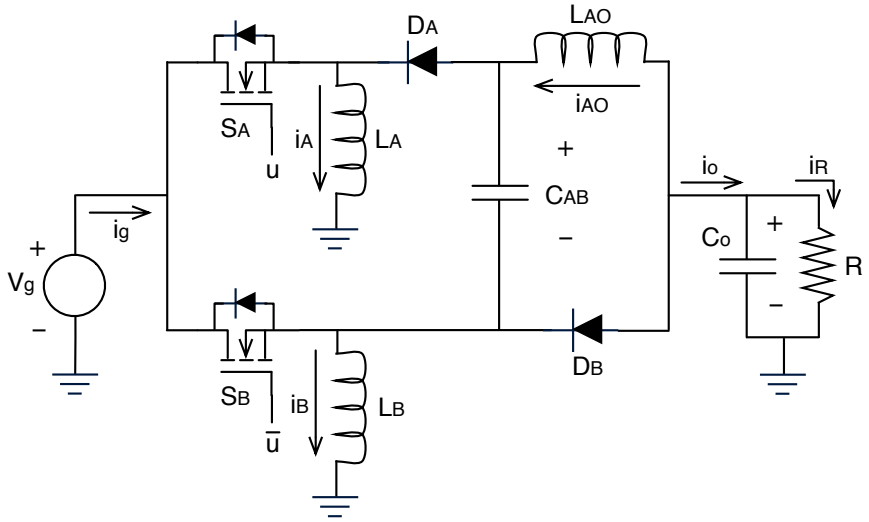
Figure 16. Circuital scheme of the IDBB converter with third-order output filter.



The topologies that take place in the AIDBB depend on the MOSFETs complementary activation and the DIODEs operation, and they are the same ones as in the AIDB. Also, similar to the AIDB, the

AIDBB exhibits the same designed sequence for duty cycles $0.382 \leq D \leq 1$, and the same undesired sequence for $0 \leq D < 0.382$.

Figure 17. Circuital scheme of the AIDBB converter.



The AIDBB input current ripple is analyzed following the same methodology used for the AIDB converter. In this way, the input current ripple in the first topology Δi_{g1} corresponds to $\Delta i_B + \Delta i_A - \Delta i_{AO}$, where Δi_B, Δi_A and Δi_{AO} represent the current ripple in inductors L_B, L_A and L_{AO}, respectively. In the second and third topologies, the input current ripples Δi_{g2} and Δi_{g3} are equal to the ripple in inductor L_A. Such a behavior can be expressed as:

$$\Delta i_{g1} = D' \cdot T \cdot \left(\frac{V_g}{L_B} + \frac{V_g - V}{L_A} + \frac{V_g}{L_{AO}} \right) \tag{55}$$

$$\Delta i_{g2} = \frac{V_g \cdot T}{L_A} \cdot (D')^2 \tag{56}$$

$$\Delta i_{g3} = \frac{V_g \cdot T}{L_A} \cdot \left(1 - D' - (D')^2\right) \tag{57}$$

Again, the input current ripple corresponds to the larger ripple in the three topologies. Adopting the design condition $L_A = L_B = L_{AO} = L$, the expression for the input current ripple in the first topology is simplified to

$$\Delta i_{g1} = D' \cdot T \cdot \frac{3V_g - V}{L} \tag{58}$$

Δi_{g1} is positive for $0.382 \leq D < 0.667$ and negative for $0.667 \leq D \leq 1$. Therefore, the input current ripple is equal to $\Delta i_{g1} + \Delta i_{g2} + \Delta i_{g3}$ for $0.382 \leq D < 0.667$ and $\Delta i_{g2} + \Delta i_{g3}$ for $0.667 \leq D \leq 1$:

$$\Delta i_g = \frac{2V_g \cdot T \cdot D'}{L} \ , \ \forall\ 0.382 \leq D < 0.667 \tag{59}$$

$$\Delta i_g = \frac{V_g \cdot T \cdot D}{L} \ , \ \forall\ 0.667 \leq D \leq 1 \tag{60}$$

Similarly, the output voltage ripple is:

$$\Delta v_o = \frac{V_g \left(D' \cdot T\right)^2}{2L_{AO} \cdot C_O} \tag{61}$$

In addition, the steady state current on L_A, L_B and L_{AO} and the steady state voltage on C_{AB} and C_O are:

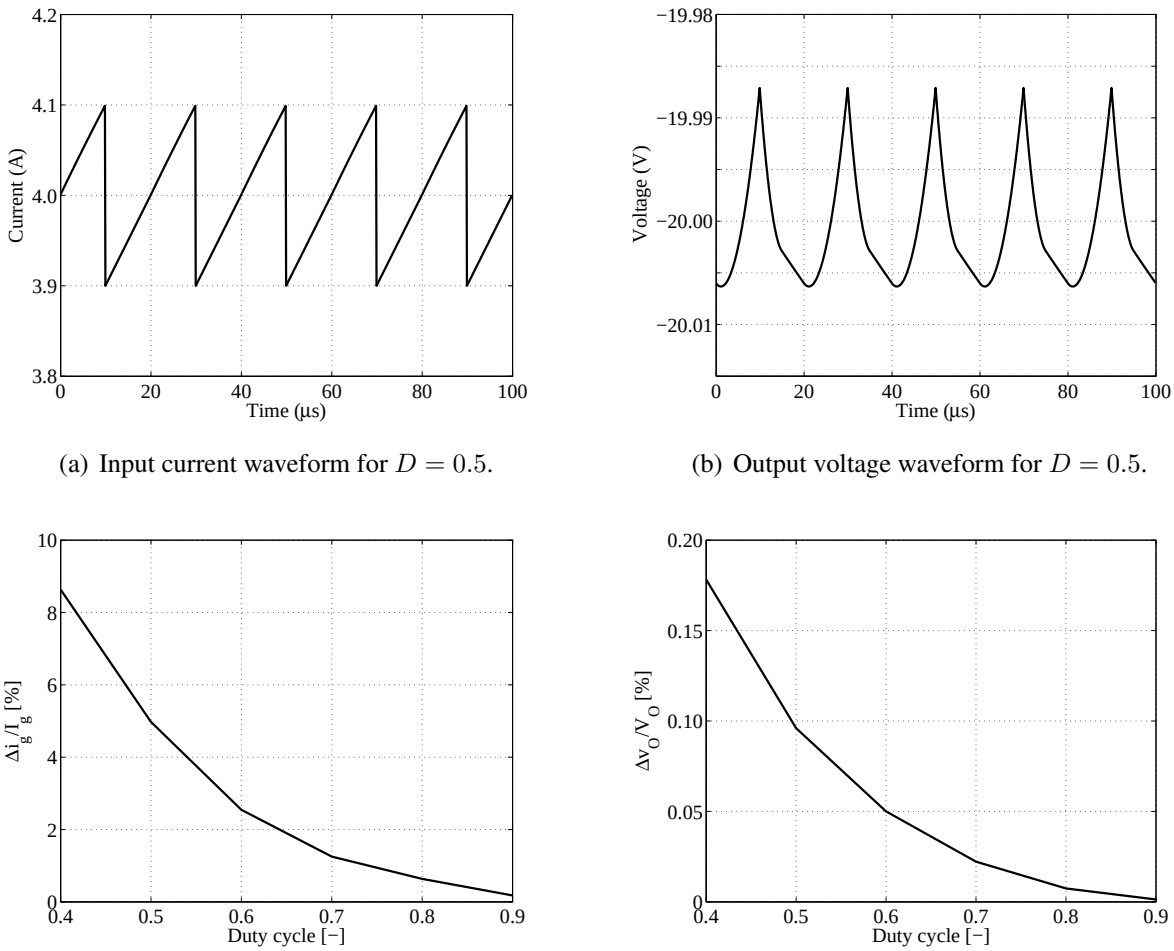
$$I_A = \frac{V_g}{R \cdot (D')^2} \tag{62}$$

$$I_B = I_{AO} = \frac{V_g}{R \cdot D'} \tag{63}$$

$$V_{AB} = V_O = -\frac{V_g}{D'} \tag{64}$$

The practical design of an AIDBB converter can be performed using the Equations (59–64) following the AIDB design process proposed in Section 3.2. Also, Equations (62) and (63) demonstrate the current sharing in a particular operating point, and similar to the AIDB case, no current control loops are required to ensure the current sharing.

Figure 18. AIDBB waveforms and ripple ratios.



(a) Input current waveform for $D = 0.5$.

(b) Output voltage waveform for $D = 0.5$.

(c) Input current ripple ratio.

(d) Output voltage ripple ratio.

An AIDBB simulation is performed using $L_A = L_B = L_{AO} = 1\ mF$, $C_{AB} = 50\ \mu$F and $C_O = 20\ \mu$F, $D = 0.5$, $V_g = 10$ V, $f_{sw} = 50$ kHz, and resistive load $R = 10\ \Omega$. Figures 18(a) and 18(b) show the input current and output voltage waveforms, respectively, where the small ripple condition is

observed. This is also evident in Figures 18(c) and 18(d), where the relative input current and output voltage ripples, both in relation with the corresponding DC values, are observed. Such simulations show the AIDBB continuous input current and output voltage waveforms, as well as input current ripples lower than 8.5% and output voltage ripples lower than 0.18% for the designed operation sequence range of $0.382 \leq D \leq 1$.

Similar to the traditional IDBB converter, the AIDBB converter provides a negative output voltage as reported in Equation (64). However, such an equation also reveals that the AIDBB converter, operating in the low ripple designed sequence, provides a voltage conversion ratio that is always greater than one. Such a limitation makes the AIDBB not useful when the voltage conversion ratio must be greater and lower than one depending on operating conditions. But as reported in Section 1, the AIC family is intended for DGS and grid-connected PV and fuel cell applications, where voltage boosting and low ripple conditions are required, which are the main characteristic of the AIDBB.

Moreover, the continuous input current of the AIDBB is a significant improvement over the discontinuous input current of the classical IDBB of Figure 16. Such a discontinuous current appears when both MOSFETs are turned off, therefore it is required to have an additional capacitor between the IDBB and the PV or fuel cell to filter the current harmonic contents.

The equivalent duty cycles of the AIDBB (D_{AIDBB}) and IDBB (D_{IDBB}) for the same voltage conversion ratio are given in Equation (66). Such a relation has been derived from the AIDBB and IDBB voltage conversion ratios given in Equations (64) and (65) [35], respectively.

$$\frac{V_O}{V_g} = \frac{D_{IDBB}}{1 - D_{IDBB}} \tag{65}$$

$$D_{IDBB} = \frac{1}{2 - D_{AIDBB}} \tag{66}$$

Equation (66) makes evident that any AIDBB duty cycle $0 < D_{AIDBB} < 1$ implies an equivalent IDBB duty cycle within $0.5 < D_{IDBB} < 1$ related by $D_{IDBB} > D_{AIDBB}$. In particular, the AIDBB duty cycle $D_{AIDBB} = 0.5$ defined in the previous example corresponds to an equivalent IDBB duty cycle $D_{IDBB} = 0.667$.

An IDBB simulation example illustrates the IDBB discontinuous input current, for the equivalent AIDBB duty cycle, using $L_A = L_B = L_{AO} = 1\ mF$, $C_{AB} = 50\ \mu$F and $C_O = 20\ \mu$F, $V_g = 10$ V, $f_{sw} = 50$ kHz, resistive load $R = 10\ \Omega$ and $D = 0.667$. Figures 19(a) and 19(b) show the waveforms of the interleaved inductor currents and the discontinuous input current waveform. In addition, Figure 19(c) shows the IDBB relative input current ripple in relation with its DC value. Contrasting such a figure with Figure 18(c), which corresponds to the AIDBB, the significant reduction of the input current ripple magnitude provided by the AIDBB is evident. Finally, Figure 19(d) reports the equivalent duty cycles of the AIDBB and IDBB converters for design purposes.

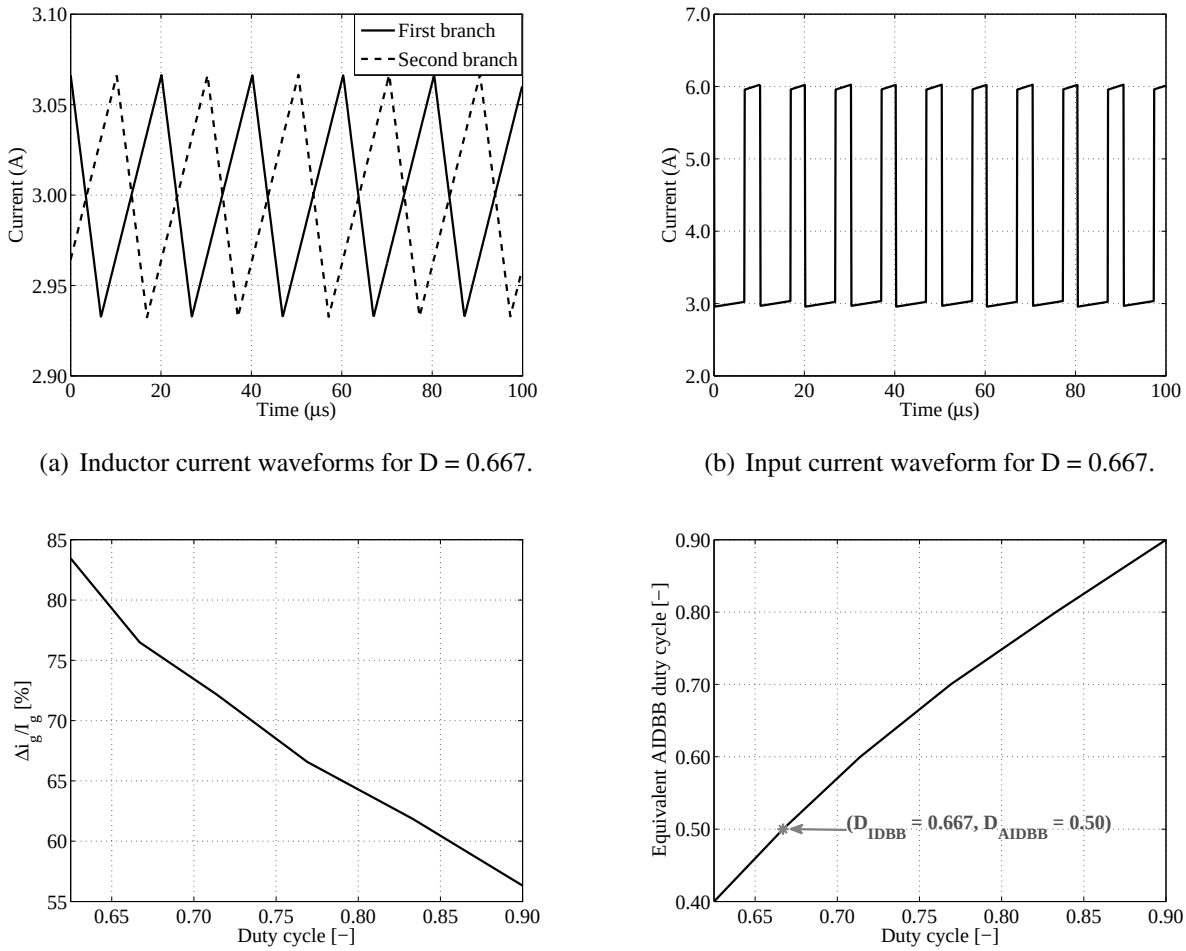
Considering an PV application, where the PV voltage ripple must be reduced to avoid power losses as described in Section 3.3, an additional filtering capacitor C_{PV} is traditionally placed between the PV module and the power converter to reduce the PV current harmonic contents. Such a capacitor, in ideal steady state conditions [26], will absorb the current ripple generated by the converter. Considering the

IDBB square-like input current waveform depicted in Figure 19(b) for D = 0.667, the voltage oscillation in C_{PV}, therefore at the PV module terminals $\Delta v_{PV_{IDBB}}$, is given by:

$$\Delta v_{PV_{IDBB}} = \frac{(0.667) \cdot \Delta i_{IDBB} \cdot T}{4 \cdot C_{PV}} \tag{67}$$

where Δi_{IDBB} represents the peak-to-peak IDBB input current ripple magnitude. This example considers a steady state PV voltage equal to 10 V, $\Delta i_{IDBB} = 3$ A from Figure 19(b), and $T = 20$ μs. To ensure a maximum PV voltage ripple of 1%, a $C_{PV} = 100$ μF is required.

Figure 19. IDBB waveforms, ripple ratios and equivalent AIDBB duty cycles.



(a) Inductor current waveforms for D = 0.667.

(b) Input current waveform for D = 0.667.

(c) Input current ripple ratio.

(d) Equivalent AIDBB duty cycles.

Similarly, considering the AIDBB triangular input current waveform depicted in Figure 18(a) for $D = 0.5$, the voltage oscillation in C_{PV} and at the PV module terminals $\Delta v_{PV_{AIDBB}}$ is given by:

$$\Delta v_{PV_{AIDBB}} = \frac{\Delta i_{AIDBB} \cdot T}{8 \cdot C_{PV}} \tag{68}$$

where Δi_{AIDBB} represents the peak-to-peak AIDBB input current ripple magnitude. The AIDBB example considers the same steady state PV voltage and switching frequency as the IDBB example, but $\Delta i_{AIDBB} = 0.2$ A from Figure 18(a). To ensure the same maximum PV voltage ripple of 1%, a

smaller $C_{PV} = 5$ μF is required. The strong reduction in the filtering capacitor required by the AIDBB is evident, which in this example is twenty times smaller than the one used for the IDBB.

In fuel cell applications, the filtering capacitor C_{FC} placed between the stack and the converter can be designed by taking into account the parallel interaction of the fuel cell steady state impedance and the capacitor impedance at the switching frequency. Considering the Nexa fuel cell steady state impedance of 268 mΩ [5], to ensure a maximum stack voltage ripple of 1% at the IDBB example voltage level, a filtering capacitor $C_{FC} = 83.6$ μF is required. In contrast, considering the AIDBB, the same maximum stack voltage ripple can be ensured without filtering capacitance. Under such voltage level and fuel cell impedance, the AIDBB will generate a maximum voltage ripple of 0.54 %. Similarly, in the PV application case, the AIDBB requirement for input filtering capacitances is smaller than in the IDBB case.

Consequently, the AIDBB is an interesting option for PV and fuel cell applications that require negative output voltages, since it exhibits a significant input current ripple reduction over the IDBB and provides higher voltage conversion ratio for the same duty cycle. In addition, the smaller input filtering requirement of the AIDBB reduces the size and weight of the final product.

5. Asymmetrical Interleaved Dual Flyback (AIDF) Converters

The Asymmetrical interleaved dual flyback (AIDF) converters are generated using the circuital modification previously presented adopting flyback transformers.

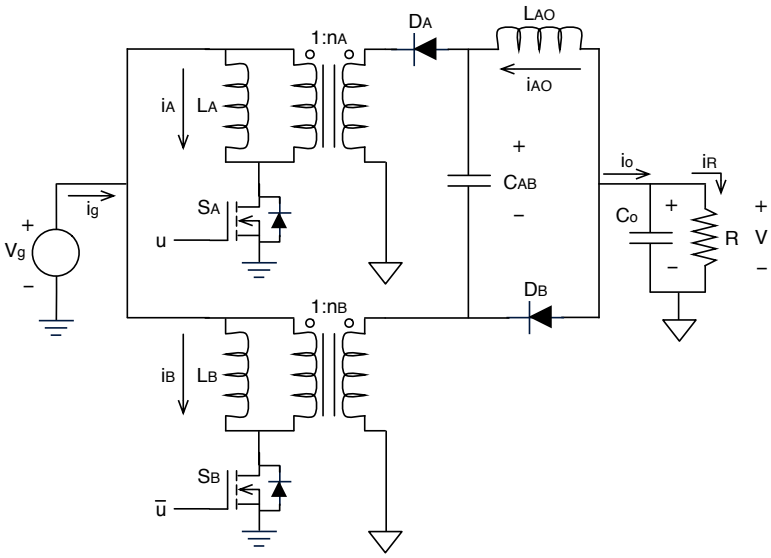
The AIDF converters have been generated from AIDBB converter by substituting the inductors with flyback transformers to obtain an improved voltage conversion ratio. Therefore, the original buck-boost structures change into flyback structures, but the resulting AIDF converters exhibit the same characteristics of the AIDBB configuration: small input current and output voltage ripples, a designed operation sequence defined by the duty cycle, and a current sharing among branches without additional control loops.

Several flyback configurations can be derived following the generation procedure, but the resulting converters will exhibit positive or negative output voltage polarity, and some of them will also provide galvanic isolation. Therefore, four configurations that provide higher voltage conversion ratios are selected to illustrate the AIDF converters: isolated inverting AIDF, isolated non-inverting AIDF, non-isolated inverting AIDF, and non-isolated non-inverting AIDF.

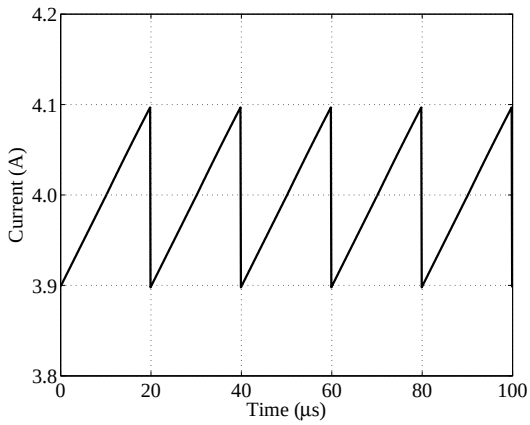
In the following, i_A and i_B represent the magnetization currents of the flyback transformers, and n_A and n_B refer to the flyback transformer turns ratio. The isolated inverting AIDF, depicted in Figure 20(a), was obtained directly from the AIDBB converter, where the voltage conversion ratio can be increased by modifying n_A and n_B. The isolated non-inverting AIDF, depicted in Figure 21(a), was generated from the isolated inverting AIDF by inverting the transformers secondary side, which causes a positive output voltage.

The non-isolated inverting AIDF of Figure 22(a) was derived from the isolated inverting AIDF by connecting the load ground to the input source, generating a floating load but breaking the galvanic isolation. This converter has a higher voltage conversion ratio, in contrast to the isolated inverting AIDF, for the same n_A and n_B.

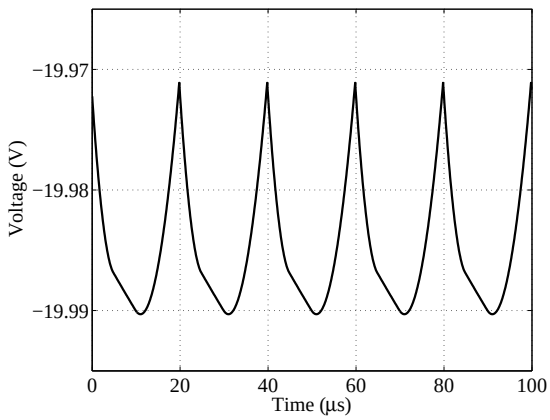
Figure 20. Isolated inverting AIDF.



(a) Circuit scheme.



(b) Input current waveform for $D = 0.5$.



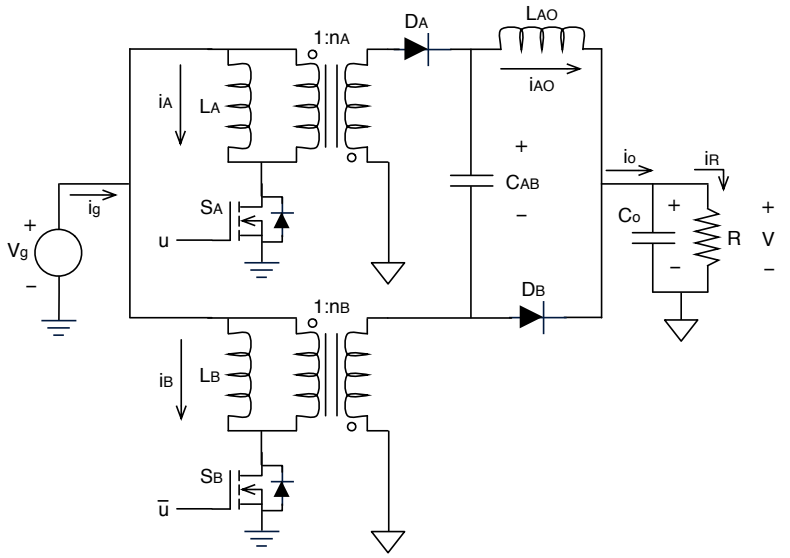
(c) Output voltage waveform for $D = 0.5$.

The non-isolated non-inverting AIDF, depicted in Figure 23(a), was generated from the isolated non-inverting AIDF by connecting the secondary side of the flyback transformers to the input source. Again, it provides an increased voltage conversion ratio with respect to the isolated non-inverting AIDF for the same transformer turns ratio, but the galvanic isolation was lost.

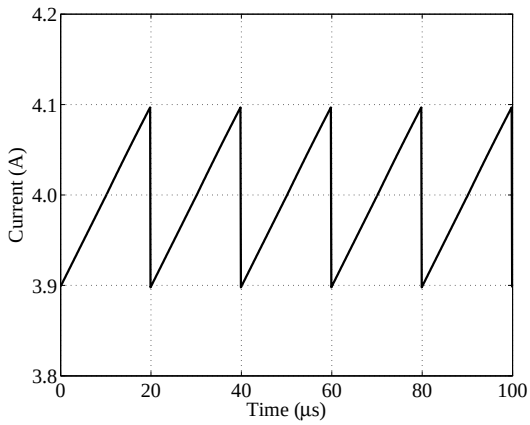
To illustrate the AIDF converter characteristics, simulations of the four configurations have been performed considering flyback transformers with $L_A = L_B = L_{AO} = 1\ mF$, $n_A = n_B = 1$, $C_{AB} = 50\ \mu$F and $C_O = 20\ \mu$F, $V_g = 10$ V, $f_{sw} = 50$ kHz, resistive load $R = 10\ \Omega$ and duty cycle $D = 0.5$.

Figures 20(b) and 20(c) show the input current and output voltage waveforms of the isolated inverting AIDF converter, where the AIC family small ripple conditions are observed. The isolated non-inverting AIDF input current and output voltage waveforms, depicted in Figures 21(b) and 21(c), exhibit the same small ripple.

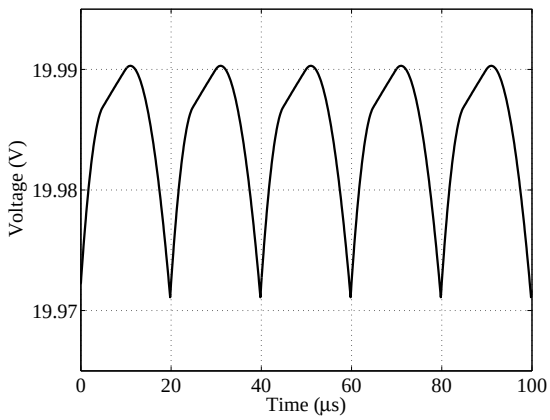
Figure 21. Isolated non-inverting AIDF.



(a) Circuit scheme.



(b) Input current waveform for $D = 0.5$.

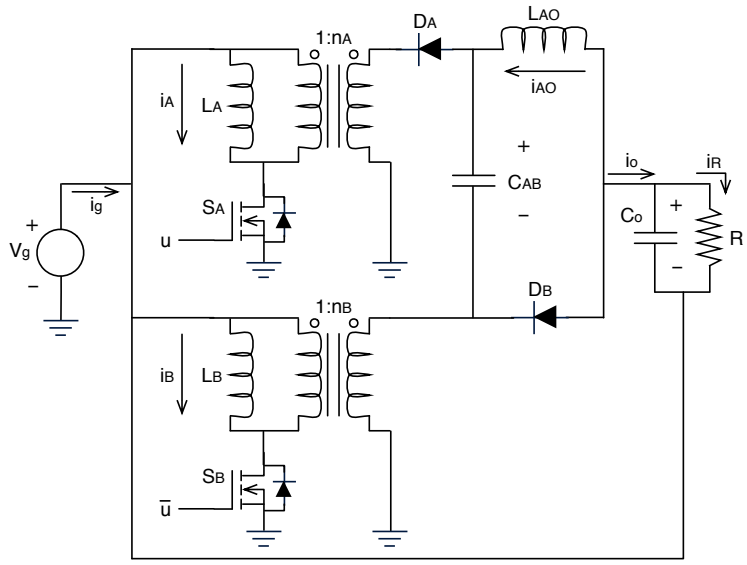


(c) Output voltage waveform for $D = 0.5$.

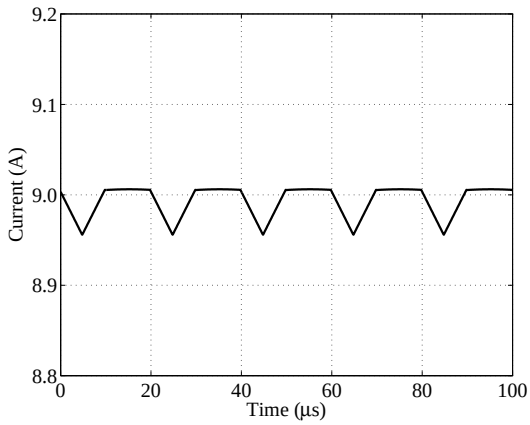
The input current and output voltage waveforms of the non-isolated inverting AIDF converter are depicted in Figures 22(b) and 22(c). This converter also exhibits the AIC family small ripples, but its voltage conversion ratio is improved due to the additional boosting generated by the floating load connection. In this non-isolated inverting AIDF, the L_{AO} current ripple is aggregated to the input current in a fraction of the switching period, generating an additional ripple mitigation that is not present in the isolated AIDF converters.

The non-isolated non-inverting AIDF converter exhibits an input current waveform, Figure 23(b), similar to the non-isolated inverting AIDF due to the connection of the transformer secondary side to the input port, allowing the interaction of the L_{AO} current ripple in a fraction of the switching period. The output voltage waveform, Figure 23(c), is in agreement with the non-isolated inverting AIDF, but its voltage polarity is positive. This non-isolated non-inverting AIDF also exhibits an increased voltage conversion ratio provided by the non-isolated interaction between the input and output ports.

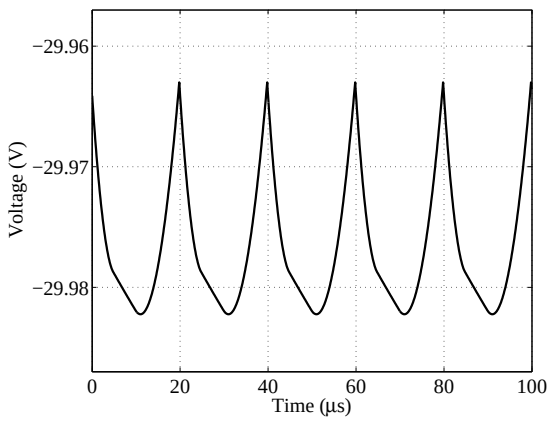
Figure 22. Non-isolated inverting AIDF.



(a) Circuit scheme.



(b) Input current waveform for D = 0.5.



(c) Output voltage waveform for D = 0.5.

The AIDF converters exhibit the same operation limit $0.382 \leq D \leq 1$ for the designed sequence, and the topologies are the same ones described for the AIDB converter. Figure 24 shows the circuital equivalents of the isolated inverting AIDF topologies. The remaining members of the AIDF group can be analyzed in a similar way.

From such topologies, and following the analytical procedure used for the AIDB converter, the steady state currents on L_A, L_B and L_{AO} and the steady state voltages on C_{AB} and C_O are respectively:

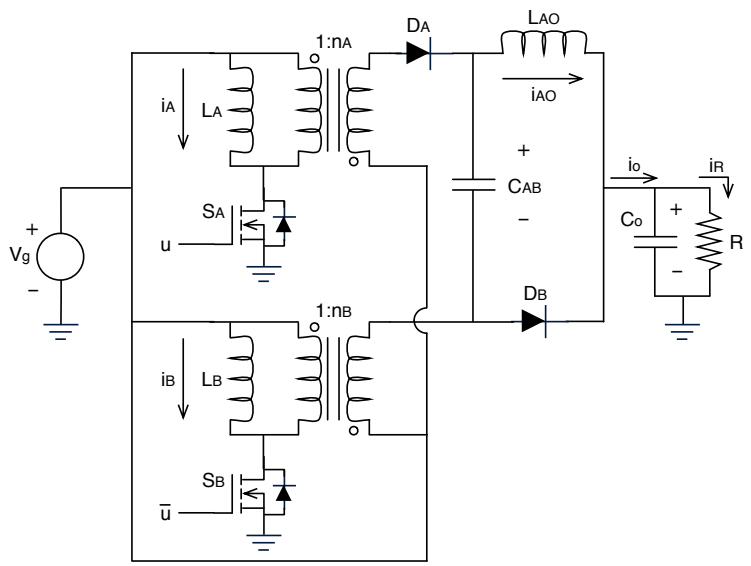
$$I_A = \frac{V_g \cdot n_A}{R \cdot (D')^2} (n_A \cdot D + n_B \cdot D') \tag{69}$$

$$I_B = \frac{V_g \cdot n_B}{R \cdot D'} (n_A \cdot D + n_B \cdot D') \tag{70}$$

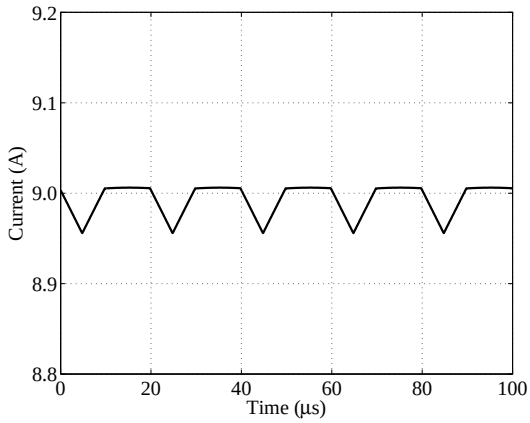
$$I_{AO} = \frac{V_g}{R \cdot D'} (n_A \cdot D + n_B \cdot D') \tag{71}$$

$$V_{AB} = V_O = -\frac{V_g}{D'} (n_A \cdot D + n_B \cdot D') \tag{72}$$

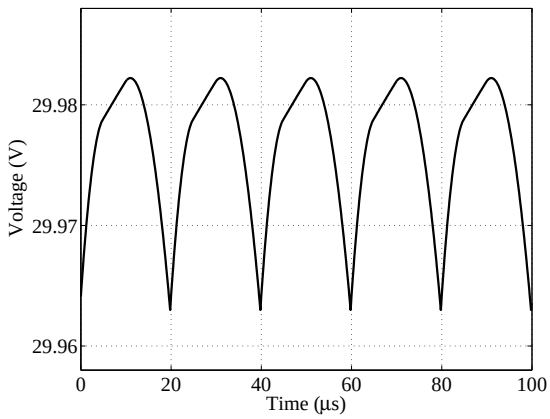
Figure 23. Non-isolated non-inverting AIDF.



(a) Circuit scheme.



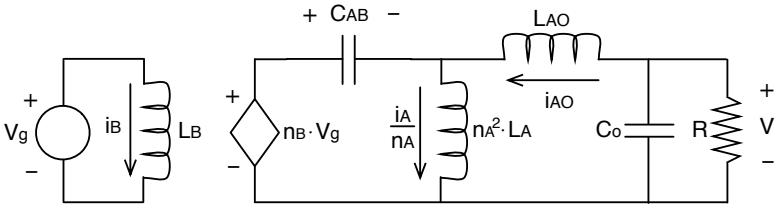
(b) Input current waveform for D = 0.5.



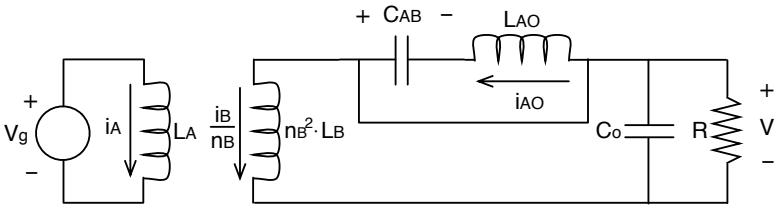
(c) Output voltage waveform for D = 0.5.

where the design criteria $L_A = L_B = L_{AO}$ have been adopted to simplify the expressions. Such equations evidently affect the transformer turns ratio. The voltage conversion ratio of this isolated inverting AIDF can be improved by asymmetrically modifying n_A and n_B, which also introduces a new degree of freedom in the I_A and I_B relation to design the current sharing in comparison with the non-flyback AIC family members. Finally, the input current and output voltage ripple magnitudes of this converter are the same ones exhibited by the AIDBB converter in Equations (59–61).

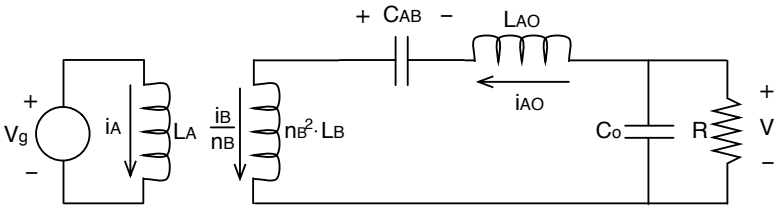
Figure 24. Isolated inverting AIDF topologies.



(a) Topology 1: $d' = d_1$.



(b) Topology 2: d_2.



(c) Topology 3: d_3.

To illustrate the AIDF converters voltage conversion ratio and input current, the following design criteria were adopted: $L_A = L_B = L_{AO}$ and $n_A = n_B = n$. The input current and output voltage steady state values for the isolated inverting AIDF ($V_{O,II}$ and $I_{g,II}$), isolated non-inverting AIDF ($V_{O,IN}$ and $I_{g,IN}$), non-isolated inverting AIDF ($V_{O,NI}$ and $I_{g,NI}$), and non-isolated non-inverting AIDF ($V_{O,NN}$ and $I_{g,NN}$), are given by:

$$V_{O,II} = -V_{O,IN} = -\frac{V_g \cdot n}{D'} \tag{73}$$

$$I_{O,II} = I_{O,IN} = \frac{V_g \cdot n}{R \cdot D'}\left(\frac{n}{D'} + n - 1\right) \tag{74}$$

$$V_{O,NI} = -V_{O,NN} = -V_g\left(\frac{n}{D'} + 1\right) \tag{75}$$

$$I_{O,NI} = I_{O,NN} = \frac{V_g}{R}\left(\frac{n}{D'} + 1\right)^2 \tag{76}$$

From Equation (73) it is noted that both isolated AIDF converters provide the same voltage conversion ratio but with opposite sign. Such a voltage conversion ratio is an improved version of the AIDBB one, since the transformer turns ratio allows to increase it. In addition, those converters provide galvanic isolation, which is required in some PV grid-connected applications [36].

Similarly, both non-isolated AIDF converters exhibit the same voltage conversion ratio but with opposite sign as reported in Equation (75). These types of AIDF converters do not provide galvanic isolation, but their voltage conversion ratio is increased over the isolated AIDF converters by the

factor $n/(n+D')$, which implies that the same output voltage can be achieved with smaller flyback transformers for the same operation conditions. Therefore, the final product will exhibit a smaller size.

6. Conclusions

An asymmetrical interleaved converter family intended for photovoltaic and fuel cell applications has been presented and analyzed. This family was developed by applying circuit structure modification with the fundamental idea of breaking the symmetry of traditional interleaved converters.

The proposed AIC family exhibits two different operating modes depending on the duty cycle. For duty cycles higher than 0.382, the converters operate on the designed topologies sequence, providing reduced input current and output voltage ripples. For duty cycles lower than 0.382, the converters enter the undesired operation sequence that generates high ripple conditions. In general, the designed sequence is characterized by a DCM condition generated by diode D_B, while the undesired sequence is characterized by a DCM condition generated by diode D_A. Such a behavior means that the AIC family inherently operates in DCM, which in addition causes the input current sharing among the parallelized branches without any specific control strategy. Compared with conventional interleaved converters, this characteristic simplifies the regulation strategy required for the AIC family, which in addition provides a higher voltage conversion ratio compared with traditional interleaved converters for the same duty cycle. Those features make the AIC family ideal for photovoltaic maximum power point tracking by perturbing directly the converter duty cycle, and also to interface fuel cells by controlling the overall input current or output voltage without any internal current control loop for each branch.

Another interesting characteristic of the AIC family concerns its reduced input current and output voltage ripple magnitudes for all the family members, which is especially important for photovoltaic and fuel cell applications. Also, the duration of the operation intervals in steady state does not depend on the circuit or load parameters as in the DCM operation of common converters, therefore an accurate design can be easily performed for non-constant load conditions using the equations provided in this paper. Such features were verified by the experimental results obtained with an AIDB converter prototype.
The AIDB converter design process for photovoltaic and fuel cell applications has been also presented. Such a procedure was based on typical application requirements. A practical example concerning a realistic photovoltaic application was developed to illustrate the design process, validating its results by means of experimental measurements. Such a design method is also applicable to all AIC family members by using the proper equations given in the corresponding sections.

The AIC family consists of the AIDB, AIDBB and AIDF converters. The first one provides a high voltage conversion ratio and small input current and output voltage ripples. Therefore, it is ideal for classical PV and fuel cell applications that require positive output voltage with reference to the input port. The second one, AIDBB, provides the same characteristics but with an opposite sign of the output voltage, hence it is ideal for PV or fuel cell applications that require such a condition.

The third type of converter, AIDF, exhibits a high voltage conversion ratio, which can be further increased by selecting a proper flyback transformer turns ratios. The AIDF group mainly consists of four configurations: the isolated inverting AIDF, the isolated non-inverting AIDF, the non-isolated inverting AIDF and the non-isolated non-inverting AIDF. The isolated configurations provide galvanic isolation, which is required by different PV or fuel cell applications. The non-isolated versions exhibit higher

voltage conversion ratios than the isolated ones, but do not provide galvanic isolation. Therefore, the AIDF converters are useful for a wide range of applications where transformers are accepted, and for transformerless applications, the AIDB and AIDBB converters provide similar features.

Finally, due to its asymmetrical structure and inherent DCM operation, the AIC family requires a new modeling technique to calculate its small-signal transfer functions for control purposes. Moreover, taking into account that the duty cycles D on the AIC family are restricted to $D > 0.382$, a proper control scheme must be designed: for example, a classical non-linear limiter on D could be adopted, or a compensation ramp could be introduced to ensure the operation at the designed sequence in the same way that classical current-programmed controllers ensure $D < 0.5$ to guarantee stability [26]. Such topics will be addressed in a second paper.

Acknowledgments

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