

Article

An Examination of AC/HVDC Power Circuits for Interconnecting Bulk Wind Generation with the Electric Grid

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Abstract: The application of high voltage dc (HVDC) transmission for integrating large scale and/or off-shore wind generation systems with the electric grid is attractive in comparison to extra high voltage (EHV) ac transmission due to a variety of reasons. While the technology of classical current sourced converters (CSC) using thyristors is well established for realization of large HVDC systems, the technology of voltage sourced converters (VSC) is emerging to be an alternative approach, particularly suitable for multi-terminal interconnections. More recently, a more modular scheme that may be termed ‘bridge of bridge’ converters (BoBC) has been introduced to realize HVDC systems. While all these three approaches are functionally capable of realizing HVDC systems, the converter power circuit design trade-offs between these alternatives are not readily apparent. This paper presents an examination of these topologies from the point of view of power semiconductor requirements, reactive component requirements, operating losses, fault tolerance, multi-terminal operation, modularity, complexity, *etc.* Detailed analytical models will be used along with a benchmark application to develop a comparative evaluation of the alternatives that maybe used by wind energy/bulk transmission developers for performing engineering trade-off studies.

Keywords: bulk transmission; HVDC; multi-terminal; offshore; wind farm; VSC; CSC; modular multilevel converter

Nomenclature

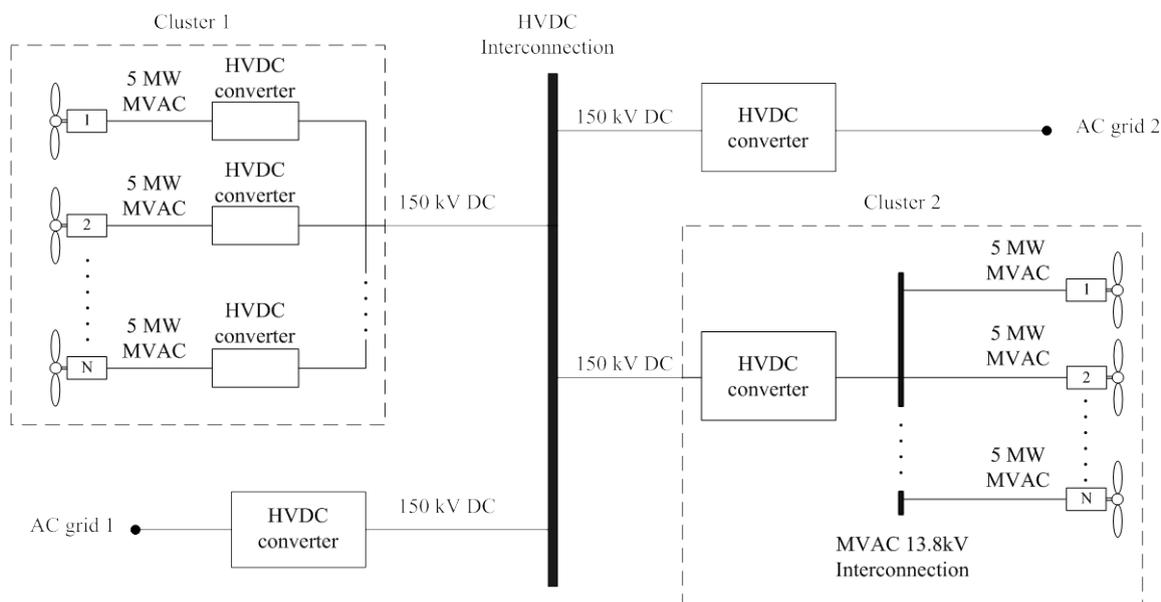
V_S	Source rms phase voltage, [kV]
V_{ph}	converter rms phase voltage, [kV]
V_{dc}	HVDC output voltage, [kV]
V_{Csm}	BoBC sub-module dc bus voltage [kV]
V_{sm}	BoBC sub-module output voltage [kV]
V_{ca}	Thyristor cathode-anode voltage [kV]
V_{ce}	IGBT collected-emitter voltage [kV]
$V_{ca i}$	IGCT cathode-anode voltage [kV]
Q_{tran}	CSC & VSC transformer turns ratio
Q_{bobc}	BoBC apparent transformer turns ratio
α	CSC thyristor firing angle
m	VSC modulation index
d_{sm}	BoBC sub-module duty cycle
I_S	Source rms phase current, [A]
I_{ph}	Converter rms phase current, [A]
I_{dc}	HVDC output current, [A]
I_{arm}	Converter rms arm current, [A]
i_{cv-rms}	VSC rms capacitor current, [A]
i_{cb-rms}	BoBC rms capacitor current, [A]
C_{vsc}	VSC dc bus capacitance, [μ F]
C_{sm}	BoBC sub-module capacitance, [μ F]
L_{csc}	CSC HVDC line inductance, [H]
L_{sm}	BoBC sub-module inductance, [μ H]
L_{arm}	BoBC arm inductance, [μ H]
N_{csc}	Number of sub-modules, CSC
N_{vsc}	Number of sub-modules, VSC
N_{bobc}	Number of sub-modules, BoBC
f_{sw}	Switching frequency
f_p	Power frequency
N_{pulse}	Lowest harmonic pulse number

1. Introduction

Increasing share of wind energy systems has prompted a concomitant attention to their integration into major electrical transmission systems, *i.e.*, the grid. Particularly, the promise for large scale generation in offshore and remote locations due to the meteorological consistency of the wind in such locations make bulk power transmission from generation centers to load locations a critical aspect of the emerging future. Despite this promise, the issue of wind turbine interconnection and bulk power transmission to the existing distribution networks has not yet been solved with certainty. High voltage direct current (HVDC) systems have been proposed by numerous authors [1–10] as a solution for integrating renewable and existing sources of energy together in configuration similar to Figure 1. Here, several power converters are used to interface multiple generation sources and load locations in a multi-terminal HVDC interconnection with power converters that may be integrated with each turbine (Cluster 1), or integrated with a group of turbines (Cluster 2). The subject of this paper is an examination of alternative power converter topologies that may be applied in the HVDC

interconnection in a centralized configuration as in Cluster 2, although the results may be extended to their application in a distributed configuration as in Cluster 1.

Figure 1. A simplified single line diagram of a sample HVDC interconnection of wind generation sources and ac grids.



Although the HVDC power converters may generally be used in either sending or receiving mode, this paper will concentrate on sending power from a generation source using one of the two canonical power converter topologies, current sourced converters (CSCs) or voltage sourced converters (VSCs). In general VSC technologies appear to be favored against the CSC to realize future HVDC installations for a variety of reasons. But a more critical analysis is necessary to establish this generalization in a definitive manner. Additionally, a new HVDC power conversion approach has recently emerged which can be potentially transformerless and utilizes a modular multi-level converter (MMLC). This converter belongs to the aptly named “bridge of bridge” converter (BoBC) family, and holds promise to be a competitive solution in the future of HVDC [11–13]. The performance trade-offs between the three types of converters have not been definitively presented in the literature, particularly in view of the application to bulk power transmission in regard to utility integration of wind power.

To be sure, a comparative evaluation of particular solutions for a given application may be made on the basis of several features. Salient power circuit features include: harmonics of waveforms, operating losses, ratings of power converters, reactive component requirements, transformer kVA requirements, and complexity of control. Given the degree of variability based on the application a definitive evaluation appears to be a formidable task. Therefore, in order to maintain a focus in the evaluation, a particular benchmark application is considered in this paper. Furthermore, the evaluation is limited to solutions that feature superior waveform quality arising from high frequency or high pulse number switching with nearly sinusoidal line current waveforms.

A focused analytical modeling and design study of a candidate application using the different approaches is performed in order to evaluate their performance. The comparison criteria used for the

evaluation include voltage, current and power throughput ratings of the main power circuit components (including transformers, capacitors, and semiconductors), quality of terminal voltage and current waveforms in terms of harmonics, and losses in power semiconductors. Although the trade-offs of complete systems using these alternative approaches may be a complex function of market trends, economic factors and engineering development, and would change considerably with respect to time and location, a preliminary estimate of these metrics together provide a basis for making a first order trade-off among these approaches.

In today's state of the art, doubly fed induction generators operating in the low voltage regime (480/690 V) are most commonly used to realize wind turbine installations. As turbine power levels steadily increase into the 5 MW+ levels, low voltage machine designs become impractical from an efficiency perspective [14]. Following this trend, wind turbine manufacturers may be expected to migrate to medium voltage generators that may be tied to the electric grid via a single power converter. The focus of this paper is to call attention to the properties of the CSC, VSC, and BoBC and compare them in a benchmark application in following this trend.

A brief background discussion of each converter is provided in Section 2 and a detailed comparison including a benchmark design follows in Section 3. Section 4 provides a summary of the conclusions.

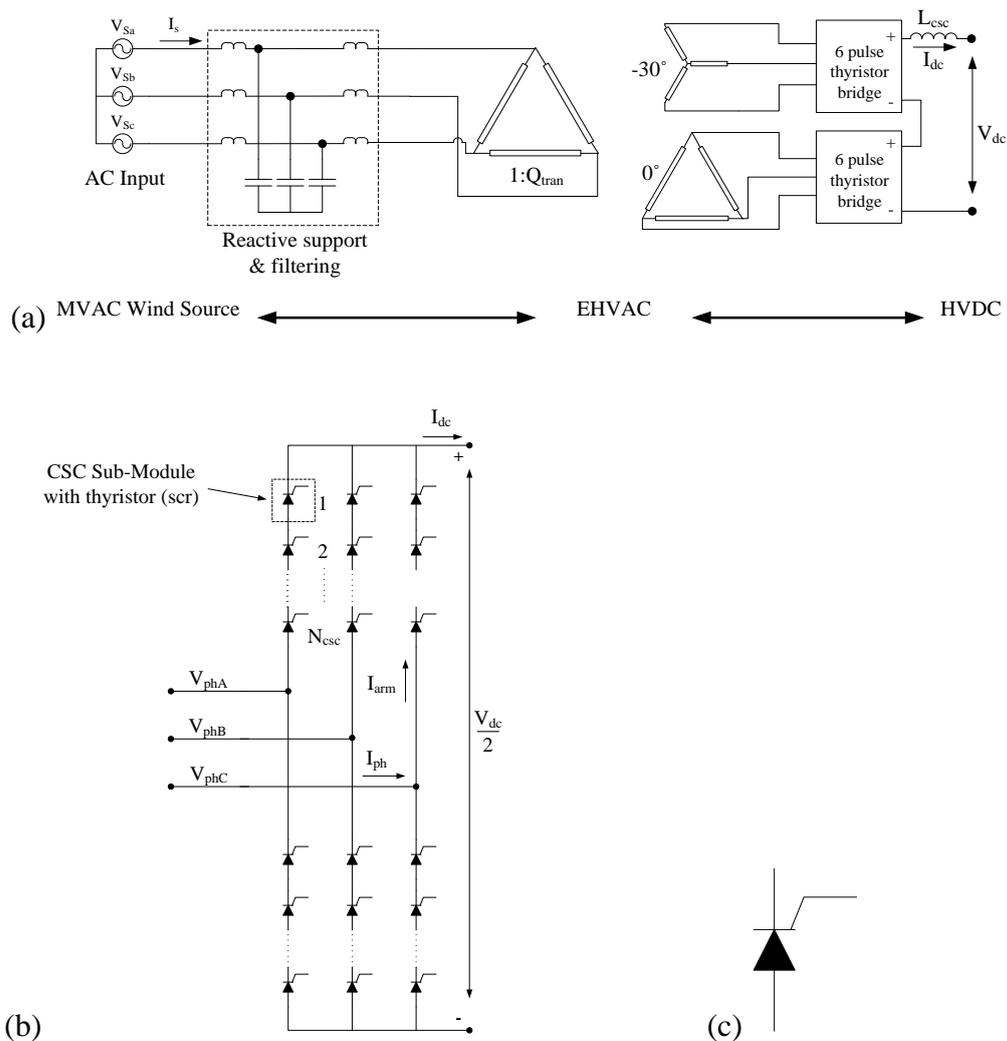
2. HVDC Converter Topologies, a Brief Review

This section introduces each of the three converter topologies in consideration and provides a background overview on their operation. Common topologies for each converter as well as operating characteristics are provided. These characteristics are explored further and compared in Section 3. While the review here is brief, and focuses on the salient features from the view of a comparative evaluation, a more detailed discussion on functioning installations of these representative technologies may be found elsewhere [12]. Notably, for a more comprehensive discussion on CSCs in wind applications, the readers may refer to recent works [15–21]. Similarly, a detailed discussion on the operational features of VSCs in wind generation applications may be found in [8,20–28], while a description and operational features of the BoBC/MMLCs may be found in [13,29–35].

2.1. Current Sourced Converter (CSC)

Since its inception in the 1950's the current sourced converter (CSC) has been the workhorse of HVDC transmission systems. Despite a gradual evolution of valve designs and harmonic suppression techniques, the conversion process has remained unchanged. Generation voltage is increased with a step-up transformer operating at the power frequency and rectified to feed a current stiff dc bus as shown in Figure 2(a), consisting of 6-pulse CSCs. In order to maintain the comparative evaluation to be of reasonable complexity while preserving the essential structural elements, the CSC illustration shown in Figure 2(a), along with sub-module realization Figure 2(b) is considered in this study. The results may be suitably modified to study alternative realizations if desired.

Figure 2. (a) Simplified schematic of the typical 12-pulse CSC implementation for HVDC (b) a 6 pulse thyristor bridge (c) thyristor (SCR) sub-module.



To improve system harmonics CSCs typically use transformers with multiple secondary windings phase shifted from one another to drive independent thyristor bridges. A series or parallel connection of the 6-pulse thyristor bridges results in a higher pulse frequency converter for enhanced performance. Although thyristor bridges with any sextuplet number of pulses can be realized in this fashion, 12-pulse systems are most common as illustrated in Figure 2.

The switching device of each of the six arms of the rectifier bridge is made up of N sub-modules connected in series to obtain the desired voltage blocking rating. Each sub-module contains a single semiconductor switch, usually a thyristor or an SCR. The rectified output is filtered using an inductor, which may be a discrete component or the transmission line’s inherent inductance, which gives the converter its “current stiff” property. Current stiffness combined with phase controlled rectification make the CSC robust against HVDC line faults. The output voltage is determined by the firing angle of the thyristors and the maximum value of the average rectified phase voltage as defined in Equation (2.1) (All nomenclature is listed in APPENDIX I).

$$V_{dc} = V_{ph} \frac{3\sqrt{6}}{\pi} \cos(\alpha) \tag{2.1}$$

Although the CSC is capable of bidirectional power flow, this requires a voltage reversal at the dc terminals when the bridges are realized with thyristors that conduct current in one direction. In practice, bi-directional power flow for CSCs may be achieved by advancing the firing angle to reverse polarity of the output voltage while maintaining current direction thus reversing power flow. However, one should exercise caution in relying on this technique in multi-terminal networks, a simple voltage reversal of the dc terminals alone may not fulfill all the requirements of power flow management across each of the terminals.

2.2. Voltage Sourced Converter (VSC)

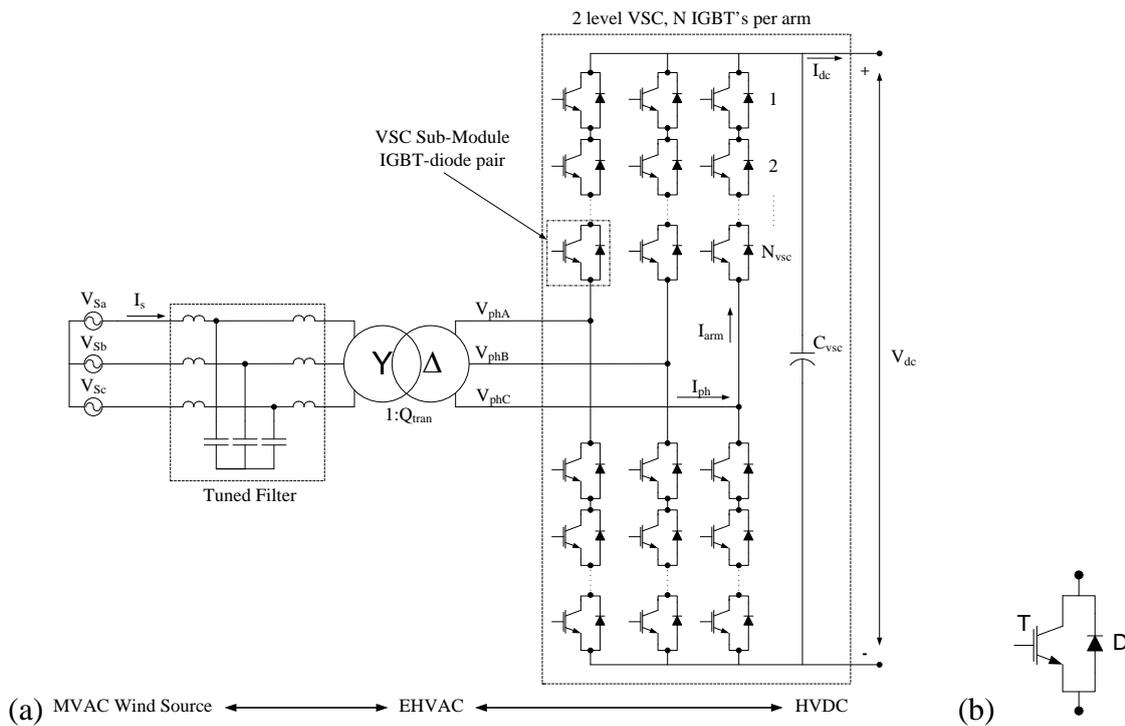
With the advances in fully controlled semiconductor switches in the last two decades, the voltage sourced converter (VSC) has become the cornerstone for industrial power conversion, while emerging as a viable option for HVDC realization. There are many different types of VSCs, such as the 2-level, neutral point clamped (NPC), and multilevel converter (MLC). Among these, the classical 2-level converter is most commonly considered for HVDC installations today [12]. Therefore, the 2-level topology will serve as the benchmark VSC for the evaluation presented in this paper and a typical configuration is illustrated in Figure 3.

Like the CSC, the VSC has six arms consisting of series connected sub-modules. However, these sub-modules differ from those of the CSC because they are realizing using fully controlled switches (e-g IGBTs) accompanied by an anti-parallel diode. The fully controlled switch and diode allow for bi-directional current flow. This added flexibility allows the VSC to operate in all four quadrants making the control of real and reactive power possible. By actively controlling the rectifier unity power factor operation can be achieved and the use of pulse width modulation (PWM) for waveform synthesis minimizes filter size on both the ac and dc sides of the converter. Although less common due to their relatively high switching frequency, it is possible to connect VSCs in a multi-pulse configuration for increased performance. The VSC phase voltage may be expressed analytically by means of a dc voltage, modulation index (m) and an averaged time-varying modulating function as described in (2.2). The modulation index m is typically limited to be under unity and is often determined in conjunction with PWM techniques such as sine-triangle comparison or space vector modulation.

$$V_{ph}(t) = V_{dc} m \cos(\omega_p t) \quad (2.2)$$

The VSC is the dual of the CSC and uses a dc bus capacitor at the dc output terminals to provide a stiff dc voltage instead of a stiff dc current. This trait lends itself well to multi-terminal operation as many converters may connect in parallel to the dc bus with ease. The drawback is that during short circuit faults, the energy stored in the dc bus capacitance feeds the fault in an uncontrolled manner.

Figure 3. (a) Simplified schematic of a 2-level voltage sourced converter HVDC implementation, (b) IGBT-diode Sub-Module.



2.3. Bridge of Bridge Converter (BoBC)

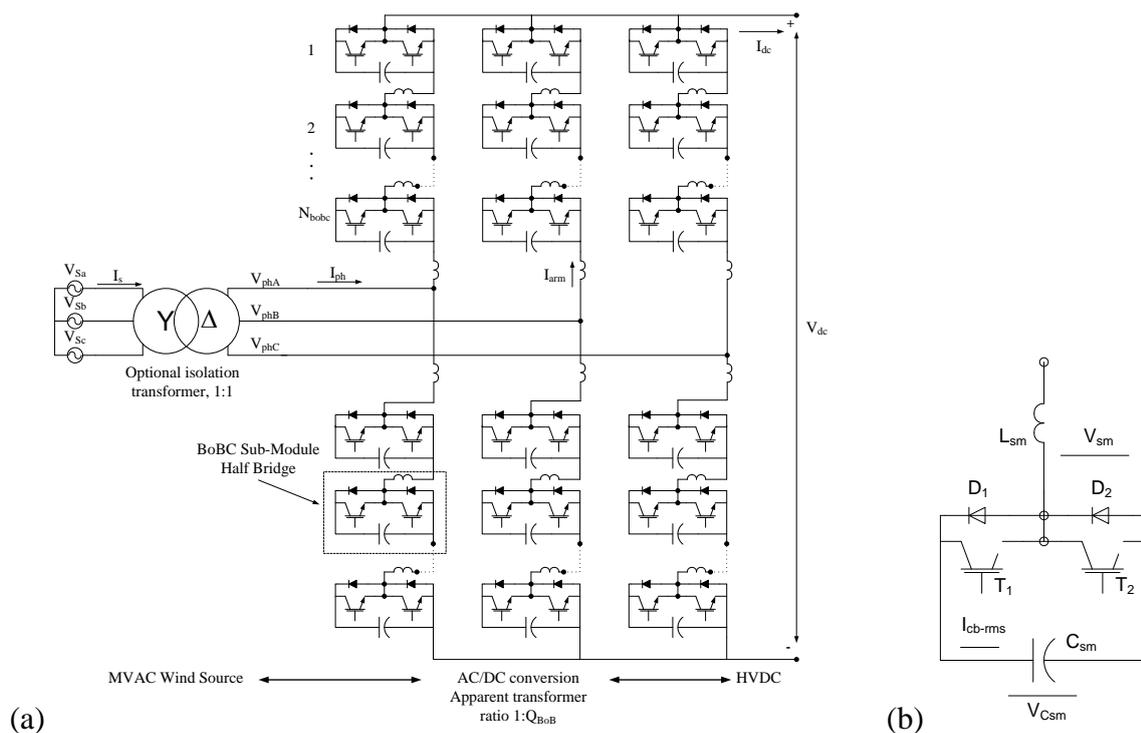
Similar to the previous two converter topologies, the BoBC also has six arms with sub-modules connected in series to realize high voltage operation. However, in this case, the sub-modules consist of power converter bridges in themselves. The BoBC or MMLC suitable for HVDC power conversion realized using individual half bridges in each sub-module is illustrated in Figure 4. These sub-modules are stand-alone power converters and any number of them may be connected in series to realize a desired voltage rating or power level. Rather than using PWM like the VSC, the BoBC may also use discrete voltage steps build waveforms which promises lower harmonic content and switching losses [13]. This characteristic also allows for the elimination of the EHV transformer, which the CSC and two-level VSC require for providing appropriate voltage matching.

While the control of the BoBC may appear to be cumbersome at the outset, the solution is relatively straight forward. Using an averaged circuit model [29], the open loop duty cycle for an arm sub-module may be calculated as (2.2).

$$d_{sm}(t) = \frac{V_{dc}/2 - V_{ph}(t)}{N_{bobc} V_{Csm}} \tag{2.3}$$

The first field application of the BoBC approach is expected to be the Trans Bay Cable project to be commissioned in 2010 under the product name *Siemens HVDC Plus* [11].

Figure 4. (a) Simplified BoBC schematic for HVDC realization (b) Simplified BoBC sub-module schematic, half bridge configuration.



3. Converter Comparison

In order to perform a comparative evaluation, the essential power circuit properties of each of the three topologies need to be related to design choices and operational variables. In the following sections, design considerations regarding semiconductor requirements, reactive component requirements & waveform quality, operating losses, multi-terminal operation, fault tolerance, and modularity/integration are discussed. An appropriate analytical model for each converter is used to identify the key design variables. A benchmark converter rating at 50 MW (base power) throughput at 150 kV (base dc voltage) from a 13.8 kV (base ac voltage) ac input is used for numerical comparison of the design variables.

3.1. Power Semiconductor Requirements

The choice of power semiconductors is perhaps the most critical design aspect in realizing any power converter topology in order to ensure efficient and reliable operation. When selecting a power semiconductor, factors such as device controllability, switching frequency capability, blocking voltage, and average current rating all factor into the design. This section delves into the device characteristics from a general and benchmark application perspective.

It is important to note that in Figures 2 and 3 the CSC and the VSC are shown with N switching device sub-modules connected in series in order to share the blocking voltage with no external components. In reality, RC networks are incorporated in parallel across each device to ensure equal voltage sharing during static and dynamic conditions [36]. On the other hand, the BoBC does not require any voltage sharing RC networks across individual devices because the maximum voltage

across the devices is defined by the dc bus voltage of each sub-module. This bus voltage may be actively regulated through appropriate control to ensure equal voltage sharing between all sub-modules without external RC networks and is discussed in [32].

In order to keep the number of sub-modules within each converter to a reasonable number, semiconductor devices of the highest possible voltage rating must be used. This is especially true for the CSC and VSC, as it is important to minimize the number of external voltage balancing RC networks. There are several types of semiconductor devices, which can operate at the kilovolt range, namely thyristors (SCRs), gate turn-off thyristors (GTOs), integrated-gate commutated thyristors (IGCTs), and insulated gate bipolar transistors (IGBTs). All of these devices, with the exception of SCRs, have a fully controllable turn-on and turn-off capability and do not require snubbers during turn off events. However due to the regenerative means that govern the turn-on process in the thyristor family of devices, a di/dt limiting reactor must be included in such designs that use the thyristor family in VSC applications. This further complicates matters as energy is stored in the limiting reactor during the on-state and must be diverted during the subsequent turn-off event. This is usually accomplished with a pole clamp and is discussed in great detail in [37]. IGBTs do not share the same regenerative turn-on process of thyristors; hence do not require external reactors to facilitate safe turn-on.

Switching frequency limitations and packaging also factor into device selection. The thyristor family comprising SCRs, GTOs, and IGCTs has an upper switching frequency limit on the order of 500 Hz. These devices are manufactured in a press-pack configuration making them ideal for low frequency series-stacking applications. On the other hand, IGBTs may switch in the multi-kHz regime, often >40 times the line frequency sufficient to maintain adequate waveform quality in utility applications. In addition to a controllable turn off, IGCTs and IGBTs are available with integrated anti-parallel diodes for two quadrant current conduction.

Having discussed the basic semiconductor performance and integration characteristics, the requirements of the three converter topologies must be matched to the appropriate semiconductor device. A CSC sub-module switches at the line frequency and does not require a controllable turn-off in most cases. This makes the thyristor family ideal for CSC realization, particularly SCRs, due to their line commutation turn off, series stacking capability, and relatively lower cost. Contrary to the CSC, VSC sub-modules require two quadrant switching at high frequency. Due to these requirements the only realistic option for the VSC are IGBTs, because the switching frequency must be sufficiently high (typically $40f_p$) for practical reactive component design such as the dc link capacitance and line filters. Furthermore, most IGBT packs have an anti-parallel diode integrated into the planar module making their implementation simpler. Unlike the CSC or the VSC, whose N series devices must switch simultaneously, the BoBC may stagger the switching amongst the sub-modules allowing each sub-module to switch at a lower frequency, typically on the order of $3f_p$ [13]. Congruence of maintaining switching signals in the BoBC is less critical due to this reason, and hence leads to a more robust realization of the control. This further has an impact on reactive component sizing and will be covered in greater detail in passive component discussion section. Due to the low switching frequency of the BoBC sub-modules, while any of the proposed two quadrant switching packages may be used for the BoBC, IGCTs become a natural choice due to their lower conduction losses in comparison to IGBTs. The viable choices for semiconductors for each converter topology are summarized in Table 1.

Table 1. A listing of candidate semiconductors for converter realization for the three topologies.

	CSC	VSC	BoBC
Device type	SCR	IGBT	IGCT

While the general considerations affect the choice of the switching device, selection of a particular device for an application requires an investigation of the average current through the semiconductor devices in order to select an appropriate current rating. The CSC is straightforward in that the average current carried by the semiconductors is equal to that of the average arm current, *i.e.*, half the average value of the rectified phase current or one third of the dc output current. The VSC arm current divides between the IGBT and its anti-parallel diode unequally resulting in asymmetrical device currents during active rectification but obviously sum to $1/3 I_{dc}$. Unlike the CSC and VSC topologies whose arm currents are entirely dc, the BoBC has both ac and dc current flowing in each arm in order to facilitate power conversion. Each of the six arms of the BoBC has an ac current component of $1/2 I_{ph}$ and a dc component of $1/3 I_{dc}$ flowing through it. Simply put, the arm current is largely ac with a dc offset. Furthermore, due to the asymmetry of the half bridge, the devices forming the two throws of the bridge have unequal current stress levels. Also note that the BoBC does not require the use a transformer to step up the generation voltage prior to the converter as in the CSC or VSC. In applications using the BoBC, the converter itself may act as the transformer for the purposes of voltage matching with an apparent transformer ratio Q_{bobc} . In such a case, Q_{bobc} for the BoBC is equivalent to Q_{tran} for the other converters, since they all perform the same task with the same input and output quantities. However, since the input ac voltage to the BoBC may be lower than the CSC or VSC by a factor of the transformer ratio Q_{tran} , conservation of energy dictates that the ac component of the BoBC arm current increase by a factor of Q_{tran} as well. On this basis of this discussion, the average converter device currents and voltages for the three topologies in their per unit form are summarized in Table 2. Detailed derivations of these quantities are shown in the Appendix.

Table 2. Analytical relationships of power semiconductor per-unitized currents and voltages.

CSC	VSC	BoBC
$I_{arm_pu} = \frac{1}{\pi\sqrt{2}Q_{tran}}(\cos(\alpha) + 1)$	$I_{arm_pu} = \frac{\sqrt{2}}{\pi Q_{tran}}$	$I_{arm_pu} = \frac{\pi}{3\sqrt{6}Q_{bobc}} + \frac{\sqrt{2}}{\pi}$
$I_{T_pu} = I_{arm_pu}$	$I_{T_pu} = \frac{1}{\sqrt{2}\pi Q_{tran}} + \frac{\pi}{6\sqrt{6}Q_{tran}}$	$I_{T1_pu} = I_{D1_pu} = \frac{1}{2\pi\sqrt{2}} - \frac{\pi\sqrt{2}}{54Q_{bobc}^2} \approx \frac{1}{2\pi\sqrt{2}}$
	$I_{D_pu} = \frac{1}{\sqrt{2}\pi Q_{tran}} - \frac{\pi}{6\sqrt{6}Q_{tran}}$	$I_{T2_pu} = I_{D2_pu} = \frac{1}{2\pi\sqrt{2}} + \frac{\pi}{3\sqrt{6}Q_{bobc}} + \frac{\pi\sqrt{2}}{54Q_{bobc}^2} \approx \frac{1}{2\pi\sqrt{2}}$
$V_{T_pu} = \frac{1}{N_{csc} + 1}$	$V_{T_pu} = V_{D_pu} = \frac{1}{N_{vsc} + 1}$	$V_{T_pu} = V_{D_pu} = \frac{1}{N_{bobc} + 1}$

In addition to the average current in each device, a sufficient number of devices are connected in series to achieve the appropriate blocking voltage. Typically the switching devices are de-rated to 50%–70% the voltage blocking capability listed by the manufacturer. Parasitic inductance within individual device packs can cause voltage overshoot during turn-on. This voltage is highly dependent

on specifics of the device parasitics and the speed at which the device switches. The other prominent factor in de-rating devices is redundancy. Should a device fail, the remaining devices must be capable of handling an increase in the blocking voltage or average current placed upon them, realized by imposing an $n + 1$ redundancy as is common in utility applications. Using the parameters for our benchmark application, and Tables 1 and 2, device selection, number of levels, and total semiconductor MVA for the three topologies is presented in Table 3. The de-rated voltages shown in Table 3 are specifically recommended by the device manufacturer and the MVA rating is defined as the product of blocking voltage and average current of each device specified in Table 2. Part numbers for semiconductors are provided in Table 3 as a reference for candidate devices whose parameters are used for loss calculations later in the paper.

Table 3. Summary of semiconductor selection and utilization data for converter realization.

	CSC	VSC	BoBC
Device Type	Thyristor (SCR)	IGBT-diode pair	IGCT –diode pair
Blocking voltage (kV)	6.5	6.5	4.5
Part number	ABB 5STP 03X6500	ABB 5SNA 0400J650100	ABB 5SHX 14H4510
De-rated application voltage V_{ca} (kV)	3.3	3	2.8
Number of series sub-modules per arm	$N_{csc} = \text{ceil}\left[\frac{V_{dc}}{V_{ca}}\right] + 1 = 46$	$N_{vsc} = \text{ceil}\left[\frac{V_{dc}}{V_{ce}}\right] + 1 = 38$	$N_{bobc} = \text{ceil}\left[\frac{V_{dc}}{V_{Csm}}\right] + 1 = 55$
Total number of devices	276 thyristors	228 IGBT-diode pairs	330 IGCT-diode pairs
Total semiconductor MVA (p.u.)	4.1	6.6	17.8

3.2. Reactive Component Requirements & Waveform Quality

Each of the converter topologies has vastly different reactive component requirements given their inherent traits. Reactive components exist in three different sections of the HVDC system: the ac side, the converter sub-modules, and the dc side. The following section will analyze each converter topology within the three sections areas to provide a design perspective on all reactive components involved.

3.2.1. AC side Reactive Components

The reactive components that potentially exist on the ac side of the system are transformers and line filters. The transformer can serve two purposes: to step up/down the line voltage to the desired value and to provide electrical isolation between the converter and the ac grid if required. The CSC and VSC rely on the transformer to step up the line voltage to the EHV level in order to rectify it for the production of HVDC transmission. The voltage step up/down property of the transformer is inherently part of the BoBC, which allows the transformer to be completely eliminated from the ac side of the system when isolation is not required. The transformer represents a significant cost for HVDC systems (20 k USD/MW, [38]) and its potential elimination may represent a large advantage for the BoBC. On the other hand, concerns regarding dc current injection into the ac terminals and protection/grounding considerations may call for an isolation transformer at the converter interface. In such cases, the

application of the transformer is purely dictated by those considerations, and does not have a power conversion role.

Often AC line filters are required for a converter system to meet power quality standards such as IEEE 519 [39]. As described in the CSC review section the benchmark CSC in this evaluation assumes a 12 pulse system which requires harmonic filtering. The design evaluation of such filters is not considered in detail in this paper, a representative ac side filter rated at 0.35 p.u. is considered to be typical as presented in recent literature [40]. An operating nominal power factor of 0.9 is assumed to determine the level of reactive support necessary for the CSC system.

Although VSCs may also use multi-pulse techniques for harmonic elimination, the use of high switching frequency of the converter leads to a more economic realization in most cases. Despite the use of high switching frequency, VSC implementations may still require tuned ac line filters between the grid connection and converter transformer to reduce the high frequency harmonics beyond the 40th harmonic. Although the design evaluation of such filters is not considered in detail in this paper, a representative ac side filter rated at 0.25 p.u. is considered to be typical [41]. Unlike the VSC, the BoBC does not require any ac side reactive components as the energy storage elements are contained within the individual sub-modules. The ac side reactive component requirements are summarized in Table 4.

Table 4. AC side reactive component summary.

	CSC	VSC	BoBC
Transformer rating MVA (p.u)	1.1	1.04	1.0 (optional)
Lowest harmonic number Pulse Number, N_{pulse}	$6N_{rect} = 12$	$f_{sw}/f_p = 40$	$N_{bobc} \cdot f_{sw}/f_p = 165$
Switching frequency filter MVA (p.u)	0.35	0.25	0
Displacement power factor correction MVA (p.u)	0.5	0	0
Total ac side reactive component MVA (p.u.)	1.95	1.29	1.0 (optional)

3.2.2. Sub-Module Reactive Components

As mentioned in the previous section, sub-module reactive components for the CSC and VSC such as voltage sharing RC networks are primarily to account for second order effects and are not investigated herein as a topological imperative. On the other hand, the BoBC half-bridge sub-modules each possess an individual dc link capacitance and pole inductance connected to the throws and poles of the switches respectively. The value of the bus capacitance may be readily calculated by utilizing the average current through the capacitor and by defining an allowable voltage ripple. The average current through the sub-module capacitor during a half cycle is given by either I_{T1} or I_{D1} from Table 2. Assuming an allowable peak-to-peak voltage ripple V_{rip} of 10% using a base time-scale of $1/\omega_B$ and dc voltage base, the capacitance may be found using (3.1) and (3.2). It should be noted that due to the inherently large arm currents of this converter each sub-module, the dc link capacitor is relatively large.

$$C_{sm_pu} = \frac{\Delta q_{pu}}{V_{rip_pu}} \tag{3.1}$$

$$\Delta q_{pu} = 2\pi \int_0^{T_p} |i_{cb_avg_pu}| dt = 4\pi I_{T1_pu} \tag{3.2}$$

where, $V_{rip_pu} = \frac{0.1}{N_{bobc}}$ and the capacitance base is C_{Bac}

Perhaps even more important than defining a value of capacitance to facilitate a stiff dc bus is the rms ripple current rating of the dc bus. The duty cycle and current through each arm sub-module are the same despite the number of levels, thus all capacitors must have identical rms ripple current ratings. Using the averaged BoBC model from Section 2, and assuming the converter is lossless, the rms current through a sub-module dc bus may be determined using (3.3) per-unitized to the source current.

$$i_{cb_rms_pu} = \sqrt{\frac{1}{16} - \frac{\pi^2}{144Q_{bobc}^2} + \frac{\pi^4}{2916Q_{bobc}^4}} \approx \frac{1}{4} \tag{3.3}$$

The pole inductance for the BoBC sub-module is the other reactive component to be characterized. It should be noted that the individual sub-module inductances may be represented as a lump sum inductance of the N_{bobc} sub-modules placed in series with the converter arm. Obviously, the inductor must be sized to accommodate the average arm current, i_{arm} in Table 2. For the purpose of selecting a necessary value of inductance, an acceptable amount of ripple current and time period due to switching must be selected. As the arm current contains significant dc and ac components, the rms combination of the two will serve as the baseline for a nominal amount of 20%. The time period over which this ripple occurs is a function of switching frequency of each level and the number of levels. If each level’s switching is phase shifted from the next, an effective pulse number from Table 4 may be used in calculating the lump sum inductance. Using the BoBC averaged model [29], the inductance may be calculated by means of (3.4) and (3.5).

$$L_{arm_pu} = \frac{V_{L_pu} \Delta t_{pu}}{\Delta I_{pu}} \tag{3.4}$$

$$L_{sm_pu} = \frac{L_{arm_pu}}{N_{bobc}} \tag{3.5}$$

where, $\Delta t_{pu} = \frac{\pi}{N_{pulse}}$ and the inductance base is L_{Bac}

The designer may now choose whether to distribute the inductance through each sub-module or lump it in series with each arm. Of the two options, the distributed option is favored due to modularity considerations. The BoBC reactive component requirements are summarized in Table 5.

Note the large amount of total energy storage of the BoBC, which comes about from maintaining a stiff sub-module bus voltage despite the large bus current. While such large stored energy leads to increased converter volume, it also gives the BoBC an advantage for riding through disturbances that may occur on a time scale of tens of power frequency cycles. This characteristic may be formally expressed in seconds or number of power frequency cycles as the ratio of the converter stored energy to the power throughput as the per unit total stored energy, included in Table 5.

Table 5. Benchmark reactive component summary for BoBC (Per-Unit).

Inductor size, L_{arm_pu}	0.031
Inductor RMS current, I_{arm}	0.5
BoBC total inductor MVA	0.028
Capacitor size, C_{sm}	70
Capacitor RMS current, i_{cb-rms}	0.25
BoBC total capacitor MVA	9.3
Sub-module stored energy	0.13
BoBC total stored energy	43

3.2.3. DC Side Reactive Components

The BoBC needs no passive components on the HVDC bus whereas the CSC and VSC require inductive and capacitive energy storage elements respectively. However, the BoBC topology is insensitive to any inherent impedance of the dc interconnection, which may be inductive in the case of a long transmission line, or capacitive in case of underground cables. The CSC line inductance may be sized by defining an allowable per-unit ripple current of 40% and employing a per-unitized energy storage approach as defined in (3.6).

$$L_{csc_pu} = \frac{4\pi}{(1.2^2 - 0.8^2)N_{pulse}} \quad (3.6)$$

where the inductance base is L_{Bdc}

It should be noted that the transmission line inductance may serve as the inductor for CSC systems whose transmission lines are long enough to achieve the desired value. If this is not the case, as in a close proximity multi-terminal or back-to-back application, a discrete inductor may be added in series with the line.

The VSC storage capacitor may be sized using an approach nearly identical to that used for the CSC inductor except using 10% ripple (3.7).

$$C_{vsc_pu} = \frac{4\pi}{(1.05^2 - 0.95^2)N_{pulse}} \quad (3.7)$$

where the capacitance base is C_{Bdc}

The realization of this capacitor can be an engineering challenge in itself and care must be taken in its design. The capacitor must withstand the HVDC bus voltage, 150 kV in our benchmark application. This is done by placing lower voltage capacitors in series, which necessitates a voltage sharing mechanism, usually a resistive network. In this case, the resistance must be low enough that the current through it is much greater than the capacitor leakage current but not so much as to consume appreciable power [42]. As with the BoBC sub module capacitors, the VSC HVDC bus capacitance must handle a given amount of ripple current. The worst-case ripple current per-unitized to the phase current for a VSC operating at near unity power factor is expressed by (3.8) [43]. The DC components for the benchmark CSC and VSC are summarized in Table 6.

$$i_{cv_rms_pu} = \frac{1}{\sqrt{2}} \quad (3.8)$$

Table 6. Benchmark DC side reactive component summary for CSC & VSC (per-unit).

	CSC	VSC
Inductor size, L_{csc}	1.3	----
Average inductor current, I_{dc}	1	----
Inductor MVA	1	----
Capacitor size, C_{vsc}	----	1.7
Capacitor RMS current, i_{cv-rms}	----	0.58
Capacitor MVA	----	0.58
Total converter stored energy	0.104	0.126

As seen in Table 7, the energy storage requirements of the CSC and VSC is considerably small compared to the BoBC, making them less effective in participating in corrective action during voltage sag or fault ride-through conditions, while also representing a smaller amount of associated risks.

3.3. System Operating Losses

The operating losses for all three converters may be separated into two distinct areas, device losses and reactive component losses. Losses associated with other support circuitry will be considered negligible. Device losses may be categorized as either conduction loss or switching loss. Conduction losses result from the voltage drop across the device during the on-state condition. For the thyristor family and IGBTs this voltage drop is modeled by a minimum on-state voltage in addition to a dynamic device resistance as shown in (3.9).

$$V_{on}(I_{on}) = V_o + r_{on} I_{on} \quad (3.9)$$

$$P_{con} = V_{on}(I_{on}) I_{avg} \quad (3.10)$$

It may be noted that the voltage drop is dependent on the current through the device during its on-state, not the average current. Using (3.10), conduction losses may be calculated using the on-state voltage drop and the average current through the semiconductor. Since the BoBC is transformerless, its device currents are greater than the CSC or VSC topologies by the ac line side transformer ratio. As it will be seen after discussing switching losses, the dominant loss mechanism in the BoBC is conduction losses due to the large arm currents.

Switching losses are characterized by discrete amounts of energy per switching event for a given reference power. Of the three devices discussed in this paper, only IGCTs and IGBTs will be categorized as possessing turn-on and turn-off energies. In the CSC the thyristors are naturally commutated and operate at line frequency so any switching loss will be considered negligible. Diode switching losses are defined by their reverse recovery energy. The VSC and BoBC use IGBTs and IGCTs with antiparallel diodes connected across them as well, so the total switching losses per switch-diode pair may be expressed as (3.11).

$$P_{sw} = \left[\frac{E_{on} I_{sw}}{I_{ref} V_{ref}} + \frac{E_{off} I_{sw}}{I_{ref} V_{ref}} + \frac{E_{rr} I_D}{I_{ref} V_{ref}} \right] \frac{V_{dc}}{N} f_{sw} \quad (3.11)$$

Switching event energy losses for a given device can be found on its datasheet along with specified reference voltages and currents. This information, in conjunction with loss Equations (3.9–3.11) and the Tables 2 and 3, yield the semiconductor losses for a converter topology. Similar to the conduction losses, it should be noted that I_{sw} and I_D are not average value currents and must be calculated using the current amplitude at the switching event. In addition, the BoBC possesses asymmetries in the converter arms regarding the direction of dc current which must be accounted for. A more thorough treatment of these two caveats may be found in [13]. As seen in (3.11), the switching losses are directly proportional to switching frequency, which characterizes the VSC as switching loss dominant. The BoBC switches at frequency $1/N_{BoBC}$ times less than the VSC due to its capability to offset switching between levels, which results in lower switching losses. This situation is the dual to the VSC and BoBC conductive losses discussed earlier. The calculated semiconductor losses for all three topologies in the benchmark application are listed in Table 7.

Of the reactive components that contribute power loss to a system only DC link capacitors will be considered in detail. The power loss in a capacitor may be described in terms of the rms current throughput and capacitor ESR (3.12).

$$P_{cap} = I_{rms}^2 R_{cap} \quad (3.12)$$

Accurate capacitor ESR data is difficult to model accurately because it is highly dependent on the ripple frequency, capacitance, and operating temperature [44]. In most high power utility inverter applications, capacitor banks are custom designed, thus specific information pertaining to ESR is not available. For this reason, (3.12) is difficult to apply in the context of this paper but is provided to illustrate the need for good capacitor design as the BoBC uses many capacitors with high rms currents. As an estimate for capacitor losses, manufacturers specify an average loss of 0.5 W/kVAR for their film capacitor technology used in high voltage inverter applications [45].

The input transformers, line filters, and inductors for the CSC and VSC are treated with a combined efficiency of 99%, as in accordance with recent DOE standards [46]. The BoBC losses do consider the use of a transformer, although the transformer itself is not necessary for functionality. Like capacitors, these components are usually custom made to suit an application. The sub-module inductors of the BoBC are not included in the analysis because their low inductance values minimize core losses and the conductors may be designed for minimal copper loss. With these assumptions, the reactive component losses are summarized in Table along with power semiconductor losses.

Table 7. 50 MW Benchmark application loss summary.

	CSC	VSC	BoBC
Device Conduction Losses (p.u.)	0.0026	0.0031	0.024
Device Switching Losses (p.u.)	----	0.023	0.0084
Total Semiconductor Losses (p.u.)	0.0026	0.026	0.033
Transformer & Filter Losses (p.u.)	0.01	0.01	0.01
Total Capacitor Losses (p.u.)	----	$3 \cdot 10^{-5}$	$4.7 \cdot 10^{-4}$
Total losses (p.u.)	0.013	0.036	0.043
Efficiency (%)	98.7	96.5	95.7

Given the results in Table 7, it is clear that efficiency of the CSC is superior in comparison to VSC and BoBC. Though the VSC has a slight efficiency advantage over the BoBC according to Table 7, given parameter and modeling uncertainties in physical parameters and calculations it would be more appropriate to consider the two topologies as equivalent in this regard.

3.4. Multi-terminal Operation

In a typical configuration in wind farm integration, multi-terminal operation is deemed necessary trait for converters that connect to a common bus. A candidate offshore wind field rated at several hundred MW interconnected to a 150 kV HVDC interconnection that is fed by banks of 50 MW converters grouped in close proximity is illustrated in Figure 1 as Cluster 2. Given such applications, it is imperative that the multi-terminal characteristics of the three converter topologies be discussed.

While it is commonly recognized that the VSC is superior to CSC from a multi-terminal dc connection; the feature depends entirely on the context of the application. This can be attributed to the fact that VSCs have a fixed output voltage polarity and bidirectional current capabilities. The BoBC shares these same traits with the VSC and for the remainder of this section the two topologies shall be considered indistinguishable. These traits allow VSCs to be paralleled easily on a common bus and enjoy bidirectional power transmission with no external switchgear. CSCs, on the other hand, may only output current in a single direction so the output voltage must change polarity in order to facilitate a directional change in power flow. In situations where multiple CSCs are connected to a common HVDC bus, firing angle control and voltage reversal leads to reversal of power flow at each of the terminals of the interconnection. In the unlikely case where an arbitrary set of power flow direction is intended, individual converter power direction reversals for CSCs are accomplished anti-parallel bridges or dual converters. However, in offshore wind farm applications the requirement of bidirectional power transmission is not required thus the question does not arise.

However, the advantage of the VSC converter is apparent in the wind farm application because it does not require a reactive power source as does the CSC. Among wind turbine generators that are based on doubly-fed induction generators, which have limited reactive power capability of their own, the use of a CSC in a wind farm application (or any other weak ac network) quite complex.

Table 8. Wind farm connection performance penalty summary.

	CSC	VSC	BoBC
Multi-terminal Operation	0	0	0
Weak ac network compatibility	1	0	0
Multi-terminal rank	2 nd	1 st	1 st

Penalty = 1, No Penalty = 0

3.5. Fault Tolerance

As in any large-scale power system installations fault tolerance and fault management are important considerations in applications of power conversion technologies. Two specific fault types will be addressed herein, namely converter faults and DC line-to-line faults. Faults occurring on the medium

voltage side of the converter are not separately addressed because they are readily understood in the context of ac power distribution system protection.

The most common converter fault is the failure of a sub-module. As discussed earlier in power semiconductor requirements, each converter is sized such that loss of numerous sub-modules does not impede operation. Sub-modules in the case of BoBC may be bypassed using mechanical or solid-state contactors. Hot-swap replacements of faulted sub-modules in such bridge configurations are not uncommon in high reliability applications [47]. Another common converter fault is high voltage transformer failure [48]. Inevitably the insulation on the high voltage secondary winding deteriorates over time and shorts the winding. The BoBC has a clear advantage in this situation since it does not require the use a high voltage transformer unlike the CSC and VSC.

Perhaps the most important fault condition in an HVDC system is a line-to-line dc short. CSCs have long proven effective in regulating fault currents due to their inherent current stiff property which limits the current at the start of a fault and the ability to adjust the commutation angle α of the thyristor bridge. This control technique is simple and requires no additional components. VSCs are much more difficult to control during a fault condition. Unlike the CSC, the VSC is voltage stiff on the dc bus and the current may change rapidly. During a HVDC bus short condition the fault current is only limited by the dc impedance of the transmission line, which can be typically quite low. The fault current will be fed initially by the HVDC link capacitance and then by the free-wheeling diodes of the converter which serve as an uncontrolled rectifier. This trait is shared by other VSC topologies as well and not just the 2-level topology discussed here. To protect the converter during fault conditions circuit breakers (CBs) are employed. CBs represent a suboptimal choice because no cost effective alternative solution exists. DC CBs traditionally used for traction applications have been connected in series to meet the voltage requirements but are prone to failure since simultaneous switching may not occur [12]. Solid state CBs are also an option, in the form of a triac configuration realized by a string of anti-parallel IGCTs or GTOs [49–51]. Although functional, this solution is very expensive and has high conduction losses, comparable to that of the VSC converter itself.

The BoBC can be described on performance basis as having the multi-terminal characteristics and dynamic response of a VSC while possessing the fault tolerance of a CSC. This comes about because the sub-modules of the BoBC may actively regulate their inductor current and there is no uncontrolled energy storage element during a line-to-line fault. By simply solving (2.3) with the output voltage set to zero a duty cycle for a line-to-line fault condition may be obtained. In our case however, the half bridge is used, so this method for controlling fault current is of limited effectiveness because the duty ratio is limited to values between 0 and 1. Nevertheless, the large amount of internal energy storage of the BoBC may be used to an advantage for up to tens of cycles of ac cycle during faults. A number of arm sub-modules can hold the upper switch (*i.e.*, T_1) in an on state, which will reverse bias the freewheeling diodes thus preventing them from feeding the fault. The number of sub-modules required during such events is determined by the magnitude of the ac line voltage.

One advantage the VSC has over the CSC is it possesses higher dynamic response due to its high PWM frequency making it less sensitive to disturbances in the ac network [20]. Line commutated CSCs have a comparatively slow dynamic response and may experience commutation errors when

disturbances in the ac network occur. This could potentially be a very large drawback for CSCs in wind farm applications since the farm-side ac connection is only as strong as the wind.

As a subjective indication of these features, a rank order consideration may be used to describe the properties of each converter topology as summarized in Table 9.

Table 9. Converter fault performance penalty summary.

	CSC	VSC	BoBC
Controllable HVDC fault current	0	1	0
HVDC breakers necessary?	0	1	0
Possible HV Transformer Fault?	1	1	0
Fast Dynamic response?	1	0	0
Fault tolerance rank	2 nd	3 rd	1 st
Penalty = 1, No Penalty = 0			

Given the results of Table 9, it may be noted that the BoBC has superior fault tolerance properties in comparison to the CSC and VSC.

3.6. Modularity & Complexity

In recent years much attention has been given to the concept of modular power converter design. In applications such as HVDC power conversion, modularity can provide a powerful manufacturing advantage by reducing the complexity, capital expenses and maintenance expenses. While each of the three converter topologies uses six converter arms and each arm consists of a string of sub-modules, the sub-modules for the CSC and VSC are formed by semiconductors and support circuitry only and cannot constitute a standalone power converter. The BoBC sub-modules however form a standalone half bridge power converter. This proves to be more versatile from a manufacturing standpoint because a single building block may be connected with others in a plethora of configurations to form different topologies at virtually any power level. Energy storage such as batteries may be readily incorporated into the sub-module dc bus structure as well yielding a fully integrated transmission-energy storage solution [30,31]. Moreover, all the components required to realize a BoBC are contained within each sub-module, whereas a CSC or VSC require numerous reactive components external to the sub-module. The absence of any separate dc link reactive element proves to be a significant advantage by eliminating the need for series connected capacitor banks, inductors with high dc voltage isolation capabilities. The dc link merely consists of the cabling and/or transmission lines to carry the currents with appropriate insulation levels.

Gate electronics prove to be challenging in HVDC applications. Gate control logic and power must be electrically isolated from the control input and structures at low voltages because the gate circuitry is referenced to EHV. Recently, Light Trigger Thyristors (LTTs) have become a viable option for CSCs [52]. Instead of a voltage applied to the gate of the device, light delivered by a fiber optic cable can facilitate turn-on directly. This mitigates the necessity for complicated EHV isolation in the gate control circuitry architecture. Unfortunately, light turn-on technology is not available in IGBTs thus VSCs require a complicated electrical isolation system for their gate electronics. The BoBC sub-module, like the CSC, is a three terminal building block; two power connections to the bridge and

a fiber optic control input. Since the BoBC sub-module has its own dc bus capacitance, energy from the bus may be used to supply power to the gate circuitry without the hassle of EHV isolation [33]. However, the price the BoBC pays for superior modularity and ease of interface is a high parts count and a relatively complicated control algorithm. Each sub-module requires its dc bus to be closed-loop regulated to ensure voltage balance [29,32]. The CSC and VSC do not require any internal control loops and have proven control methods, which are well established.

Table 10. Converter modularity and integration penalty summary.

	CSC	VSC	BoBC
Degree of Modularity	1	1	0
Stand Alone Sub-Module	1	1	0
Ease of integration	0	1	0
Relative control complexity	0	0	1
Modularity & integration rank	2 nd	3 rd	1 st

Penalty = 1, No Penalty = 0

4. Conclusions

In this paper the CSC, VSC, and BoBC converters have been evaluated for a benchmark offshore wind farm application with regard to power semiconductor requirements, reactive component requirements, operating losses, fault tolerance, multi-terminal operation, modularity, and complexity. A summary of the quantitative and qualitative characteristics of all three converters is presented in Table 11 in a per unit description, and in Table 12 in rank classification respectively.

While in applications where power flow is unidirectional with a strong ac network the CSC has superior performance given its high efficiency, robust fault tolerance, and simple design, their application at the sending end of wind generation sources poses a particularly challenging problem due to the limited reactive power capacity of typical wind generation sources.

On the other hand, the VSC and the BoBC are attractive for multi-terminal applications connected to weak ac networks. Among the two the BoBC has superior fault tolerance and ease of integration but at the cost of large per unit power semiconductor ratings and capacitive energy storage which is strikingly evident in Table 11.

In contrast to the Cluster 1 configuration, the Cluster 2 configuration illustrated in Figure 1 features a separate sending end HVDC converter applied at each turbine independently, and the generators may not require an explicit electrical isolation requirement, and thus may be apt for application of BoBCs on a local basis. At the receiving end, a conventional CSC may be applied in conjunction with a stiff grid present close to the load center with an appropriate transformer to provide the isolation and voltage matching. Such a hybrid approach that draws upon the synergistic features of the BoBC at sending end wind generation sources in a distributed configuration, and the CSC at receiving end ac grid interfaces may be a competitive and favored architecture.

Table 11. Summary of converter quantitative characteristics for the candidate topologies.

	CSC	VSC	BoBC
Semiconductor MVA	4.1 (p.u.)	6.6 (p.u.)	17.8 (p.u.)
Total capacitor MVA	----	0.58 (p.u.)	9.3 (p.u.)
Total inductor MVA	1 (p.u.)	----	0.028 (p.u.)
AC filter/reactor & transformer MVA	1.95 (p.u.)	1.29 (p.u.)	1 (p.u.) optional
Stored energy	0.104 (p.u.)	0.126 (p.u.)	43 (p.u.)
Converter losses	0.013 (p.u.)	0.036 (p.u.)	0.043 (p.u.)
Converter efficiency	98.7%	96.5%	95.7%

Table 12. Summary of converter qualitative characteristics for the candidate topologies.

	CSC	VSC	BoBC
Multi-terminal operation rank	2nd	1st	1st
Fault tolerance rank	2nd	3rd	1st
Modularity & integration rank	2nd	3rd	1st
Technology maturity level	1st	2nd	3rd

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References

1. Prasai, A.; Yim, J.; Divan, D.; Bendre, A.; Sul, S. A new architecture for offshore wind farms. *IEEE Trans. Power Electr.* **2008**, *23*, 1198-1204.
2. Jovcic, D.; Strachan, N. Offshore wind farm with centralised power conversion and DC interconnection. *Generat. Transmis. Distribut. IET.* **2009**, *3*, 586-595.
3. Jovcic, D.; Milanovic J.V. Offshore wind farm based on variable frequency mini-grids with multiterminal DC interconnection. AC and DC Power Transmission Conference, London, UK, March 2006.
4. Jovcic, D. Interconnecting offshore wind farms using multiterminal VSC-based HVDC. Presented at IEEE Power Engineering Society General Meeting, Montreal, QB, Canada, October 2006.
5. Kling, W.L.; Hendriks, R.L.; den Boon, J.H. Advanced transmission solutions for offshore wind farms. Presented at IEEE Power and Energy Society General Meeting—Conversion And Delivery of Electrical Energy in the 21st Century, Pittsburgh, PA, USA, July 2008.
6. Cole, S.; van Hertem, D.; Meeus, L; Belmans, R. Technical developments for the future transmission grid. Presented at Future Power Systems Conference, Amsterdam, The Netherlands, November 2005.
7. Bresesti, P; Kling, W.L.; Hendriks, R.L.; Vailati, R. HVDC connection of offshore wind farms to the transmission system. *IEEE Trans. Energy Convers.* **2007**, *22*, 37-43.

8. Chaudhary, S.K.; Teodorescu, R.; Rodriguez, P. Wind farm grid integration using VSC based HVDC transmission—An overview. Presented at IEEE Energy 2030 Conference, Atlanta, GA, USA, November 2008.
9. Kirby, N.M.; Xu, L.; Luckett, M.; Siepmann, W. HVDC transmission for large offshore wind farms. *Power Eng. J.* **2002**, *16*, 135-141.
10. Morton, A.B.; Cowdroy, S.; Hill, J.R.A.; Halliday, M.; Nicholson, G.D. AC or DC? Economics of grid connection design for offshore wind farms. Presented at AC and DC Power Transmission Conference, London, UK, March 2006.
11. Cole, S.; Belmans, R.; Transmission of Bulk Power. *IEEE Industr. Electr. Mag.* **2009**, *3*, 19-24.
12. Flourentzou, N.; Agelidis, V.G.; Demetriades, G.D. VSC-Based HVDC power transmission systems: An overview. *IEEE Trans. Power Electr.* **2009**, *24*, 592-602.
13. Allebrod, S.; Hamerski, R.; Marquardt, R. New transformerless, scalable modular multilevel converters for HVDC-transmission. Presented at IEEE PESC, Rhodes, Greece, March 2008.
14. Faulstich, A.; Stinke, J.K.; Wittwer, F. Medium voltage converter for permanent magnet wind power generators up to 5 MW. Presented at Power Electronics and Applications, Dresden, Germany, August 2006.
15. Zargari, N.R.; Xiao, Y.; Wu, B. A multi-level thyristor rectifier with improved power factor. *IEEE IAS* **1996**, *2*, 967-972.
16. Li, R.; Bozhko, S.; Asher, G.M.; Clare, J.C.; Yao, L.; Sasse, C. Grid frequency control design for offshore wind farms with naturally commutated HVDC link connection. *IEEE Industr. electr.* **2006**, *2*, 1595-1600.
17. Foster, S.; Xu, L.; Fox, B. Control of an LCC HVDC system for connecting large offshore wind farms with special consideration of grid fault. IEEE Power and Energy Society General Meeting—Conversion and Delivery of Electrical Energy in the 21st Century, Pittsburgh, PA, USA, July 2008.
18. Bozhko, S.V.; Blasco-Gimenez, R.; Li, R.; Clare, J.C.; Asher, G.M. Control of offshore DFIG-based wind farm grid with line-commutated HVDC connection. *IEEE Trans. Energy Convers.* **2007**, *22*, 71-78.
19. Bozhko, S.; Li, R.; Blasco-Gimenez, R.; Asher, G.M.; Clare, J.C.; Yao, L.; Sasse, C. STATCOM-controlled HVDC power transmission for large offshore wind farms: Engineering issues. Presented at IECON, Paris, France, November 2006.
20. Sood, V.A. *HVDC and FACTS Controllers, Applications of Static Converters in Power Systems*; Pai, M.A., Stankovic, A., Eds.; Kluwer Academic Publishers: Norwell, MA, USA, 2004.
21. Krein, P.T. *Elements of Power Electronics*; van Valkenburg, M., Sedra, A.S., Lightner, M.R., Eds.; Oxford University Press: New York, NY, USA, 1998.
22. de la Villa, J.A.; Acha, E.; Exposito, A.G. Voltage Source Converter Modeling for Power System State Estimation: STATCOM and VSC-HVDC. *IEEE Trans. Power Syst.* **2008**, *23*, 1552-1559.
23. Yazdani, A.; Irvani, R. Dynamic model and control of the NPC-based back-to-back HVDC system. *IEEE Trans. Power Deliv.* **2006**, *21*, 414-424.
24. Yao, X.; Sui, H.; Xing, Z. The study of VSC-HVDC transmission system for offshore wind power farm. Presented at The International Conference on Electrical Machines and Systems, Seoul, South Korea, October, 2007.

25. Xu, L.; Agelidis, V.G. VSC transmission system using flying capacitor multilevel converters and hybrid PWM control. *IEEE Trans. Power Deliv.* **2007**, *22*, 693-702.
26. Saeedifard, M.; Iravani, R.; Pou, J. A Space Vector Modulation Strategy for a Back-to-Back Five-Level HVDC Converter System. *IEEE Trans. Industr. Electr.* **2009**, *56*, 452-466.
27. Lee, G.B.; Engelbrecht, F.; Beukes, H.J. Series-stacked and neutral point clamped multilevel converter topologies for MVDC transmission. *IEEE Conf. Afr.* **2002**, *2*, 735-741.
28. Zhou, K.; Fu, X.; Cheng, M.; Zhu, X.; Wang, W.; Wang, T. Topologies and control of VSC-HVDC systems for grid connection of large-scale off-shore wind farms. The International Conference on Electrical Machines and Systems, Wuhan, China. February 2009. pp. 2357-2361.
29. Ludois, D.C.; Reed, J.; Venkataramanan, G. Hierarchical control of bridge of bridge multilevel power converters. *IEEE Trans. Industr. Electr.* **2010**, in press.
30. Maharjan, L.; Inoue, S.; Akagi, H.; Asakura, J. A transformerless battery energy storage system based on a multilevel cascade PWM converter. IEEE Power Electronics Specialists Conference, Rhodes, Greece, June 2008.
31. Maharjan, L.; Inoue, S.; Akagi, H. A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration. *IEEE Trans. Industr. Appl.* **2008**, *44*, 1621-1630.
32. Hagiwara, M.; Akagi, H. PWM control and experiment of modular multilevel converters. Presented at IEEE Power Electronics Specialists Conference, Rhodes, Greece, June 2008.
33. Glinka, M.; Marquardt, R. A new AC/AC multilevel converter family. *IEEE Trans. Industr. Electr.* **2005**, *52*, 662-669.
34. Erickson, R.W.; Al-Naseem, O.A. A new family of matrix converters. *IEEE Industr. Electr. Soc.* **2001**, *2*, 1515-1520.
35. Ding, G.; Tang, G.; He, Z.; Ding, M. New technologies of voltage source converter (VSC) for HVDC transmission system based on VSC. IEEE Power and Energy Society General Meeting—Conversion and Delivery of Electrical Energy in the 21st Century, Pittsburgh, PA, USA, July 2008.
36. Baek, J.W.; Yoo, D.W.; Kim, H.G. High voltage switch using series-connected IGBTs with simple auxiliary circuit. IEEE Industry Applications Conference, Rome, Italy, October 2000.
37. Bhattacharya, S. Series connected IGCT based high power three-level neutral point clamped voltage source inverter pole for FACTS applications. In IEEE Power Electronics Specialists Conference, Pittsburgh, PA, USA, July 2005.
38. Staff of RSMMeans. *RSMMeans Electrical Cost Data*, 29th ed.; Reed Construction Data: Kingston, MA, USA, 2006.
39. *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*; IEEE Standard 519-1992; IEEE: New York, NY, USA, 1993.
40. ABB Online Library. Bernt Bergdahl R.D. AC-DC harmonic filters for three Gorges-Changzhou 500 kV HVDC project. Available online: <http://www.abb.com> (accessed on 9 June 2010).
41. Rockhill, A.A.; Liserre, M.; Teodorescu, R.; Rodriguez, P. Grid filter design for a multi-megawatt medium voltage voltage source inverter. *IEEE Trans. Industr. Electr.* 2010, in press.
42. Nian, M.; Yinhong, L.; Xianzhong, D.; Jiang, Y.; Chuang, F. Study on high voltage capacitor unbalance protection in HVDC projects. In Asia-Pacific Power And Energy Engineering Conference, Wuhan, China, March 2009.

43. Kolar, J.W.; Round, S.D. Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems. In IEE Proceedings: Electric Power Applications Conference, Canterbury, UK, September 2006.
44. Cornell Dubilier Staff. Application Guide to Aluminum Electrolytic Capacitors. Available online: <http://www.abb.com> (accessed on 9 June 2010).
45. ABB Staff. Product Guide LV Products and Systems Power Quality Product Data. Available online: <http://www.abb.com> (accessed on 9 June 2010).
46. Saint, B. DOE distribution transformer efficiency standards. Presented at IEEE Rural Electric Power Conference. Charleston, SC, USA, April 2008.
47. Siemens MV Drive Product Guide. ROBICON Perfect Harmony, Answers for Industry. Available online: <http://www.sea.siemens.com> (accessed on 9 June 2010).
48. Bhuvaneswari, G; Mahanta, B.C. Analysis of converter transformer failure in HVDC systems and possible solutions. *IEEE Trans. Power Deliv.* **2009**, *24*, 814-821.
49. Meyer, C.; Schroder, S.; De Doncker, R.W. Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems. *IEEE Trans. Power Electr.* **2004**, *19*, 1333-1340.
50. Meyer, C.; De Doncker, R.W. Solid-state circuit breaker based on active thyristor topologies. *IEEE Trans. Power Electr.* **2006**, *21*, 450-458.
51. Tang, L.; Ooi, B. Protection of VSC-multi-terminal HVDC against DC faults. Presented at IEEE Power Electronics Specialists Conference, Cairns, Queensland, Australia, June 2002.
52. Power Transmission & Distribution: High Power Direct-Light-Triggered Thyristor Valve Technology. Available online: <http://www.sea.siemens.com> (accessed on 9 June 2010).

Appendix: Per-Unit base quantities and selected derivations

Table A1. Per-Unit base quantities for benchmark application

Power base, P_B	50 MVA
Frequency base, f_B, ω_B	60 Hz, 377 rads/s
Energy base, E_B	$E_B / f_B = 833$ kJ
AC source voltage base, V_{Bs}	13.8 kV rms
Converter AC voltage base, V_{Bph}	117 kV rms
DC voltage base, V_{Bdc}	150 kV
AC source current base, I_{Bs}	$P_B / \sqrt{3} V_{Bs} = 2092$ A rms
DC current base, I_{Bdc}	$P_B / V_{Bdc} = 333$ A
AC Impedance base, Z_{Bac}	$V_{Bs} / I_{Bs} = 6.6$ Ω
DC Impedance base, Z_{Bdc}	$V_{Bdc} / I_{Bdc} = 450$ Ω
AC Inductance base, L_{Bac}	$Z_{Bac} / \omega_B = 17.5$ mH
DC Inductance base, L_{Bdc}	$Z_{Bdc} / \omega_B = 1.2$ H
AC Capacitance base, C_{Bac}	$1 / (Z_{Bac} \omega_B) = 400$ μ F
DC Capacitance base, C_{Bdc}	$1 / (Z_{Bdc} \omega_B) = 5.9$ μ F

*Please refer to the respective converter diagrams in section 2 for voltage and current definitions.

Current Sourced Converter semiconductor selected derivations

Average arm/device current over a power cycle:

$$I_T = \frac{1}{2\pi} \int_{\alpha}^{\pi} \sqrt{2} I_{ph} \sin(\theta) d\theta = \frac{I_{ph} \sqrt{2}}{2\pi} (\cos(\alpha) + 1)$$

where: $I_{ph} = \frac{I_s}{Q_{tran}}$

Note: The thyristor only conducts for a half cycle thus the integral is bounded by π .

I_T per-unitized to the source current yields:

$$I_{T_pu} = \frac{1}{\pi \sqrt{2} Q_{tran}} (\cos(\alpha) + 1)$$

The device voltage may be determined as the dc voltage divided by the number devices in series and accounting for an additional redundant module:

$$V_T = \frac{V_{dc}}{N_{csc} + 1}$$

per-unitized to the dc voltage:

$$V_{T_pu} = \frac{1}{N_{csc} + 1}$$

To accurately size the CSC output inductor, a simple energy approach is employed.

$$\frac{1}{2} L_{csc} (I_{max}^2 - I_{min}^2) N_p f_p = P_{out}$$

$$L_{csc} = \frac{2P_{out}}{(I_{max}^2 - I_{min}^2) N_p f_p}$$

Selecting $L_B = \frac{P_B}{I_{Bdc}^2 \omega_B}$ and a 20% ripple $L_{csc_pu} = \frac{4\pi}{(1.1^2 - 0.9^2) N_p}$

Voltage Sourced Converter semiconductor device current and voltage derivations

For a VSC the average arm, transistor, and diode currents may be defined as [13]:

$$I_{arm} = \frac{\sqrt{2}}{\pi} I_{ph}, I_T = \frac{1}{\pi \sqrt{2}} I_{ph} + \frac{1}{6} I_{dc} \text{ and } I_D = \frac{1}{\pi \sqrt{2}} I_{ph} - \frac{1}{6} I_{dc}$$

where: $I_{ph} = \frac{I_s}{Q_{tran}}$ & $I_{dc} = \frac{\pi I_{ph}}{\sqrt{6}}$

After substituting I_{ph} and I_{dc} and per-unitizing to the source current the arm/device currents may be written as:

$$I_{arm_pu} = \frac{\sqrt{2}}{\pi Q_{tran}}, I_{T_pu} = \frac{1}{\sqrt{2} \pi Q_{tran}} + \frac{\pi}{6 \sqrt{6} Q_{tran}} \text{ and } I_{D_pu} = \frac{1}{\sqrt{2} \pi Q_{tran}} - \frac{\pi}{6 \sqrt{6} Q_{tran}}$$

The device voltage may be determined as the dc voltage divided by the number devices in series and accounting for an additional redundant module:

$$V_T = V_D = \frac{V_{dc}}{N_{vsc} + 1}$$

per-unitized to the dc voltage: $V_{T_pu} = V_{D_pu} = \frac{1}{N_{vsc} + 1}$

To accurately size the VSC dc bus capacitor, a simple energy approach is employed.

$$\frac{1}{2} C_{vsc} (V_{max}^2 - V_{min}^2) f_{sw} = P_{out}$$

$$C_{vsc} = \frac{2P_{out}}{(V_{max}^2 - V_{min}^2) f_{sw}}$$

selecting $C_B = \frac{P_B}{V_{Bdc}^2 \omega_B}$ and a 10% ripple $C_{vsc_pu} = \frac{4\pi}{(1.05^2 - 0.95^2) N_{pulse}}$

Bridge of Bridge Converter semiconductor device current and voltage derivations

The BoBC arm current may be defined as having dc and ac current components. In this case, 1/3 the dc current and 1/2 the phase current flow in each arm [13].

$$I_{arm}(t) = \frac{I_{ph}}{\sqrt{2}} \sin(\omega t) + \frac{I_{dc}}{3}$$

The sub-module dc bus capacitor current is defined as the product of the arm current $I_{arm}(t)$ and the sub-module duty ratio $d_{sm}(t)$. Since the average capacitor current over a power cycle must be zero the transistor and diode currents I_{T1} and I_{D1} must have equivalent average values over one cycle as well. With this, the currents may be calculated as follows:

$$d_{sm}(t) = \frac{V_{dc}/2 - V_{ph}(t)}{N_{bobc} V_{Csm}}$$

where: $V_{ph}(t) = V_{ph} \sqrt{2} \sin(\omega t)$ & assuming $V_{Csm} = \frac{V_{dc}}{N_{BoBC}}$

$$I_{cap_avg} = 2I_{T1} = 2I_{D1} = \frac{1}{T_p} \int_0^{T_p} |I_{arm}(t) d_{sm}(t)| dt$$

solving for I_{T1} and I_{D1} , we obtain:

$$I_{T1} = I_{D1} = \frac{I_{dc}}{12} + \frac{I_{ph}}{\pi 2\sqrt{2}} - \frac{V_{ph}}{12V_{dc}} \left(3I_{ph} + \frac{4}{\pi} \sqrt{2} I_{dc} \right)$$

The average arm current is calculated in a similar fashion

$$I_{arm_avg} = \frac{1}{T_p} \int_0^{T_p} |I_{arm}| dt \quad I_{arm_avg} = \frac{I_{dc}}{3} + \frac{\sqrt{2} I_{ph}}{\pi}$$

We will now re-write these expressions in terms of the source current and the BoBC apparent transformer ratio Q_{bobc} , which is identical to the ratio of the actual transformer used in the CSC and VSC.

$$V_{dc} = \frac{6}{\pi} \int_0^{\pi/6} \sqrt{2}\sqrt{3}Q_{bobc}V_{ph} \cos(\theta)d\theta, V_{dc} = \frac{3\sqrt{6}Q_{bobc}}{\pi}V_{ph}$$

Assuming unity power factor operation, we may write the dc current in terms of the phase current

$$V_{dc}I_{dc} = 3V_{ph}I_{ph}, I_{dc} = \frac{\pi}{\sqrt{6}Q_{bobc}}I_{ph}$$

$I_{ph} = I_s$ since $Q_{tran} = 1$, i.e., the BoBC uses an isolation transformer with a 1:1 ratio or no transformer at all. After substituting V_{dc} , I_{dc} , and I_{ph} along with per-unitizing to the source current the arm and device currents may be written as:

$$I_{arm} = \frac{\pi}{3\sqrt{6}Q_{bobc}} + \frac{\sqrt{2}}{\pi}, I_{T1} = I_{D1} = \frac{1}{2\pi\sqrt{2}} - \frac{\pi\sqrt{2}}{54Q_{bobc}^2} \approx \frac{1}{2\pi\sqrt{2}} \text{ as } Q_{bobc} \text{ grows large}$$

$$I_{T2} = I_{D2} = \frac{I_{arm}}{2} - I_{T1} = \frac{1}{2\pi\sqrt{2}} + \frac{\pi}{3\sqrt{6}Q_{bobc}} + \frac{\pi\sqrt{2}}{54Q_{bobc}^2} \approx \frac{1}{2\pi\sqrt{2}} \text{ as } Q_{bobc} \text{ grows large}$$

The device voltage may be determined as the dc voltage divided by the number of sub-modules in series plus an additional redundant module:

$$V_T = V_D = \frac{V_{dc}}{N_{bobc} + 1}$$

per-unitized to the dc voltage: $V_{T_pu} = V_{D_pu} = \frac{1}{N_{bobc} + 1}$

The rms sub-module capacitor current may be calculated as follows:

$$i_{cb_rms} = \sqrt{\frac{1}{T_p} \int_0^{T_p} (I_{arm}(t)d_{sm}(t))^2 dt}$$

This after evaluation and algebraic manipulation may be expressed as:

$$i_{cb_rms} = \sqrt{\frac{I_{ph}^2}{16} - \frac{I_{dc}^2}{24} + \frac{I_{dc}^2V_{ph}^2}{9V_{dc}^2}}$$

This expression may be per-unitized to the source current after writing the dc values in terms of the source and phase quantities respectively with the identities used in earlier BoBC derivations.

$$i_{cb_rms_pu} = \sqrt{\frac{1}{16} - \frac{\pi^2}{144Q_{bobc}^2} + \frac{\pi^4}{2916Q_{bobc}^4}} \approx \frac{1}{4} \text{ as } Q_{bobc} \text{ grows large}$$