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Variable Amplitude Gate Voltage Synchronous Drive Technique for Improving Dynamic Current Balancing in Paralleled IGBTs

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Abstract: The problem of current sharing imbalance in the parallel connection of IGBT multi-modules affects the wide-scale application of parallel IGBT. The current imbalance problem in the dynamic process is mainly caused by the difference in control loop parameters. In parallel IGBT applications, current sharing is a critical concern. Objective differences in IGBT module and driver circuit parameters, as well as incomplete symmetry in the power circuit, lead to inconsistent parasitic parameters, resulting in both static and dynamic current-sharing issues. Static current sharing refers to the uneven distribution of load current under static operating conditions, while dynamic current sharing refers to the imbalance in current distribution among parallel IGBT modules during turn-on and turn-off processes. This is mainly influenced by the synchronization of turn-on and turn-off timings and the consistency of collector current change rates during these processes. The difference in characteristic parameters of IGBT modules is an important factor leading to the difference in control loop parameters, which has a profound impact on the dynamic current-sharing characteristics of IGBT parallel applications. In the case where the device parameters cannot be changed, some drive compensation controls can compensate for the influence of device differences on dynamic current sharing. Accurate identification of the characteristic parameters of the IGBT module is the key to this method. This paper mainly studies a synchronous variable-amplitude drive scheme and studies the influence of parameters such as synthetic gate resistance, gate-emitter capacitance, and on-off gate threshold voltage on the dynamic current-sharing characteristics. The correlation characteristics of the characteristic parameters of the IGBT device body are studied, and the characteristic model of each parameter and the influencing variable is constructed. The parallel working model of PSpice devices is established, and the influence of different characteristic parameters on the current-sharing characteristics is evaluated, and its sensitivity is summarized through simulation analysis. Through the 1700 V/300 A IGBT parallel switch characteristic experiment, the current sharing effectiveness of the synchronous variable amplitude driving method is verified. Finally, the effects of different gate control voltages and different action times on the dynamic current-sharing characteristics are summarized.

Keywords: paralleled IGBT; dynamic current-sharing characteristics; gate voltage control; synchronous variable-amplitude drive

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1. Introduction

Due to the reliable hardware structure, simple control system, and low overall system cost, paralleling IGBT modules is an effective way to increase the transmission capacity of the converter system in high-voltage and large-capacity converter applications such as traction drive, wind power generation, and smart grid. When multiple IGBT modules are used in parallel, the power loop structure, drive control capability, IGBT device characteristic

parameters, and junction temperature variation distribution may cause static and dynamic uneven current problems of IGBT. Optimizing the control structure and the power loop design can minimize the influence of different branch parameters on the current sharing [1–4]. The symmetrical design of the power loop is adopted to optimize the layout's physical size and mounting structure [5]. The power loop's equivalent circuit impedance formation material, form, and current path are considered for impedance matching design in [6–8]. In addition, the low-inductance connection technology, the optimization of the electromechanical connection, and device layout design [9] are adopted, which can effectively reduce the influence of power loop impedance differences and parasitic parameters on current inhomogeneity. The current density distribution of parallel branches caused by the difference in physical structure and stray impedance when the same circuit has different layouts and optimizes the design of the parallel power circuit is studied in [10]. The difference in control loop parameters is the key to affecting the dynamic current-sharing characteristics of IGBTs in parallel. In practical applications, most control loops are symmetrically designed to synchronize the gate pulses to reduce the influence [11–13]. Using a universal grid design, the collector current balance is adjusted by controlling the grid resistance and parasitic inductance values to minimize delay and voltage level issues.

Furthermore, temperature is an important parameter affecting and relating to static current sharing. To ensure the consistency of characteristic parameters, it is necessary to realize parallel current sharing [14,15]. Consistency requirements include the characteristic curve $V_{CE(sat)}$-i_C, the batch of modules with a positive temperature coefficient, and the same $V_{GE(th)}$ and temperature T_j. The higher the temperature, the higher the saturation. The larger the voltage drop, the more suitable for a parallel connection. In the literature [16], an asynchronous drive method is proposed to adjust the consistency of the opening and closing moments of each branch.

Due to the inherent differences in the characteristic parameters of the power devices in each parallel branch and the objective constraints of the design of the drive signal branch, there are certain differences in the dynamic current-sharing characteristics. Using a fully synchronous driving voltage to control the opening and closing of parallel IGBTs cannot achieve better dynamic current sharing [17]. By analyzing the relationship between voltage and current in the dynamic process, one branch is selected as the reference branch, and a driving voltage with a set amplitude is applied for some time during the current change stage of the other branch, so that the current slope of the controlled branch changes, to achieve the purpose of equalization. Reduce or even offset the above effects as much as possible.

This paper proposes a synchronous variable-amplitude current-sharing method and a current-sharing index to evaluate the current distribution. First, the four characteristic parameters of the IGBT module device body are studied [18–20], and the influencing variables of the characteristic parameters are analyzed. Then, the mathematical expression and physical model of the characteristic parameters are constructed, and the compensation value of the synchronous variable amplitude drive is deduced and calculated. Through the simulation analysis and experimental test, the effectiveness of the synchronous variable-amplitude driving method is verified. Finally, through parameter extraction, the characteristic parameters of the IGBT module with two modules connected in parallel are obtained, and the influence of different gate control voltages and different action times on the dynamic current-sharing characteristics is verified.

2. Modeling and Analysis of the Method of Synchronous Variable-Amplitude Drive of IGBTs in Parallel for Current Sharing Control

Figure 1 shows the circuit diagram of the parallel IGBT application circuit diagram including characteristic parameters affecting current sharing. The separate drive circuit and control loop correspond to the individual IGBT module. In the figure, the power loop is symmetrical and centralized. The drive and control loops are independent.

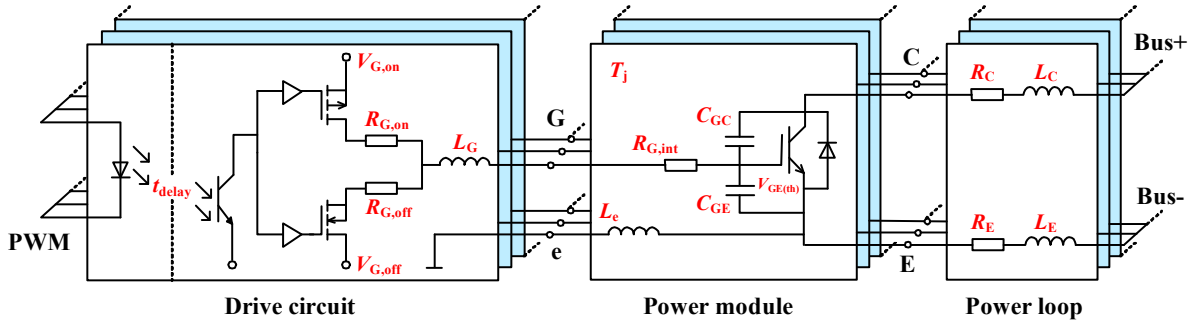
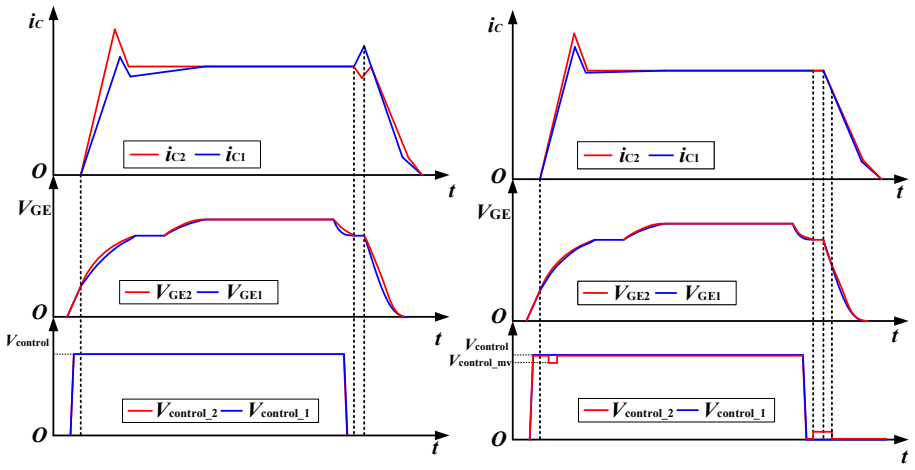


Figure 1. Circuit diagram of the parallel IGBT application circuit diagram including characteristic parameters affecting current sharing.

Among them, t_{delay} is the signal transmission delay time; $V_{G,on}$ is the gate turn-on voltage; $V_{G,off}$ is the gate turn-off voltage; $R_{G,on}$ is the gate turn-on resistance; $R_{G,off}$ is the gate turn-off resistance; $R_{G,int}$ is the gate module internal resistance; T_j is the junction temperature; L_e is the module emitter inductance; C_{GC} is the gate collector capacitance; C_{GE} is the gate emitter capacitance; L_G is the gate inductance; L_C is the collector inductance; L_E is the emission pole inductance; R_C is the collector resistance; R_E is the emitter resistance.

The driving principle of the synchronous variable-amplitude driving method is shown in Figure 2. For the case of ordinary synchronous pulse driving, it is shown in Figure 2a, assuming that the power loop parameters of IGBT module 1 and module 2 are completely consistent. Under the action of $V_{control\_2}$, due to the differences in the characteristic parameters of the drive circuit such as gate resistance, gate threshold voltage, and input capacitance, the variation trends of the gate voltage V_{GEx} and collector current i_{Cx} of modules 1 and 2 are different in the dynamic process. The main performance is the dynamic uneven current caused by the asynchrony of the collector current at the turn-on and turn-off moments and the difference in rising and falling rates. As shown in Figure 2b, the synchronous variable-amplitude driving method introduces the calculated gate control voltage into the IGBT module 1 driving circuit to improve the synchronization of the two modules at the time of turning on and off, thereby improving the dynamic current sharing.



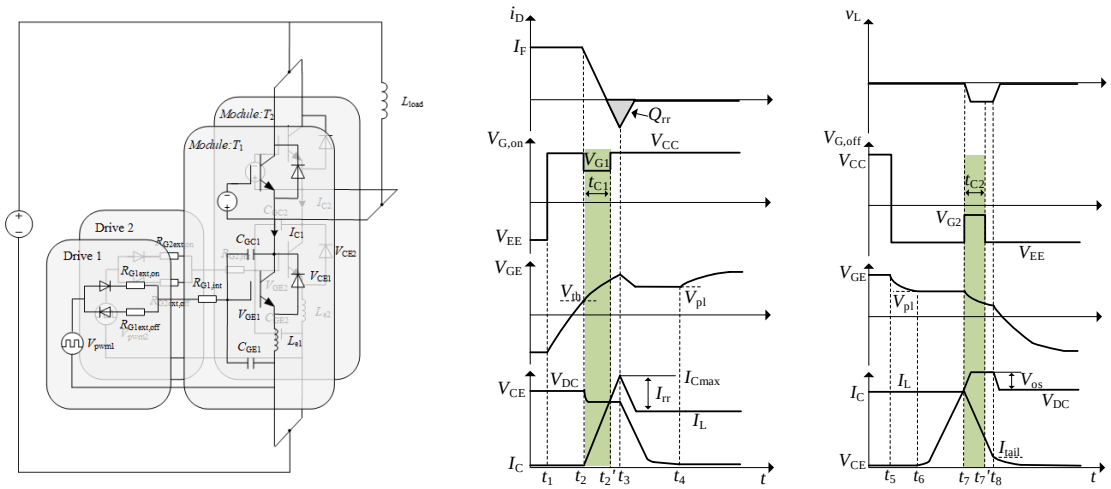
(**a**) Uncompensated (**b**) Compensated

Figure 2. The principle of synchronous variable-amplitude driving method.

2.1. Analysis of the IGBT Operation Process with Synchronous Variable-Amplitude Driving Method

For better description and illustration, this paper analyzes the case of two IGBT modules connected in parallel, as shown in Figure 3a. Figures 3b and 3c represent the

waveforms of the turn-on and turn-off processes. The gate loop parameters can significantly impact the switching process. Meanwhile, the influence of gate loop parameters on IGBT operation concentrates on the turn-on delay, the collector current rise, the turn-off delay, and the collector voltage rise.



(**a**) Dual-module parallel equivalent circuit model

(**b**) Turn on waveform

(**c**) Turn off waveform

Figure 3. Dual-module parallel equivalent circuit model and process waveform.

2.1.1. Turn-On Delay

The driving circuit applies a forward voltage $V_{\mathrm{Gx,on}}$, representing the parallel branch number, defined as 1, 2 in this paper). It charges the input capacitor C_{iesx} through the gate resistor $R_{\mathrm{Gx,on}}$. Hence, the voltage across C_{iesx} gradually rises. The input capacitor C_{iesx} is the gate-emitter capacitor C_{GEx}. The IGBT gate voltage V_{GEx} rises to the turn-on threshold voltage $V_{\mathrm{GE(th)x}}$.

At t_1~t_2 stage, the MOS channel has not yet been formed, the collector current i_{Cx} is 0, and the collector-emitter voltage V_{CE} is the same as the bus voltage. The circuit formula is as follows:

$$\begin{cases} V_{\mathrm{Gx,on}} = R_{\mathrm{Gx,on}} C_{\mathrm{iesx}} \frac{dv_{\mathrm{GEx}}}{dt} + v_{\mathrm{GEx}} \\ V_{\mathrm{GEx}}(0) = V_{\mathrm{Gx,off}} \\ I_{\mathrm{Cx}} = 0 \end{cases} \tag{1}$$

where $V_{\mathrm{Gx,on}}$ is the turn-on drive voltage used by the drive control circuit, and $V_{\mathrm{Gx,off}}$ is the turn-off drive voltage used by the drive control circuit. The turn-on gate resistance $R_{\mathrm{Gx,on}}$ is the sum of the external drive resistance and the built-in resistance of the IGBT module given in the device manual for actual use.

The turn-on delay stage expression of the gate voltage V_{GE} is obtained by solving the resistor-capacitance circuit formula, and the turn-on delay time $t_{\mathrm{d(on)x}}$ is obtained by substituting $V_{\mathrm{Gex}} = V_{\mathrm{GE(th)x}}$, as shown in Formula (2):

$$t_{\mathrm{d(on)x}} = -C_{\mathrm{iesx}} R_{\mathrm{Gx},on} \cdot \ln \frac{V_{\mathrm{G,on}} - V_{\mathrm{GE(th)x}}}{V_{\mathrm{Gx,on}} - V_{\mathrm{Gx,off}}} \tag{2}$$

2.1.2. Collector Current Rise

When the gate voltage exceeds the turn-on threshold voltage, the collector current i_{Cx} rises rapidly. The anti-parallel diode goes to the off-state. At the same time, the V_{CE} begins to drop until i_{Cx} rises to the load current. At this stage, the gate circuit is shown in Formula (3). The expression of the collector current is shown in Formula (4):

$$V_{\mathrm{Gx,on}} = v_{\mathrm{GEx}} + R_{\mathrm{Gx,on}} C_{\mathrm{iesx}} \frac{dv_{\mathrm{GEx}}}{dt} + L_{\mathrm{Ex}} \frac{di_{\mathrm{Cx}}}{dt} \tag{3}$$

$$i_{Cx} = \begin{cases} 0 & v_{GEx} \le V_{GE(th)x}, V_{CE} < 0 \\ K\left((v_{GEx} - V_{GE(th)x}) - \frac{1}{2}V_{CE}^2\right) & v_{GEx} > V_{GE(th)x}, V_{CE} \le v_{GEx} - V_{GE(th)x} \\ \frac{K}{2}(v_{GEx} - V_{GE(th)x})^2 & V_{CE} > v_{GEx} - V_{GE(th)x} > 0 \end{cases} \quad (4)$$

where L_{Ex} is the auxiliary emitter inductance, and K is the equivalent transconductance. g_{fsx} is the forward transfer rate and can be expressed as:

$$g_{fsx} = \frac{di_{Cx}}{dv_{GEx}} = K\left(v_{GEx} - V_{GE(th)x}\right) \quad (5)$$

The above Formulas (3)–(5) can be derived to calculate the collector current rise rate, as shown in Formula (6):

$$\frac{di_{Cx}}{dt} \approx \frac{V_{GEx} - V_{GE(th)x}}{R_{Gx,on}C_{iesx}/g_{fsx} + L_{Ex}} \quad (6)$$

The current overshoot caused by the reverse recovery of the diode after the current rising stage reaches the rated value of the load current can be expressed as Formula (7), as one of the parameters for judging the dynamic characteristics of the module.

$$I_{rrx} = \sqrt{\frac{2Q_{rrx}dI_{Cx(on)}/dt}{(S+1)}} = \sqrt{\frac{2Q_{rrx}}{(S+1)}}\sqrt{\frac{V_{CC} - (\frac{I_L}{g_{fsx}} + V_{GE(th)x})}{\frac{R_{Gx,on}C_{iesx}}{g_{fsx}} + L_{Ex}}} \quad (7)$$

The equivalent principle of the current rise rate under the action of the drive control voltage is shown in Figure 4. The idea of average equivalent is adopted in the whole current change process [21], and the current rise rate before and after the drive control is added is replaced by the equivalent current rise rate. The analysis of current unbalance is calculated by the equivalent current rise rate.

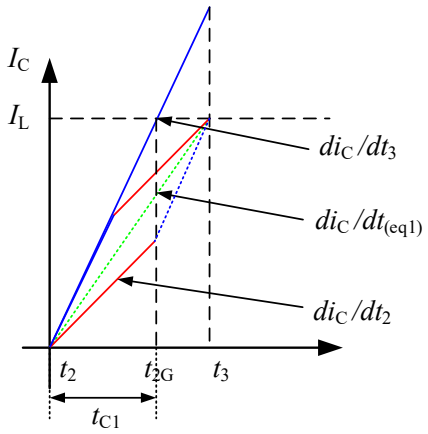


Figure 4. Equivalent schematic diagram of turn-on current rise rate.

In Figure 4, t_3 represents the moment when the collector current i_C rises to the maximum value i_{Cmax}, the gate control voltage in the initial state is V_{CC}, when the gate drive control voltage introduced in the t_2-t_{2G} stage is V_{G1}, the corresponding current slope is di_C/dt_2, the action time of introducing V_{G1} is t_{C1}; after the action time ends, the gate drive voltage returns to V_{CC} in the t_{2G}~t_3 stage, and the corresponding current slope is di_C/dt_3, and di_C/dt_2 and di_C/dt_3, etc. The effect is the current slope $di_C/dt_{(eq1)}$, which can be equivalently expressed by di_C/dt_2 and di_C/dt_3 as:

$$\frac{di_C}{dt_2}t_{C1} + \frac{di_C}{dt_3}(t_3 - t_2 - t_{C1}) = \frac{di_C}{dt_{(eq1)}}(t_3 - t_2) = I_L \quad (8)$$

Substituting Formula (8) into Formula (6), the relationship between the equivalent current slope $di_C/dt_{(eq1)}$ and characteristic parameters can be obtained as:

$$\frac{di_C}{dt_{(eq1)}} = \frac{di_C}{dt_3} I_L / [I_L + (\frac{di_C}{dt_3} - \frac{di_C}{dt_2}) t_{C1}] = \frac{V_{CC} - (\frac{I_L}{g_{fs}} + V_{GE(th)})}{(\frac{R_{G,on} C_{ies}}{g_{fs}} + L_E) + \frac{(V_{CC} - V_{G1}) t_{C1}}{I_L}} \tag{9}$$

From the Formula (9), it can be known that the gate control voltage V_{G1} and the action time t_{C1} have a control effect on the equivalent current slope $di_C/dt_{(eq1)}$, and the action time t_{C1} ranges from 0 to t_3-t_2. The duration of this stage is divided into the current rising from 0 to the load current, and the current rising from the load current to the maximum current overshoot under the action of the anti-parallel diode. The duration of the ramp-up to load current phase can be expressed as:

$$t_{2-2G} = \frac{I_L}{\mathrm{d}i_C/\mathrm{d}t_{(eq1)}} = \frac{I_L \cdot \left(\frac{R_{G,on} C_{ies}}{g_{fs}} + L_E\right) + (V_{CC} - V_{G1}) t_{C1}}{V_{CC} - \left(\frac{I_L}{g_{fs}} + V_{GE(th)}\right)} \tag{10}$$

The equivalent current overshoot I_{rr} can be obtained by solving Formulas (7) and (9):

$$I_{rr} = \sqrt{\frac{2 Q_{rr} di_C/dt_{(eq1)}}{(S+1)}} = \sqrt{\frac{2 Q_{rr}}{(S+1)}} \sqrt{\frac{V_{CC} - (\frac{I_L}{g_{fs}} + V_{GE(th)})}{(\frac{R_{G,on} C_{ies}}{g_{fs}} + L_E) + \frac{(V_{CC} - V_{G1}) t_{C1}}{I_L}}} \tag{11}$$

The reverse recovery time factor usually takes S = 1, so the duration of the t_{2G}~t_3 stage from the load current rise to the maximum current overshoot is:

$$t_{2G-3} = \sqrt{Q_{rr} \frac{(\frac{R_{G,on} C_{ies}}{g_{fs}} + L_E) + \frac{(V_{CC} - V_{G1}) t_{C1}}{I_L}}{V_{CC} - (\frac{I_L}{g_{fs}} + V_{GE(th)})}} \tag{12}$$

From Formulas (11) and (12), we can see that $t_{2–3}$ is negatively correlated with V_{G1} and positively correlated with t_{C1}, and I_{rr} is positively correlated with V_{G1} and negatively correlated with t_{C1}.

In the case of parallel connection of IGBT modules T_1 and T_2, the current rise rate of module T_2 is adjusted with module T_1 as a reference, that is, $di_{C1}/dt = di_{C2}/dt_{eq1}$, so after compensation, the current rise rate compensation value at this stage is:

$$\begin{aligned} \varepsilon_{on} &= (V_{CC} - V_{G1}) t_{C1} \\ &= I_L \cdot \left[\frac{V_{CC} - \left(\frac{I_L}{g_{fs2}} + V_{GE(th)2}\right)}{V_{CC} - \left(\frac{I_L}{g_{fs1}} + V_{GE(th)1}\right)} \left(\frac{R_{G1,on} C_{ies1}}{g_{fs1}} + L_{E1}\right) - \left(\frac{R_{G2,on} C_{ies2}}{g_{fs2}} + L_{E2}\right) \right] \end{aligned} \tag{13}$$

2.1.3. Turn-Off Delay

The turn-off process is the capacitor discharge process, which is the opposite of the turn-on process. Before the shutdown signal arrives, the IGBT is in the on-state [22–24]. And the gate voltage is $V_{GEx} = V_{Gx,on}$. Hence, the collector voltage is the on-state saturation voltage drop $V_{CE(sat)}$. After the shutdown signal arrives, the input capacitor C_{iesx} begins to discharge, and the gate voltage drops until it reaches $V_{GE(pl)x}$. Similar to the turn-on delay stage, the turn-off delay time of this stage is shown in the Formula (14):

$$t_{d(off)x} = -C_{iesx} R_{Gx,off} \ln \frac{V_{GE(pl)x} - V_{Gx,off}}{V_{Gx,on} - V_{Gx,off}} \tag{14}$$

2.1.4. Collector Voltage Rise

When the gate voltage drops to the Miller plateau, the gate current i_{Gx} passes almost only through the gate collector capacitor C_{GCx}, and the collector voltage rises. The gate voltage is maintained near the Miller plateau voltage $V_{GE(pl)x}$. The rising rate of the collector voltage at this time is shown in Formula (15):

$$\frac{dv_{CEx}}{dt} = \frac{i_{Gx}}{C_{GCx}} = \frac{V_{GE(pl)x} - V_{Gx,off}}{R_{Gx,off}C_{GCx}} \tag{15}$$

2.1.5. Collector Current Drop Stage

After V_{CE} reaches V_{DC}, the collector current starts to drop from the load current. The current drop rate in this stage can be expressed as:

$$\frac{di_{Cx}}{dt} = \frac{V_{Gx,off} - (\frac{I_L}{g_{fsx}} + V_{GE(th)x})}{\frac{R_{Gx,off}C_{iesx}}{g_{fsx}} + L_{Ex}} \tag{16}$$

The collector voltage process generated at this stage is mainly due to the induced voltage generated by the current change on the parasitic inductance of the power loop, and the voltage overshoot V_{os} can be expressed as:

$$V_{os} = L_p\left|\frac{di_{c(off)}}{dt}\right| = L_p\frac{(\frac{I_L}{g_m} + V_{th}) - V_{EE}}{\frac{R_{\Sigma}C_{ies}}{g_m} + L_E} \tag{17}$$

Similarly, according to the current equivalent principle of the equivalent schematic diagram of the turn-off current drop rate in Figure 5, where the influence of the tail current is ignored, it is considered that the current is zero at time t_8, and the equivalent current slope di_C/dt of the turn-off process at this time can be expressed as:

$$\frac{di_c}{dt_{(eq2)}} = \frac{V_{EE} - (V_{GE(th)} + \frac{I_L}{g_{fs}})}{(\frac{R_{G,off}C_{ies}}{g_{fs}} + L_E) + \frac{(V_{EE}-V_{G2})t_{C2}}{I_L}} \tag{18}$$

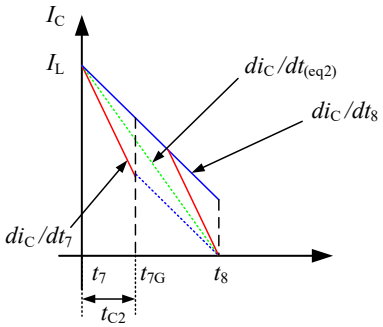


Figure 5. Equivalent schematic diagram of turn-off current rise rate.

It can be seen from the Formula (18) that the gate control voltage V_{G2} and the action time t_{C2} have a control effect on the equivalent current slope $di_C/dt_{(eq2)}$ in the current falling stage, ignoring the influence of the tail current, and the value range of the action time t_{C2} is 0~t_8-t_7.

Solving the Formulas (17) and (18), the equivalent voltage overshoot V_{os} of the turn-off process can be obtained as:

$$V_{os} = L_P\left|\frac{di_C}{dt_{(eq2)}}\right| = L_P\frac{(V_{GE(th)} + \frac{I_L}{g_{fs}}) - V_{EE}}{(\frac{R_{G,off}C_{ies}}{g_{fs}} + L_E) + \frac{(V_{EE}-V_{G2})t_{C2}}{I_L}} \tag{19}$$

The duration of this phase can be expressed as:

$$t_{7-8} = \frac{I_L - I_{tail}}{\left|di_c/dt_{eq2}\right|} = (I_L - I_{tail})\frac{\left(\frac{R_{G,off}C_{ies}}{g_{fs}} + L_E\right) + \frac{(V_{EE}-V_{G2})t_{C2}}{I_L}}{\left(V_{GE(th)} + \frac{I_L}{g_{fs}}\right) - V_{EE}} \tag{20}$$

From the Formulas (19) and (20), we can see that the voltage overshoot V_{os} is negatively correlated with V_{G2} and positively correlated with t_{C2}; t_{7-8} is negatively correlated with V_{G2} and positively correlated with t_{C2}.

In the case of parallel connection of IGBT modules T_1 and T_2, module T_1 is used as a reference to adjust the current rise rate of module T_2, that is, $di_{C1}/dt = di_{C2}/dt_{eq2}$. Therefore, after compensation, the compensation value of the current drop rate at this stage is:

$$\begin{aligned} \varepsilon_{off} &= (V_{EE} - V_{G2})t_{C2} \\ &= I_L \cdot \left[\frac{V_{EE} - \left(\frac{I_L}{g_{fs2}} + V_{GE(th)2}\right)}{V_{EE} - \left(\frac{I_L}{g_{fs1}} + V_{GE(th)1}\right)}\left(\frac{R_{G1,off}C_{ies1}}{g_{fs1}} + L_{E1}\right) - \left(\frac{R_{G2,off}C_{ies2}}{g_{fs2}} + L_{E2}\right)\right] \end{aligned} \tag{21}$$

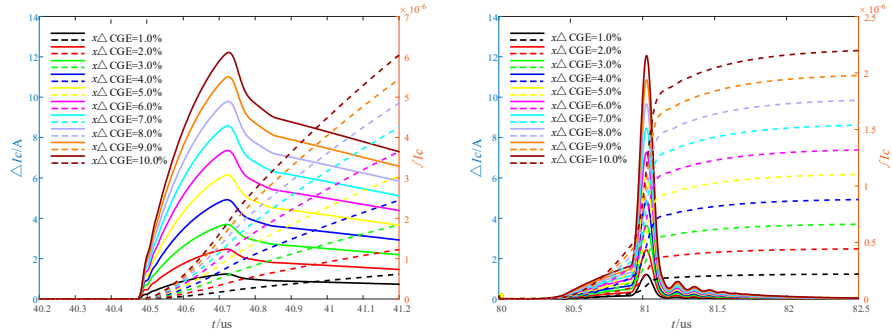
Through the analysis of the turn-on and turn-off process, it can be seen that the characteristic parameters of the drive circuit, including the gate-emitter capacitance C_{GE}, the gate-collector capacitance C_{GC}, the gate resistance R_G and the turn-on threshold voltage $V_{GE(th)}$, will affect the parameters of each parallel branch. Current dynamic characteristics in the process of IGBT switching.

2.2. PSpice Modeling with the IGBT Parameters

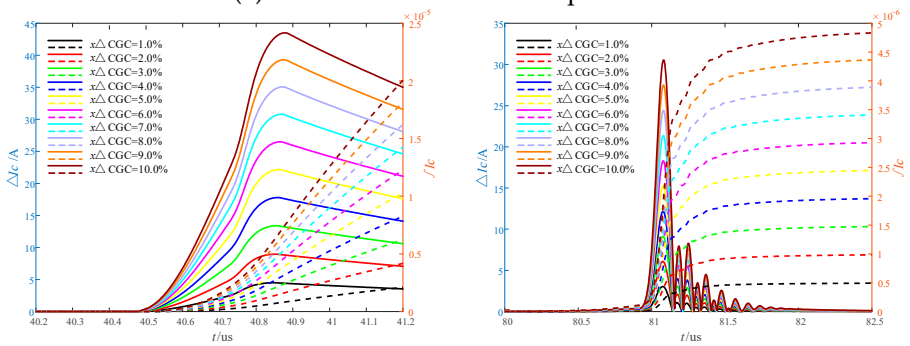
The synchronous variable-amplitude driving model is constructed using PSpice for two parallel IGBTs. Meanwhile, the influence of the gate loop characteristic parameters on the current sharing is compared and analyzed. ΔIc is the collector current difference between T_1 and T_2 modules, expressed as $\Delta Ic = Ic_1 - Ic_2$. This value can represent the degree of current balance in the switching process. The formula follows $\int_{t_0}^{t_1} \Delta I_C = \int_{t_0}^{t_1} |I_{C1} - I_{C2}| dt$ (t_0~t_1 is the opening process) and $\int_{t_2}^{t_3} \Delta I_C = \int_{t_2}^{t_3} |I_{C1} - I_{C2}| dt$ (t_2~t_3 is the shutdown process). The current difference and current integral can be used as the evaluation index of current balance. At the same time, the degree of current imbalance can be expressed as:

$$\delta = \frac{I_{Cmax} - I_{Cmin}}{I_{Cmax} + I_{Cmin}} \tag{22}$$

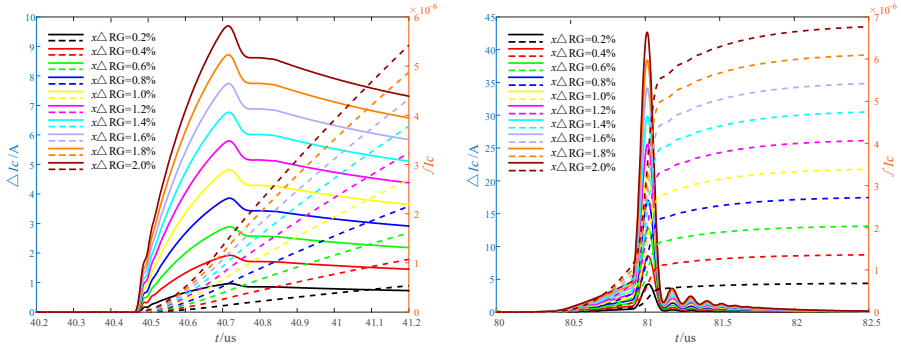
Figure 6a shows the current difference curve and integral curve when the relative difference of the gate-emitter capacitance of the T_1 and T_2 modules is different, reflecting the current difference of the two branches under this working condition. It can be seen from the figure that the gate-emitter capacitance error has a greater impact on the turn-on process; the greater the relative value of the gate-emitter capacitance difference, the smaller the current rise rate, and the more unbalanced the current distribution in the dynamic process. Figure 6b shows the influence of the relative difference of the gate-collector capacitance parameters on the turn-on and turn-off processes. It can be seen that the gate-emitter capacitance error has a more obvious impact on the turn-on process, the greater the relative value of the gate-emitter capacitance parameter difference, the smaller the current rise rate, and the more unbalanced the current distribution in the dynamic process. Figure 6c shows the influence of the relative difference of gate resistance parameters on the turn-on and turn-off processes. It can be seen that the larger the relative value of the gate resistance difference, the smaller the current rise rate, and the more unbalanced the current distribution in the dynamic process, and the impact on the turn-off process is more obvious than that in the turn-on process. Figure 6d shows the influence of the relative difference of the conduction threshold voltage parameter on the turn-on and turn-off processes. The larger the relative value of the conduction threshold voltage parameter difference, the smaller the current rise rate, and the more unbalanced the dynamic current distribution.



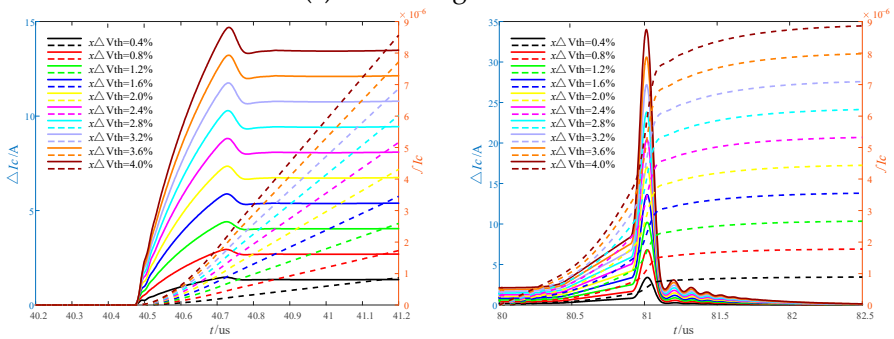
(**a**) Different Gate-Emitter capacitance



(**b**) Different Gate-Collector capacitance



(**c**) Different gate resistors

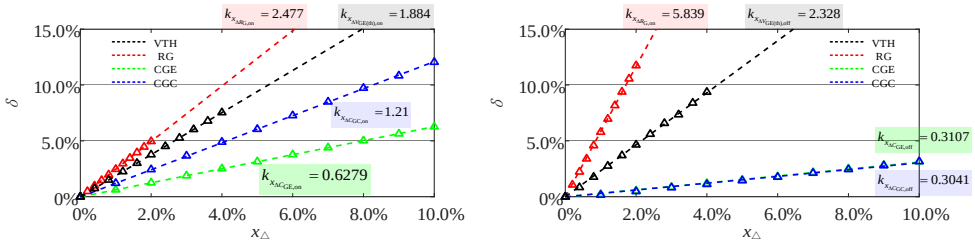


(**d**) Different turn-on threshold voltages

Figure 6. Simulation results of the influence of relative errors of different parameters on the switching process.

Combining the data comparison of the device manual and the simulation test parameters of multiple working conditions, considering the change of a single parameter itself, regardless of the simultaneous change of different parameters, the characteristic parameters and influencing factor change curves of the IGBT device are fitted, as shown in Figure 7. The figure shows the relationship between the degree of difference of different parameters and the degree of current imbalance. It can be seen that when the relative

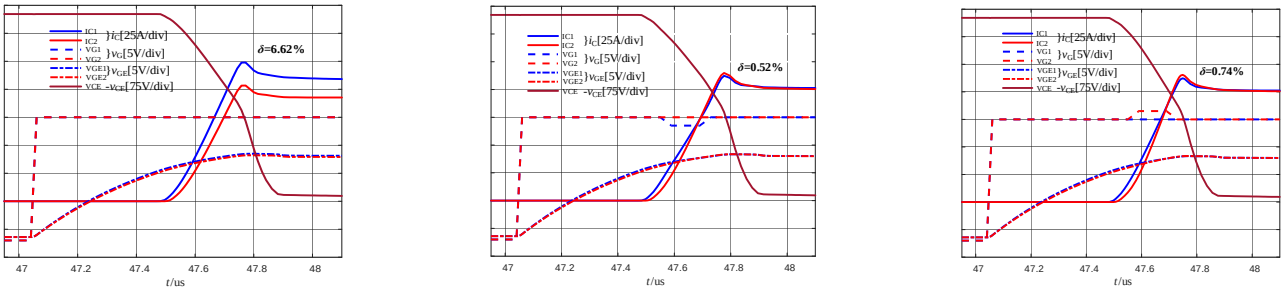
degree of difference is the same, the gate resistance has a greater impact on the turn-on and turn-off processes.



(**a**) Turn on process (**b**) Turn off process

Figure 7. The influence of different parameters on the opening and closing process. (Each triangle represents a data point).

Through the simulation analysis of the synchronous variable-amplitude driving method in PSpice, its control effect on the turn-on and turn-off process is verified. If the gate on-resistance difference of the two branches is 3.0%, compare the synchronous variable-amplitude drive method before and after compensation, as shown in Figure 8, in which (a) is the current state without synchronous variable-amplitude drive control. The current unbalance degree is 6.62%. (b) Add synchronous variable-amplitude drive control to module 1. At this time, the current unbalance degree is 0.52%. Similarly, (c) add synchronous variable-amplitude drive control to module 2. At this time, the current unbalance degree is 0.74%. It can be seen that the synchronous variable-amplitude control is effective in the opening process.

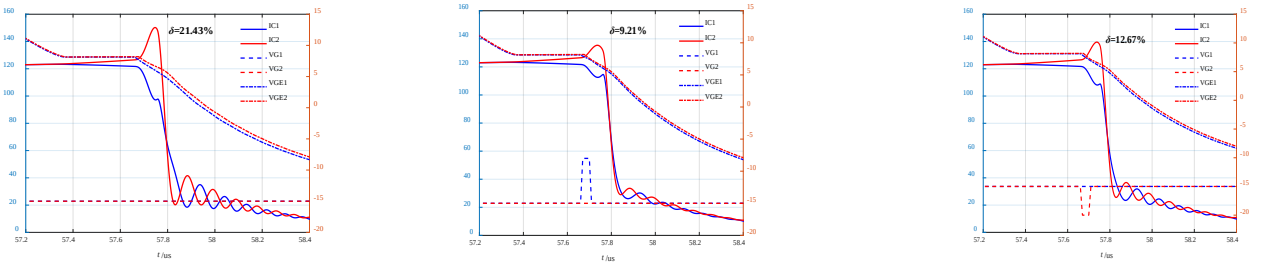


(**a**) No compensation (**b**) Module 1 adds synchronous variable-amplitude drive control (**c**) Module 2 adds synchronous variable-amplitude drive control

Figure 8. Comparison pre- and post-sync amplitude drive control in turn-on process.

If there is a gate turn-off resistance difference of 3.0% in the two branches, compare the synchronous variable-amplitude drive method before and after compensation, as shown in Figure 9a, which is the current state without adding synchronous variable-amplitude drive control. The unbalance degree is 21.43%. Figure 9b adds synchronous variable-amplitude drive control to module 1, and the current unbalance degree is 9.21%. Similarly, Figure 9c adds synchronous variable-amplitude drive control to module 2. At this time, the current unbalance degree is 12.67%, which shows the effectiveness of synchronous variable-amplitude drive control in the turn-off process. It can be seen that this method has a better current-sharing effect for the control of the turn-on process, and a symmetrical current process in the turn-off process cannot be eliminated.

Comparing the control effect of synchronous variable-amplitude drive control on the opening and closing process horizontally, it can be seen that its control process parameter adjustment in the opening process is more sensitive, so it is necessary to further analyze the adjustment range of synchronous variable-amplitude drive control.



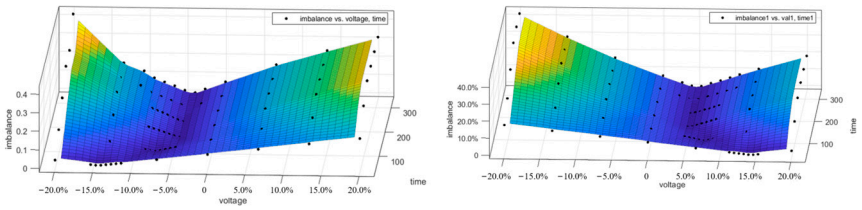
(**a**) No compensation

(**b**) Module 1 adds synchronous variable-amplitude drive control

(**c**) Module 2 adds synchronous variable-amplitude drive control

Figure 9. Comparison pre- and post-sync amplitude drive control in turn-off process.

After the addition of synchronous variable-amplitude drive control to module T_1, the action time changes from 30 ns to 330 ns with a gradient of 60 ns, and the drive control voltage changes with a gradient of 1 V from 12 V to 18 V. Do multiple simulations near the lowest point of current imbalance to analyze this. The three-dimensional relationship between gate control voltage, action time, and current imbalance can be obtained, as shown in Figure 10a. Similar to the analysis of the turn-on process, keep the gate resistor parameter variance at 3%. In this process, the parameter of the gate turn-off resistance of the T_1 module is small, and it is turned off first, and the current drop rate is larger, and the drop is slower. Considering the reliability of the module gate, the gate peak voltage is $\pm$20 V, so the simulation process adds a synchronous differential voltage to the T1 module. In amplitude control, the action time is changed from 30 ns to 120 ns according to the gradient of 30 ns, the driving control voltage is changed from $-$18 V to $-$2 V according to the gradient of 2 V, and multiple groups of simulations are performed near the lowest point of current imbalance to analyze the voltage change value during this process A summary of changes in current unbalance degree is shown in Figure 10b.



(**a**) Turn-on process

(**b**) Turn-off process

Figure 10. The three-dimensional relationship among drive control voltage, action time, and current unbalance degree in the turn-on and turn-off process. (The darker the color, the smaller the degree of current imbalance, while the lighter the color, the larger the degree of current imbalance.)

In Figure 10, the dark blue part represents the optimal relationship between the driving control voltage, action time, and current imbalance. This also conforms to an inverse proportional function relationship, and the time beyond the current decline stage no longer has a control effect. However, if the action time is continuously increased, other stages will be affected and the current distribution will further deteriorate. When using the synchronous variable-amplitude driving method, it is necessary to extract and analyze the parameters first. The control function can effectively reduce the current imbalance.

Among the characteristic parameters related to the dynamic characteristics of the IGBT module, the turn-on threshold voltage $V_{GE(th)}$, saturation voltage drop $V_{CE(sat)}$, rise time t_r, fall time t_f, turn-on delay time $t_{d(on)}$, turn-off delay time $t_{d(off)}$, the basic data can be queried from the chip manual, but the gate resistance R_G, gate-collector capacitance C_{GC}, and gate-emitter capacitance C_{GE} inside the module cannot be obtained from the chip manual. To obtain more accurate characteristic parameters from the drive control circuit, it is necessary to refer to the data in the chip manual and verify and identify it through the experimental test data.

3. Identification of the Characteristic Parameters for Parallel IGBT Modules

The parameter difference between the parallel IGBT modules and the delay time difference can be obtained by identifying the gate drive loop characteristic parameters. A control basis for the synchronous variable amplitude drive can also be provided. The specific parameters calculation formula can be deduced by analyzing the turn-on and turn-off processes. An experimental platform is built for the double-pulse test, the current and voltage waveforms of the double-pulse test are analyzed, and the actual difference range of characteristic parameters is obtained.

The principle of the IGBT module parameter extraction circuit is shown in Figure 11. The part in the dotted box is the IGBT module to be tested. The gate turn-on resistance $R_{G,on}$ and the gate turn-off resistance $R_{G,off}$ are usually composed of the gate resistance $R_{G,int}$ inside the module and the external resistance $R_{G,ext}$ on the gate drive circuit. When the collector current is the same, the observed platform voltages $V_{G2(pl),on}$ and $V_{G2(pl),off}$ during turn-on and turn-off can be expressed as:

$$V_{G2(pl),on} = V_{GE(pl)} + I_{G,on}R_{G,int} \tag{23}$$

$$V_{G2(pl),off} = V_{GE(pl)} + I_{G,off}R_{G,int} \tag{24}$$

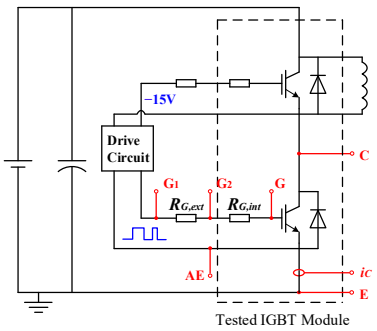
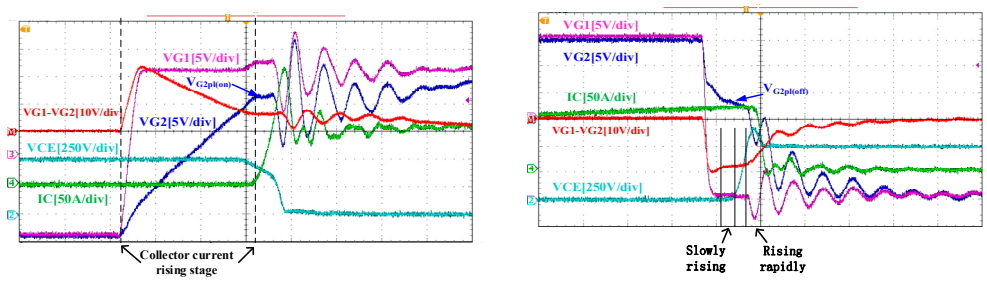


Figure 11. IGBT module parameter extraction circuit.

Since the current direction of the internal gate resistance is opposite during the turn-on and turn-off process, the inner gate resistance $R_{G,int}$ can be calculated by the Miller plateau voltage difference and the gate current difference. Figure 12 shows the experimental waveform of the double-pulse test.



(**a**) Waveform of turn-on process (**b**) Waveform of turn-off process

Figure 12. Experimental waveform of characteristic parameter extraction of IGBT module.

When the experimental data obtained in Figure 12 is substituted into the above formula, the Miller plateau voltage and the voltage of the external gate resistance can be extracted. As a result, the internal gate resistance can be calculated. In this paper, the main focus is the dynamic process of turn-on and turn-off. It can be seen from the datasheet that the junction capacitance of the IGBT module changes accordingly under the action of V_{CE}. When V_{CE} increases, the junction capacitance is stable within a stable range. In the turn-on stage, V_{CE} is high, and the capacitance is kept at a stable range. When V_{CE} drops

low, i_C reaches the rated value. Hence, the junction capacitance obtained by this parameter identification method is a relatively stable value.

The equivalent gate capacitance C_{GE} can be calculated from the loop formula in the rising stage of the collector current, as shown in formula (25):

$$\begin{aligned} v_{G_2E}(t) &= v_{GE}(t) + i_G R_{G,int} \\ &= V_{G,off} + (V_{G,on} - V_{G,off})(1 - e^{-\frac{t}{C_{GE} R_{G,on}}}) + i_G R_{G,int} \end{aligned} \tag{25}$$

By observing V_{G2E} in Figure 10a, the time and gate current of the rising stage can be obtained, and the equivalent gate capacitance C_{GE} can be solved by formula (25). The equivalent gate-collector capacitance C_{GC} is calculated by measuring the collector voltage and gate current at turn-off, according to the charging and discharging formula of the capacitor. The definition takes V_1 as the boundary to divide into the slow rise of collector voltage and the rapid increase in collector voltage. When the turning voltage V_1 is substituted into formula (26), the solution to C_{GC1} and C_{GC2} can be obtained:

$$\begin{cases} I_{G1} = C_{GC1} \frac{V_1 - V_{CE(sat)}}{\Delta T_1} \\ I_{G2} = C_{GC2} \frac{V_{CE(dc)} - V_1}{\Delta T_2} \end{cases} \tag{26}$$

The turning voltage V_1 adopts the finite difference method to carry out the quadratic derivation, and the maximum curvature point is obtained. The curvature of a curve is the rate of rotation of the tangent direction angle of an end to the arc length through differentiation, which mathematically represents the curvature of the curve at a certain point. The formula for calculating curvature is:

$$\varepsilon = |y''| / \left(1 + y'^2\right)^{\frac{3}{2}} \tag{27}$$

When $y = V_{CE(t)}$ is substituted into the above formula, the obtained V_{CE} value of the maximum point of curvature ε is the turning voltage V_1.

4. Characteristic Parameter Identification and Current Sharing Experiment

4.1. Characteristic Parameter Identification

In this paper, two FF300R17KE3 modules produced by Infineon are used as the tested objects. Through the parameter verification and identification method in this paper, the difference range of the characteristic parameters of the gate drive circuit of the two IGBTs is measured, which provides a data basis for subsequent parallel experiments. The test platform sets the bus voltage to 900 V, the load inductance to 100 μH, the gate output of the upper tube of the IGBT module is −15 V to keep it off reliably, and the gate driver of the lower tube outputs a double pulse of 15 V/−15 V. We observed the voltage V_{G1} between G1 and AE, the voltage V_{G2} between G2 and AE, the collector current IC and the collector voltage V_{CE}.

For the external resistance $R_{G,ext}$, a high-precision LCR bridge is used to measure the resistance to obtain the external turn-on gate resistance $R_{Gon,ext}$ and the external turn-off gate resistance $R_{Goff,ext}$. For the internal $R_{G,int}$, the resistance is obtained by measuring the platform voltages $V_{G2(pl)on}$ and $V_{G2(pl)off}$ and the gate currents $I_{G,on}$ and $I_{G,off}$ of the voltages between G2 and AE during the turn-on and turn-off process.By substituting them into Formulas (23) and (24), the gate turn-on resistance $R_{G,on}$ and the gate turn-off resistance $R_{G,off}$ can be obtained by combining the measured external resistance.

For the equivalent gate capacitance C_{GE}, the turn-on delay phase can be obtained by measuring the waveform during the turn-on process. The matching gate capacitance can be calculated using Formula (25). For the equivalent gate-collector capacitances C_{GC1} and C_{GC2}, the turning voltage takes the maximum point of V_{CE} rising slope curvature considering the V_{CE} rising waveform during the turn-off process. When it is substituted into Formula (26),

the equivalent capacitance of the Miller plateau can be calculated. Table 1 summarizes the extraction results of the four modules' gate drive loop characteristic parameters.

Table 1. Transmission extraction results of characteristic parameters of the gate drive circuit of each module.

Parameter Name	Parameter Values	
Test Conditions	V_{DC} = 900 V, I_L = 250 A	
IGBT Modules	1700 V^{-1}	1700 V^{-2}
$R_{G,int}$	2.41 Ω	2.33 Ω
$R_{G,on}$	4.41 Ω	4.65 Ω
$R_{G,off}$	4.39 Ω	4.35 Ω
C_{GE}	28.98 nF	29.92 nF
C_{GC1}	9.17 nF	9.29 nF
C_{GC2}	0.62 nF	0.64 nF

4.2. Current-Sharing Experiment

In the experiment, the two tested FF300R17KE3 half-bridge IGBT modules T_1 and T_2 paralleled by parameter extraction were used for double-pulse experiments. The experimental hardware circuit is shown in Figure 13. We observed the current distribution of the two modules during the turn-on and turn-off process, as shown in Figure 14a, and calculated the compensation value of the turn-on process to be 27.6. It can be seen that the current rise rate of module 1 in the turn-on process before the synchronous variable-amplitude drive compensation is introduced is larger, consistent with the calculation results and theoretical analysis trends. Before the introduction of synchronous variable-amplitude drive control, the current unbalance degree in the opening process is 12.36%, and the current peak value is 582 A. At this time, the turn-off process is relatively current sharing, and the turn-on process needs to introduce synchronous variable-amplitude compensation.

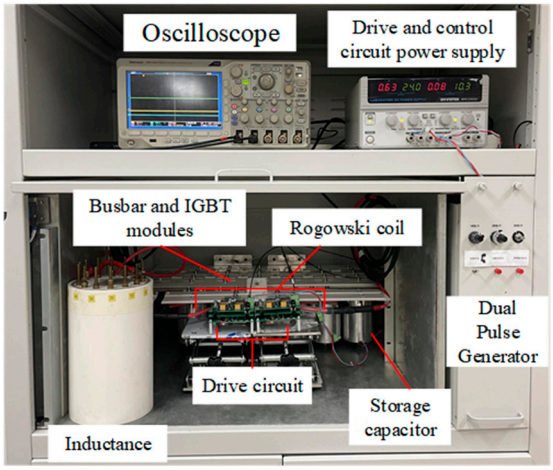
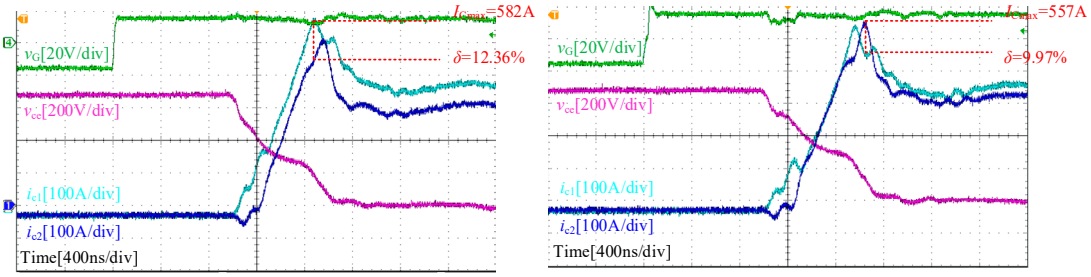


Figure 13. The experimental hardware circuit of the synchronous variable-amplitude drives method.

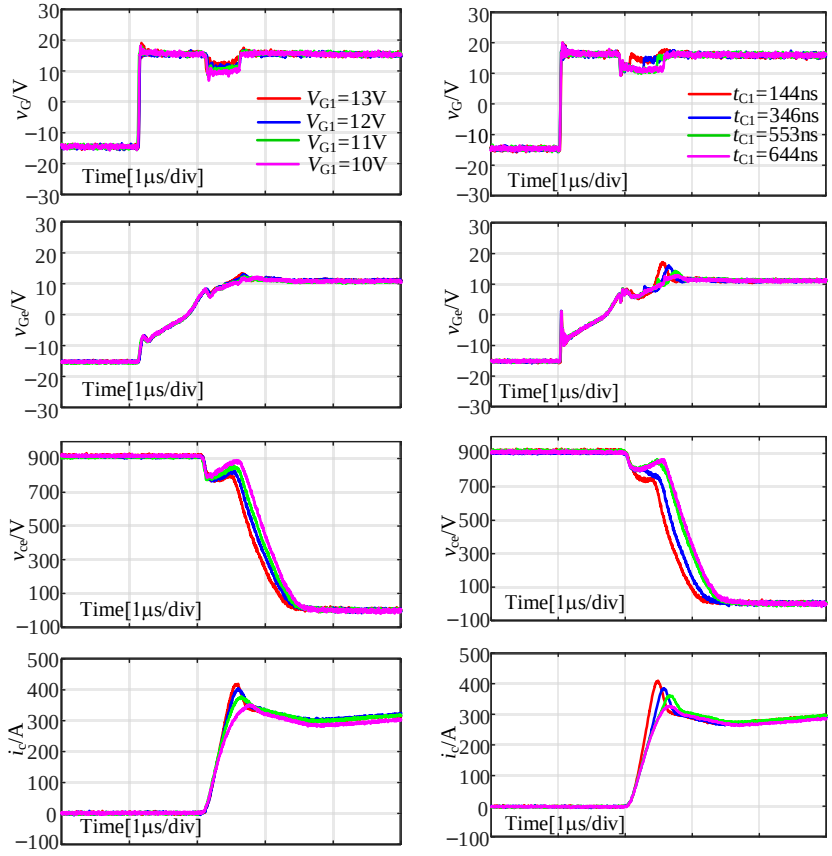
Figure 14b is the experimental waveform result after adding synchronous variable-amplitude drive control, and the current unbalance degree at that point in time was 9.97%. It can be seen that the T_1 tube is turned on first during the turn-on process, which leads to a greater current stress on the module when it is first turned on, a large rate of rise in the turn-on current, and an unbalanced current distribution in the dynamic process. When the collector current rises, the synchronous variable-amplitude drive control is added to adjust its current rising rate, so that its equivalent current rising rate is consistent with the No. 2 branch, and the current sharing effect of the synchronous variable-amplitude drive control is verified.



(**a**) Turn-on process (**b**) Turn-off process

Figure 14. Waveform results of the parallel experiment of the two modules without compensation.

At the same time, the experimental verification is carried out through the current sharing effect of multiple groups of different gate drive voltages and action times, as shown in Figure 15. The dynamic characteristics of the turn-on process under the control of different gate control voltages and action times are the same as the analysis and simulation results.

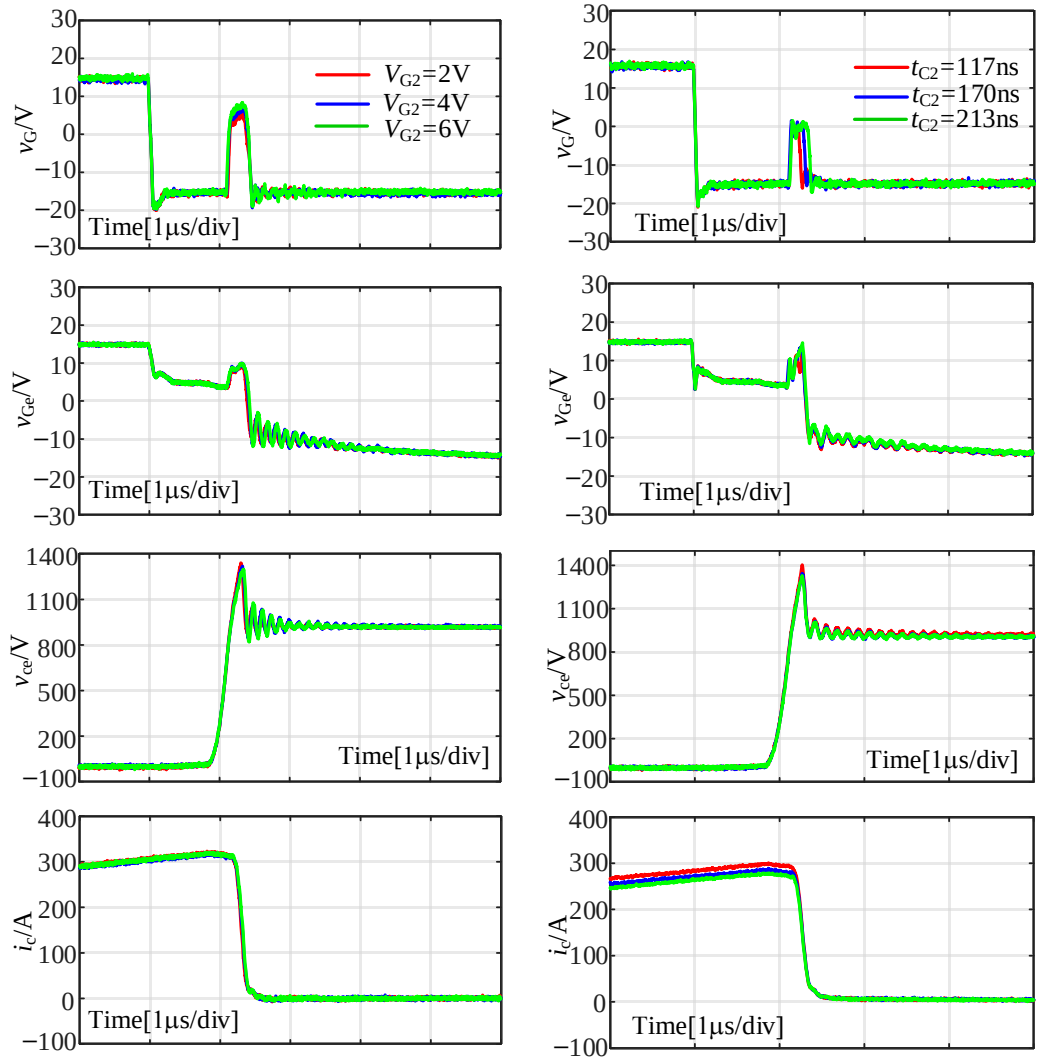


(**a**) Waveform of turn-on process (**b**) Waveform of turn-off process

Figure 15. The control effect of V_{G1} and t_{C1} on the turn-on process.

As shown in Figure 16, the dynamic characteristics of the turn-off process under the control of different gate control voltages and action times are the same as the analysis and simulation results. It can be seen from the horizontal comparison that its control effect in the turn-off process is weaker than that in the turn-on process.

Similar to the simulation results, within a certain range of gate voltage amplitudes or action times, the current imbalance issue in parallel modules can be improved.



(**a**) Waveform of turn-on process (**b**) Waveform of turn-off process

Figure 16. The control effect of V_{G2} and t_{C2} on the turn-on process.

5. Conclusions

In this paper, the characteristic parameters of parallel dynamic current sharing are analyzed through simulation modeling and experiments, and the influence of characteristic parameters on parallel dynamic current sharing characteristics and the sensitivity under the same relative difference degree is obtained. A synchronous variable-amplitude driving method is proposed, which mainly includes the following:

1. Considering the relative difference of body parameters, the influence of each dynamic characteristic parameter on the parallel application of IGBT is analyzed, and the variation law is further analyzed through simulation. When selecting the parallel IGBT module, paying attention to the consistency of these characteristic parameters as much as possible can effectively improve the degree of parallel current sharing. The current difference and current integral value are proposed as the evaluation indexes of current sharing.
2. Through the verification and identification of the characteristic parameters, the characteristic parameters of the gate drive circuit that are not easy to obtain in the datasheet are modeled and analyzed, and the method of calculating the gate characteristic parameters through the experimental data of the turn-on and turn-off process is studied. This allows for the determination of the composite parameter differences

between modules can be obtained so that IGBT modules with similar parameter characteristics are selected for parallel use and provide parameter basis for synchronous variable-amplitude drive compensation.

3. A synchronous variable-amplitude driving method is proposed, and the working principle of this method is clarified in conjunction with the dynamic process circuit model. The effectiveness of this method is verified by simulation. And through multiple sets of simulations, the three-dimensional relationship among gate control voltage, action time, and current unbalance degree is fitted.
4. Based on the obtained characteristic parameters of two sets of IGBT modules, synchronous and asymmetric drive compensation was performed, leading to an improvement in current equalization characteristics. This validated the effectiveness of the method. Furthermore, the impact of different gate control voltages and action times on the dynamic current equalization characteristics of parallel operation was further verified. This provides a theoretical basis for subsequent parallel experiments.

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Notations

Symbol	Description	Unit
$V_{CE(sat)}$	the collector voltage	V
i_C	the collector current	A
$V_{GE(th)}$	the gate voltage	V
T_j	the junction temperature	°C
t_{delay}	the signal transmission delay time	ms
$V_{G,on}$	the gate turn-on voltage	V
$V_{G,off}$	the gate turn-off voltage	V
$R_{G,on}$	the gate turn-on resistance	Ω
$R_{G,off}$	the gate turn-off resistance	Ω
$R_{G,int}$	the gate module internal resistance	Ω
C_{GC}	the gate collector capacitance	nF
C_{GE}	the gate emitter capacitance	nF
L_G	the gate inductance	mH
L_C	the collector inductance	mH
L_E	the emission pole inductance	mH
R_C	the collector resistance	Ω
R_E	the emitter resistance	Ω
C_{iesx}	the input capacitor of branch x	nF
V_{GEx}	the gate voltage of branch x	V
i_{Cx}	the collector current of branch x	A
$R_{Gx,on}$	the gate resistor of branch x	Ω
V_{CEx}	the collector voltage of branch x	V
$V_{GE(th)x}$	the turn-on threshold voltage	V
C_{GEx}	the gate-emitter capacitor of branch x	nF
t_n	the time point	ms
$V_{Gx,on}$	the turn-on drive voltage used by the drive control circuit	V

$V_{Gx,off}$	the turn-off drive voltage used by the drive control circuit	V
$R_{Gx,on}$	the sum of the external drive resistance	Ω
$t_{d(on)x}$	the turn-on delay time	ms
L_{Ex}	the auxiliary emitter inductance	mH
K	the equivalent transconductance	-
g_{fsx}	the forward transfer rate	-
V_{CC}	the initial gate control voltage	V
V_{G1}	the gate control voltage	Wb/m^2
I_{rr}	the equivalent current overshoot	A
$V_{GE(pl)x}$	the Miller plateau voltage	V
V_{os}	the voltage overshoot	V
ΔIc	the collector current difference	A
δ	the degree of current imbalance	-
$R_{G,ext}$	the external resistance	Ω
ε	the curvature	-

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