

Article

Accurate Circuit-Level Modelling of IGBTs with Thermal Phenomena Taken into Account

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Abstract: This paper proposes a new compact electrothermal model of the Insulated Gate Bipolar Transistors (IGBT) dedicated for SPICE (Simulation Program with Integrated Circuit Emphasis). This model makes it possible to compute the non-isothermal DC characteristics of the considered transistor and the waveforms of terminal voltages and currents of the investigated device and its internal temperature at transients. This model takes into account the nonlinearity of thermal phenomena in this device. The form of the formulated model is described and the problem of estimating its parameter values is discussed. The correctness of the proposed model was verified experimentally both at DC operation and at transients. The obtained results are compared to the results of computations performed with the use of the classical literature model. A very good agreement between the results of measurements and computations performed with the new model is obtained at different cooling conditions and in a wide range of changes of parameters characterising the electrical excitation of the tested device.

Keywords: IGBT; modelling; thermal phenomena; SPICE; compact electrothermal model; self-heating



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1. Introduction

IGBTs (Insulated Gate Bipolar Transistors) [1] are popular, fully voltage-controlled power semiconductor devices which make it possible to switch voltages and currents of high values [2]. They are used in such power converters as inverters [3–5] or DC-DC converters [6–8]. During operation of the considered transistors, their internal temperature increases as a result of self-heating phenomena [9–13]. An increase in this temperature causes shortening of the device life-time [13–16] and changes in the course of their characteristics [17–19].

Computer simulations are an important part of the process of designing electronic circuits. It can be realised e.g., in SPICE (Simulation Program with Integrated Circuit Emphasis) [9,20–22] or PLECS (Piecewise Linear Electrical Circuit Simulation) [23], which are the most popular tools to simulate power electronic networks [24–27]. Accuracy of the performed simulations depends on accuracy of the applied models of all components of the analysed network. Unfortunately, models of IGBTs built-in in popular simulation programmes are characterised by low accuracy [19,28]. In turn, as is shown in the cited papers the literature models often do not take into account the influence of such essential physical phenomena such as, e.g., self-heating or the sub-threshold effect [11,28–37], which can influence the shape of both dc and dynamic characteristics of an IGBT in an essential manner [19].

In the literature, a lot of IGBTs models of different accuracy can be found. Such models belong to one of the following groups: detailed models [38,39] or compact models [12,17,18,31]. Detailed models make it possible to obtain higher accuracy of computations of space-time distribution of, e.g., current density in the considered device can be computed with these models. Such a kind of model is especially dedicated to designers of semiconductor devices. Unfortunately, a high level of complexity of such models causes

problems connected with the convergence of the computer analysis of electronic networks with many semiconductor devices [16]. Such analyses are very time consuming. Therefore, compact models [40–44] of semiconductor devices are commonly used in the analysis of electronic networks. Such models contain equations describing dependences between voltages and currents of these devices.

In order to take into account self-heating phenomena in the computer analyses, electrothermal models should be used [17,18]. In the analysis of electronic circuits, compact models are universally used. Compact electrothermal models make it possible to compute not only voltages and currents in the network, but also internal temperatures of semiconductor devices.

Models of the considered transistors of different accuracy and dedicated to different simulation environments are widely described in the literature. The review of some of these models is presented in the paper [19]. Each of the models described in the literature is dedicated to specific applications, but there is no universal model that takes into account all the essential physical phenomena occurring in the IGBT.

To formulate such a model, the classical network representation of the IGBT shown in Figure 1 is used. In this circuit a connection of the MOS transistor (MOS), the bipolar transistor (BJT) and the p-n diode (D) is visible [1,26].

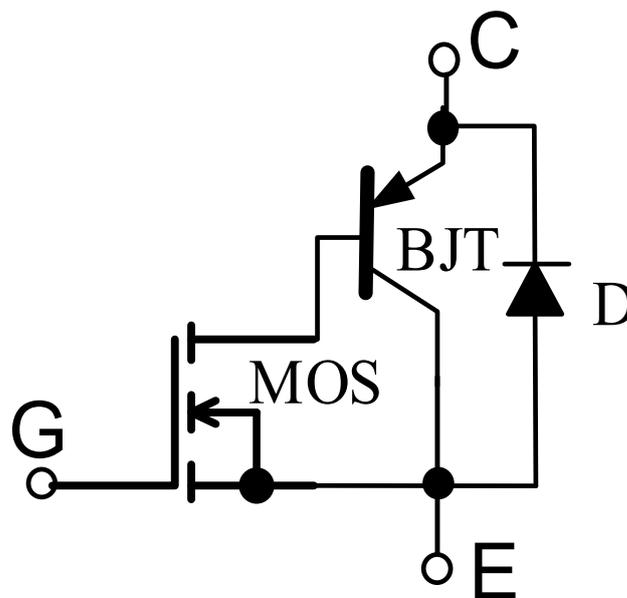


Figure 1. Network representation of the IGBT structure.

In the paper [45] it is shown that for the structure in Figure 1, two dies are mounted in the common case. One of these dies contains the transistor and the other—the diode.

In our previous papers [19,28] the accuracy of selected literature models proposed in [18,46] was analysed. The results of computations and measurements of dc and dynamic characteristics presented in these papers proved that the considered literature models correctly model DC characteristics only at room temperature and at a high value of voltage controlling the gate. Especially, essential divergences among the results of computations and measurements are visible for temperatures higher than 100 °C and within the range of gate-emitter voltage lower than threshold voltage (the sub-threshold range). They reach even several orders of magnitude.

As it results from the literature review, well-known models are imperfect. They skip, among others, phenomena occurring in the operation of the structure MOS contained in the IGBT within the sub-threshold range. Many models proposed in the literature do not take into account self-heating phenomena. Additionally, parameters occurring in these

models often refer to the realisation technology of the considered devices. The values of these parameters are often not available for the users.

For some years we have been trying to elaborate an electrothermal model of the IGBT which can properly describe both electrical and thermal properties of the considered device. Some steps of our investigations were reported in the papers [17,19,28,47]. In the paper [19], an isothermal DC model of the IGBT was proposed, whereas in the paper [28] a dynamic isothermal model of such a transistor was described. In the paper [17], a dc electrothermal model of the considered device was proposed, and its version additionally taking into account thermal inertia was described in the paper [47]. In the electrothermal models described in the cited papers, the nonlinearity of cooling processes and internal parasitic capacitances of the IGBT were omitted. As indicated in the papers [45,48], the omission of the nonlinear dependence of thermal resistance of the IGBT junction temperature significantly influences the accuracy of determining the transistor junction temperature.

In the paper [17], it was shown that self-heating phenomena strongly influence the shape of dc characteristics of IGBTs, particularly at weak control. On these characteristics the electrothermal breakdown, which occurs at the values of the transistor output voltage V_{CE} considerably smaller than the admissible value declared by the producer, was observed. In turn, in the paper [49] it is shown that thermal resistance of the IGBT strongly depends on the used cooling system, the value of the transistor internal temperature and ambient temperature. At a change of the value of the mentioned temperatures in the admissible range, the value of thermal resistance can change even by 30%. Only a nonlinear thermal model makes it possible to properly describe the mentioned dependence.

In this paper a new electrothermal model of the IGBT is proposed. This model has the form of a subcircuit dedicated to the SPICE software. In contrast to the models described in the literature, the new model takes into account simultaneously the sub-threshold effect, electrical and thermal inertia, and the nonlinearity of thermal phenomena occurring in the modelled device. It is also taken into account that the modelled device consists of two semiconductor dies (the IGBT and the diode). Therefore, it is possible to obtain internal temperatures of both the dies using the proposed model taking into account self-heating phenomena in both the dies and mutual thermal couplings between these dies. When formulating this model, the classical network representation of the IGBT shown in Figure 1 was used. The correctness of the proposed model is verified experimentally both at the steady state and at transients. The obtained results are compared to the results of computations performed with the use of the classical literature model currently implemented in the SPICE software. Particularly, an influence of the non-linearity of thermal phenomena on the computed characteristics is shown and discussed.

In Section 2, the structure and equations describing the new compact large-signal electrothermal models of the IGBT dedicated for SPICE are presented. In Section 3, the manner of estimating the values of parameters of this model is described. In Section 4, the results of the experimental verification of this model in DC and the dynamic conditions for the transistor operating at different cooling conditions are presented.

2. Model Form

The electrothermal model of the IGBT formulated by the authors has a form of the subcircuit for SPICE. The network representation of this model is presented in Figure 2.

This model consists of three parts: the electrical model, the thermal model, and the power model. In the further part of this section, the mentioned components of the new model are described. Section 2.1 contains a description of the electrical model, the Section 2.2, the power model, whereas Section 2.3, the thermal model.

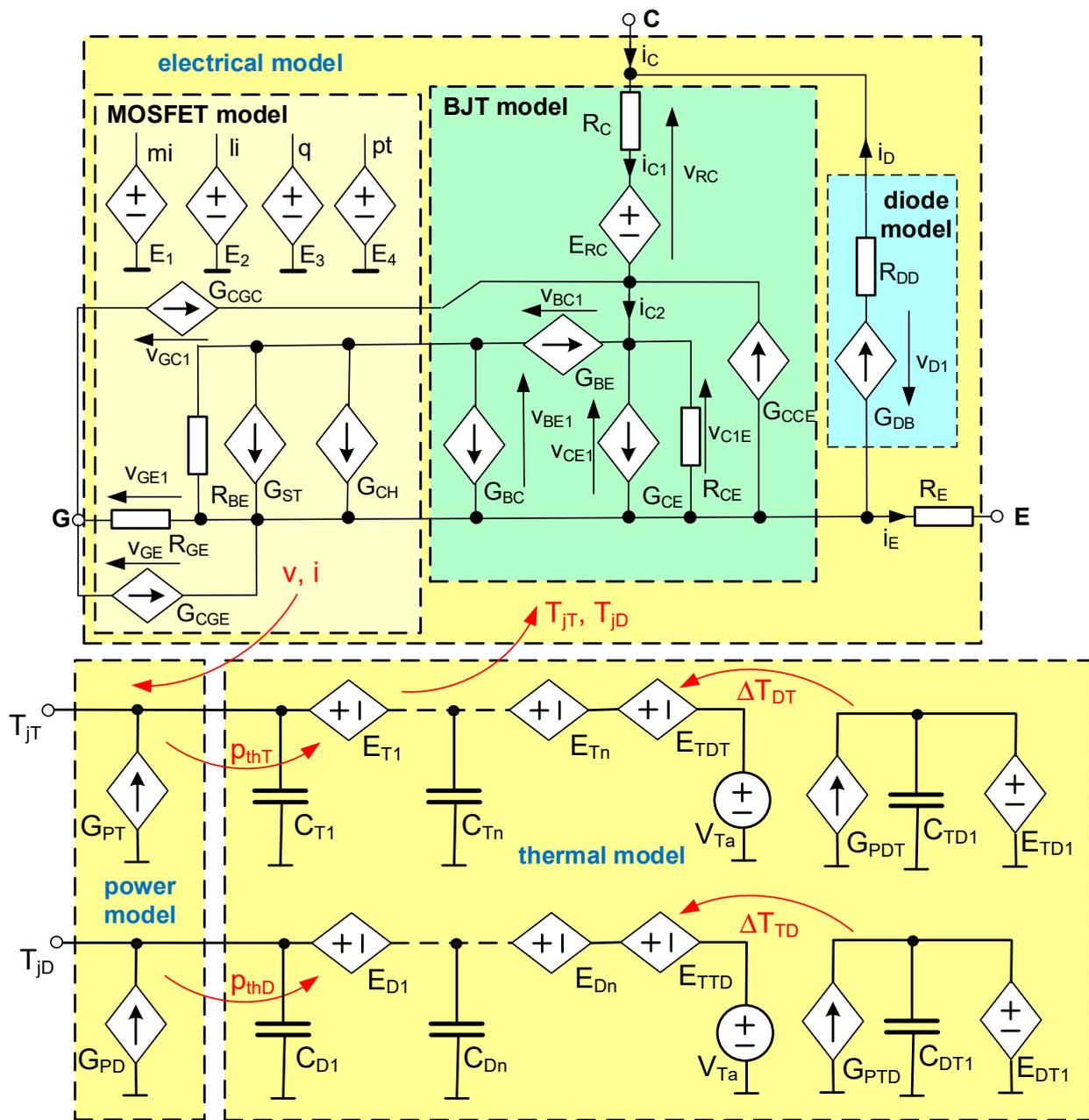


Figure 2. Network representation of a large-signal electrothermal model of the IGBT.

2.1. Electrical Model

In formulating the electrical model, the classical network representation of the IGBT was used. Therefore, in this model 3 blocks appear. They represent models of the input MOS structure, the output BJT and the diode, respectively. In order to formulate this model, the equations describing the DC characteristics of the transistor MOS given in the paper [50], the equations describing the DC characteristics of the BJT [16] and the equations describing the DC characteristics of the diode proposed in the paper [19] were used. Each dependence existing in the considered model is represented by the controlled voltage and the current sources. These dependences are elaborated for IGBTs made of silicon.

Series resistances of the emitter and the collector are modelled by linear resistors R_E and R_C . Controlled voltage source E_{RC} models the linear dependence of the collector series

resistance R_C on temperature. Resistors R_{CE} , R_{BE} and R_{GE} model the leakage currents flowing between each pair of terminals of the transistor.

The drain current of the MOS transistor is modelled by two controlled current sources: G_{ST} and G_D . The first of these sources model the drain current in the sub-threshold range, whereas the source G_D —the channel current of this transistor. The output currents of the mentioned sources are described with the following equations [50]

$$I_{GST} = I_{PO} \cdot \left(\frac{T_{jT}}{T_0}\right) \cdot \exp\left(-\frac{V_{go}}{T_{jT} \cdot k/q}\right) \cdot \left(\exp\left(\frac{\text{LIMIT}(v_{GE1} - v_{PH}, 0, v_{VT} - v_{PH})}{n_p \cdot T_{jT} \cdot k/q}\right) - 1\right) \quad (1)$$

$$I_{GD} = B \cdot v_{mi} \cdot v_{BE1} / |v_{BE1}| \quad (2)$$

Values of parameters I_{PO} , n_p and B occurring in the Equations (1) and (2) correspond to reference temperature T_0 , V_{go} corresponds to a band-gap of silicon and amounts to 1.206 V, T_{jT} is the device internal temperature, k is the Boltzmann constant, and q is the electron charge. $\text{LIMIT}(x, \min, \max)$ is a standard-function of SPICE, whose value is equal to \min , if $x < \min$, \max , if $x > \max$, and in other cases it is x . Voltages v_{BE1} and v_{GE1} are marked in Figure 2. In turn, v_{mi} and v_{PH} mark voltages on terminals of controlled voltage sources E_1 and E_4 , respectively.

Controlled voltage sources E_1 and E_2 were applied to compute the value of voltage v_{mi} according to the equations contained in the paper [50], and voltages between connectors of controlled voltage sources E_3 and E_4 describing linear dependences of threshold voltage v_{VT} (E_3) and the Fermi level v_{PH} (E_4) on temperature.

Current transfluent between the base and the emitter of the bipolar transistor contained in the structure of the modelled IGBT is modelled by controlled current source G_{BE} . The output current of this source is given by the equation:

$$I_{GBE} = -\frac{I_O}{\beta_F} \cdot \left(\frac{T_{jT}}{T_0}\right)^2 \cdot \exp\left(\frac{-V_{go}}{n_1 \cdot T_{jT} \cdot k/q}\right) \cdot \left(\exp\left(\frac{-v_{BC1}}{n_1 \cdot T_{jT} \cdot k/q}\right) - 1\right) \quad (3)$$

where I_O denotes a model parameter, n_1 —the emission coefficient of the base-emitter junction, voltage v_{BC1} is marked in Figure 2, and β_F is the coefficient of current amplification of the BJT operating within the forward active mode. The value of this coefficient depends on the collector current i_{C1} and temperature T_{jT} . This dependence is given in the paper [16].

Controlled current source G_{BC} models current flowing between the base and the collector of the BJT. The current of this source is given by the formula:

$$I_{GBC} = -\frac{I_O}{\beta_R} \cdot \left(\frac{T_{jT}}{T_0}\right)^2 \cdot \exp\left(\frac{-V_{go}}{n_{10} \cdot T_{jT} \cdot k/q}\right) \cdot \left(\exp\left(\frac{-v_{BE1}}{n_{10} \cdot T_{jT} \cdot k/q}\right) - 1\right) \quad (4)$$

where n_{10} is the emission coefficient of the base-collector junction, voltage v_{BE1} is marked in Figure 2, β_R is the coefficient of reverse current amplification of the BJT; β_R linearly depends on temperature T_{jT} .

The main current of the IGBT is modelled by controlled current source G_{CE} , whose output current is described by the equation:

$$I_{GCE} = I_O \cdot \left(\frac{T_{jT}}{T_0}\right)^2 \cdot \exp\left(\frac{-V_{go}}{n_1 \cdot T_{jT} \cdot k/q}\right) \cdot \left(1 + \frac{v_{CE1}}{U_{AN}}\right) \cdot \left(\exp\left(\frac{-v_{BC1}}{n_{10} \cdot T_{jT} k/q}\right) - \exp\left(\frac{-v_{BE1}}{n_1 \cdot T_{jT} k/q}\right)\right) \quad (5)$$

where U_{AN} denotes early voltage.

The DC characteristic of the antiparallel diode is modelled by controlled current source G_{DB} . The output current of this source is equal to the sum of diffusive and generation-recombination components and it is described by the formula given in the paper [19].

In order to take into account electric inertia in the described model, three controlled current sources G_{CGE} , G_{CCE} and G_{CGC} are applied. The mentioned sources model current flowing through parasitic capacitances situated between each pair of the transistor removals. Capacitance C_{GE} is connected to the input MOS structure and it is described by the following formula:

$$C_{GE} = C_{GE0} \cdot w + x \cdot (T_{jT} - T_0) + \begin{cases} 0 & \text{if } v_{GE} < V_{GEmin} + v_{C1E} \\ C_{ox} \cdot k_1 \cdot (C_{G1} \cdot V_{GC1} + C_{G2}) & \text{if } V_{GEmin} + v_{C1E} < v_{GE} \leq V_{GEmax} + v_{C1E} \\ C_{ox} & \text{if } v_{GE} > V_{GEmax} + v_{C1E} \text{ and } v_{C1E} < 0 \\ C_{ox} \cdot \left[u \cdot (T_{jT} - T_0) + 0.75 \cdot \left(\frac{v_{GC1}}{2 \cdot v_{GE} + v_{C1E}} \right)^2 \right] & \text{if } v_{GE} > V_{GEmax} + v_{C1E} \text{ and } v_{C1E} \geq 0 \end{cases} \quad (6)$$

where C_{ox} means capacitance dependent on thickness t_{OX} of the layer of SiO_2 under the gate, w is width of the channel of the MOS structure, C_{GE0} is capacitance between the gate and the emitter per unit of widths of the channel, V_{GEmax} , V_{GEmin} , C_{G1} , C_{G2} , x , u and k_1 are parameters of the model, whereas voltages v_{GE} , v_{GC1} and v_{C1E} are marked in Figure 2.

Capacitance C_{ox} occurring in the Equation (6) is connected with the SiO_2 layer under the gate of the transistor and it is described by the formula [47]

$$C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{ox} \cdot L \cdot w}{t_{OX}} \quad (7)$$

where L denotes the length of the channel of the MOS structure, ϵ_0 is dielectric permeability of free air, and ϵ_{ox} —relative dielectric permeability of silicon.

In turn, the output capacitance of the modelled device corresponds to the junction capacitance of the antiparallel diode and it is described by the following equation:

$$C_{CE} = C_{CE0} \cdot (1 + v_{CE}/V_j)^{-M_j \cdot (1+r \cdot (T_{jD} - T_0))} \quad (8)$$

where v_{CE} denotes the collector-emitter voltage, C_{CE0} is output capacitance at zero voltage on the antiparallel diode, V_j is built-in potential of this diode, M_j is a parameter describing the doping profile of the junction of this diode, r is the temperature coefficient of parameter M_j .

Capacitance between the gate and the collector corresponds to capacitance of the base-emitter junction of the BJT and to the gate-drain capacitance of the MOS transistor and it is described by the dependence of the form

$$C_{GC} = C_2 \cdot \frac{i_C \cdot q}{k \cdot T_{jT}} + \begin{cases} C_1 \cdot w & \text{if } v_{GC1} < V_{GCmin} + e \cdot (T_{jT} - T_0) \\ [C_{GDO} + y \cdot (T_{jT} - T_0)] \cdot w \cdot \left(1 + \frac{v_{C1E}}{V_{jC}} \right)^{-M_{j2} + n \cdot (T_{jT} - T_0)} & \text{if } v_{GC1} \geq V_{GCmin} + e \cdot (T_{jT} - T_0) \end{cases} \quad (9)$$

where C_{GD0} is capacitance between the gate and the drain per unit of widths of the channel, C_1 , C_2 , y , e , n , V_{GCmin} are parameters of the model, V_{jC} is built-in potential of the base-emitter junction of the BJT, M_{j2} is a parameter describing the doping profile of this junction.

The output currents of the considered controlled current sources (G_{CCE} , G_{CGE} and G_{CGC}) are equal to the product of capacitances described by the Equations (6)–(9) and the time derivative of the voltage on these sources. The network used to compute each capacitive current contains the controlled current source G_{C1} modelling parasitic capacitance, the linear capacitor of the fixed capacitance connected in series to the voltage sources of zero value.

2.2. Power Model

The power model describes the dependence of thermal power dissipated in the transistor and in the diode on terminal voltages and currents of the modelled device.

Thermal power is equal to the difference between the total power lost in this transistor and the instantaneous power dissipated in internal capacitances of this device [50].

For the modelled transistor, power p_{thT} is described by the Formula (10), whereas power p_{thD} dissipated in the diode is given by the Formula (11).

$$p_{thT} = i_{C1} \cdot v_{RC} + i_{C2} \cdot v_{CE1} + R_E \cdot i_E^2 \quad (10)$$

$$p_{thD} = i_D^2 \cdot R_{DD} + i_D \cdot v_{D1} \quad (11)$$

where currents i_D , i_{C1} , i_{C2} and i_E , as well as voltages v_{RC} and v_{CE1} are marked in Figure 2.

In Figure 2 thermal power p_{thT} is represented by controlled current source G_{PT} , the current of which is given by the Equation (10), whereas thermal power p_{thD} , by controlled current source G_{PD} given by the Equation (11).

2.3. Thermal Model

The thermal model describes the dependence of internal temperatures T_{jT} of the transistor and T_{jD} of the diode on thermal power dissipated in these components p_{thT} and p_{thD} , respectively. This model describes self-heating in the transistor and in the diode as well as mutual thermal couplings between them. This model is described by the network analogue containing four non-linear Cauer networks proposed in the paper [49]. This model takes into account the influence of ambient temperature T_a and the transistor and the diode internal temperatures T_{jT} and T_{jD} on thermal resistances occurring in this model. For example, thermal resistance of transistor R_{thT} is described by means of the equation of the form

$$R_{thT} = R_{thT1} \cdot (1 - a \cdot (T_a - T_0)) \cdot \exp(-(T_{jT} - T_a)/T_Z) + R_{thT0} \cdot (1 - b \cdot (T_a - T_0)) \quad (12)$$

where R_{thT1} , R_{thT0} , a , b , T_0 and T_Z are model parameters.

In the network representation of the thermal model of the modelled device, four sub-circuits occur. The networks visible on the right-hand side model mutual thermal coupling between the diode and the transistor, whereas the networks visible on the left-hand side model self-heating in the transistor and in the diode. Voltage source V_{Ta} represents ambient temperature T_a , capacitors correspond to heat capacitances of each component of the heat flow path, whereas controlled voltage sources E_{T1}, \dots, E_{Tn} describe dependences $R_{thT}(T_a, T_{jT})$, E_{D1}, \dots, E_{Dn} describes dependences $R_{thD}(T_a, T_{jD})$, and E_{DT1} and E_{TD1} , dependences of transfer thermal resistances $R_{thDT}(T_a, T_{jD})$ and $R_{thTD}(T_a, T_{jT})$, respectively. Controlled voltage sources E_{TTD} and E_{TDT} model an increase of internal temperatures of the transistor and the diode, respectively, caused by mutual thermal couplings between these devices.

3. Estimation of the Model Parameters

The practical application of the formulated model demands an effective procedure to estimate values of its parameters. Such a procedure was prepared based on the idea of the local estimation described in the paper [51].

According to this idea, the value of each parameter of the model is estimated on the basis of the coordinates of points lying on the measured characteristics of the investigated device. These points are selected in such a manner that the considered characteristics can be described with the use of the simplified analytic formulas, containing fewer parameters. After transforming these formulas, the equations make it possible to calculate values of each parameter of the formulated model.

Values of parameters are computed in the strictly defined order in a multi-stage procedure including measurements and computations. Practical equations used to compute the value of each parameter contain the coordinates of measuring points and values of parameters of the model estimated in the previous stages of the estimation procedure.

The procedure of estimating the values of parameters of the electrical model of the IGBT is described in the paper [19], whereas the manner of estimating parameters of the thermal model is presented in the paper [49]. While estimating values of parameters of the

electrical model, suitable current-voltage characteristics or dependences of capacitances on voltages measured at selected values of ambient temperature and in the conditions making it possible to omit self-heating phenomena are used. In turn, to compute the value of parameters of the thermal model, waveforms of transient thermal impedance measured at selected values of ambient temperature and power dissipated in the modelled transistor are used.

4. Verification of the Formulated Model

In order to verify the correctness of the proposed model, the DC and dynamic characteristics of the silicon IGBT of the type IRG4PC40UD [52] operating in different cooling conditions were measured and computed with the use of this model. This transistor is characterised by the maximum allowable value of collector current equal to 15 A and the maximum allowable value of collector-emitter voltage equal to 600 V [52]. The estimated value of the threshold voltage of the investigated transistor is equal to $V_{th0} = 5.82$ V at temperature $T_0 = 300$ K. Investigations were performed for the mentioned device contained in the case TO-247 situated on the heat-sink shown in Figure 3 and for this device operating without any heat-sink. The results of these measurements and computations are presented in Figures 4–9 in this Section.

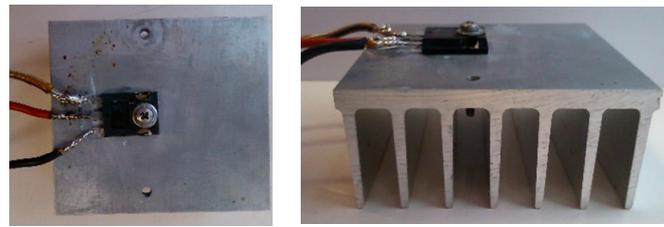


Figure 3. View of the tested device situated on the heat-sink.

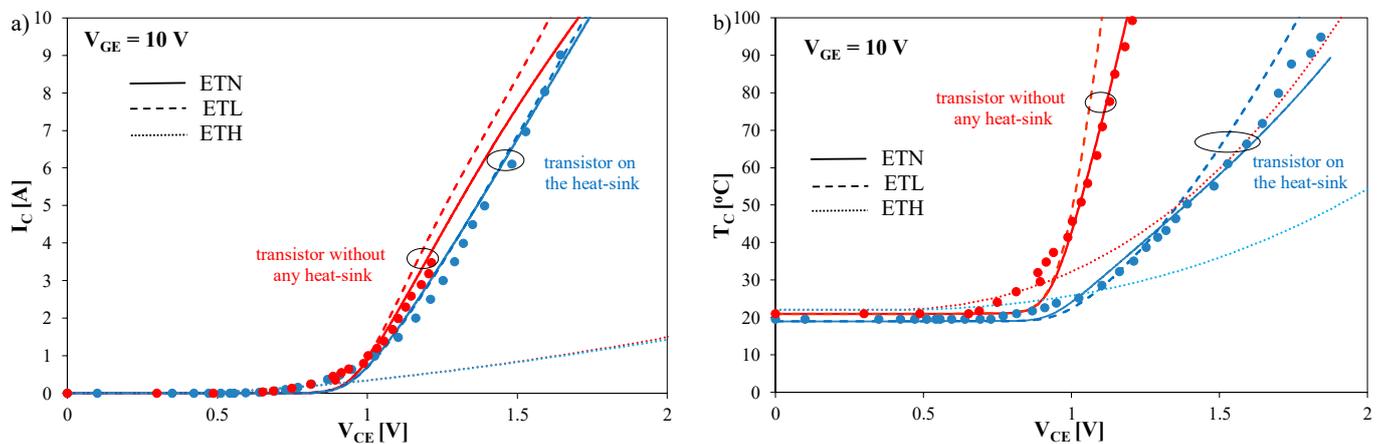


Figure 4. Computed and measured output characteristics of the tested transistor operating at strong steering (a) and dependences of the case temperature on voltage V_{CE} (b).

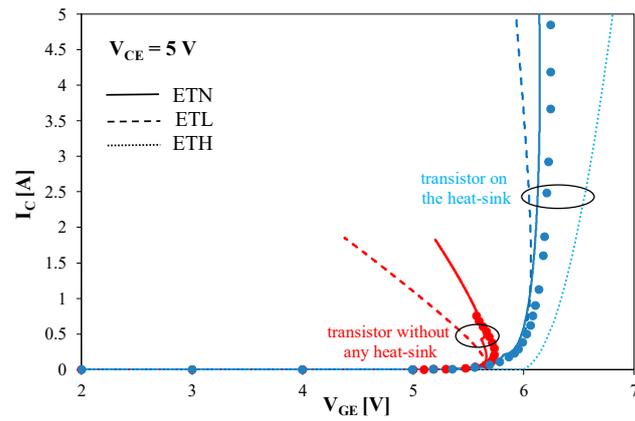


Figure 5. Computed and measured transfer characteristics of the tested transistor.

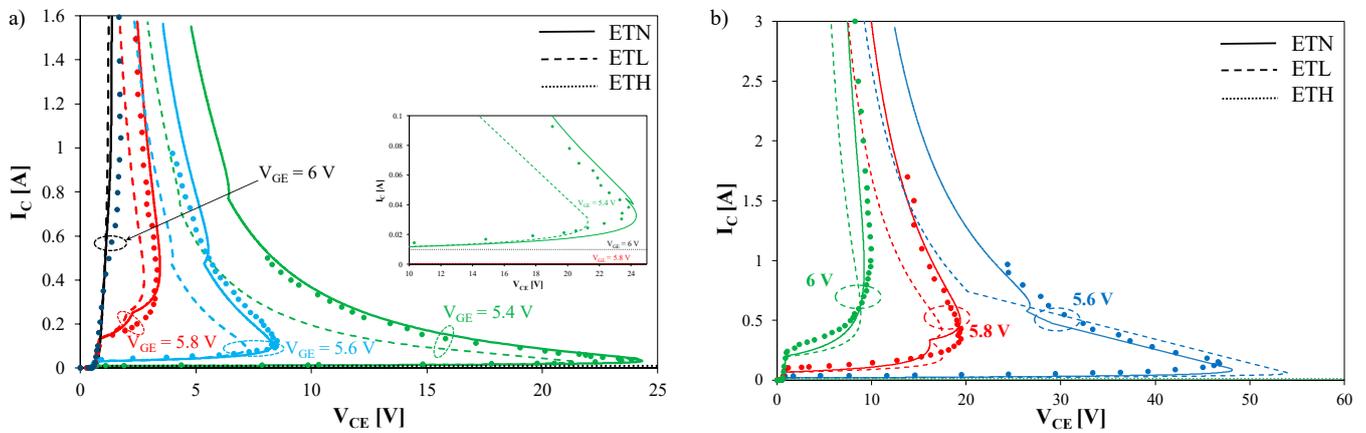


Figure 6. Computed and measured output characteristics at weak steering for the transistor operating without any heat-sink (a) and situated on the heat-sink (b).

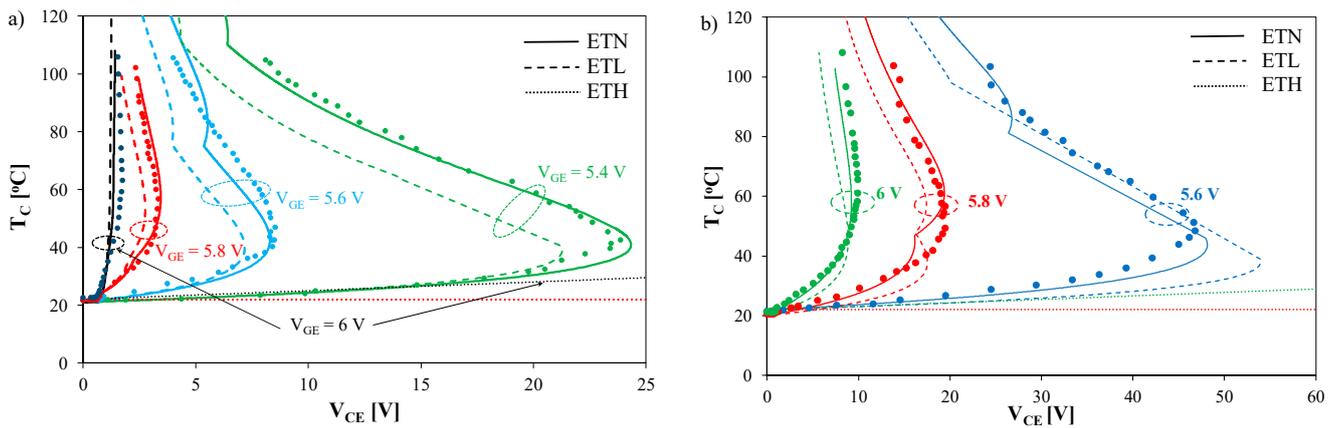


Figure 7. Computed and measured dependences of the case temperature on output voltage at weak steering for the transistor operating without any heat-sink (a) and situated on the heat-sink (b).

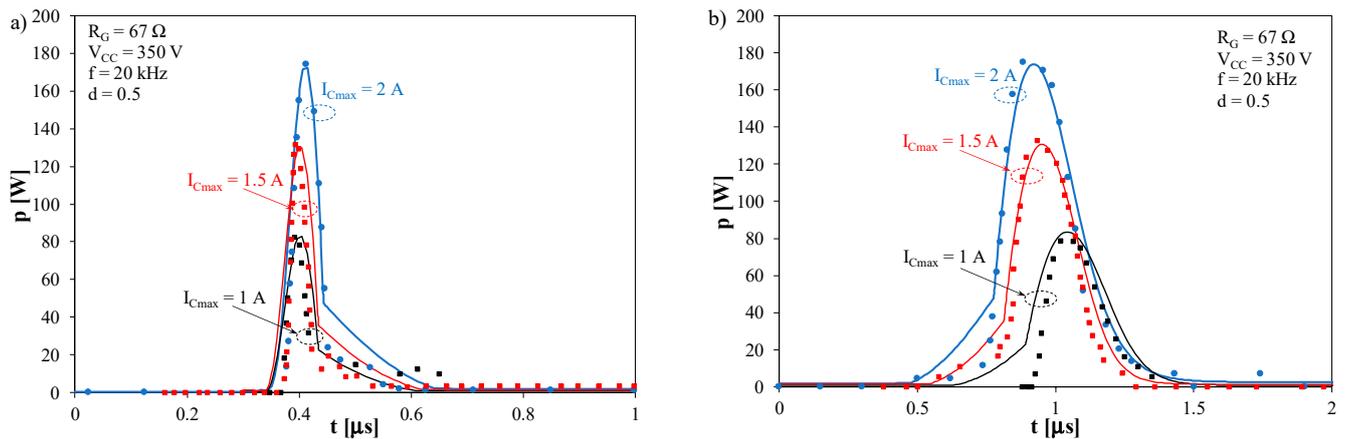


Figure 8. Computed and measured waveforms of power lost in the tested transistor at switching-on (a) and switching-off (b).

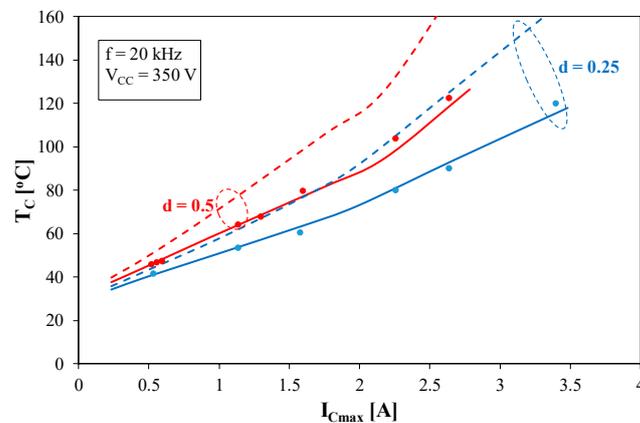


Figure 9. Computed and measured dependences of the case temperature of the transistor operating in the circuit of a switch at the steady state on the maximum value of the collector current.

In all these figure's points represent the results of measurements, and solid lines—the results of computations obtained by means of the formulated model (ETN). Dashed lines represent the results of computations obtained with the use of the same electrothermal model containing the linear thermal model (ETL), in which the dependence $R_{th}(T_j, T_a)$ is omitted. At first, the DC characteristics of the considered transistor are presented, and next, the results of investigations on its dynamic proprieties are shown. Additionally, the results of computations obtained with the use of the model performed by A.R. Hefner and described in the papers [18,53–55] are marked with dotted lines (ETH). The isothermal version of this model is built-in in the current version of the SPICE software commonly used in analyses of electronic and power electronic networks. In the computations performed with this model, self-heating phenomena are taken into account using the separated iterations method described in [56]. The values of the model parameters were estimated using the PSPICE Model Editor, which is a part of the SPICE software. The PSPICE Model Editor uses the catalogue data as the input data. The case temperature T_C is measured with the use of an infrared pyrometer. The values of this temperature are computed with the use of the following formula [23].

$$T_C = T_a + \frac{T_{jT} - T_a}{R_{thT}} \cdot (R_{thT} - R_{thj-c}) \quad (13)$$

where R_{thj-c} denotes thermal resistance between the die of the IGBT and the device case. The value of this parameter is given by the producer [52].

In order to obtain the characteristics presented in the further part of this section, we performed the classical DC sweep or transient analyses in the PSPICE software using the considered models of the IGBT. The computations were performed in classical networks used to measure the considered characteristics including voltage sources, resistors and the tested IGBT. In each characteristic, the results corresponding to the thermally steady state are presented.

In Figure 4, the output characteristics of the tested transistor (Figure 4a) obtained at strong steering (voltage $V_{GE} = 10$ V) and, corresponding to them, dependences of the case temperature T_C of the transistor on its output voltage (Figure 4b) are presented. The results obtained for the transistor situated on the heat-sink are marked with blue colour, and for the transistor operating without any heat-sink, with red colour.

As can be observed in Figure 4a, all the presented characteristics are monotonically increasing functions. The slope of these functions visibly increases for voltage $V_{CE} > 0.9$ V. The cooling conditions of the transistor do not influence in an essential manner the obtained courses of characteristics $I_C(V_{CE})$. With the worsening cooling conditions, a small shift left of the considered characteristics is visible. It is connected with a decrease of the forward voltage of the base-emitter junction of the internal BJT due to an increase in internal temperature T_{JT} . For the models ETN and ETL, a good agreement between the results of computations and measurements is obtained (the differences are smaller than 0.1 A), whereas the results obtained by the Hefner model visibly differ from the results of measurements (the differences exceed even 90%).

Cooling conditions strongly influence the dependence $T_C(V_{CE})$ shown in Figure 4b. This dependence is an increasing function. At the collector current equal to about 3 A (at $V_{CE} = 1.2$ V), the transistor without any heat-sink attains the case temperature equal even to 100 °C. Meanwhile, for the transistor operating on the heat-sink at current $I_C = 10$ A (at $V_{CE} = 1.7$ V) temperature T_C reaches only just 80 °C. The differences between the results of measurements and computations performed with the ETN do not exceed a few celsius degrees. For the other considered models, these differences are much more visible, even exceeding 50 °C.

Figure 5 illustrates transfer characteristics of the tested transistor.

The characteristics $I_C(V_{GE})$ obtained at different cooling conditions of the transistor differ in shape. For the transistor situated on the heat-sink, the measured dependence $I_C(V_{GE})$ is an increasing function. In turn, the characteristic for the transistor without any heat-sink shows a negative slope at current $I_C > 0.2$ A. This non-typical shape of the considered characteristic results from a rise of internal temperature of the transistor and a fall in the value of its threshold voltage. At current $I_C = 1$ A voltage, V_{GE} decreases even by 0.5 V as a result of changes of the cooling conditions, causing an increase in the case temperature T_C even by 85 °C. The characteristics obtained with the Hefner model are practically the same for both types of the cooling conditions and they do not change with temperature T_C due to neglecting the sub-threshold effect in this model. For the ENL model, the value of temperature T_C is overestimated and the characteristics $I_C(V_{GE})$ show a shift to the left and differ visibly from the measurement results. The differences in the measured and computed with the ETN model values of V_{GE} voltage do not exceed 0.1 V, whereas for the other models these differences exceed even 1 V and they increase with an increase of I_C current.

At weak steering (at values V_{GE} nearing the value of the threshold voltage) ambiguous output characteristics of the considered transistor are obtained. These characteristics are shown in Figure 6a for the transistor operating without any heat-sink and in Figure 6b for the transistor situated on the heat-sink, whereas the corresponding dependences of the case temperature on voltage V_{CE} are shown in Figure 7.

At both types of the cooling conditions ambiguous characteristics $I_C(V_{CE})$ are obtained. On each characteristic, the point of the electrothermal breakdown, in which the sign of the slope of these characteristics changes from the positive to negative, is visible. Such a shape of the output characteristics is well-known for other power semiconductor devices, e.g.,

power MOS transistors [50] and power BJTs [16]. Such a shape of the output characteristics also means that the breakdown in the investigated transistor can be observed at a considerably lower value of voltage V_{CE} than its admissible catalogue value.

As it is visible in Figure 6, the breakdown can appear even for V_{CE} smaller than 10 V, whereas the admissible value of this voltage given by the producer amounts to 600 V [52]. It is worth noticing that the value of voltage V_{CE} , at which the electrothermal breakdown appears, decreases together with an increase in voltage V_{CE} and when its cooling conditions worsen.

While analysing characteristics $T_C(V_{CE})$ it is visible that in the point of the electrothermal breakdown temperature, T_C amounts to about 50 °C. This means that an increase in internal temperature of the investigated device over ambient temperature equal to about 30 °C is sufficient for the electrothermal breakdown to occur. The value of this increase is practically the same for both the considered types of cooling conditions.

In Figure 6, the results obtained with the use of the Hefner model overlap with the V_{CE} axis due to the omission of the sub-threshold effect in this model. As a result of a very low value of current i_C obtained using this model, values of the computed temperature T_C (shown in Figure 7) are practically equal to the ambient temperature. For the ETL model, the computed value of the voltage corresponding to electrothermal breakdown is underestimated even by 3 V due to the overestimation of T_{JT} temperature. It is a result of omitting in this model the dependence of the thermal resistance on the device internal temperature.

The next figures (Figures 8 and 9) illustrate the influence of self-heating phenomena on parameters values of a switching process of the transistor. This transistor is excited by a rectangular pulses train of frequency f , duty cycle d and voltage levels equal to zero and 15 V, respectively. The circuit of the collector is supplied from voltage source V_{CC} through resistor R_L .

In order to take into account self-heating phenomena in transient analyses of the circuits described by means of considerably different time constants, a special method of the analysis described in the paper [57] is applied. In this method only one non-physical thermal time constant of the value considerably longer than electrical time constants characterising the examined circuit is used. In the case of the considered model of the IGBT in its thermal model, only one capacitor representing heat capacitance of the arbitrarily selected value 50 $\mu\text{J}/\text{K}$ and one controlled voltage source representing thermal resistance of the whole transistor are used.

In the paper [28], we showed that in the isothermal conditions the computed by means of the considered electrical model and measured waveforms of the collector current of the IGBT at switching were convergent. A good agreement between the results of computations and measurements was obtained in wide ranges of the values of load resistance and voltage supplying the collector circuit changed. In the cited paper, it is also shown that the waveforms $i_C(t)$ computed using the Hefner model visibly differ from the results of measurements. The values of switch-on and switch-off times obtained with this model differ even by 50% from the results of measurements. Therefore, in order to have the clear picture of the presented results of the investigations, the results obtained using the Hefner model are omitted in Figures 8 and 9.

In Figures 8 and 9, the results of computations and measurements at the thermally steady state are presented. In Figure 8, waveforms of power lost in the transistor when switched-on (Figure 8a) and switched-off (Figure 8b) at selected values of current of the switched-on transistor $I_{C_{\max}}$ are shown.

It is proper to notice that power losses at switching-on and switching-off are considerably bigger than power losses at the on and off states of the transistor. In the impulse this power attains even 180 W. The time duration of a switching process causes energy at switching-off to be higher than energy at switching-on. The values of these energies are computed as a result of integration of the shown waveforms $p(t)$. Together with an increase in the value of current $I_{C_{\max}}$, the maximum value of power lost in the transistor in the

switching process increases. A very good agreement between the results of measurements and computations is obtained.

In Figure 9, the computed and measured dependences of the case temperature of the transistor without any heat-sink operating in the considered switch with resistive load on current I_{Cmax} are shown. The presented results were obtained at frequency of the control signal $f = 20$ kHz and selected values of the duty cycle d .

It is visible that for both values of the duty cycle, the dependence $T_C(I_{Cmax})$ is an increasing function. An increase in the value of the coefficient d causes also an increase in temperature T_C . At lower values of the coefficient d , the operation of the transistor with a higher value of the collector current at the on-state is possible without a risk of exceeding the admissible value of internal temperature. For the ETN model, a very good agreement between the results of computations and measurements is obtained. The differences do not exceed 2 °C, whereas for the ETL model these differences are much bigger, even up to 40 °C.

5. Conclusions

In this paper a new compact large-signal electrothermal model of the IGBT dedicated for SPICE was proposed. This model makes it possible to compute the values of terminal voltages and currents of the considered device and its internal temperature taking into account both electrical phenomena occurring in this device and self-heating phenomena. The formulated model takes into account such phenomena that are omitted in other models of this device described in the literature: operation in the sub-threshold region and the nonlinearity of thermal properties of the modelled device, which means the dependence of thermal resistance on internal temperature and ambient temperature.

The correctness of the model was verified experimentally at both the dc and dynamic operating conditions of the investigated transistor. Different cooling conditions of this transistor were taken into account. It was proved that for all the considered cases of the operation of the investigated device, a good agreement between the results of computations and measurements was obtained using our model (ETN). It was also shown that at weak control of the investigated device, the accuracy obtained using our model was much better than for the classical models presented in the literature. The characteristics obtained for this range using the ETH have different shapes than the measured characteristics. In turn, the use of the ETL causes underestimating of V_{CE} voltage in the electrothermal breakdown range even by 3 V. In contrast, for the ETN these differences are much smaller and they do not exceed 0.2 V. The ETN model makes it also possible to compute more accurately the device internal and case temperatures than the other considered models.

The presented results of computations and measurements illustrate interesting properties of the considered device. Among other things, it was shown that the ambiguous non-isothermal characteristics $I_C(V_{GE})$ of the transistor can be obtained. It was also shown that at the values of voltage V_{GE} nearing the threshold voltage, the ambiguous non-isothermal output characteristics of this transistor can be obtained. At these characteristics the so-called electrothermal breakdown is observed. This breakdown appears at the values of the transistor output voltage V_{CE} considerably lower than the admissible catalogue value of this voltage. The electrothermal breakdown can be a destructive occurrence for the investigated device. It was also observed that an increase in the internal temperature of the transistor only just by 30 °C above ambient temperature was sufficient to cause the electrothermal breakdown. It was proved that a good agreement between the computed and measured characteristics of the IGBT operating at different cooling conditions in a wide range of changes of its terminal currents and voltages is possible to achieve only taking into account the nonlinearity of the thermal model.

When the transistor operates as a switch with resistive load, one can notice that on-time and off-time of the transistor change with the changes in the value of the collector current in the on-state. Additionally, the value of internal temperature of the transistor at the steady-state strongly depends on load resistance, frequency and the duty cycle of the

signal controlling the gate of such a transistor. It is a result of dynamic power losses in the IGBT, which are properly described in the proposed model.

The proposed model of the IGBT was elaborated and verified for the devices made of silicon only. This model can be useful for designers of electronic and power electronic networks containing the IGBT. The presented characteristics of this transistor will help also identify the causes of damage of the networks containing IGBTs.

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Nomenclature

isothermal characteristics	characteristics determined at a constant value of the device internal temperature
non-isothermal characteristics	characteristics determined with thermal phenomena taken into account
electrothermal model	a model describing current-voltage-temperature dependences with thermal phenomena taken into account
i_C	collector current of the IGBT
k	the Boltzmann constant
LIMIT(x, min, max)	a standard-function of SPICE, whose value is equal to min, if $x < \min$, max, if $x > \max$, and in other cases it is equal to x
P_{thT}	thermal power dissipated in the transistor
P_{thD}	thermal power dissipated in the diode
q	electron charge
R_{thT}	thermal resistance of the transistor
R_{thD}	thermal resistance of the diode
R_{thTD}	transfer thermal resistance between the transistor and the diode
$R_{thT1}, R_{thT0}, a, b, T_Z$	parameters occurring in the dependence $R_{thT}(T_a, T_{jT})$
T_a	ambient temperature
T_{jD}	internal temperature of the diode
T_{jT}	internal temperature of the IGBT
T_0	reference temperature
$V_{BE1}, V_{GE1}, V_{BC1}, V_{GE}, V_{GC1}, V_{CE1E}$	voltages between the internal terminals of the BJT and the MOSFET contained in the structure of the IGBT marked in Figure 2
V_{CE}	collector-emitter voltage of the IGBT
V_{GE}	gate-emitter voltage of the IGBT
V_{go}	voltage corresponding to a band-gap of silicon
ϵ_0	dielectric permeability of free air
ϵ_{ox}	relative dielectric permeability of silicon
Parameters of a MOS transistor:	
B	parameter of the main component of drain current
C_{GD0}	capacitance between the gate and the drain per unit of widths of the channel
C_{GE0}	capacitance between the gate and the emitter per unit of widths of the channel
C_{ox}	capacitance dependent on thickness t_{OX} of the layer of SiO_2 under the gate
$C_1, C_2, y, e, n, V_{GCmin}$	parameters describing C_{GD0} capacitance
i_D, i_{C1}, i_{C2}, i_E	currents marked in Figure 2
I_{PO}	parameter of sub-threshold current
L	length of the channel
n_p	the emission coefficient of sub-threshold current
v_{mi}	voltages on terminals of controlled voltage sources E_1 , to which the main part of drain current is proportional; the value of this voltage depends on voltages v_{GE1}, v_{BG1} and v_{VT}

v_{PH}	the Fermi level linearly dependent on temperature T_{jT}
v_{VT}	threshold voltage linearly dependent on temperature T_{jT}
w	width of the channel
$V_{GEmax}, V_{GEmin}, C_{G1}, C_{G2}, x, u$ and k_1	parameters of the model describing C_{GE0} capacitance
Parameters of a BJT:	
I_0	parameter, to which the collector current is proportional
M_{j2}	parameter describing the doping profile of the base-emitter junction
n_1	the emission coefficient of the base-emitter junction
U_{AN}	Early voltage
V_{jC}	built-in potential of the base-emitter junction
v_{RC}, v_{CE1}	voltages between the internal terminals of the BJT marked in Figure 2
β_F	the current amplification coefficient within the forward active mode; this coefficient depends on temperature T_{jT} and the collector current
Parameters of a diode:	
C_{CE0}	capacitance at zero voltage on the diode
I_{0D}	parameter, to which the diode current is proportional
M_j	parameter describing the doping profile of the junction
n_D	the emission coefficient of the diode
r	the temperature coefficient of parameter M_j .
V_j	built-in potential

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