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High-Efficiency DC–DC Converter with Charge-Recycling Gate-Voltage Swing Control

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Abstract: This paper proposes a high-efficiency DC–DC converter with charge-recycling gate-voltage swing control with a light load. By achieving a variable gate-voltage swing in a very efficient manner by charge recycling, the power efficiency has been substantially improved due to the lower power consumption and the achieved balance between the switching and conduction losses. A test chip was fabricated using 65-nm CMOS technology. The proposed design reduces the gate-driving loss by up to 87.7% and 47.2% compared to the conventional full-swing and low-swing designs, respectively. The maximum power conversion efficiency was 90.3% when the input and output voltages are 3.3 V and 1.8 V, respectively.

Keywords: Buck converter; high efficiency; charge-recycling; gate-voltage swing control

1. Introduction

Portable devices, such as mobile phones, tablets and MP3 players, have become essential in our daily life. Since these devices require a long battery lifetime, power efficiency has become one of the important design considerations. To extend the battery lifetime by maximizing the power efficiency, the switching regulators must be used for transforming battery supplies into various regulated voltages [1,2]. In particular, since many portable devices stay in standby mode for most of their operation time, improving the light-load efficiency of the switching regulators is a very important design concern [3,4].

Conduction and switching losses are the two main types of power loss in the switching regulators. The conduction loss occurs by the current flowing across resistive components, which mainly happens through the power transistors. The switching loss occurs by the current charging and discharging parasitic capacitances, which are majorly used for driving the power switches. The switching loss of a power stage is largely caused by the switching power consumption of CMOS circuits, which can be expressed as:

$$P_{SW} = CV_{in}{}^2 f_s \quad (1)$$

where C is the switching capacitance of a power stage, V_{in} is the input voltage and f_S is the switching frequency. In the common DC–DC converters, the switching loss is dominant in the light load, whereas the conduction loss is dominant in the heavy load. Thus, in order to improve the performance of DC–DC converters in terms of the light-load efficiency, the switching power consumption governed by Equation (1) has to be minimized.

According to Equation (1), the switching loss can be scaled down by reducing the switching frequency of a converter or by minimizing the amount of switching capacitance. Various design techniques have been reported for reducing the switching loss. Pulse frequency modulation

(PFM) [5–8], pulse skip mode [9] and burst-mode scheme [10] are several representative frequency control techniques. However, they have poor output regulation and experience the electromagnetic interference (EMI) noise problem. A segmented power stage (SPS) control can be used to optimize the trade-off between the effective gate capacitance and the power transistor on-resistance [11]. However, it can increase the switching activities and complexities. An alternative approach is the adaptive gate swing (AGS) control [12,13], in which the gate drive voltage is adjusted depending on the load current. However, AGS needs two additional reference voltages that require additional power consumption. Moreover, AGS control needs information about the power transistor on-resistance and the gate voltage characteristic to define an optimal gate-drive voltage under various load conditions [14]. To minimize the switching portion of the power consumption for a given switching capacitance, the charge-recycling technique can also be used [15–17]. In [15], the power switch gate charge was stored in an explicit storage node for use in the next cycle. The additional capacitor and inductor for these schemes may occupy a large area and require complex control. In [16], the charge in PMOS buffer stage was reused in the NMOS buffer stage. Although it can improve the light-load efficiency, the gate voltage swing is fixed and cannot be controlled. In [17], the power switch gate charge is stored at the output node and recycled in the buffer stage. However, the overall efficiency is not so high since the amount of power saved by charge recycling must all be resupplied from the input.

The proposed buck converter combines the charge-recycling and variable gate-voltage swing schemes in order to improve the power efficiency when there is a light load. This paper is organized as follows: Section 2 presents the variable-swing charge-recycle technique. In Section 3, the chip test results are discussed and finally, the conclusions are provided in Section 4.

2. Proposed Buck Converter

Figure 1 shows the overall block diagram of the proposed voltage-mode pulse-width modulation (PWM) buck converter, which is composed of the power MOSFETs (M_P and M_N), an LC filter, a type-III compensation network, a charge-recycling variable-swing gate driver, a bias selector, a comparator, a dead time controller, a zero current detector and an adaptive frequency ramp generator. The charge-recycling variable-swing gate driver is used to adaptively adjust the gate voltage swing of power transistors through charge recycling. The adaptive frequency ramp generator provides a sawtooth signal V_{RAMP}, which has a frequency that is determined by the load current. Since the L-C_L output filter generates low-frequency complex poles and the equivalent series resistance (ESR) of the output capacitor produces a zero in the feedback loop, a compensation network is required. The type-III compensation network generates two zeros and two poles. Two poles are set at the switching frequency of the converter to nullify the ESR zero and attenuate the high frequency noise. A voltage regulation is provided by a negative feedback, which amplifies the difference between the output voltage V_{OUT} and reference voltage V_{REF}. The duty ratio of the PWM signal V_{PWM}, which is defined as the ratio of the time that the power switch is in a cycle, is obtained by comparing V_{EA} with V_{RAMP} in order to regulate the output voltage to the reference voltage.

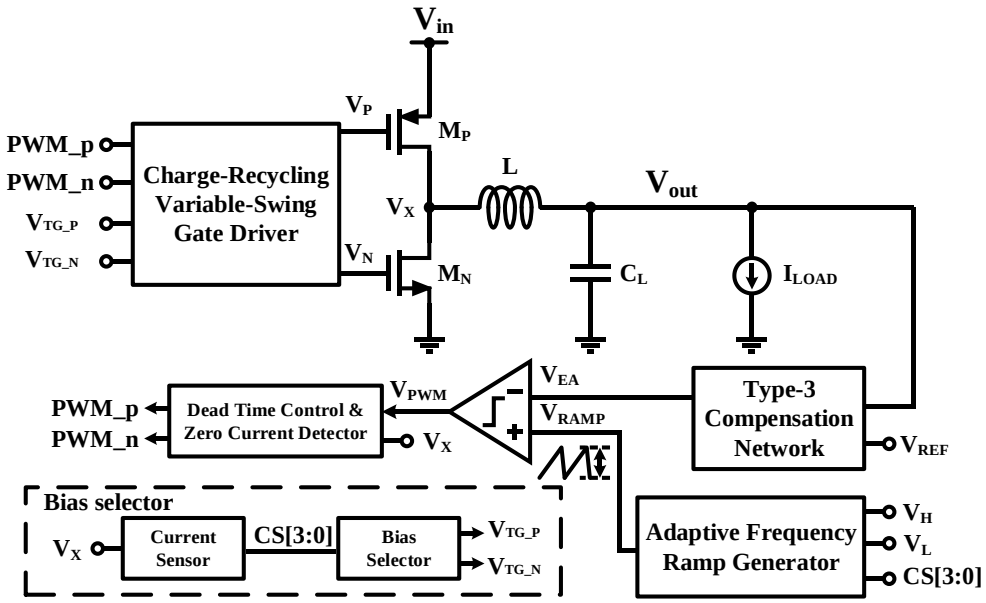

Figure 1. Proposed PWM buck converter with charge-recycling variable-swing gate driver.

2.1. Charge-Recycling Gate Driving

Figure 2 depicts the generic structure of the proposed charge-recycling variable-swing gate driver, which is exemplified by using two-stage tapered buffers (the actual design can have more stages). The driver consists of a pair of tapered buffers, which are namely the P-buffer and N-buffer, a charge-recycling capacitor (C_{REC}) and a variable resistance switch. This driver performs the charge-recycling and variable voltage-swing operation. The driver allows for the electric charge used to charge the gate capacitance of M_P to be recycled for charging the gate capacitance of M_N. The variable resistance switch is implemented by a transmission gate that is driven by the bias voltages V_{TG_P} and V_{TG_N}. This switch can modulate the gate voltage swing by changing the bias levels depending on the load condition. It is important to note that since the proposed circuit is designed to have an identical size for power transistors, the gate capacitances of M_N and M_P are equal to each other. The capacitance value of C_{REC} is also equal to that of a power transistor.

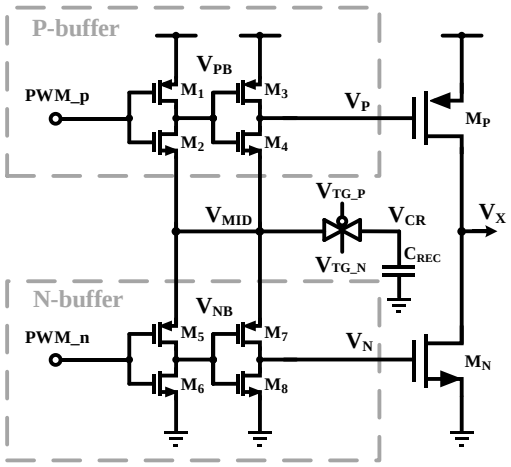

Figure 2. Proposed charge-recycling variable-swing gate driver.

The transient waveforms for illustrating the operation of the buffer are shown in Figure 3. PWM_p and PWM_n are the inputs to the P- and N- buffers, respectively, which is depicted in Figure 2. V_{PB} and V_{NB} are the internal nodes of the P- and N- buffers, respectively. V_{MID} is the mid-node between the

stacked buffers and V_{CR} is the recycle capacitor node. V_P and V_N are the outputs of the buffers that are used to drive the power transistors M_P and M_N, respectively. To explain the charge-recycling aspect of the driver operation, let us assume that V_{TG_P} and V_{TG_N}, the bias voltages determining the on/off state of the transmission gate connecting V_{MID} and V_{CR}, are set to 0 V and 3.3 V, respectively, so that the transmission gate stays fully on. (With these bias voltages, the gate voltage swing will be fixed and the variable gate voltage swing will be considered in Section 2.2.) Thus, V_{MID} and V_{CR} are at the same voltage level and assumed to be at 2.2 V. When PWM_p rises from 0 V to 3.3 V (period ① in Figure 3), M_1 and M_2 turn off and on, respectively. After this, the voltage of V_{PB} follows that of V_{MID} and V_{CR} since the parasitic capacitance of V_{PB} is much smaller than the sum of the parasitic capacitance at V_{MID} and the recycle capacitor C_{REC}. This implies that the charge on V_{PB} is not discarded to the ground but is instead stored in C_{REC} for future use. After this, because V_{PB} falls from 3.3 V to 2.2 V, M_3 is turned on and M_4 is turned off. This results in the output V_P of the P-buffer being 3.3 V, which turns the power transistor M_P off. After that, when PWM_n rises from 0 V to 3.3 V (period ②), M_5 and M_6 are turned off and on, respectively. Thus, V_{NB} becomes 0 V, turning M_7 on and M8 off. After this, the output V_N of the N-buffer rises from zero to the voltage of V_{MID}. This means that the charge stored in C_{REC} is recycled to drive the power transistor M_N. For determining the resulting voltage of V_N, we can use the charge conservation law during the state transition from period ① to period ②, which is described as follows:

$$\begin{aligned} Q_{①\rightarrow②} &= (C_{REC}+C_{MID}+C_{PB})\,V_{CR} \\ &= (C_{GN}+C_{REC}+C_{MID}+C_{PB})V_N \end{aligned} \tag{2}$$

where C_{PB} is the gate capacitance of the last stage of P-buffer, C_{MID} is the parasitic capacitance of V_{MID} and C_{GN} is the gate capacitance of M_N. Thus, V_N can be found to be:

$$V_N = \frac{(C_{REC}+C_{MID}+C_{PB})\,V_{CR}}{C_{GN}+C_{REC}+C_{MID}+C_{PB}}. \tag{3}$$

The gate capacitances of the power transistors are much larger than the gate capacitances of the buffers ($C_{GN} >> C_{PB}$) and the recycle capacitance value is much larger than the parasitic capacitances of V_{MID} and V_{PB} ($C_{REC} >> C_{MID}$). Thus, V_N can be written as:

$$V_N \approx \frac{C_{REC}}{C_{GN}+C_{REC}} V_{CR}. \tag{4}$$

From Equation (4), if C_{GN} and C_{REC} are equal in size and V_{CR} is 2.2 V, the voltage at V_N and V_{MID} will become 1.1 V.

When PWM_n is reduced from 3.3 V to 0 V (period ③), M_5 is turned on and M_6 is turned off, respectively. As the parasitic capacitance of V_{NB} is very small compared to C_{REC}, the voltage of V_{NB} then follows that of V_{MID} and C_{REC}, which implies that the stored charge C_{REC} is recycled to drive the N-buffer. After this, since V_{NB} increases from 0 V to 1.1 V, M_7 is turned off and M_8 is turned on. This results in the output V_N of the N-buffer being 0 V, which turns off the power transistor M_N. After that, when PWM_p is reduced from 3.3 V to 0 V (period ④), M_1 is turned on and M_2 is turned off, respectively. Thus, V_{PB} becomes 3.3 V, turning M_3 off and M_4 on. This allows the output of P-buffer to fall from 3.3 V to V_{MID}. This means that the charge stored in C_{GP} is not wasted to the ground but is instead shared in C_{REC} for future use. Using the same procedure as before, the charge conservation law (from period ③ to period ④) gives:

$$\begin{aligned} Q_{③\rightarrow④} &= C_{GP}V_{in} + (C_{REC}+C_{MID}+C_{NB})\,V_{CR} \\ &= (C_{GP}+C_{REC}+C_{MID}+C_{NB})V_P \end{aligned} \tag{5}$$

where C_{NB} is the gate capacitance of the last stage of N-buffer. After this, V_P can be written as:

$$V_P = \frac{C_{GP}V_{in}+(C_{REC}+C_{MID}+C_{NB})\,V_N}{C_{GN}+C_{REC}+C_{MID}+C_{NB}}. \quad (6)$$

Furthermore, C_{PB}, C_{NB} and C_{MID} are ignored because they are very small compared to C_{GP}, C_{GN} and C_{REC}. Thus, V_P can be written as:

$$V_P \approx \frac{C_{GP}V_{in}+C_{REC}V_N}{C_{GP}+C_{REC}}. \quad (7)$$

In this design, C_{GP} and C_{REC} are equal in size. In period ③, V_N is 1.1 V and V_{in} is 3.3 V so V_P and V_{CR} are determined as 2.2 V according to Equation (7). Since the charge recycling capacitor, the power PMOS gate capacitor and the power NMOS gate capacitor have the same capacitance, V_P, V_N and V_{CR} will have the same voltage swing difference. That is, V_P (V_N) swings from 2.2 V to 3.3 V (from 0 V to 1.1 V) and V_{CR} swings from 2.2 V to 3.3 V. Accordingly, V_{PB} and V_{NB} swing from 1.1 V to 3.3 V and from 0 V to 2.2 V, respectively.

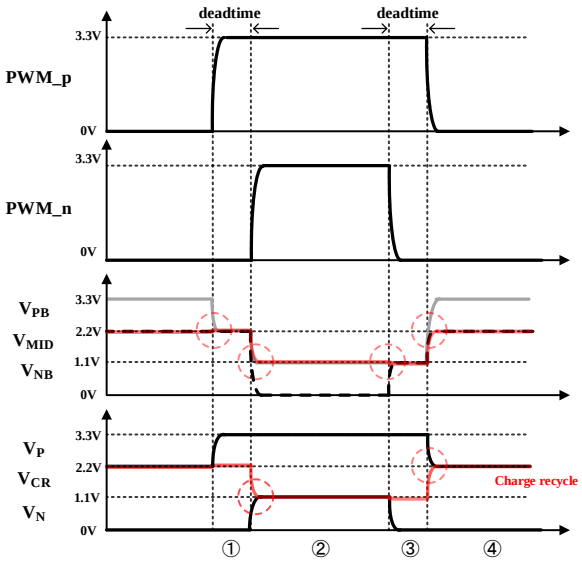

Figure 3. Timing diagram of the proposed gate driver.

Figure 4 compares the operations of the conventional full-swing driver and the proposed charge-recycling gate driver in order to compare their effectiveness in terms of energy consumption. In the conventional full-swing driver, the amount of charge used by the gate capacitance during one period can be written as:

$$\begin{aligned} Q_{P\_fullswing} &= C_{GP}(V_{in}-0) + C_{PB}(V_{in}-0) \\ &= C_{GP}V_{in}+C_{PB}V_{in} \end{aligned} \quad (8)$$

$$\begin{aligned} Q_{N\_fullswing} &= C_{GN}(V_{in}-0) + C_{NB}(V_{in}-0) \\ &= C_{GN}V_{in}+C_{NB}V_{in}. \end{aligned} \quad (9)$$

In the conventional design, since the ratio of PMOS and NMOS is 2:1, the power switches have:

$$C_{GP} = 2C_{GN}. \quad (10)$$

Ignoring the gate capacitance of each buffer stage, the total charge used by the conventional full-swing driving can be expressed as:

$$\begin{aligned} Q_{total\_fullswing} &= Q_{p\_fullswing} + Q_{N\_fullswing} \\ &\approx C_{GP}V_{in} + C_{GN}V_{in} = \tfrac{3}{2}C_{GP}V_{in}. \end{aligned} \tag{11}$$

For the proposed charge-recycling gate driver, the amount of charge used by the gate capacitance during one period can be written as:

$$\begin{aligned} Q_{P\_prop} &= C_{GP}(V_{in} - \tfrac{2}{3}V_{in}) + C_{PB}(V_{in} - \tfrac{1}{3}V_{in}) \\ &= \tfrac{1}{3}C_{GP}V_{in} + \tfrac{2}{3}C_{PB}V_{in} \end{aligned} \tag{12}$$

$$Q_{N\_prop} = 0 \tag{13}$$

As the charge used by the P-buffer is recycled by the N-buffer, the proposed scheme only needs the charge for the P-buffer stage. After again ignoring the gate capacitance of each buffer stage, the total charge used by the proposed charge-recycling variable-swing driving is given by:

$$Q_{total\_prop} = Q_{P\_prop} + Q_{N\_prop} \approx \frac{1}{3}C_{GP}V_{in}. \tag{14}$$

As shown in Equations (11) and (14), the total charge used by the proposed charge-recycling gate driver for switching the power transistors can be decreased by 77.8% as compared to the conventional full-swing driver.

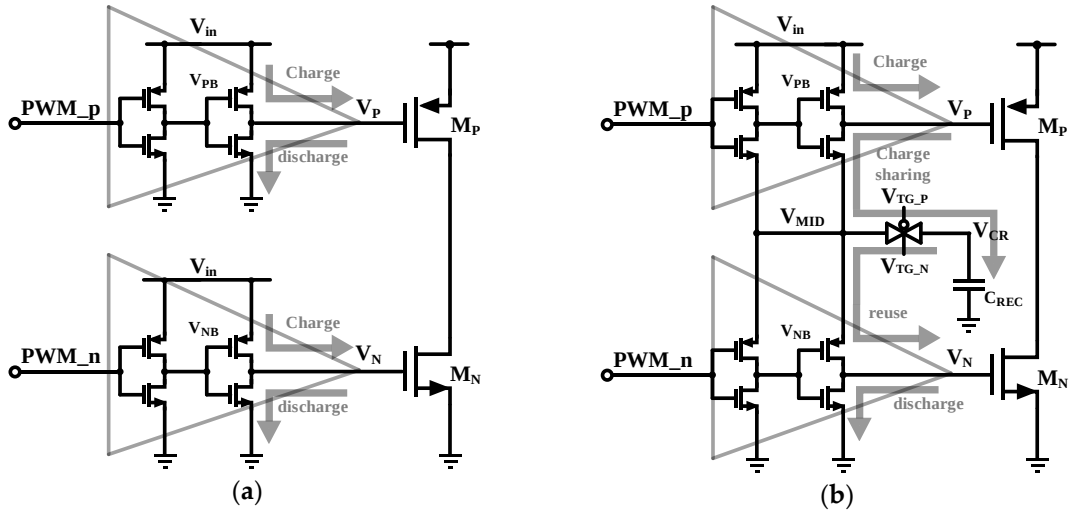

Figure 4. Gate driver operation: (**a**) conventional full-swing gate driver and (**b**) proposed charge-recycling gate driver.

2.2. Variable Gate-Voltage Swing Control

As explained in the previous section, when the voltage swing at the gate of a power transistor is reduced, the switching loss will decrease. However, the conduction loss may increase since the on-resistance of the power transistors will be larger. Hence, an optimum voltage swing will exist, at which the sum of the switching and conduction losses is minimized at each given load condition [2]. In order to achieve maximum energy efficiency, the power transistors and the tapered buffers need to operate with this optimum voltage swing. To obtain this optimum voltage swing, the gate-voltage swing must be adaptively controlled since the amount of load current can change arbitrarily. All the current conventional charge-recycling buffers have a constant gate-voltage swing and are not controlled adaptively [15–17]. The proposed charge-recycling gate driver described in the previous

section can be adjusted to have variable gate-voltage swing by controlling the amount of current flowing into or out of the recycle capacitor.

In order to provide the variable gate-voltage swing capability to the proposed charge-recycling gate driver in Figure 2, we need to adjust the bias voltage levels of V_{TG_P} and V_{TG_N} for the transmission gate in the driver. The bias level selector determines the bias voltages for a given load condition. The current sensor senses the amount of the load current and generates an output V_{SENSE}. After this, a 4-bit thermometer code (CS[3:0]) is generated by comparing the peak voltage of V_{SENSE} to a set of reference voltages, which can be used to adjust the bias voltage levels of V_{TG_P} and V_{TG_N}. In this design, the light (very light) load condition is defined when the load current is less than 100 mA (50 mA), in which the bias voltage is adjusted. When the load current is in the heavy load condition, the bias voltages V_{TG_P} and V_{TG_N} are selected to be 0 V and 3.3 V, respectively. As the load current decreases and enters the light load condition, the voltage level of V_{TG_P} (V_{TG_N}) can be properly increased (decreased) to control the amount of charge shared between the power transistor gate capacitance and C_{REC}. As the amount of charge shared is reduced, the gate voltage swing of power transistors will decrease. Figure 5 shows the signal waveforms of the p-type and n-type power transistor gate voltages and V_{MID} depending on the amount of the load current, which is exemplified by the operation in the very light load condition. If the load current is over 50 mA, V_P swings from 2.2 V to 3.3 V and V_N swings from 0 V to 1.1 V, which means that the power transistor gate voltage swing is 1.1 V. As the load current decreases by 10 mA, the power transistor gate voltage swing is reduced by 50 mV. Overall, the power transistor gate voltage swing ranges between 1.1 V and 900 mV depending on the load condition, which can minimize the switching loss in the light load.

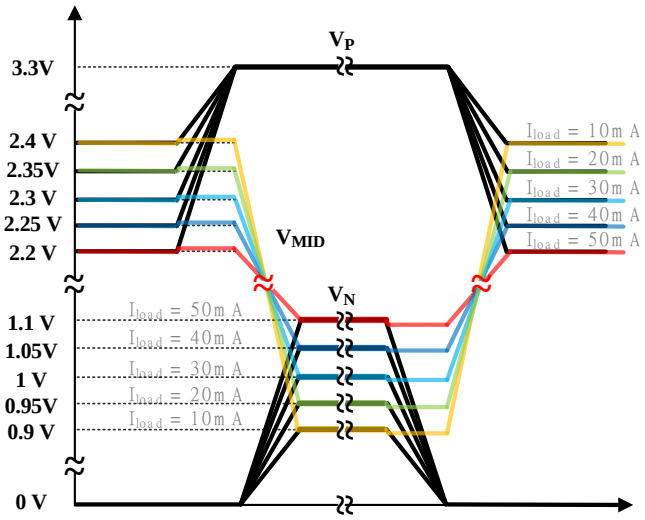

Figure 5. Power transistor gate voltage waveforms depending on the amount of load current.

Since it is well known that operating at a low switching frequency is another effective way of decreasing the switching loss, the proposed converter is designed to adjust the switching frequency. Figure 6a shows the schematic diagram of the adaptive frequency ramp generator for controlling the switching frequency of the converter. It is composed of a ramp capacitor, a reset switch, comparators and an SR latch. V_H and V_L are the reference voltages that make the peak and valley of the ramp signal. I_{BIAS} is charged in C_{RAMP} before V_{RAMP} rises until V_H is reached. When V_{RAMP} reaches V_H, the SR latch generates the reset signal V_{PULSE}. After this, M_{RESET} discharges C_{RAMP} until V_{RAMP} reaches V_L. The frequency of V_{RAMP} can be expressed as:

$$f_s \propto \frac{I_{BIAS}}{C_{RAMP}(V_H - V_L)} \tag{15}$$

where C_{RAMP} is the total capacitance of the cap bank. The frequency is proportional to I_{BIAS} while this frequency is inversely proportional to C_{RAMP} and the difference between V_H and V_L. If the load current is so small that the buck converter operates in a very light load condition, C_{RAMP} is increased by the 4-bit code (CS[3:0]) generated by the bias selector. After this, the frequency is decreased as the load current decreases, which is shown in Figure 6b. The ramp frequency control range is set between 6.5 MHz and 2.8 MHz depending on the load condition. Thus, the total efficiency is improved by reducing the switching loss.

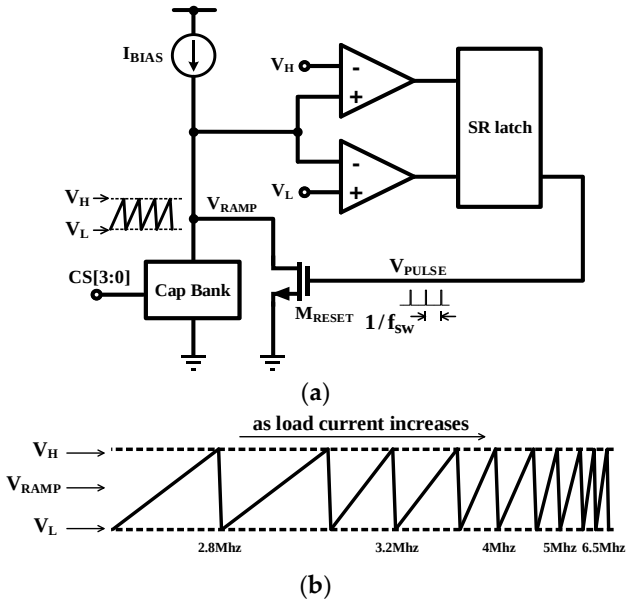

Figure 6. Adaptive frequency ramp generator: (**a**) schematic and (**b**) ramp waveform.

3. Measurement Results

The proposed high-efficiency buck converter with a charge-recycling variable gate-voltage swing control was fabricated using a 65-nm CMOS technology. The input supply voltage is 3.3 V. The regulated output voltage ranges from 1.2 V to 2.3 V and the maximum load current is 700 mA. The conventional full-swing and low-swing converters [12] have also been designed. The chip microphotograph of the buck converter is shown in Figure 7, which has a die size of about 1.3 mm^2, including pads. The filtering inductor (L) and the output capacitor (C_L) are attached as off-chip components.

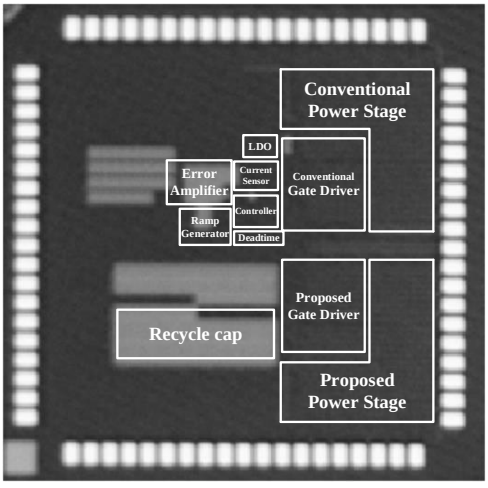

Figure 7. Microphotograph of the test chip.

In the proposed prototype design, two reference voltages were employed for the implementation of the adaptive voltage swing and switching frequency adjustment in Figure 6. There were three different groups according to the load current: over 100 mA, 50–100 mA and under 50 mA. Figure 8 shows the measured gate voltages of the power MOSFETs. When the load current is over 100 mA, the voltage swing of V_P and V_N are 1.21 V and 1.20 V, respectively, which is shown in Figure 8a. When the load current is in the range between 50 mA and 100 mA, since the bias voltage level of V_{TG_P} (V_{TG_N}) is controlled and subsequently increased (decreased), V_P and V_N swings are reduced to 1.00 V and 1.07 V, respectively, which is shown in Figure 8b. When the load current is under 50 mA, for the same reason, V_P and V_N swing range are reduced to 0.60 V and 0.76 V, respectively, which is shown in Figure 8c. Figure 9 depicts the measurement results for the ramp waveforms. The ramp amplitude is fixed at 1.5 V and the ramp frequency is controlled by the size of C_{RAMP}. As mentioned earlier, the total capacitance of cap bank is controlled by the 4-bit thermometer code from the bias selector. When the load current is over 100 mA, the ramp frequency is 4 MHz, which is shown in Figure 9a. According to Equation (15), the frequency decreases as the C_{RAMP} increases, which is achieved by controlling the bias voltages. The ramp frequency becomes 3 MHz when the load current is in the range of 50–100 mA as shown in Figure 9b. Likewise, when the load current is under 50 mA, the ramp frequency is 2 MHz, which is shown in Figure 9c. In this way, the gate-driving loss can be effectively reduced by variable gate-voltage swing and adaptive switching frequency controls when the converter is operating in the light load region.

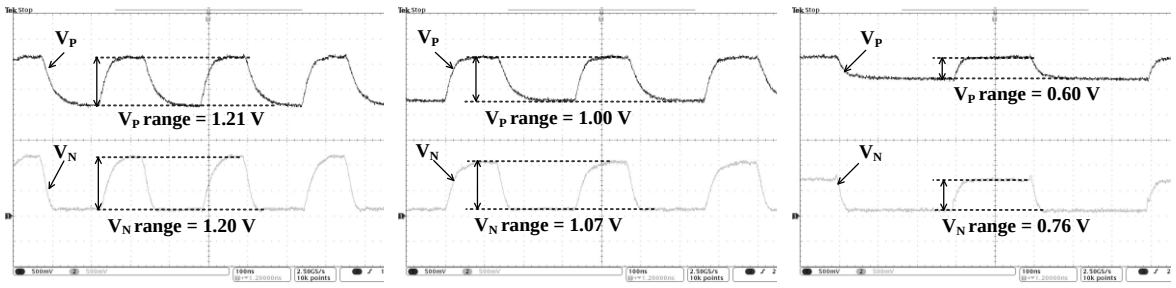

Figure 8. Measured power MOSFET gate voltage swing with bias control: (**a**) I_{LOAD}: over 100 mA, (**b**) I_{LOAD}: from 50 mA to 100 mA and (**c**) I_{LOAD}: under 50 mA.

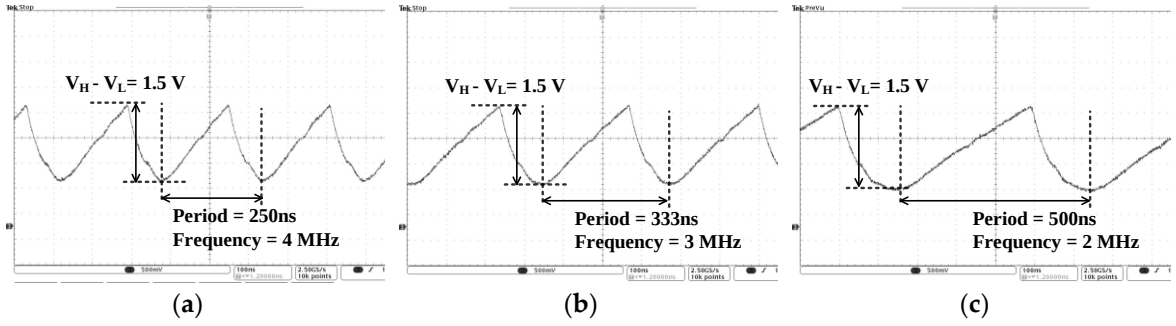

Figure 9. Measured ramp waveform: (**a**) normal load condition (I_{LOAD}: over 100 mA), (**b**) light load condition (I_{LOAD}: from 50 mA to 100 mA) and (**c**) very light load condition (I_{LOAD}: under 50 mA).

Figure 10 compares the measured gate-driving loss of buck converters according to the load condition. The conventional full-swing converter has a fixed gate-voltage swing of 3.3 V and a constant switching frequency of 4 MHz regardless of the amount of load current. The conventional low-swing converter has the same constant switching frequency but a variable gate-voltage swing of 1.2–0.60 V, which is set to be the same as that of the proposed converter. As explained previously, the proposed buck converter utilizes charge recycling, variable gate-voltage swing and adaptive switching

frequency control. When the load current is over 100 mA at a switching frequency of 4 MHz, the conventional full-swing and low-swing buck converters have gate-driving losses of 19.6 mW and 7.8 mW , respectively. For the same load current, the proposed buck converter has a gate-driving loss of 4.7 mW , which indicates improvements of up to 76.3% and 40.1% in terms of the gate-driving loss, respectively. The former improvement comes from the reduced gate voltage swing, charge recycling and adaptive ramp frequency while the latter is purely due to the charge recycling. When the load current is in the range of 50–100 mA, the conventional full-swing converter has the same gate-driving loss of 19.6 mW since the gate voltage swing and the switching frequency are not changed. The conventional low-swing converter has a smaller gate-driving loss of 6.3 mW (improvement of 19.3% compared to 100-mA-load case), which is mAinly due to the reduction of the gate voltage swing from 1.21 V to 1.00 V (the switching frequency is the same). For the proposed buck converter, a greater reduction of 3.4 mW (improvement of 27.9% compared to 100-mA-load case) in the gate-driving loss is obtained since in addition to the charge recycling, the gate voltage swing is reduced from 1.21 V/1.20 V to 1.00 V/1.07 V (in terms of V_P/V_N, see Figure 8) and the switching frequency is reduced from 4 MHz to 3 MHz. As a result, the proposed buck converter achieves improvements of 82.9% and 46.5% in overall performance in terms of the gate-driving loss compared to the conventional full-swing and low-swing converters. When the load current is reduced to under 50 mA, the conventional full-swing converter still has a gate-driving loss of 19.6 mW whereas the conventional low-swing buck converter has a reduced gate-driving loss of 4.6 mW . The proposed buck converter has a further reduction in its gate-driving loss (2.4 mW), which is mainly due to the further reduction in the gate voltage swing and switching frequency as well as charge recycling, which indicates improvements of up to 87.7% and 47.2% in terms of gate-driving loss. Figure 11 depicts the measured power efficiency of conventional and proposed buck converters for the load current of 10–150 mA at a given voltage conversion from 3.3 V to 1.8 V. The proposed buck converter has the maximum power efficiency of 90.27% at a load current of 100 mA. In the range of the light load (less than 100 mA), the maximum power efficiency improvements occurring at a load current of 20 mA are 16.3% and 5.0% compared to the conventional full-swing and low-swing buck converters, respectively. Table 1 summarizes the measured performances and design specifications of the proposed, conventional low-swing [4], variable frequency control [5], pulse-frequency-control (PFM) [6,8], adaptive gate swing control [13], charge-recycling [15,16] and switched capacitor hybrid [18] DC–DC converters. Compared to conventional works, the proposed buck converter has a wide range of output voltage from 1.2 V to 2.3 V and can be used in applications requiring various output voltages. Furthermore, it achieves a small area of 1.3 mm^2 and a peak efficiency of 90.3%. Considering that the area and efficiency are both indicated by a matrix of 'area/efficiency', the proposed converter has good performance. It also has the highest maximum load current of 700 mA.

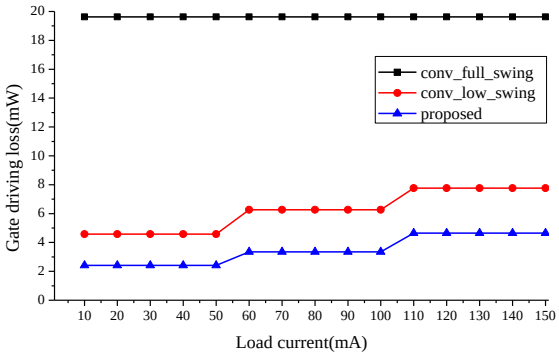

Figure 10. Measured gate driving loss of buck converters.

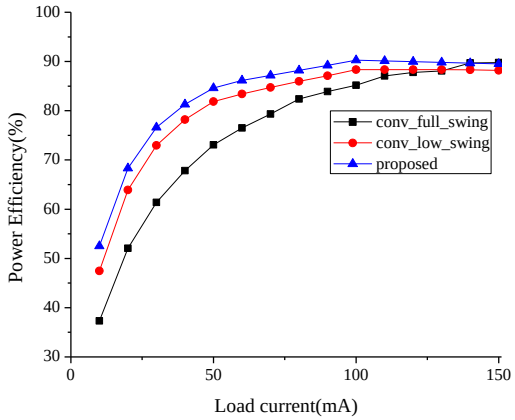

Figure 11. Measured power efficiency of buck converters.

Table 1. Performance comparison of DC–DC converter.

	[4]	[5]	[6]	[8]	[13]	[15]	[16]	[18]	This Work
Technology (nm)	350	350	180	180	180	500	180	65	65
Supply voltage (V)	2.6–3.6	2.7–5	0.22–1.3	1.2	0.9–1.4	3.6	2.2	1.2	3.3
Output Voltage (V)	0.6–2.1	1	1.8	1.8	2.5	1.8	0.75–1.0	0.1–1.1	1.2–2.3
Inductor (μH)	22	10	4.7	10	1	4.7	2.2×10^{-3}	5.8×10^{-3}	4.7
Capacitor (μF)	22	10	N/A	47	10	3.3	1.1×10^{-3}	4.4×10^{-3}	4.7
Frequency (MHz)	1	0.1–0.6	0.02–0.06	0.001–0.04	0.8	3	660	10–40	2–4
Die area(mm^2)	3.04	3.57	0.72	0.43	1.5	5.3	2.5	2.34	1.3
Load current (mA)	450	460	50	50	60	500	40–55	100	1–700
Max. efficiency (%)	90	95	90.6	88.39	88	89.1	65	93.2	90.3
Area/efficiency	2.74	3.39	0.79	0.49	1.70	5.95	3.85	2.51	1.44

4. Conclusions

This paper presents a high-efficiency buck converter with a charge-recycling variable gate-voltage swing control. The measurement results indicated that the gate-driving loss of the proposed buck converter was decreased by up to 87.7% and 47.2% compared to the conventional full-swing and low-swing buck converters, respectively, in the very light load condition. The overall power efficiency at the light load region was also improved, with the highest efficiency reaching 88.3%. The proposed converter can also supply a large load current with a wide output voltage range and occupy a relatively small area. Therefore, the proposed buck converter architecture is suitable for applications in highly efficient portable electronic systems.

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