





A Novel Filter Extracted Equivalent Control Based Fixed Frequency Sliding Mode Approach for Power Electronic Converters

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Abstract: The key issue in the implementation of the Sliding Mode Control (SMC) in analogue circuits and power electronic converters is its variable switching frequency. The drifting frequency causes electromagnetic compatibility issues and also adversely affect the efficiency of the converter, because the proper size of the inductor and the capacitor depends upon the switching frequency. Pulse Width Modulation based SMC (PWM-SMC) offers the solution, however, it uses either boundary layer approach or employs pulse width modulation of the ideal equivalent control signal. The first technique compromises the performance within the boundary layer, while the latter may not possess properties like robustness and order reduction due to the absence of the discontinuous function. In this research, a novel approach to fix the switching frequency in SMC is proposed, that employs a low pass filter to extract the equivalent control from the discontinuous function, such that the performance and robustness remains intact. To benchmark the experimental observations, a comparison with existing double integral type PWM-SMC is also presented. The results confirm that an improvement of 20% in the rise time and 25.3% in the settling time is obtained. The voltage sag during step change in load is reduced to 42.86%, indicating the increase in the robustness. The experiments prove the hypothesis that a discontinuous function based fixed frequency SMC performs better in terms of disturbances rejection as compared to its counterpart based solely on ideal equivalent control.

Keywords: DC-DC converter; fixed frequency sliding mode control (SMC); pulse width modulation (PWM); filter extracted equivalent control (FEEC)

1. Introduction

Disturbance rejection, order reduction and capability to handle systems with un-modeled dynamics are the key properties of Sliding Mode Control (SMC) that make it a good choice to control non-linear systems with perturbations. The system under SMC becomes invariant to parametric changes and its performance is completely robust against matched disturbances [1–4]. Due to these properties, SMC finds a wide range of applications in motor control, PWM drives, power electronics, robotics, micro-grids and automotive control [5–12]. Moreover, the complexity of feedback control design is reduced by SMC because it decouples the system into reduced order dynamics [13].

In power electronic converters, the output voltage is controlled by switching the semi-conductor device between two states, ON and OFF. Thus, the control input can only take a value from the discrete set of $\{0,1\}$. This particular nature of switching converter makes SMC an appropriate choice for controlling such circuits [14].

The SMC is ideally implemented using a discontinuous function that operates the switch at infinite frequency. Thus forcing the state trajectories to slide along the designed manifold towards the origin. However, it is not possible to achieve infinite switching frequency in physical systems. The first realistic approach towards SMC implementation is presented in [15], where the discontinuous sign function is replaced by a hysteresis comparator which is tuned to limit the maximum switching frequency according to the physical limits of the system. The scheme results in finite, but time varying switching frequency [16]. As a result, finite magnitude oscillations, known as chattering, appear in the

output of the system [17]. The chattering is acceptable within limits for a particular system. However, the problem of variable switching frequency becomes a serious issue for electronic converters. They need a fixed frequency operation [18–20] because they consist of passive energy storing components (inductors and capacitors) and their correct size primarily depend upon the switching frequency. Moreover, the varying switching frequency degrades the power quality and makes it non-trivial to suppress electromagnetic interference (EMI) [21,22].

The researchers have proposed different methods to address the above-mentioned problem by fixing the switching frequency in SMC. A method using a comparator with adaptive hysteresis band is proposed in [23–25]. This method varies the hysteresis band such that the switching frequency remains fixed. This adaptation requires knowledge of the system states and consequently needs additional sensors and state observers that increase the implementation cost and complexity.

The schemes in [26–29] use an additional PI control loop that adjusts the width of the hysteresis band in order to achieve fixed switching frequency. This design requires the dynamics of the Frequency Control Loop (FCL) to be much slower as compared to the dynamics of the voltage and current control loops, as the faster dynamics may cause interaction with the outer control loops [26,27], hence the stability of the linearized system may not be ensured in this scenario [28,29]. In [30], the authors have proposed an FCL that monitors the time period of each switching cycle and compares it with a reference switching period. The difference in switching period is fed to a frequency regulation controller that updates the values of hysteresis band accordingly. The common drawback of these schemes is the addition of another control loop that increases the cost and complexity of the design.

The techniques presented in [31,32] demonstrate the use of external signal to enforce constant switching frequency in SMC. The scheme shows good results when the switching frequency is kept low as compared to the time constant of the system. However, if the frequency is increased, the system states drift away causing a steady state error.

In [33], Zero Average Dynamics (ZAD) method is used to achieve fixed switching frequency and is practically demonstrated in [34]. The scheme works by computing a duty ratio that ensures a zero T-periodic mean of the switching function. As a result the switching frequency is fixed during the steady state operation of the closed loop system. However, complex calculations and the compulsion of a fast processor are major drawbacks of this scheme. A second order sliding mode controller with constant switching frequency, utilizing the concept of state machine is presented in [35]. However, the requirements like fast analogue to digital converter and the need for an FPGA based processing module, limits its applications.

Fixed switching frequency in SMC using pulse width modulation (PWM) is reported in [36,37]. The authors have smoothened the control law within a boundary layer. In this boundary, the discontinuous function is replaced by a smooth linear function which is PWM implemented to achieve fixed switching frequency. The drawback of this technique is that it sacrifices the disturbance rejection performance in this boundary layer. The fixed switching frequency using PWM is also reported in [38–45]. However, in this work the ideal equivalent control signal, computed from the measured system states, is PWM modulated. The scheme is named as PWM-SMC. In [46,47], a bandwidth based parameter selection of the sliding surface is proposed for PWM-SMC. It is important to emphasize that in SMC, the robustness against unknown disturbances and parameter changes is achieved because of the discontinuous control term. However, in PWM-SMC, the ideal equivalent control does not evolve from a discontinuous function, rather it is computed from the measured states of the system, which may result in loss of

inherent properties of SMC like order reduction and disturbance rejection [30,48]. It is important to mention that the actual equivalent control of the system can be extracted from the discontinuous control and its first evidence is found in [49], where chattering reduction is achieved by tuning the gain of the discontinuous function according to the Filter Extracted Equivalent Control (FEEC). The scheme achieves reduction in chattering amplitudes, however, the switching frequency of the system is not fixed.

Hence, it may be concluded that the existing techniques for fixing frequency in SMC are either too complex or they compromise one or the other properties of SMC. Consequently, there is a need for a comprehensive, fixed frequency SMC design which is low cost, simple to implement using commercially available integrated circuits (ICs) and also retains the inherent properties of SMC. Moreover, in the present era of industrialization, robust fixed frequency controllers for power electronic converters are a necessary need as they find applications in heating furnaces, speed drives of induction motors, fluorescent lamps, grid connected energy storage systems and regulated power supplies of modern electronic equipment [50–52].

This paper addresses the issue by proposing a novel method for fixing the switching frequency in SMC. The actual equivalent control of the system is extracted from the discontinuous function by means of a low pass filter and is used to achieve fixed frequency SMC which to the best of authors' knowledge, has not been previously reported. The technique is implemented on a boost converter and the results are compared with existing PWM-SMC having a double integral type sliding surface. The experimental results demonstrate that the proposed technique achieves zero steady state error with improved dynamic response, and also exhibits better disturbance rejection properties as compared to PWM-SMC. The highlights of the contributions are:

- Achieving precise voltage regulation in presence of unknown load disturbances and un-modeled dynamics of the system.
- Extraction of the actual equivalent control from the discontinuous function under sliding mode operation.
- Improvement in both the dynamic response and the robustness of the closed loop system in comparison with double integral sliding mode control.

The rest of the article is organized as follows: The proposed technique is presented in Section 2. Fixed frequency PWM-SMC is discussed in Section 3. Experimental results and comparison of controllers is presented in Section 4, followed by the conclusion in Section 5.

2. Proposed Technique

The proposed technique is demonstrated on a boost type DC-DC converter. Conventionally, the two state variables are the inductor current I_L and the output voltage V_{out} . Using circuit analysis techniques in Figure 1, the mathematical model of the converter is derived as:

$$\dot{I}_{L} = -\tilde{u}\frac{1}{L}V_{out} + \frac{V_{in}}{L}$$

$$\dot{V}_{out} = \tilde{u}\frac{1}{C}I_{L} - \frac{V_{out}}{R_{L}C}$$
(1)

where V_{in} is the input voltage of the converter. The control input is denoted by u while $\tilde{u} = (1 - u)$. The inductance (μ H), capacitance (μ F) and load resistance (Ω) are denoted by L, C, R_L . The power electronic converters are designed to operate as a switch and can be either ON or OFF. Therefore, the input signal of the converter is discrete in nature and mathematically $u \in \{0, 1\}$. The value of control input with respect to the conduction state of the semiconductor switch is defined as:

$$u(t) = \begin{cases} 1, & \text{Conducting,} \\ 0, & \text{Open circuit.} \end{cases}$$
(2)



Figure 1. Block diagram of the proposed filter extracted equivalent control based sliding mode control (FEEC-SMC) for voltage regulation in boost converter.

The boost converters exhibit a non-minimum phase nature [53,54] which makes it more difficult to control as compared to other converters. The system becomes unstable if the feedback is designed based upon output voltage only [55]. However, the problem is solved by a cascade control scheme, where a two loop based structure is designed to control the inductor current and output voltage. This is an application of singular perturbation theory that can be applied where the motion rate of inner loop is much faster as compared to the outer loop [56,57]. The outer loop for voltage control is implemented using PI controller. Defining the error voltage e_v as:

$$e_v = V_{ref} - V_{out} \tag{3}$$

where V_{ref} and V_{out} are the reference and output voltages respectively. A PI controller for the outer loop is designed as:

$$i_{ref}^{*} = K_{p}e_{v} + K_{i} \int_{0}^{t} e_{v} dt$$
(4)

where K_p and K_i are the proportional and integral gains respectively while i_{ref}^* is the reference current for the inner current loop. If a feed forward reference current i_{fd} is also considered in (4), then the reference current I_{ref} is written as:

$$I_{ref} = i_{fd} + i_{ref}^* \tag{5}$$

The equilibrium points of the system are obtained by setting the time derivatives in (1) to zero. Hence we get,

$$V_{out} = V_d \tag{6}$$

$$I_{L_{eq}} = \frac{V_d^2}{R_L V_{in}} \tag{7}$$

where V_d and $I_{L_{eq}}$ are the desired capacitor voltage and the inductor current at the equilibrium.

The sliding surface σ for the inner current loop is designed on the basis of current error as:

$$\sigma = I_{ref} - I_L \tag{8}$$

The control law that enforces I_L to track I_{ref} is defined as:

$$u = \frac{1}{2}(1 + sign(\sigma)) \tag{9}$$

The stability of the system can be ensured by applying the convergence condition $\sigma \dot{\sigma} < 0$. By using the dynamics of the system from (1) we get:

$$\dot{\sigma} = \tilde{u} \frac{1}{L} V_{out} - \frac{V_{in}}{L} \tag{10}$$

Since $\tilde{u} = 1 - u$ and using $u = 1 + sign(\sigma)$, we get $\tilde{u} = -sign(\sigma)$. Hence (10) becomes:

$$\dot{\sigma} = -\frac{V_{out}}{L}sign(\sigma) - \frac{V_{in}}{L}$$
(11)

The condition $\sigma \dot{\sigma} < 0$ is satisfied if:

$$\|V_{out}\| > \|V_{in}\| \tag{12}$$

Stability condition in terms of the equivalent control u_{eq} can be written as:

$$0 < u_{eq} = 1 - \frac{V_{in}}{V_{out}} < 1$$
 (13)

Analysis of (12) shows that V_{out} shall be greater than V_{in} , in order to ensure the stable operation of the converter. It is important to note that when a physical converter is initially turned on, its output voltage V_{out} may be less than V_{in} . Practically this problem can be worked out by operating the system in an open loop manner and finally plugging in the controller when $V_{out} > V_{in}$. For PWM based control, the problem can be solved by using a voltage limiter circuit that keeps the control signal V_c less than the peak amplitude of the modulating ramp signal. This ensures the stable switching operation until $V_{out} > V_{in}$. This paper also uses a voltage limiter circuit which is easily realized by using a zener diode.

Ideally, SMC operates the switch at infinite frequency, however, due to physical constraints the system needs to operate at finite frequency. This causes the state to oscillate within a boundary layer of width Δ close to the sliding manifold $\sigma = 0$. These oscillations consist of two components. The low frequency component coincides with equivalent control of the system and can be obtained from the actual discontinuous control by means of a low pass filter [4]. The time constant of the low pass filter shall be selected such that the low frequency component passes without any distortion while the high frequency component is removed. In this research, a first order low pass filter used. The mathematical relationship between the discontinuous control input *u* and the output of the filter *y*(*t*) is obtained using Kirchhoff's voltage law as:

$$u = R_{fl}i(t) + y(t)$$

= $R_{fl}C_{fl}\frac{d}{dt}y(t) + y(t)$
= $\tau \frac{d}{dt}y(t) + y(t)$ (14)

where i(t) is the instantaneous current through the filter capacitor. It is shown in [4,58] that the output of this filter gives u_{eq} under the following ideal condition:

$$\lim_{\tau \to 0, f \to \infty} y(t) = u_{eq} \tag{15}$$

where *f* is the switching frequency. As *f* increases, the motion of the states becomes more near to ideal SMC and the width Δ in which the states oscillates, approaches zero. Hence as $f \to \infty$, $\Delta \to 0$. The necessary condition to filter out the high frequency component and extract u_{eq} is that the switching frequency must be much higher than $1/\tau$ or equivalently:

$$\frac{1}{f} << \tau \tag{16}$$

It is important to note that the FEEC contains information regarding the parameter changes and disturbances acting upon the system. The equivalent control under SMC coincides with the duty ratio of PWM converters [59,60], establishing the relationship $u_{eq} = d$ which provides the basic theoretical background for development of PWM based SM-controllers. Once the u_{eq} is extracted, the control signal V_c for PWM implementation is derived as:

$$u_{eq} = d = \frac{V_c}{V_{ramp}} \tag{17}$$

where V_{ramp} is the peak voltage of modulating ramp signal. The switching sequence provided by PWM according to (17) results in a fixed frequency operation of the SM-controller.

3. PWM-SMC with Double Integral Type Sliding Surface

For bench marking purpose, PWM-SMC is implemented and for the sake of completeness and better understanding, its design is also presented. In order to ensure best performance, a double integral type sliding surface is chosen [38,45]. The sliding manifold σ is defined as:

$$\sigma = c_1 \int \int e_i(t)dt \, dt + c_2 \int e_i(t)dt + c_3 e_i(t) \tag{18}$$

where $e_i(t) = (I_{ref} - I_L)$. Mathematically, the ideal equivalent control signal $u_{eq_{(ideal)}}$ for PWM-SMC is derived by putting $\dot{\sigma} = 0$. Thus we get:

$$\dot{\sigma} = c_3 \dot{e}_i(t) + c_2 e_i(t) + c_1 \int e_i(t) dt = 0$$
(19)

Using (1) and (19) we get:

$$\tilde{u}_{eq_{(ideal)}} = \frac{V_{in}}{V_{out}} - L\frac{c_2}{c_3}\frac{e_i(t)}{V_{out}} - L\frac{c_1}{c_3}\frac{\int e_i(t)dt}{V_{out}}$$

By using definition $\tilde{u} = (1 - u)$ we get:

$$u_{eq_{(ideal)}} = (1 - \frac{V_{in}}{V_{out}}) + L\frac{c_2}{c_3}\frac{(I_{ref} - I_L)}{V_{out}} + L\frac{c_1}{c_3}\frac{\int (I_{ref} - I_L)dt}{V_{out}}$$
(20)

Choosing $V_{ramp} = V_{out}$ we derive V_c as:

$$V_{c} = (V_{out} - V_{in}) + L \frac{c_{2}}{c_{3}} (I_{ref} - I_{L}) + L \frac{c_{1}}{c_{3}} \int (I_{ref} - I_{L}) dt$$
(21)

while

$$V_{ramp} = V_{out}$$

It is important to note that the magnitude of the ramp signal needs to be adaptively changed with respect to V_{out} . This makes this technique robust to input voltage variations as compared to conventional PID controllers [40]. However, this adaptive nature of V_{ramp} adds complexity to the design and causes over modulation of PWM signal during start up. Additional circuitry is required to prevent this over modulation. A salient feature of the proposed FEEC-SMC is that it achieves robustness against input voltage variations without requiring adaptive control of the ramp signal.

Stability of Inner Loop

Sliding mode can only exist on manifold $\sigma = 0$ if the following constraint is satisfied.

$$\lim_{\sigma \to 0} \sigma \dot{\sigma} < 0 \tag{22}$$

Using (1) and (18) we get:

$$\dot{\sigma} = c_1 \int e_i(t)dt + c_2 e_i(t) + c_3 \left(\frac{V_{out}}{L}\tilde{u} - \frac{V_{in}}{L}\right)$$
(23)

The control law for the system is defined as:

$$u = \frac{1}{2} + \frac{1}{2}sign(\sigma) \tag{24}$$

when $\sigma \to 0^+$ then (22) implies that $\dot{\sigma} < 0$. The control law turns u = 1. This gives the following condition:

$$\frac{c_3}{L}V_{in} > c_1 \|g_1(t)\| + c_2 \|g_2(t)\|$$
(25)

where $g_1(t) = \int e_i(t)dt$ and $g_2(t) = e_i(t)$. The output of both the op-amps calculating $g_1(t)$ and $g_2(t)$ are limited to ± 5 and ± 8 , thus mathematically:

$$\|g_1(t)\| < 5$$

 $\|g_2(t)\| < 8$ (26)

Now by appropriate choice of c_1 , c_2 and c_3 the inequality (25) is satisfied.

When $\sigma \to 0^-$ then the control law sets u = 0 and stability is guaranteed if $\dot{\sigma} > 0$. By using Equation (23) we get the following condition:

$$\frac{c_3}{L}(V_{out} - V_{in}) > c_1 \|g_1(t)\| + c_2 \|g_2(t)\|$$
(27)

Again by appropriate choice of design constants, (27) is satisfied. Finally, for the sake of protection the maximum duty cycle of the PWM output is limited to 95%. This is accomplished by using a shunt voltage regulator TL431 at the output of the op-amp computing V_c . TL431 cannot regulate voltages lower than 2.5 V. Hence V_c and V_{ramp} both are amplified by a gain of 2 and TL431 is adjusted to clip voltages above 4.8 V. This gain of 2 has no effect on the duty ratio because the same constant is multiplied in the numerator and denominator of the fraction. Thus the control law becomes:

$$d = \frac{2 \times V_c}{2 \times V_{ramp}} \tag{28}$$

4. Experimental Results and Discussion

The performance of the above-mentioned controllers is compared on the following basis of steady state error, transient response and robustness to load variations.

4.1. Experimental Setup

The parameters of the boost converter are shown in Table 1 while the complete schematic of the controller is shown in Figure 2. The electronic switch consists of a power MOSFET IRF540 with 0.06 Ω channel resistance with maximum current capability of 20 A. The converter is operated with switching frequency of 32 kHz. It is important to note that increasing the switching frequency also increases the switching losses whereas lower switching frequency increases the chattering amplitude. Thus there is a compromise between the two factors. The efficiency of the converter also drops with increase in the switching frequency due to increase in switching losses. The efficiency of the boost converter is measured to be 93%.



Figure 2. Complete circuit diagram of the proposed FEEC-SMC.

path of the inductor current. By Ohm's law inductor current $I_L = V_{me}/R_{me} = 2.1V_{me}$. Hence the voltage sensed at R_{me} is amplified by a gain of 2.1 to give exact value of the inductor current. All the waveforms presented in the paper are obtained using 70 MHz Rigol oscilloscope having sampling rate of 1 G samp/s. The control circuitry is powered with 0.1 V accurate power supply.

4.2. Steady State Error

Figure 3 presents the response of the boost converter with PWM-SMC. Figure 4 shows the response of the proposed FEEC-SMC. Both the controllers have zero steady state error and their output voltage converges to the desired 24 V as shown in Figures 3a and 4a. It is worth mentioning that FEEC-SMC achieves zero steady state error without having any integral term in the sliding surface. This factor simplifies the design and makes the proposed technique cost effective as compared to the PWM-SMC design.



Figure 3. Experimental waveforms of the closed loop system with PWM-SMC. (a) Step response of the closed loop system. (b) Output voltage when load is shifted from 82 Ω to 29.88 Ω (c) Inductor current and gating signal at output of LM311 during steady state operation. (d) Chattering in the output voltage.

4.3. Transient Response

The transient response of the system is obtained by switching the input voltage at 0.4 Hz using Rigol function generator. The output of the function generator is applied to the base of an NPN transistor C1383 which drives a PNP power transistor TIP147 so that V_{in} is connected and disconnected accordingly. The experimental results show that the rise time (t_r) for the PWM-SMC is 40 ms and its settling time (t_s) is 75 ms. The t_r and t_s for the closed loop system obtained using FEEC-SMC are 32 ms and 56 ms respectively. This indicates an improvement of 20% in t_r and 25.3% in t_s which is a direct consequence of the fact that the discontinuous function is directly implemented and no indirect approach is adopted to compute equivalent control.

4.4. Robustness to Load Variations

In order to establish the robustness of the proposed FEEC-SMC, experiments are conducted by abruptly increasing the load resistance. A switching network is used to increase the load by connecting a resistor of 47 Ω in addition to the existing 82 Ω load. Figure 3b shows that PWM-SMC exhibits an undershoot of 2.8 V while FEEC-SMC shows 42.86% improvement by reducing the voltage dip to 1.6 V as indicated in Figure 4b. PWM-SMC recovers in 250 η s while FEEC-SMC recovers in 85 η s which shows an improvement of 66% in recovery time. Experimental setup to evaluate the performance of the controllers is shown in Figure 5.



Figure 4. Experimental waveforms of the closed loop system with FEEC-SMC. (a) Step response of the closed loop system. (b) Output voltage when load is shifted from 82 Ω to 29.88 Ω indicating robustness of the closed loop system. (c) Inductor current and gating signal at output of LM311 during steady state operation. (d) Chattering in the output voltage.

5. Conclusions

This research highlights the importance of the discontinuous function as the primary source of robustness and disturbance rejection in the domain of variable structure systems. However, it has a shortcoming in that its presence causes frequency drifts. This research reports a novel and intuitive method, namely FEEC-SMC, to achieve fixed frequency SMC by low pass filtration of the discontinuous function. An experimental comparison with PWM-SMC reveals that FEEC-SMC not only improves the dynamic response but also increases the robustness of the closed loop system against load variations and parameter drifts. Moreover, it achieves zero steady state error without any integral term in the sliding surface which gives it an advantage over PWM-SMC which requires a double integral type sliding surface to achieve zero steady state error. In contrast with PWM-SMC, the FEEC-SMC achieves robustness against input voltage variations without requiring complex adaptive control of the ramp signal. Finally, due to the direct implementation of a discontinuous function, FEEC-SMC retains the properties like order reduction and parameter invariance, which may be lost if the ideal equivalent control is constructed without involving a discontinuous function.

Future work may extend our results to other types of converters including Buck and C'uk converters and may also explore how to improve the robustness of micro-grids along with achieving precise voltage regulation.



Figure 5. Experimental setup to evaluate the performance of the controllers.

Description	Symbol	Value
Input voltage	Vin	12 V
Desired output voltage	V_d	24 V
Capacitance	С	1000 µF
Capacitor ESR	r _C	21 mΩ
Inductance of coil	L	100 µH
Resistance of coil	r_L	$0.18 \ \Omega$
Switching frequency	fsw	32 kHz
Load resistance	R_L	15–100 Ω

Table 1.	Parameters	of Buck	Converter.
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