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Control Design, Stability Analysis and Experimental Validation of New Application of an Interleaved Converter Operating as a Power Interface in Hybrid Microgrids

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Abstract: This paper presents a new and specific use of a bidirectional interleaved converter to perform a power interface in hybrid microgrids. The converter is responsible for regulating the power flow between the direct-current (DC) microgrid and the rest of the hybrid microgrid by controlling the DC microgrid voltage. The authors present a detailed modeling of the mentioned system in order to develop the system control design and a stability analysis. In addition, the authors propose a new control design strategy aiming at improving the voltage control disturbance rejection characteristic, while maintaining a good dynamic behavior regarding the reference tracking functionality. In this hybrid microgrid topology, a back-to-back converter connects the main grid to the AC microgrid. The main objective of this converter is to provide a high-power-quality voltage to critical and sensitive loads connected to the microgrid. The interleaved converter adjusts the DC microgrid voltage according to the operational voltage of the back-to-back converter DC link. In the DC microgrid case, the variation of load and generation connection could lead to serious voltage sag and oscillations that could be harmful to the sensitive loads. The voltage controller must be capable of rejecting these disturbances in order to maintain a high-power-quality voltage. Furthermore, experimental results are provided in order to validate this specific application of the interleaved converter and the presented control design strategy.

Keywords: interleaved converter; hybrid microgrids; power flow interface; linear control theory

1. Introduction

Over the years, many different studies related to microgrids have been developed due to the high increase of the distributed generation penetration in the electrical systems [1–6], which is a consequence of the advances that have been occurring with the solar and wind generation systems and with power electronics technology. When designed in the alternating-current (AC) form, the microgrid might present some power quality issues related to harmonic currents and voltages, as well as related to frequency regulation [4–6].

DC microgrids are widely used in telecommunication systems as well as in electric vehicles [2] and have been proposed in order to solve some of the mentioned problems related to the AC

microgrids [5–8], besides allowing for a better integration of DC systems and devices such as the photovoltaic generation, energy storage systems and electronic loads [5–7]. In this context, many works have been published proposing the use of hybrid microgrids [2,3,9–13] aiming at taking advantage of the benefits of both AC and DC microgrids.

A method for implementing such a system was proposed in [10] in which the DC link of a back-to-back converter is used to form the DC microgrid. The mentioned back-to-back converter acts as a power interface between the main grid and the AC microgrid. This topology may require the use of an additional DC–DC converter in order to perform a power interface between the back-to-back converter DC link and the DC microgrid while maintaining its voltage regulated in the desired level, which may be different from the back-to-back converter DC-link voltage.

The N-phase bidirectional interleaved converter is a static converter with high reliability since it can keep operating even if one of its phases is damaged or suffers a fault [14,15]. Another important characteristic of this topology is the possibility of ripple reduction in the output current, obtained through the proper modulation strategy [16–19]. This fact leads to a reduction of the output DC capacitor, resulting in a lighter and more compact solution.

The interleaved converter has been used in many different applications that require a regulated power source with high reliability and low weight. Most of these applications are related to energy storage systems and electric vehicles [20–31].

Most of the applications found in the literature of interleaved converters in microgrids are related to the connection of DC loads, energy storage systems or generation sources to a microgrid [32–36]. To the authors' knowledge, no other work has reported the use of an interleaved converter as a power interface between microgrids.

This paper proposes the use of a three-phase interleaved converter in order to form the DC microgrid voltage profile while controlling the power flow between the DC microgrid and the rest of the hybrid microgrid. Since the DC microgrid voltage level is supposed to remain constant, the voltage control must be designed in such a way to be more effective in rejecting load disturbances rather than tracking the provided reference. In other words, the voltage reference will remain constant, but the control must be very effective in handling the load and generation variations that might occur in the DC microgrid. Those variations could produce severe voltage sags and fluctuations that could be serious to sensitive loads present in the DC microgrid. Thus, a new method for tuning the voltage controller parameters, in order to obtain a fast disturbance rejection characteristic, is proposed aiming at maintaining a high-power quality microgrid voltage.

Some of the ideas expressed in this paper were first introduced by the authors in [37]. However, in the present paper, a more detailed explanation on the system modeling and a deeper stability analysis are developed proving the enhancement on the converter disturbance rejection capability. In addition, this paper presents experimental results that validate the proposed interleaved converter application.

2. System Topology

The analysis carried out in this paper is based on the application of an interleaved converter as a power interface in a hybrid microgrid. In other words, taking into account the hybrid microgrid depicted in Figure 1, the interleaved converter operates regulating the DC-microgrid voltage level according to a given back-to-back converter operational DC-link voltage. The back-to-back converter mentioned connects the main grid to an AC microgrid. This hybrid microgrid topology could be suited for applications in remote areas with a low-power-quality main-grid voltage, in which the back-to-back converter would be responsible for generating a high-power-quality AC microgrid voltage, despite the main-grid-voltage power quality, in order to protect local sensitive loads. The interleaved converter acts as the interface with the local DC microgrid that operates with a different voltage level in relation to the DC link of the back-to-back converter. In addition, the interleaved converter control can improve the microgrid voltage profile by rejecting load disturbances as will be further explained later in this paper.

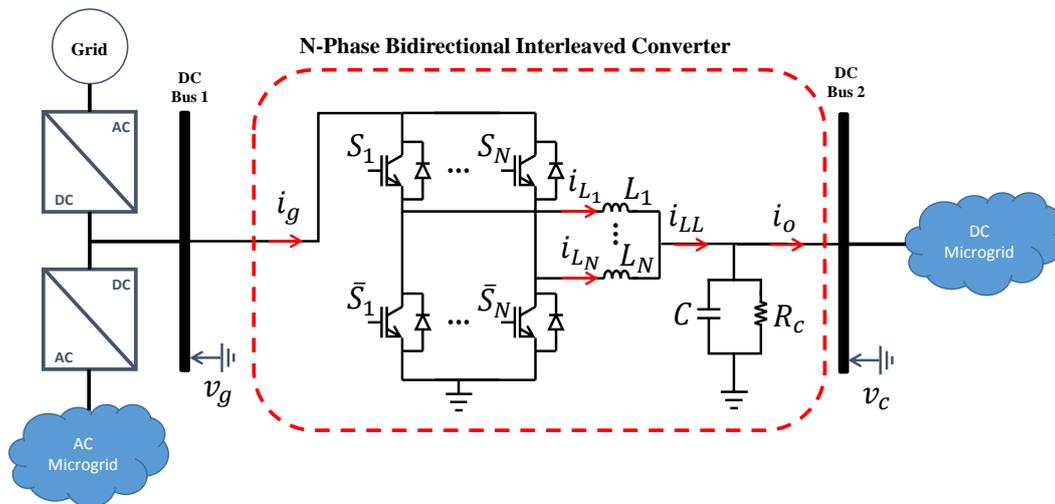


Figure 1. Hybrid microgrid topology that uses the interleaved converter as a power interface.

3. Interleaved Converter Modeling

The N-phase bidirectional interleaved converter, described in the previous section, can be modeled as the equivalent circuit shown in Figure 2. In this figure, each of the interleaved converter phases is represented by its inductor parameters (L_1, L_2, \dots, L_N and R_1, R_2, \dots, R_N) and by controlled voltage sources with values equal to the product of the duty cycles (d_1, d_2, \dots, d_N) by the input voltage (v_g), which is the main back-to-back converter DC-link voltage. Finally, an equivalent capacitance (C), which represents the total output DC-link capacitance, along with an equivalent resistance (R_c), which represents the balancing resistors, compose the interleaved converter's output-DC-link model, as shown in Figure 2. The DC-microgrid load and generation are represented by a current source with the value equal to i_{dc} .

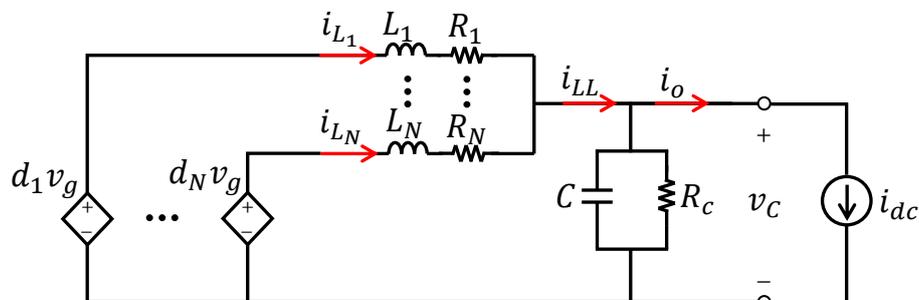


Figure 2. N-phase interleaved converter equivalent circuit.

Using the interleaved converter equivalent circuit (neglecting the balancing resistor (R_c)), the average large signal model is obtained through the Kirchoff's laws, as shown in (1) and (2), in which N is the interleaved converter number of phases and $k = 1, \dots, N$ represents a given phase k :

$$-d_k v_g + L_k \frac{di_{Lk}}{dt} + R_k i_{Lk} + v_c = 0, \quad (1)$$

$$\sum_{k=1}^N i_{Lk} - i_o - C \frac{dv_c}{dt} = 0. \quad (2)$$

Equations (1) and (2) can be represented in the Laplace- s domain as follows:

$$-d_k(s) V_g + (L_k s + R_k) I_{Lk}(s) + V_c(s) = 0, \quad (3)$$

$$\sum_{k=1}^N I_{L_k}(s) - I_o(s) - CsV_c(s) = 0. \quad (4)$$

The phase inductors must be as similar as possible in order to avoid an uneven current flow through the phases. This fact leads to the following approximation: $L_1 = L_2 = \dots = L_N = L$ and $R_1 = R_2 = \dots = R_N = R$. Applying the mentioned approximation into (3) and summing all the N equations (corresponding to $k = 1, \dots, N$) leads to:

$$- \sum_{k=1}^N d_k(s) V_g + (Ls + R) \sum_{k=1}^N I_{L_k}(s) + N V_c(s) = 0. \quad (5)$$

Considering that ideally V_g is constant, the topology results in a MIMO (multiple input multiple output) system with the state variables as outputs ($I_{L1}, I_{L2}, \dots, I_{LN}$ and V_c) and the phase duty cycles (d_1, d_2, \dots, d_N) along with the load current (I_o) as inputs. Then, if it is desirable to analyze the effect of a single input (for example a given duty cycle d_n of a given phase n) on the system dynamics, all the other inputs must be set to zero. In other words, $d_k(s) = 0, \forall k \neq n$ and $I_o(s) = 0$. Thus, Equation (5) can be rewritten as:

$$- d_n(s) V_g + (Ls + R) \sum_{k=1}^N I_{L_k}(s) + N V_c(s) = 0. \quad (6)$$

Moreover, Equation (4) can be rewritten as:

$$\sum_{k=1}^N I_{L_k}(s) = CsV_c(s). \quad (7)$$

By substituting (7) into (6), the following equation is obtained:

$$- d_n(s) V_g + (CLs^2 + CRs + N)V_c(s) = 0. \quad (8)$$

Using (3) for the given phase n leads to:

$$V_c(s) = d_n(s)V_g - (Ls + R)I_{L_n}(s). \quad (9)$$

The substitution of (9) into (8) leads to the following transfer function, representing the relation between duty cycle and phase current:

$$\frac{I_{L_n}(s)}{d_n(s)} = \frac{V_g}{(Ls + R)} \frac{(CLs^2 + CRs + (N - 1))}{(CLs^2 + CRs + N)}. \quad (10)$$

Finally, since $L_1 = L_2 = \dots = L_N = L$, (4) can be approximated by the following equation:

$$NI_{L_n}(s) - I_o(s) - CsV_c(s) = 0. \quad (11)$$

If the load current disturbance (I_o) is neglected, the following transfer function can be obtained:

$$\frac{V_c(s)}{I_{L_n}(s)} = \frac{N}{Cs}. \quad (12)$$

4. Control Design

The control strategy used in this paper is based on two control loops as shown in Figure 3. An outer voltage loop that is responsible for the output DC-bus voltage (DC Bus 2) regulation and an inner current loop that is responsible for the phase currents' regulation. The current control is

accomplished using different controllers for each phase current with phase-shifted modulating carriers, which leads to balanced and stable currents.

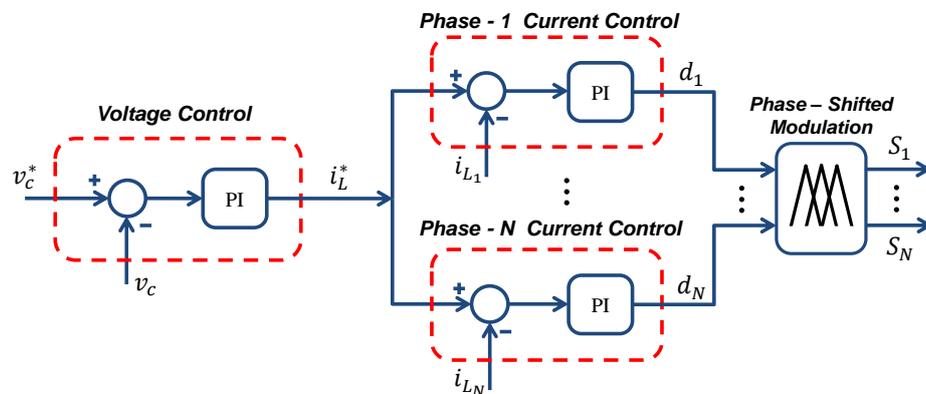


Figure 3. Cascade-control-strategy topology.

4.1. Conventional Control Design

In order to design the current controllers and voltage controller parameters, the transfer functions described in (10) and (12) are used as shown in the block diagram depicted in Figure 4.

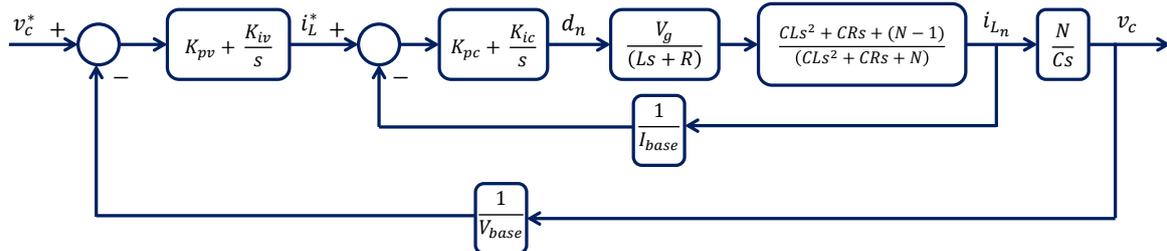


Figure 4. Linear closed-loop system.

The proximity of the roots of $CLs^2 + CRs + (N - 1)$ and $CLs^2 + CRs + N$ can lead to a simplification of the transfer function (10). In other words, these poles and zeros are close to each other in such a way that their effects in the system dynamic behavior cancel each other out. Thus, if these poles and zeros are neglected, (10) can be approximated by the following transfer function:

$$\frac{I_{L_n}(s)}{d_n(s)} = \frac{V_g}{(Ls + R)}. \tag{13}$$

Therefore, the current loop of the system shown in Figure 4 can be represented by the block diagram shown in Figure 5.

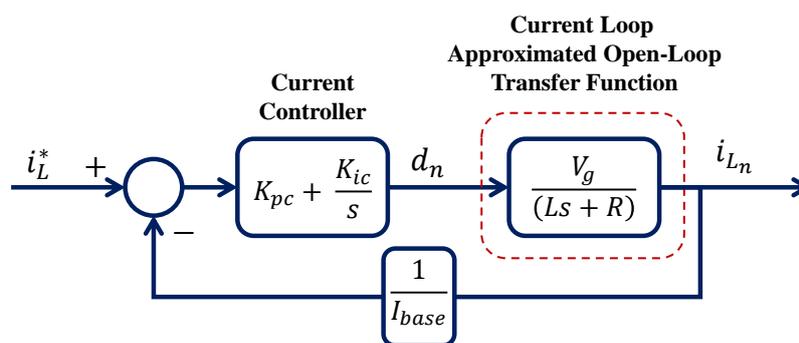


Figure 5. Current loop using the approximated open-loop transfer function.

The methodology proposed by Gao in [38], which is a general control design technique, suggests the tuning of the controller parameters in such a way that the system closed-loop transfer function operates with the desired bandwidth (ω_c). In the present case, the current controller parameters are designed as follows:

$$k_{pc} = \frac{\omega_c L I_{base}}{V_g}, \quad (14)$$

and

$$k_{ic} = \frac{\omega_c R I_{base}}{V_g}. \quad (15)$$

In other words, if the controller parameters are designed according to (14) and (15) and applied to the model depicted in Figure 5, the resulting current control closed-loop transfer function will be:

$$\frac{I_{Ln}}{I_L^*} = \frac{\omega_c}{s + \omega_c}. \quad (16)$$

This is the transfer function of a low-pass filter with the desired bandwidth (ω_c). Thus, the outer control loop (voltage control) will be described by the block diagram depicted in Figure 6.

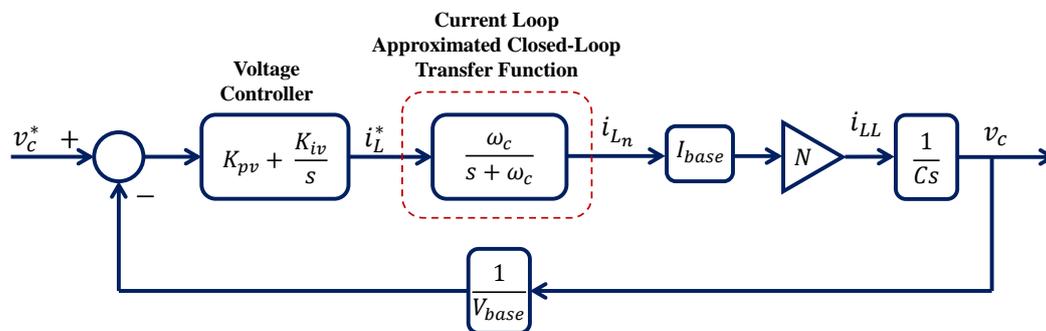


Figure 6. Voltage loop using the current loop approximated closed-loop transfer function.

In order to analyze if the approximation made (to neglect the poles $CLs^2 + CRs + N$ and zeros $CLs^2 + CRs + (N - 1)$) is acceptable, a comparison was made between the designed bandwidth ω_c and the actual bandwidth obtained considering the complete transfer function without the mentioned approximation. This comparison is shown in Figure 7, in which the ratio $\frac{\omega_{-3dB}}{\omega_c}$ is plotted as a function of the number of phases N .

In Figure 7, one can notice that, for every value of N , the obtained bandwidth is approximately 4% higher than the designed bandwidth (ω_c). This small difference is due to the fact that the mentioned poles and zeros were disregarded when designing the current controller's parameters using Gao's method. The authors consider that this small bandwidth difference is acceptable and will not have much influence on the design accuracy.

The control theory literature widely reports that, in a cascade control topology, inner control loops must be considerably faster than outer control loops. In the present case, it means that the voltage loop bandwidth (ω_v) must be considerably smaller than the current control bandwidth (ω_c). In this context, the design criteria $\omega_v = \frac{\omega_c}{10}$ is used in this paper. Thus, from the voltage loop controller design point of view, the current loop dynamics can be neglected (the closed loop transfer function is approximated by a unitary gain) as will be shown later.

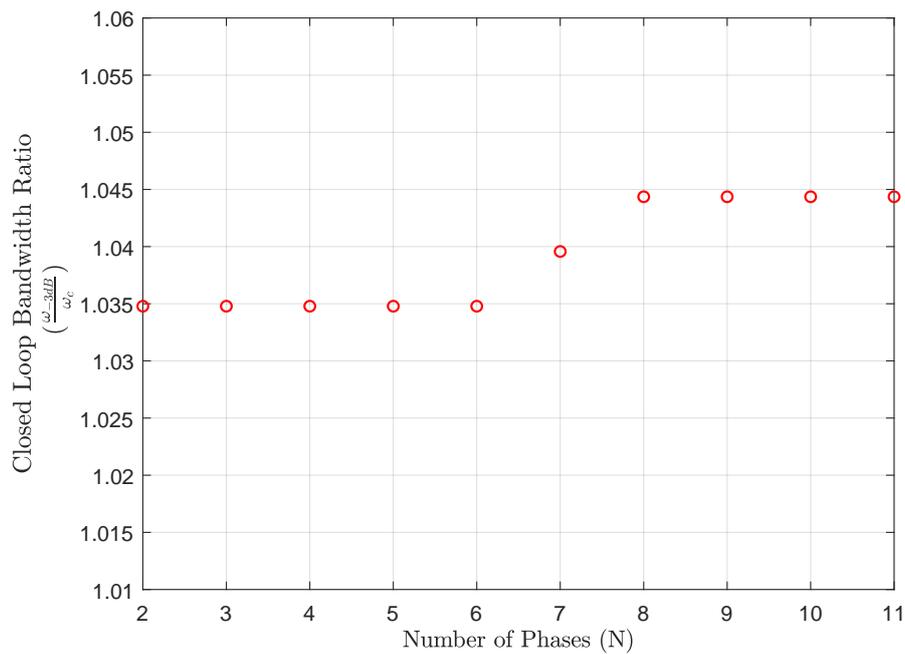


Figure 7. Difference between the designed bandwidth (ω_c) and the actual obtained bandwidth (for the complete transfer function taking into account the poles and zeros that were neglected) for different values of N.

In order to design the voltage controller parameters, the output DC-link balancing resistor (R_c) must be taken into account, so that it is possible to apply the method presented in [38]. Thus, (4) can be written as:

$$\sum_{k=1}^N I_{L_k}(s) - I_o(s) - CsV_c(s) - \frac{V_c}{R_c} = 0. \quad (17)$$

The transfer function (12) becomes:

$$\frac{V_c(s)}{I_{L_n}(s)} = \frac{N}{Cs + \frac{1}{R_c}}. \quad (18)$$

Through the block diagram shown in Figure 8 and once again using the method described in [38], the voltage controller parameters can be defined as shown in (19) and (20):

$$k_{pv} = \omega_v \frac{C}{N} \frac{V_{base}}{I_{base}}, \quad (19)$$

and

$$k_{iv} = \omega_v \frac{1}{R_c N} \frac{V_{base}}{I_{base}}. \quad (20)$$

Using these controller parameters, the voltage loop will have the dynamic behavior related to the desired bandwidth (ω_v); in other words, the closed-loop transfer function will be: $\frac{V_c}{V_c^*} = \frac{\omega_v}{s + \omega_v}$.

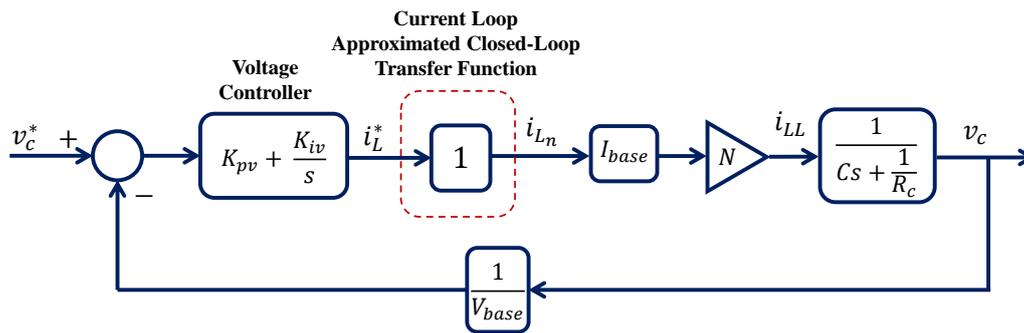


Figure 8. Approximated voltage control loop with the current control closed-loop transfer function as a unitary gain.

4.2. Proposed Control Design Method

According to the methodology presented in the previous subsection, the voltage control will have the desired dynamic behavior related to the bandwidth ω_v . The mentioned dynamics are related to the voltage control reference tracking ability.

However, in the present application, one should notice that a more important functionality of the interleaved converter voltage control is that of rejecting load disturbances. In other words, the voltage control reference (output DC-link voltage reference) is constant in this application. It means that, once the output DC-link voltage reaches its reference value, the voltage controller will not need to apply much control effort in order to track the reference. It is very important that it can reject disturbances related to power variations demanded by the DC microgrid though.

Thus, a transfer function with the load current (I_o) as an input and with the output DC-link voltage (V_c) as an output is required. This transfer function can be obtained through (4), taking into account the load current (I_o), leading to the block diagram shown in Figure 9.

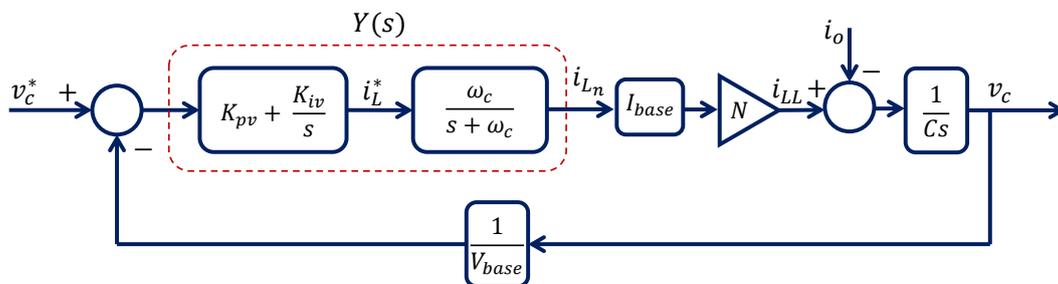


Figure 9. Block diagram used to extract the system transfer function in order to analyze the controller disturbance rejection functionality.

In Figure 9, $Y(s)$ is described as follows:

$$Y(s) = \left(k_{pv} + \frac{k_{iv}}{s} \right) \frac{\omega_c}{s + \omega_c}. \tag{21}$$

Setting the voltage reference to zero ($v_c^* = 0$) in Figure 9 and using (21), the closed-loop transfer function describing the effect of the load disturbance on the output voltage is obtained:

$$\frac{V_c(s)}{I_o(s)} = \frac{\frac{1}{Cs}}{1 + \frac{NI_{base}}{V_{base}} \frac{Y(s)}{Cs}}. \tag{22}$$

Equation (22) can be rewritten as:

$$\frac{V_c(s)}{I_o(s)} = \frac{\frac{s(s+\omega_c)}{C}}{s^3 + \omega_c s^2 + \left(\frac{NI_{base}\omega_c k_{pv}}{V_{base}C}\right)s + \frac{NI_{base}\omega_c k_{iv}}{V_{base}C}}. \quad (23)$$

In this paper, the authors propose the following new method for tuning the voltage controller integral gain:

$$k_{iv} = \frac{\gamma\omega_v C}{N} \frac{V_{base}}{I_{base}}. \quad (24)$$

By substituting (19) and (24) into (23), the following characteristic equation is obtained:

$$s^3 + \omega_c s^2 + \omega_v \omega_c s + \gamma \omega_v \omega_c = 0. \quad (25)$$

Through (25), one can design the voltage control behavior, regarding the disturbance rejection functionality, as a function of the parameters ω_v , ω_c and γ , independently of the plant parameters C and N , and of the electrical quantities' base values. In other words, two different converters with different electrical parameters could operate with the same reference tracking and disturbance rejection dynamic behavior if equal values of the parameters k_{pc} , k_{ic} , k_{pv} , k_{iv} and γ are used.

An interesting fact is that it is possible to tune the parameter γ in order to obtain a robust dynamic response, regarding disturbance rejection, while only slightly changing the control dynamics regarding the reference tracking functionality, as will be shown later in this paper. In other words, Gao's tuning method allows one to design the controllers' parameters in order to obtain the proper reference tracking dynamics. Then, the proposed method allows one to reset the controller's integral parameter (k_{iv}), maintaining a dynamic behavior similar to the original one, regarding the reference tracking functionality, while considerably improving the system's disturbance rejection characteristic, which is essential for this application.

5. Stability Analysis

As previously mentioned, after using Gao's method to tune the parameters ω_c and ω_v and obtain the desired reference tracking dynamics, one can plot a root locus of the system (using (25)) as a function of the parameter γ in order to also obtain the desired dynamic behavior regarding the disturbance rejection functionality. The mentioned root locus is shown in Figure 10.

By analyzing Figure 10, one can notice that, as the value of γ increases, there is a dominant pole that moves away from the system origin towards the left side of the root locus and that eventually encounters the other pole as they become a pair of complex conjugate poles. In other words, it means that the system dynamics, regarding disturbance rejection, becomes faster as the value of γ increases, and eventually starts to oscillate. This analysis provides a good direction of how to correctly tune the parameter γ in order to obtain the desired behavior.

However, this analysis is not enough to describe the entire system's dynamic behavior. As previously mentioned, this is a MIMO system in which the disturbance current (I_o) and the duty cycles (d_n) are inputs and the output DC-link voltage (V_c) and output current (I_{LL}) are outputs. In other words, the load disturbance (I_o) directly affects the output DC-link voltage (V_c), but also indirectly affects the output DC-link voltage (V_c) through the output current (I_{LL}), which affects the duty cycle (d) disturbing the output DC-link voltage (V_c). In order to completely describe the system's dynamic behavior, the block diagram depicted in Figure 11 must be considered.

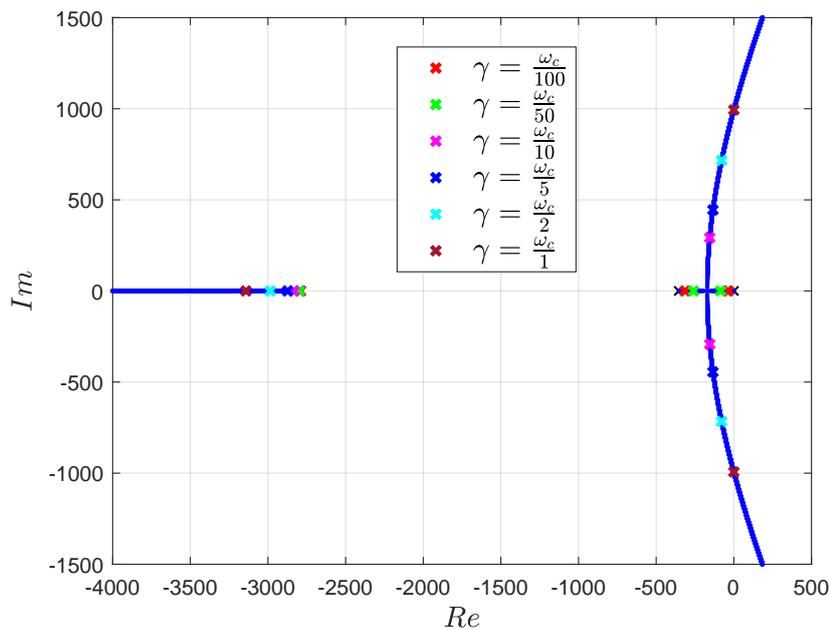


Figure 10. Root locus of Equation (25) for different values of γ with $\omega_v = 100\pi$ rad/s and $\omega_c = 1000\pi$ rad/s.

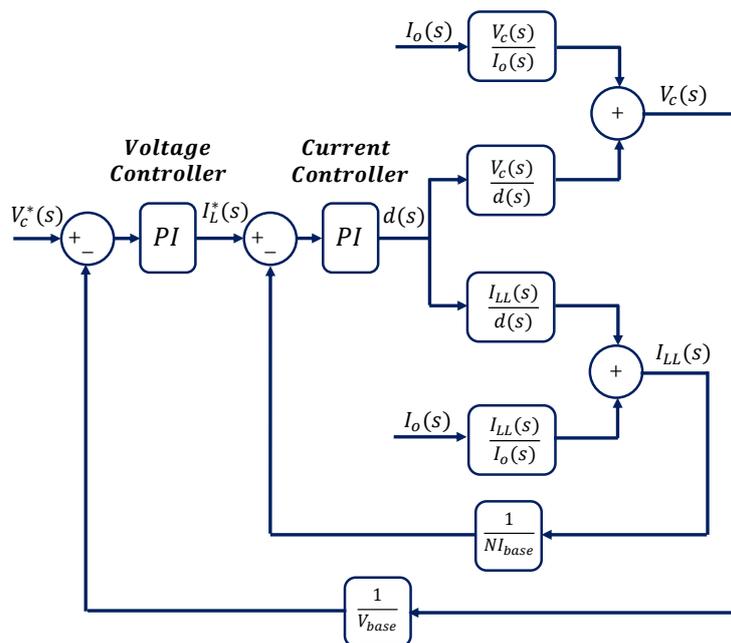


Figure 11. Block diagram representing the MIMO system, taking into account the current and voltage controllers' dynamics.

In order to obtain each of the transfer functions represented in Figure 11, a mean value model of (3) and (4) must be considered as follows:

$$-d(s)V_g + \frac{(Ls + R)}{N}I_{LL}(s) + V_c(s) = 0, \tag{26}$$

$$I_{LL}(s) - I_o(s) - CsV_c(s) = 0. \tag{27}$$

By setting $I_o(s) = 0$, the following transfer functions can be obtained through (26) and (27):

$$\left. \frac{V_c(s)}{d(s)} \right|_{I_o(s)=0} = \frac{NV_g}{LCs^2 + RCs + N'} \quad (28)$$

$$\left. \frac{I_{LL}(s)}{d(s)} \right|_{I_o(s)=0} = \frac{NCV_g s}{LCs^2 + RCs + N}. \quad (29)$$

By setting $d(s) = 0$, the following transfer functions can be obtained through (26) and (27):

$$\left. \frac{V_c(s)}{I_o(s)} \right|_{d(s)=0} = \frac{-(Ls + R)}{LCs^2 + RCs + N'} \quad (30)$$

$$\left. \frac{I_{LL}(s)}{I_o(s)} \right|_{d(s)=0} = \frac{N}{LCs^2 + RCs + N}. \quad (31)$$

By setting $V_c^* = 0$ in Figure 11 and using (28), (29), (30) and (31), it is possible to obtain the desired transfer function $\left. \frac{V_c(s)}{I_o(s)} \right|_{V_c^*(s)=0}$.

However, this is a really complex transfer function to obtain analytically; therefore, the authors implemented the block diagram shown in Figure 11 on Simulink (MATLAB R2018b) and used the linear analysis tools to obtain the root locus, Bode and Nyquist plots depicted in Figure 12.

The curves represented in Figure 12a–e are related to the transfer function $\left. \frac{V_c(s)}{I_o(s)} \right|_{V_c^*(s)=0}$. The curves represented in Figure 12f,g are related to the transfer function $\left. \frac{I_{LL}(s)}{I_o(s)} \right|_{V_c^*(s)=0}$. The curves represented in Figure 12h–j are related to the transfer function $\left. \frac{V_c(s)}{V_c^*(s)} \right|_{I_o(s)=0}$.

In Figure 12a,b, one can analyze the disturbance rejection Bode plot as a function of ω_c using $\gamma = \frac{\omega_c}{10}$. It is clear that the faster the current control is, the better the disturbance rejection capability becomes (higher negative gain, meaning that, for the same value of load disturbance (I_o), less impact is caused to the output voltage (V_c)). For the following analysis, the authors chose $\omega_c = 1000\pi = 2\pi \frac{F_s}{10}$ that is a safe value in relation to the switching frequency $F_s = 5$ kHz. Thus, the voltage control bandwidth is chosen as follows: $\omega_v = \frac{\omega_c}{10} = 100\pi$.

By analyzing the dominant poles as a function of the parameter γ of the root locus represented in Figure 12c, one can notice that, in fact, as γ increases, the system response becomes faster, but it also becomes more oscillatory.

In Figure 12d,e, one can analyze the disturbance rejection Bode plot as a function of γ . It becomes clear that, as the value of the parameter γ increases, the system disturbance rejection capability increases as well. In other words, the system gain reduces, meaning smaller variation in $V_c(s)$ for a given input value of $I_o(s)$, and the Bode curves' cutoff frequencies become higher, meaning faster response, resulting in a more robust system. For high values of γ , resonance peaks appear reflecting the complex poles shown in Figure 12c.

In Figure 12f,g, one can observe the effect of the load disturbance ($I_o(s)$) on the output current ($I_{LL}(s)$) for different values of γ . It is clear that, as the value of γ increases, the output current becomes more oscillatory, as will be shown later in the experimental results.

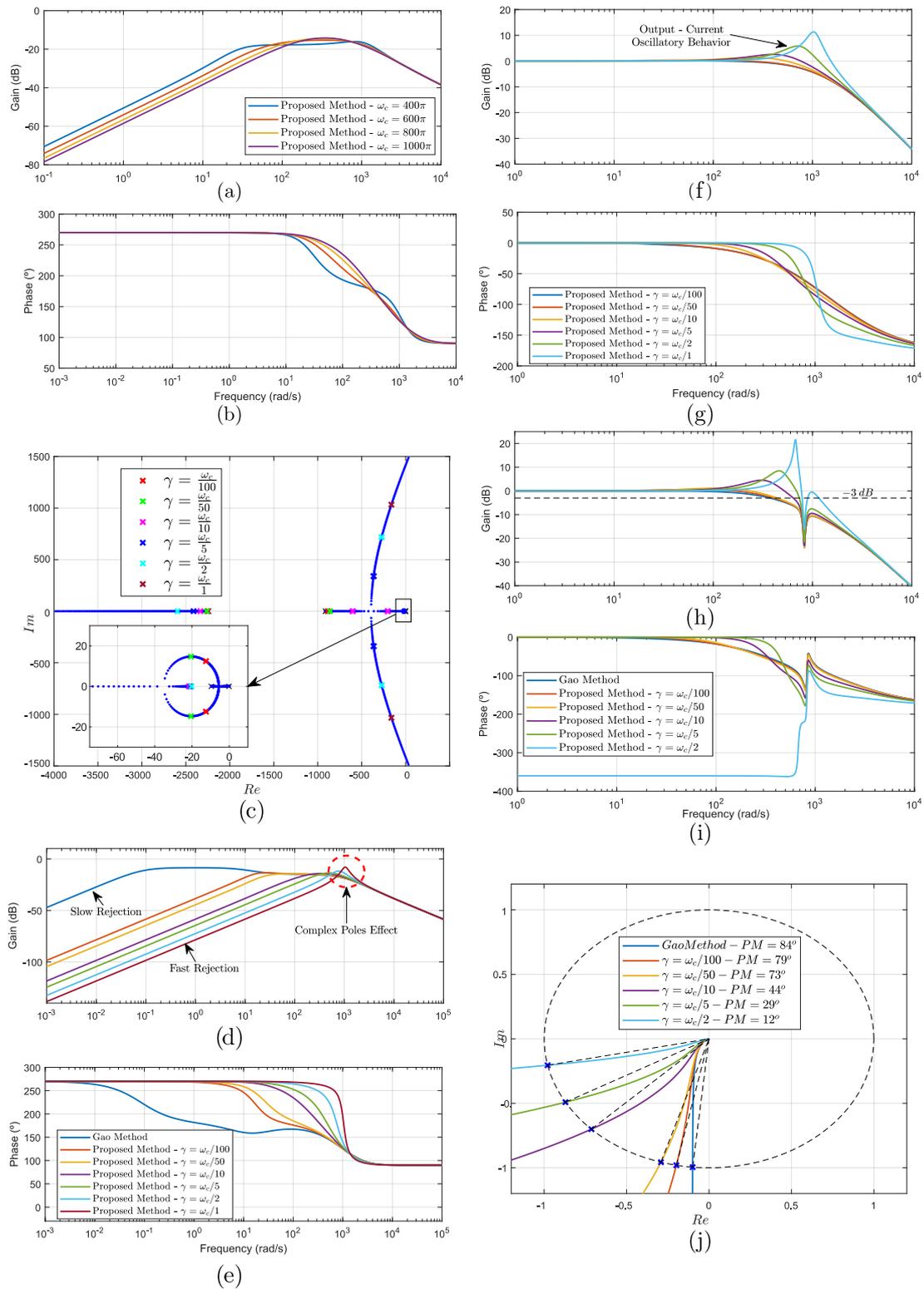


Figure 12. (a,b) Bode plot of the transfer function $\left. \frac{V_c(s)}{I_o(s)} \right|_{V_c^*(s)=0}$ using $\gamma = \frac{\omega_c}{10}$; (c) root locus of the transfer function $\left. \frac{V_c(s)}{I_o(s)} \right|_{V_c^*(s)=0}$; (d,e) Bode plot of the transfer function $\left. \frac{V_c(s)}{I_o(s)} \right|_{V_c^*(s)=0}$; (f,g) Bode plot of the transfer function $\left. \frac{I_{LL}(s)}{I_o(s)} \right|_{V_c^*(s)=0}$, (h,i) Bode plot of the transfer function $\left. \frac{V_c(s)}{V_c^*(s)} \right|_{I_o(s)=0}$ and (j) Nyquist plot of the transfer function $\left. \frac{V_c(s)}{V_c^*(s)} \right|_{I_o(s)=0}$.

In Figure 12h,i, one can analyze the reference tracking Bode plot as a function of γ . It is interesting to notice that it is possible to considerably increase the value of γ , improving the voltage-control disturbance-rejection functionality (see Figure 12d), while only slightly changing the reference tracking Bode curves in comparison to the curve obtained using Gao's tuning method (see Figure 12h). One can compare, for example, the Bode plots referenced as *Gao Method* and as $\gamma = \frac{\omega_c}{50}$ in Figure 12d,h. In Figure 12d, the Bode curves referenced as *Gao Method* and as $\gamma = \frac{\omega_c}{50}$ are very different (meaning considerable disturbance rejection improvement), while, in Figure 12h, the Bode curves referenced as *Gao Method* and as $\gamma = \frac{\omega_c}{50}$ are quite similar (meaning small variation in the reference-tracking behavior). In other words, through the k_{iv} tuning method proposed in this paper, one can improve the disturbance rejection capability while barely changing the reference tracking behavior. Of course, as the value of γ increases, at a certain point, the reference tracking behavior starts to become poorly damped, moving towards instability. This fact is related to the resonance peaks shown in Figure 12h and can be confirmed by analyzing Figure 12j that shows the system phase margins as a function of γ , through Nyquist plots.

6. Simulation Results

6.1. Hybrid Microgrid Operating with Bidirectional Power Flow

The first simulation results are obtained using the software PSCAD/EMTDC (v4.6.0) and implementing the entire hybrid microgrid as shown in Figure 13. In this simulation, there are loads and distributed generation (DG) sources in both AC and DC microgrids in such a way that a bidirectional power flow occurs between the AC microgrid and the main grid, and between the DC microgrid and the rest of the hybrid microgrid.

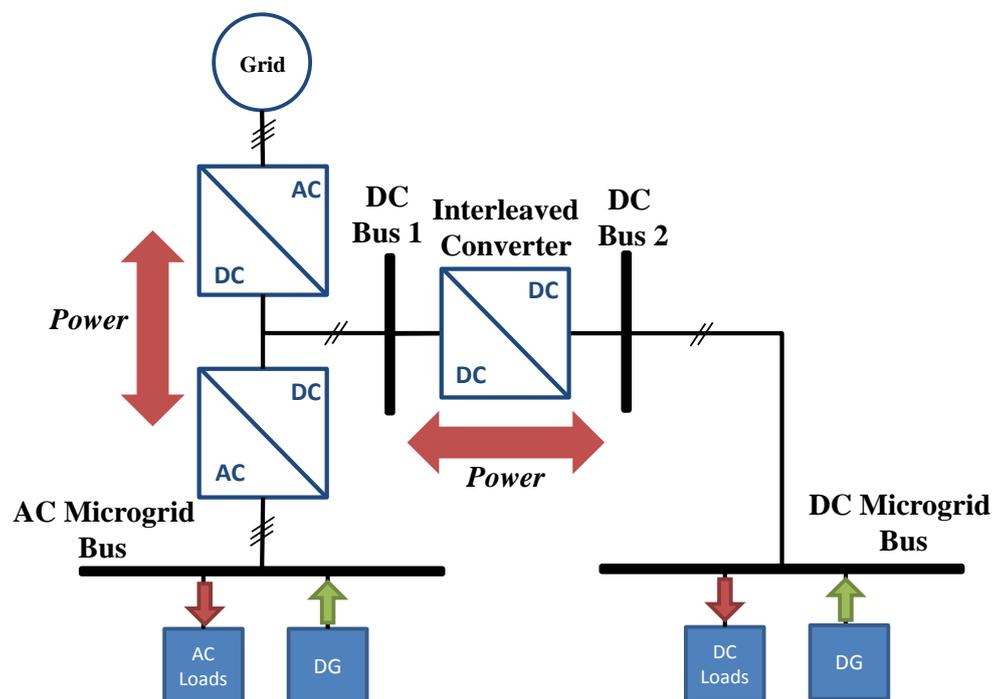


Figure 13. Topology implemented in PSCAD/EMTDC with a complete hybrid microgrid operating with bidirectional power flow between the AC microgrid and main grid and between the DC microgrid and the rest of the system.

The parameters used in this simulation are the ones shown in Table 1. The microgrid rated power is equal to $P_{base} = 56$ kW, which is ten times higher than the one of the experimental test bench of the

present work. In this simulation, the authors wanted to reproduce high power variations, leading to high output-voltage disturbances.

Table 1. Parameters used in PSCAD/EMTDC simulation.

Parameter	Value
N	3
V_g	980 V
V_c^*	450 V
L	2.5 mH
C	9.3 μ F
R	0.0 Ω
V_{base}	450 V
I_{base}	124 A
P_{base}	56 kW
ω_v	100 π rad/s
ω_c	1000 π rad/s
γ	$\frac{\omega_c}{10}$

As one can see, Figures 14–16 show the simulation results related to the bidirectional operation of the DC microgrid receiving/exporting power from/to the rest of the hybrid microgrid. The signals presented in these figures are a result of a variety of connections and disconnections of different loads and generation sources to both AC and DC microgrids. A positive value of power means power being consumed by the DC microgrid loads and negative values of power means power being exported from the DC microgrid to the rest of the hybrid microgrid.

At $t = 1.7$ s, a power flow reversion occurs. Right before this instant, the AC microgrid load and generation sources were all disconnected and all the DC microgrid sources were generating and exporting power (1 pu). After $t = 1.7$ s, simultaneously, all the generation sources in the DC microgrid are disconnected and all the loads in the DC microgrid are connected. This corresponds to a really severe power step to the DC microgrid, resulting in a very severe voltage disturbance to the output-DC-link capacitors. This severe disturbance is imposed to the system in order to test the control disturbance rejection dynamics.

By analyzing Figures 15 and 16 (zoom of the power flow inversion instant of Figure 15), one can notice that the output voltage (v_c) only suffers a small sag of approximately 11% and recovers to 1 pu in about 10 ms with an overshoot of about 1.7%, after suffering from the power flow inversion. This result shows the high-disturbance-rejection characteristic obtained by tuning the voltage controller's parameter using the proposed technique. This high-power-quality microgrid voltage is very important when feeding power to sensitive loads.

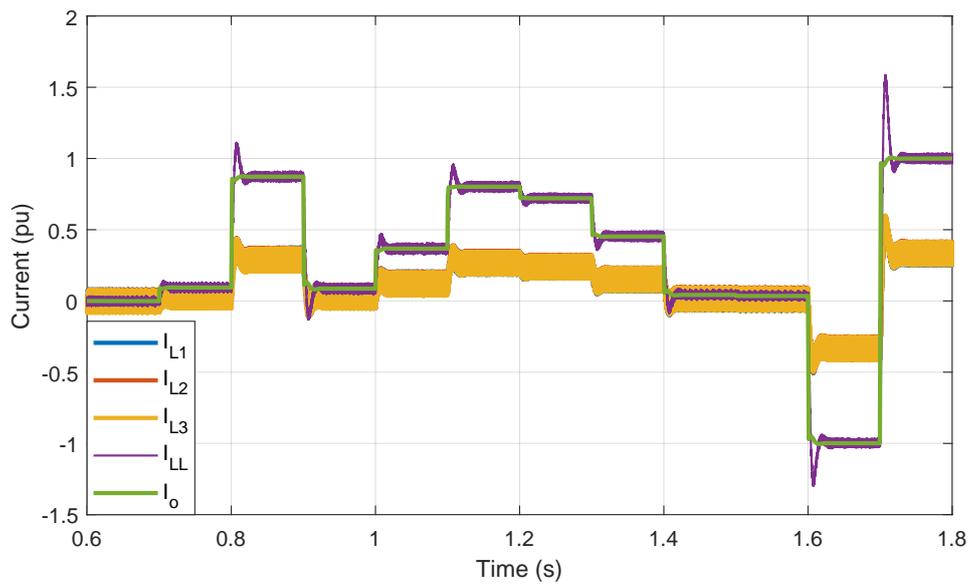


Figure 14. DC microgrid operating with bidirectional power flow and with different levels of load and generation connection resulting in different power steps imposed on the DC microgrid. In this figure, the phase currents (i_{L_a} , i_{L_b} and i_{L_c}), the reduced-ripple output current (i_{LL}) and the load current (i_o) are shown.

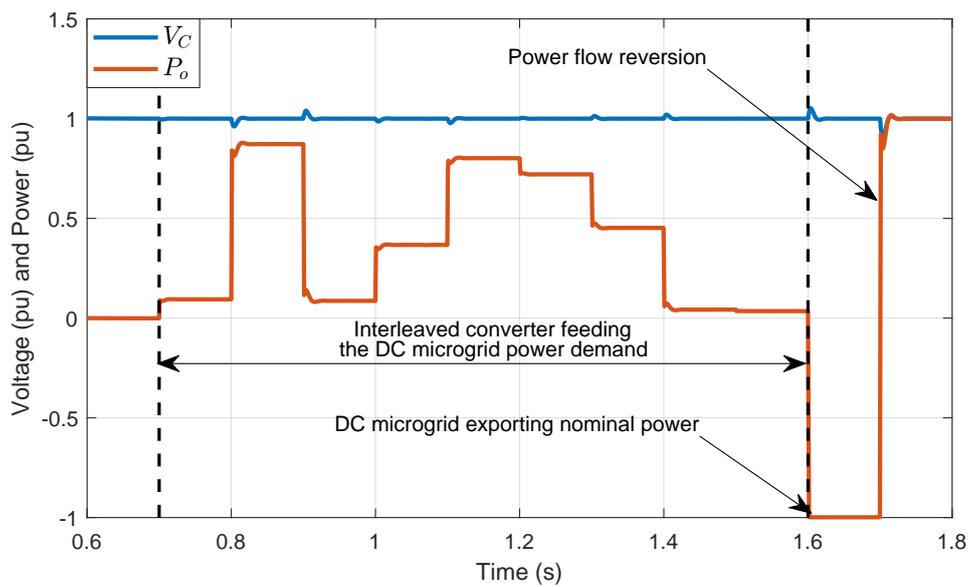


Figure 15. DC microgrid operating with bidirectional power flow and with different levels of load and generation connection resulting in different power steps imposed on the DC microgrid. In this figure, the output voltage (v_c) and the output power (P_o) are shown.

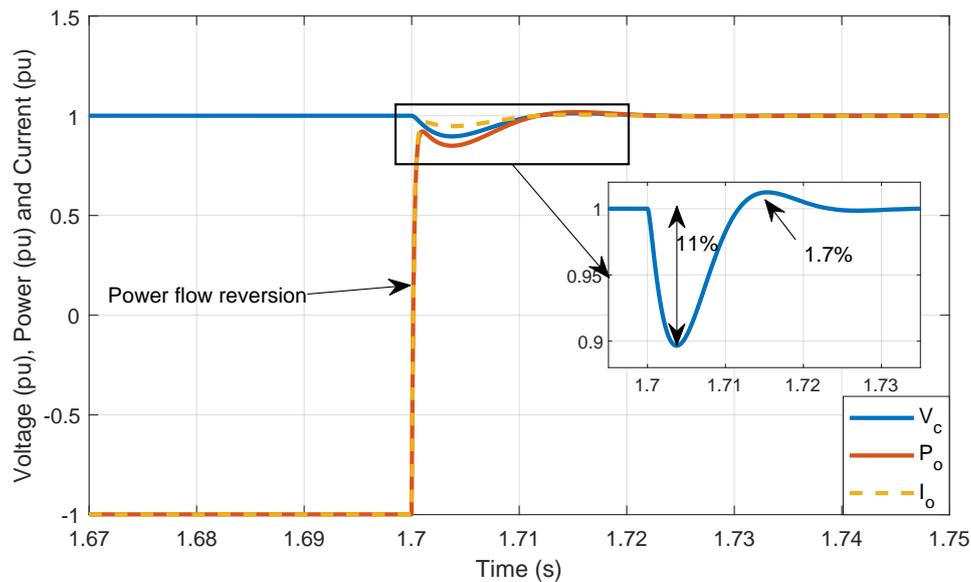


Figure 16. DC microgrid operating with bidirectional power flow and with different levels of load and generation connection resulting in different power steps imposed on the DC microgrid. In this figure, the output voltage (v_c), the output power (P_o) and the load current (i_o) are shown.

6.2. Evaluation of the Proposed Voltage Controller's Design Technique in a Simulation Environment

A simulation was carried out in Simulink/MATLAB, using the block diagram depicted in Figure 11. The parameters used are described in Table 2. The results are shown in Figures 17 and 18. At $t = 5$ s, a load step is imposed on the system in the form of a current source corresponding to a 5.6 kW step.

Table 2. Parameters used in Simulink/MATLAB simulation.

Parameter	Value
N	3
V_g	360 V
L	2.5 mH
C	1.175 mF
R	0.0 Ω
V_{base}	200 V
I_{base}	28 A
ω_v	100 π rad/s
ω_c	1000 π rad/s

In Figure 17, it is possible to analyze the output voltage (V_c) behavior for different values of γ . These results are in accordance with the root locus and Bode plot presented in Figure 12c and Figure 12d, respectively, since the disturbance rejection is improved (smaller voltage sag and faster recovery time) as γ increases and, at a certain point, the voltage behavior becomes oscillatory. These results will be compared to the experimental results later in this paper.

In Figure 18, one can notice that the system's disturbance rejection behavior using $\gamma = \frac{\omega_c}{100}$, which is the value of gamma related to the proposed control method with the slowest response, is still much faster than the behavior obtained when the voltage controller's parameters are designed using Gao's method. Gao's method only takes into account the system's reference tracking behavior and disregards that of the disturbance rejection.

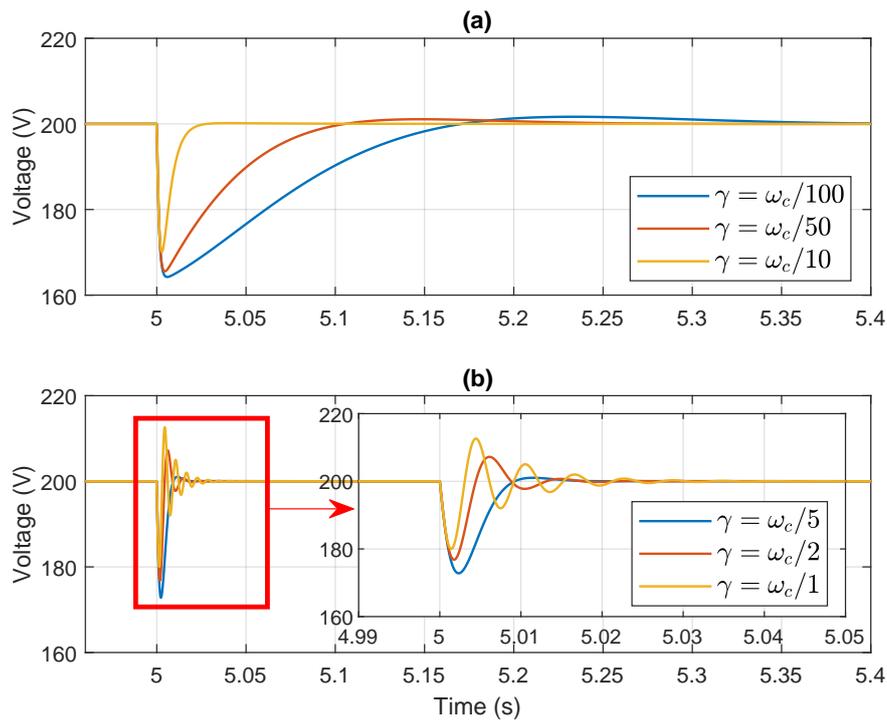


Figure 17. Simulation results showing the output voltage behavior for different values of γ . (a) Values of γ that result in slower dynamics, (b) values of γ that result in faster dynamics.

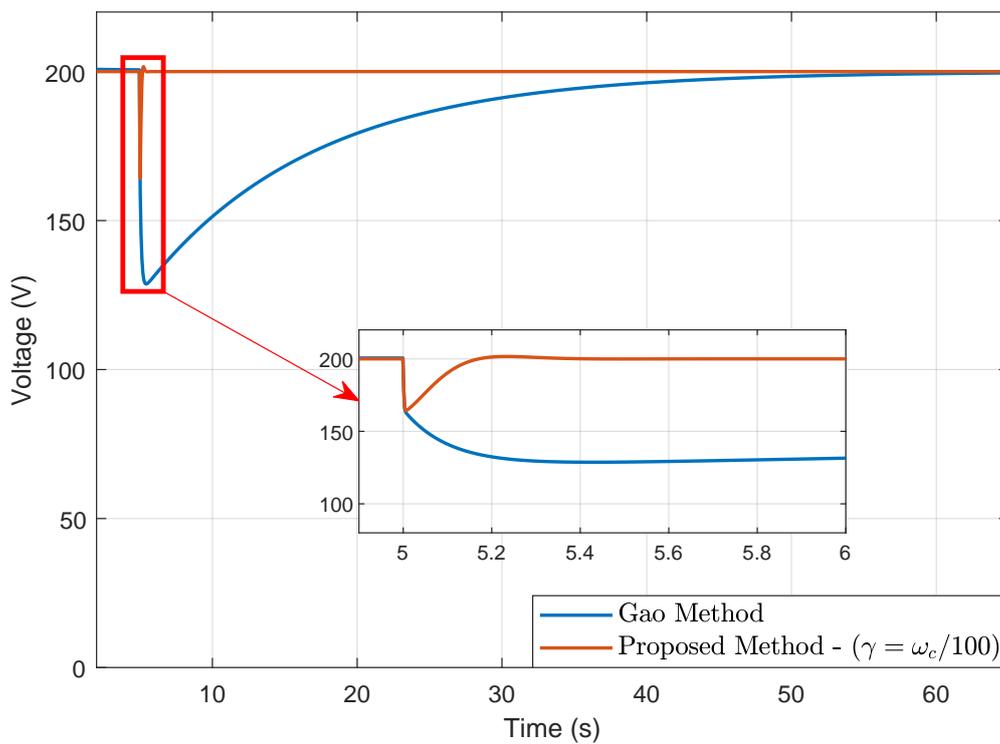


Figure 18. Simulation results showing the output voltage behavior when the voltage controller is tuned using Gao’s method and when the proposed tuning method with $\gamma = \frac{\omega_c}{100}$ is used.

7. Experimental Results

The experimental validation of the proposed topology and proposed method for designing the controller's parameters was executed using an experimental setup according to the diagram shown in Figure 19 with a three-leg interleaved converter ($n = 3$).

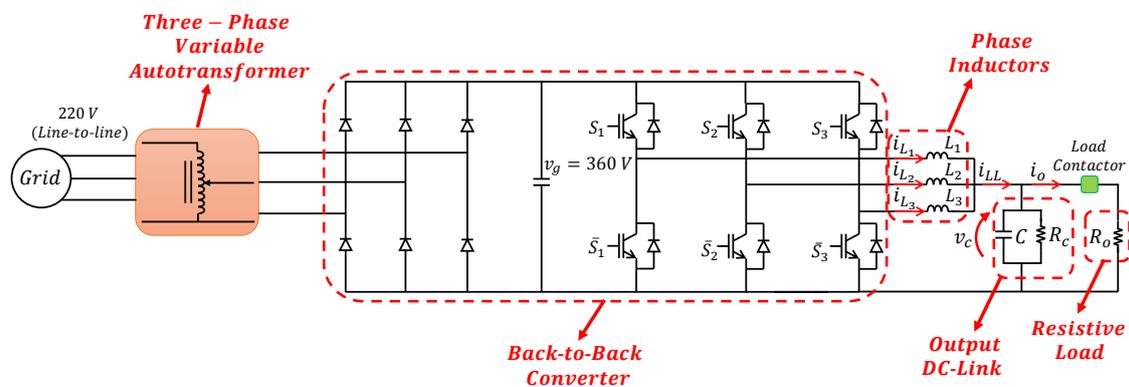


Figure 19. Experimental setup diagram.

The main goal of the experimental results is to validate the proposed control design method aiming at improving the voltage controller disturbance rejection functionality. Thus, only unidirectional power flow is taken into account, through the connection and disconnection of a resistive load in the DC microgrid. In order to generate the DC-link voltage ($V_g = 360$ V), a full bridge diode rectifier is used. Moreover, a three-phase variable autotransformer is used in order to increase the AC voltage to a level corresponding to the DC-rectified voltage equal to 360 V. A contactor is used to connect and disconnect the resistive load (R_o) to the DC microgrid in order to produce power steps that disturb the output DC voltage (v_c). The voltage controller, tuned according to the proposed method, should be able to reject these disturbances.

In this test bench, the components described in Table 3 were used. Moreover, the output DC-link voltage reference (v_c^*) has a value equal to 200 V, which leads to an output current (i_o) of approximately 27 A and an output power (P_o) of approximately 5.6 kW, since the load resistance R_o has the value equal to 7.5 Ω . The results are obtained with $\omega_v = 100\pi$ rad/s and $\omega_c = 1000\pi$ rad/s. A picture of the experimental setup is shown in Figure 20.

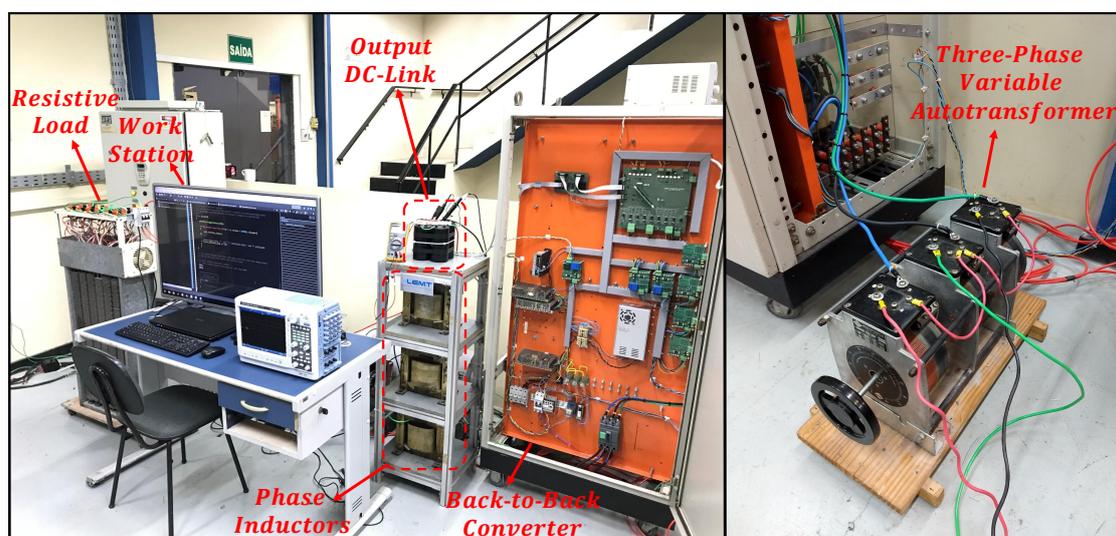


Figure 20. Experimental test bench setup.

Table 3. Experimental test-bench parameters.

Component	Value
L_k	2.5 mH
C	1.175 mF
R_c	47.0 k Ω
R_o	7.5 Ω

7.1. Transient Operation Caused by Load Connection

In this subsection, experimental results are shown in order to verify the system's dynamic behavior for different values of the parameter γ . In other words, the output voltage (v_c), the output power (P_o), the phase-1 current (i_{L1}), the reduced-ripple output current (i_{LL}) and the load current (i_o) are shown during a transient situation caused by the connection of the load (R_o).

By analyzing Figure 21, one can notice that, for the different applied values of γ , the real system behaves according to the expected from the root locus and Bode plots presented in Figure 12c and Figure 12d, respectively, demonstrating the proposed tuning technique's efficiency. In other words, as the value of γ increases, the voltage sag amplitude decreases and the voltage recovery time becomes faster. However, as γ increases, the signals' oscillatory behavior increases as well, since the complex conjugate poles' values become higher. It is important to notice that these results are very similar to the ones obtained in the simulation results.

It is also important to analyze the output current (I_{LL}) behavior for different values of γ , which reflects the expected from the Bode plot shown in Figure 12f. In other words, for $\gamma = \frac{\omega_c}{2}$ and $\gamma = \frac{\omega_c}{1}$, the output current presents an undesired oscillatory behavior, with considerably high overshoots, that could exceed components' current limits.

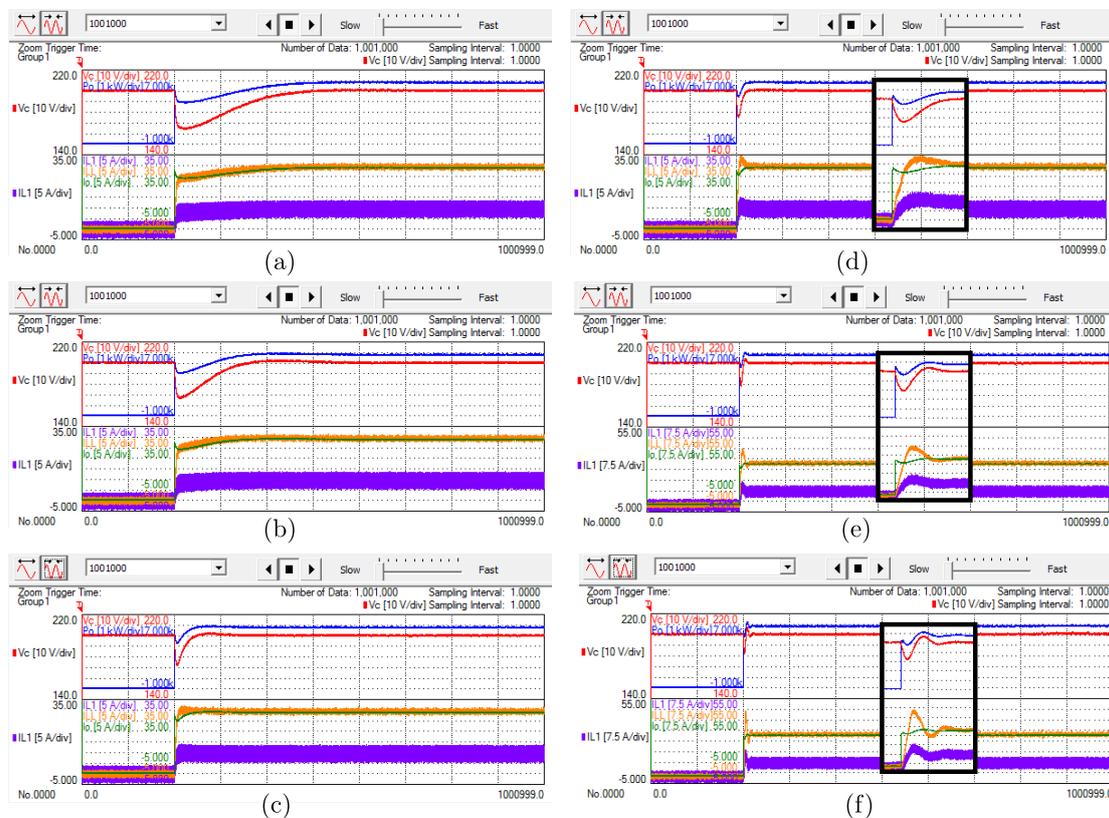


Figure 21. DC microgrid operation as a response to a 5.6 kW load connection for different values of γ . (a) $\gamma = \frac{\omega_c}{100}$; (b) $\gamma = \frac{\omega_c}{50}$; (c) $\gamma = \frac{\omega_c}{10}$; (d) $\gamma = \frac{\omega_c}{5}$; (e) $\gamma = \frac{\omega_c}{2}$ and (f) $\gamma = \frac{\omega_c}{1}$. In these figures, the time axis has 50 ms/div.

7.2. Microgrid Operation with Load Connection and Disconnection

In Figure 22, one can observe the DC microgrid operation during transient moments caused by a 5.6 kW load connection and disconnection using $\gamma = \frac{\omega_c}{10}$, $\omega_c = 1000\pi$ and $\omega_v = 100\pi$. This figure demonstrates that the system is stable and very robust since the microgrid voltage is kept constant during the transient moments, suffering a very negligible impact with the load steps (negligible sags and swells), resulting in a high power quality.

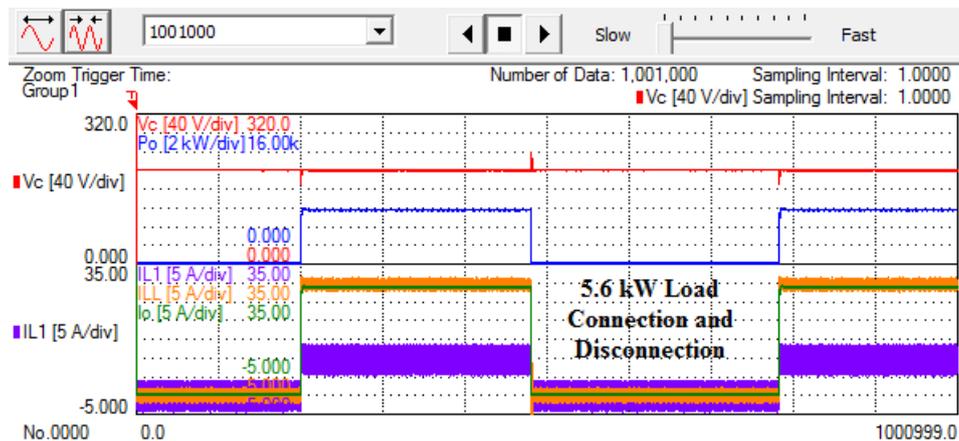


Figure 22. Microgrid stable and robust operation with load connection and disconnection. In this figure, the time axis has 1 s/div.

7.3. Steady-State Operation

The steady-state results are presented as depicted in Figures 23 and 24. In Figure 23, one can notice the balanced phase currents (i_{L1} , i_{L2} and i_{L3}) obtained in the experimental analysis, which have a mean value of approximately 9 A.

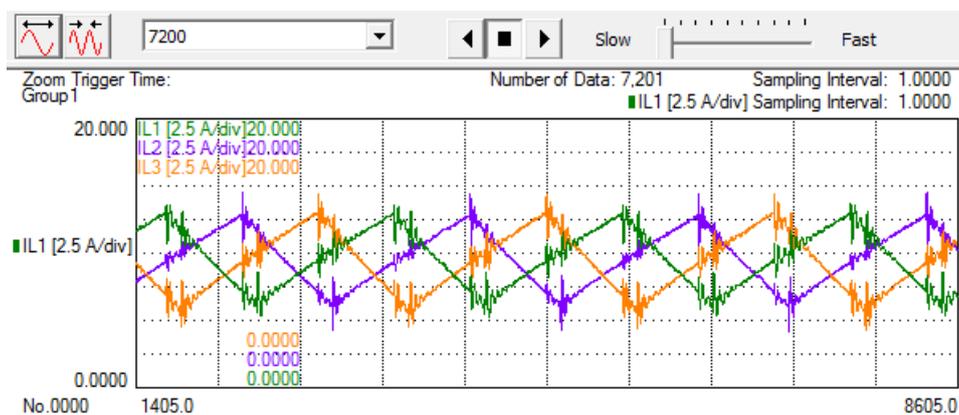


Figure 23. Steady-state phase currents.

In Figure 24, one can observe the phase-1 current (i_{L1}) as well as the reduced-ripple output current (i_{LL}) and the load current (i_o). It can be observed that i_{LL} , with an approximate value of 28 A, is practically a constant signal with no ripple, proving that the interleaved topology along with the modulation technique using phase-shifted carrier signals work properly in producing an output current with reduced ripple, which diminishes the voltage ripple across the output capacitor. Since this reduced voltage ripple is obtained, a capacitor with reduced size and cost can be used in this application.



Figure 24. Phase-1 current, reduced-ripple output current and load current.

8. Conclusions

This paper introduced a new application of an interleaved converter as a power interface in a hybrid microgrid. The converter is responsible for regulating the DC microgrid voltage while controlling the power flow through the system. The authors proposed a new method for tuning the voltage controller in such a way as to improve the load disturbance rejection, which is a highly desired functionality in such application. Moreover, the authors presented a deep modeling of the MIMO system in order to execute the control design and a stability and robustness analysis. Finally, experimental results were presented validating the proposed topology and modeling.

The tuning technique proved to be efficient in designing the voltage controller aiming at obtaining robust disturbance rejection characteristics while maintaining proper reference tracking behavior. In addition, the experimental results proved that the topology and control allow for a satisfactory operation of the microgrid regarding its voltage profile (high power quality), besides allowing for the reduction of the output-DC-link capacitors, due to the obtained low-ripple output current, reducing the system's size and weight.

Author Contributions: T.T. established the major part of this paper which includes conceptualization, modeling, simulation, investigation and experimental validation. G.G. contributed with conceptualization, modeling, experimental validation and was responsible for writing the original draft preparation. M.N. contributed with the experimental validation. M.S. contributed with conceptualization, text review and editing. M.A. provided resources, helped with funding acquisition and provided supervision. J.M.G. provided supervision and text review.

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References

1. Parhizi, S.; Lotfi, H.; Khodaei, A.; Bahramirad, S. State of the art in research on microgrids: A review. *IEEE Access* **2015**, *3*, 890–925. [\[CrossRef\]](#)
2. Wang, X.; Guerrero, J.M.; Blaabjerg, F.; Chen, Z. A Review of Power Electronics Based Microgrids. *J. Power Electron.* **2012**, *12*, 181–192. [\[CrossRef\]](#)
3. Guerrero, J.M.; Chandorkar, M.; Lee, T.L.; Loh, P.C. Advanced Control Architectures for Intelligent Microgrids—Part I: Decentralized and Hierarchical Control. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1254–1262. [\[CrossRef\]](#)
4. Guerrero, J.M.; Loh, P.C.; Lee, T.L.; Chandorkar, M. Advanced Control Architectures for Intelligent Microgrids—Part II: Power Quality, Energy Storage, and AC/DC Microgrids. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1263–1270. [\[CrossRef\]](#)

5. Dragicevic, T.; Lu, X.; Vasquez, J.C.; Guerrero, J.M. DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques. *IEEE Trans. Power Electron.* **2016**, *31*, 4876–4891. [[CrossRef](#)]
6. Dragicevic, T.; Lu, X.; Vasquez, J.; Guerrero, J.M. DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues. *IEEE Trans. Power Electron.* **2016**, *31*, 3528–3549. [[CrossRef](#)]
7. Che, L.; Shahidehpour, M. DC Microgrids: Economic Operation and Enhancement of Resilience by Hierarchical Control. *IEEE Trans. Smart Grid* **2014**, *5*, 2517–2526.
8. Saeedifard, M.; Graovac, M.; Dias, R.F.; Irvani, R. DC Power Systems: Challenges and Opportunities. In Proceedings of the IEEE PES General Meeting, Providence, RI, USA, 25–29 July 2010; pp. 1–7.
9. Liu, X.; Wang, P.; Loh, P.C. A Hybrid AC/DC Microgrid and Its Coordination Control. *IEEE Trans. Smart Grid* **2011**, *2*, 278–286.
10. Majumder, R. A Hybrid Microgrid With DC Connection at Back to Back Converters. *IEEE Trans. Smart Grid* **2014**, *5*, 251–259. [[CrossRef](#)]
11. Zhu, J.P.; Zhou, J.P.; Zhang, H. Research Progress of AC, DC and Their Hybrid Micro-grids. In Proceedings of the 2014 IEEE International Conference on System Science and Engineering (JCSSE), Shanghai, China, 11–13 July 2014.
12. Syed, M.H.; Zeineldin, H.H.; El Moursi, M.S. Hybrid micro-grid operation characterisation based on stability and adherence to grid codes. *IET Gener. Transm. Distrib.* **2014**, *8*, 563–572. [[CrossRef](#)]
13. Baumann, M.; Peters, J.; Weil, M.; Marcelino, C.; Almeida, P.; Wanner, E. Environmental Impacts of different Battery Technologies in Renewable Hybrid Micro-Grids. In Proceedings of the 2017 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe), Torino, Italy, 26–29 September 2017.
14. Hedel, K.K. High-Density Avionic Power Supply. *IEEE Trans. Aerosp. Electron. Syst.* **1980**, *AES-16*, 615–619. [[CrossRef](#)]
15. Shortt, D.J.; Michael, W.T.; Avant, R.L.; Palma, R.E. A 600 watt four stage phase-shifted-parallel DC-to-DC converter. In Proceedings of the 1985 IEEE Power Electronics Specialists Conference, Toulouse, France, 24–28 June 1985; pp. 136–143.
16. Miwa, B.A.; Otten, D.M.; Schlecht, M.F. High efficiency power factor correction using interleaving techniques. In Proceedings of the 1992 Applied Power Electronics Conference and Exposition, APEC '92, Boston, MA, USA, 23–27 February 1992.
17. Chang, C.; Knights, M.A. Interleaving Technique in Distributed Power Conversion Systems. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **1995**, *42*, 245–251. [[CrossRef](#)]
18. Chang, C. Current Ripple Bounds in Interleaved DC–DC Power Converters. In Proceedings of the 1995 International Conference on Power Electronics and Drive Systems, PEDS 95, Singapore, 21–24 February 1995; Volume 2, pp. 738–743.
19. Balogh, L.; Redl, R. Power-Factor Correction with Interleaved Boost Converters in Continuous-Inductor-Current Mode. In Proceedings of the Eighth Annual Applied Power Electronics Conference and Exposition, San Diego, CA, USA, 7–11 March 1993; pp. 168–174.
20. Chandrasekaran, S.; Gokdere, L.U. Integrated Magnetics for Interleaved DC–DC Boost Converter for Fuel Cell Powered Vehicles. In Proceedings of the 2004 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; pp. 356–361.
21. Hirakawa, M.; Watanabe, Y.; Nagano, M.; Andoh, K.; Nakatomi, S.; Hashino, S.; Shimizu, T. High Power DC / DC Converter using Extreme Close-Coupled Inductors aimed for Electric Vehicles. In Proceedings of the 2010 International Power Electronics Conference—ECCE ASIA, Sapporo, Japan, 21–24 June 2010; pp. 2941–2948.
22. Hirakawa, M.; Nagano, M.; Watanabe, Y.; Ando, K.; Nakatomi, S.; Hashino, S. High Power Density Interleaved DC/DC Converter using a 3-phase Integrated Close-Coupled Inductor Set aimed for Electric Vehicles. In Proceedings of the 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, USA, 12–16 September 2010.
23. Schroeder, J.C.; Wittig, B.; Fuchs, F.W. High Efficient Battery Backup System for Lift Trucks Using Interleaved-Converter and Increased EDLC Voltage Range. In Proceedings of the IECON 2010—36th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ, USA, 7–10 November 2010; pp. 2334–2339.
24. Ni, L.; Patterson, D.J.; Hudgins, J.L. High Power Current Sensorless Bidirectional 16-Phase Interleaved DC–DC Converter for Hybrid Vehicle Application. *IEEE Trans. Power Electron.* **2012**, *27*, 1141–1151. [[CrossRef](#)]

25. Hegazy, O.; Mierlo, J.V.; Lataire, P. Analysis, Modeling, and Implementation of a Multidevice Interleaved DC/DC Converter for Fuel Cell Hybrid Electric Vehicles. *IEEE Trans. Power Electron.* **2012**, *27*, 4445–4458. [[CrossRef](#)]
26. Schroeder, J.C.; Petersen, M.; Fuchs, F.W. One-Sensor Current Sharing in Multiphase Interleaved DC/DC Converters with Coupled Inductors. In Proceedings of the 15th International Power Electronics and Motion Control Conference, EPE-PEMC 2012 ECCE Europe, Novi Sad, Serbia, 4–6 September 2012; pp. 1–7.
27. Lu, S.; Mu, M.; Jiao, Y.; Lee, F.C.; Zhao, Z. Coupled inductors in interleaved multiphase three-level DC–DC Converter for High Power Energy Storage Applications. In Proceedings of the 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), Beijing, China, 31 August–3 September 2014; pp. 1–6.
28. Magne, P.; Liu, P.; Bilgin, B.; Emadi, A. Investigation of Impact of Number of Phases in Interleaved dc-dc Boost Converter. In Proceedings of the 2015 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, USA, 14–17 June 2015.
29. Jung, M.; Lempidis, G.; Hölsch, D.; Steffen, J. Optimization considerations for Interleaved DC–DC Converters for EV Battery charging applications, in terms of partial load efficiency and power density. In Proceedings of the 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCEurope), Geneva, Switzerland, 8–10 September 2015.
30. Schumacher, D.; Magne, P.; Preindl, M.; Bilgin, B.; Emadi, A. Closed Loop Control of a Six Phase Interleaved Bidirectional dc-dc Boost Converter for an EV/ HEV Application. In Proceedings of the 2016 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, USA, 26–29 June 2016.
31. Karimi, R.; Kaczorowski, D.; Zlotnik, A.; Mertens, A. Loss Optimizing Control of a Multiphase Interleaving DC–DC Converter for Use in a Hybrid Electric Vehicle Drivetrain. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016.
32. Melo, R.R.; Antunes, F.L.M.; Daher, S. Bidirectional interleaved dc-dc converter for supercapacitor-based energy storage systems applied to microgrids and electric vehicles. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, 26–28 August 2014.
33. Chaitanya, N.; Anjaneyulu, K.S.R.; Sekhar, K.C. Performance Analysis of a Hybrid Power System with Three Phase Interleaved Bidirectional Converter. In Proceedings of the 2014 International Conference on Smart Electric Grid (ISEG), Guntur, India, 19–20 September 2014; pp. 1–8.
34. Correa-Betanzo, C.; Calleja, H.; Morales-Morales, C.; López-Zapata, B. An Interleaved Single Phase Grid Tied Converter aimed at DC Microgrid Applications. In Proceedings of the 2016 13th International Conference on Power Electronics (CIEP) An, Guanajuato, Mexico, 20–23 June 2016; pp. 277–282.
35. Krishna, D.S.G.; Patra, M. Modeling of Multi-Phase DC–DC Converter with A Compensator for Better Voltage Regulation in DC Micro-grid Application. In Proceedings of the International Conference on Signal Processing, Communication, Power and Embedded System (SCOPEs)—2016 Modeling, Odisha, India, 3–4 October 2016; pp. 989–994.
36. Kan, Z. Interleaved Three-Level Bi-directional DC–DC Converter and Power Flow Control. In Proceedings of the 2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG), Yilan, Taiwan, 22–25 April 2018; pp. 1–4.
37. Tricarico, T.; Soares, M.; Gontijo, G.; Oliveira, D.; Dicler, F.; Aredes, M. Design, Control and Stability Analysis of an Interleaved DC Converter for Voltage Interfacing Application in Microgrids. In Proceedings of the XXII Brazilian Conference on Automation (CBA 2018), João Pessoa, Brazil, 9–12 September 2018.
38. Gao, Z. Scaling and Bandwidth-Parameterization Based Controller Tuning. In Proceedings of the 2003 American Control Conference, Denver, CO, USA, 4–6 June 2003; pp. 4989–4996.

