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A Composite Strategy for Harmonic Compensation in Standalone Inverter Based on Linear Active Disturbance Rejection Control

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Abstract: This paper proposes a harmonic compensation control with disturbance rejection function for a standalone inverter. Due to the LC type three-phase three-leg inverter is connected to nonlinear loads, low-order harmonic components appears in the inverter output current. These harmonic current generate harmonic voltage drops when flowing through the filter inductor and the feeder impedance, which causes the output voltage of the inverter distorted. In order to compensate harmonics and produce sinusoidal voltage without additional compensation devices, virtual harmonic impedance method can be added to the fundamental voltage control. Due to the compensation effect of virtual harmonic impedance are very sensitive to the fluctuation of filter inductance. Therefore, inductance variation, as a disturbance in physical system, should be considered. In this paper, linear active disturbance rejection control (LADRC) is proposed in the fundamental voltage control loop to reduce the sensitivity of virtual harmonic impedance and decouple the model. Compared with traditional dual-loop PI control, the proposed strategy has faster dynamic response in control performance and fewer acquisition modules in engineering applications. The whole design process of virtual harmonic impedance and stability analyses of this strategy are provided. The simulation and experiment results show the good performance of the proposed strategy.

Keywords: harmonic; standalone inverter; virtual harmonic impedance; LADRC

1. Introduction

With the application of distributed energy resources, the penetration rate of renewable energy sources has been greatly increased. While bringing low carbon and economic benefits, intermittency and poor power quality also appear. Therefore, the concept of microgrid is proposed, which combines distributed energy resources with utility grid to effectively overcome these shortcomings [1–3]. In order to guarantee the power quality of demand side, many standards have been proposed, especially for harmonic problems. Current harmonic distortion increases the additional losses of electrical equipment, overheating the equipment, reducing equipment efficiency and utilization [4–6].

Various researches focus on the harmonic problem of the microgrid. There are two main sources of harmonics in microgrids: power electronic devices and nonlinear loads. Power electronic devices have been widely used in many places, such as inverters, rectifiers, static compensators, etc. The switching of transistors generates high frequency harmonics, which can be suppressed by LC or LCL filter. However, the harmonics generated by nonlinear loads are difficult to be eliminated only by the design of the filter circuit. In an isolated island microgrid, the main reason for generating output voltage harmonics is that nonlinear loads is connected to the inverter terminal to make the output

current distorted. When these distorted current flow through the linear electrical components, the corresponding harmonic voltage drop is generated, which eventually leads to the distortion of the inverter output voltage waveform. In order to reduce harmonics and improve system efficiency, harmonic compensation strategies have been extensively studied.

The existing harmonic control researches can be mainly divided into two categories: one is to use the additional compensation devices; the other is to use the harmonic current detection and control algorithm for feedforward compensation without additional compensation devices. Active power filter (APF) is a mature harmonic compensation device, it injects harmonic compensation current with equal magnitude and opposite phase into harmonic source [7–9]. Authors in [10] use the least mean squares (LMS, NLMS) and recursive least squares (RLS) algorithms for shunt APF to reduce the total harmonic distortion (THD). But this algorithm has a large computational burden. In [11], a composite control method based on the combination of proportional integral (PI) control and fast repetitive control (FRC) is proposed, which can stabilize the output compensation current in 1/6 grid cycle. However, APF as an additional compensation device in the system, the loss and cost of the device are increased [12–14].

Hence, a feedforward compensation strategy based on current detection and control algorithms without additional compensation equipments is considered. A closed loop control of the RMS value of each of the voltage harmonics using PI controller proposed in [15]. The method can suppress each harmonic independently, but it needs to detect the amplitude and phase of each harmonic, and the compensation effect depends on the accuracy of the detection method. Authors in [16] transforms the output voltage of the inverter to the *dq* synchronous reference frame through the Park transform, and then uses the PI controller to track the reference values of fundamental voltage and harmonics. This method can effectively suppress certain subharmonics, but it needs to design the controller at each compensated harmonics, which makes the control structure complex and parameter tuning difficult. The use of virtual harmonic impedances has also been proposed to harmonic compensation in existing literature [17–19]. Authors in [20] proposes a control strategy employs negative virtual harmonic impedance to compensate for effect of line impedance on harmonic power delivery. Authors in [21] propose a composite control strategy of PI and virtual harmonic impedance, and considers the time delay of system. Authors in [22] replaces the PI controller of the fundamental voltage in [21] with the PR controller, which improves the tracking accuracy of the feedback loop. However, the effects of the output inductance value fluctuation on the virtual harmonic impedance compensation effect are not solved in [20–22]. Authors in [23] propose adaptive virtual harmonic impedance based on the required voltage quality at the load bus, which solved the uncertainties of virtual harmonic impedances to some extent. But it requires additional calculations for virtual harmonic impedances.

The virtual harmonic impedance can compensate the specific harmonic effectively and simply, but the compensation effect of virtual harmonic impedance is very sensitive to the fluctuation of filter inductance. In order to solve this problem, a composite control strategy combining disturbance rejection control with the virtual harmonic impedance can be considered. At present, common disturbance rejection control strategies include active disturbance rejection control (ADRC), disturbance-observer-based control (DOBC), composite hierarchical antidisturbance control (CHADC) and disturbance accommodation control (DAC), etc. [24]. Unlike many existing control methods, the ADRC does not require the accurate mathematical model of the plant. Therefore, ADRC has been paid more and more attention for its excellent engineering application and disturbance rejection performance, and has been applied in many industries [25–28]. Authors in [29] proposes a robust active damping method based on the LADRC, to solve the control problem of LCL-filtered grid-connected Inverter in the case of disturbance and parameter uncertainty. A linear auto-disturbance rejection control method based on LCL type grid-connected inverter was proposed in [30], which realized high rejection performance against external interference, internal decoupling and parameter variation.

On the basis of the existing research, Section 2 of this paper firstly models and simplifies the inverter in the *dq* synchronous reference frame, and then Section 3.2 designs the LADRC controller structure through the relative order of the model and gives the parameter tuning method. In Section 3.1,

the virtual harmonic impedance is designed for the high harmonic components of output voltage and feedforward to the fundamental voltage control loop. In Section 4, the stability analysis of LADRC controller and the validity analysis of virtual harmonic impedance are given in the frequency domain. Finally, the good performances of the proposed strategy are shown in Section 5.

2. System Configuration

2.1. Modeling in the dq Synchronous Reference Frame

The LC type three-phase three-leg inverter with proposed control strategy is shown in Figure 1. The LC filter consists of capacitor C_f, inductor L_f and parasitic resistor r. Although LC filters can reduce switching harmonic, it also produces the output current distortion when feeding nonlinear loads. When these harmonic current flow through the filter inductance and the feeder impedance, it will cause a voltage drop and a output voltage distortion.

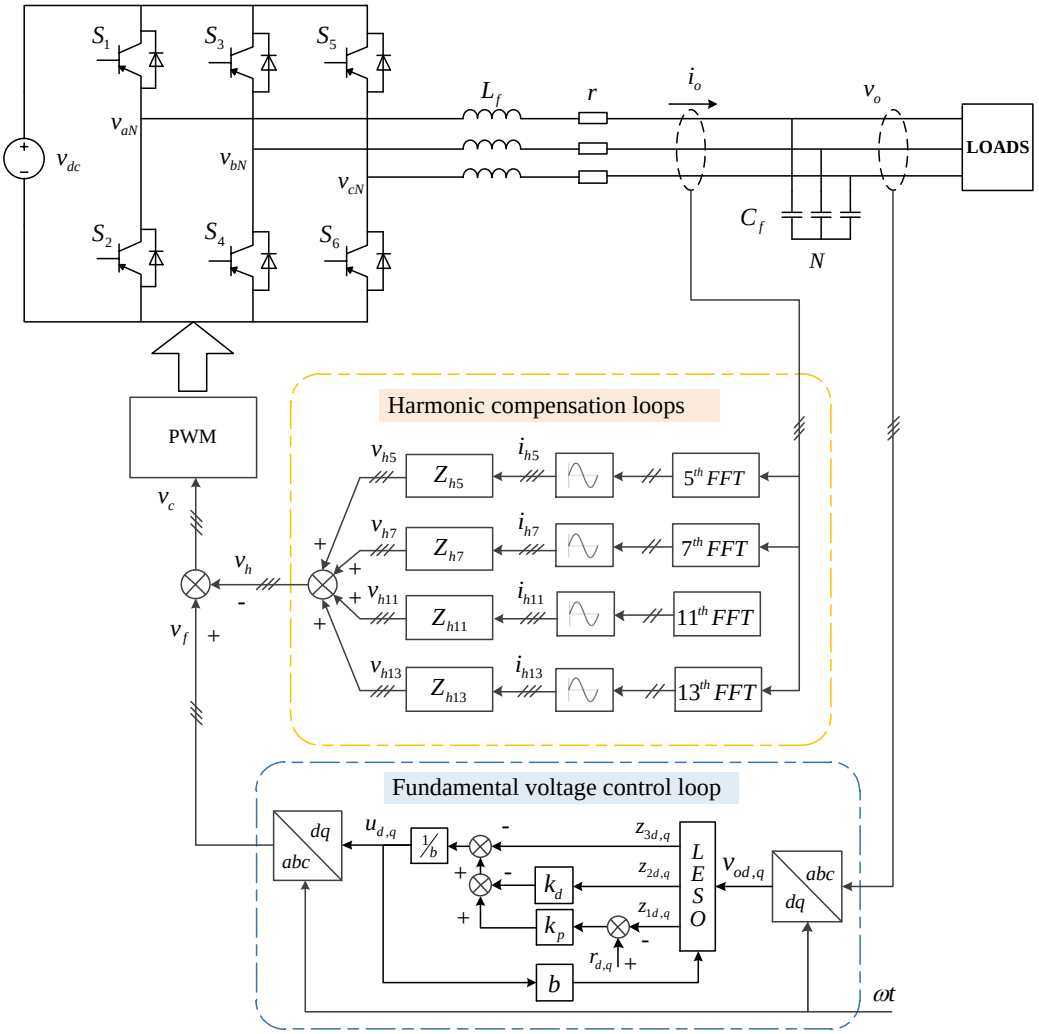


Figure 1. A LC type three-phase three-leg inverter with proposed control strategy.

According to kirchhoff voltage law and current law, the system model in the *abc* reference frame can be written as:

$$\begin{cases} L_f \frac{di_{Lk}}{dt} = v_{kN} - v_{ok} - i_{Lk} r, \\ C_f \frac{dv_{ok}}{dt} = i_{Lk} - i_{ok}. \end{cases} \tag{1}$$

where $k = a, b, c$.

Next, the system model in *abc* reference frame can be transfromed into *dq* synchronous reference frame by Park transformation. The system (1) can be expressed as:

$$\begin{cases} L_f \frac{di_{Ld}}{dt} = v_{dN} - v_{od} - i_{Ld}r + \omega L_f i_{Lq}, \\ L_f \frac{di_{Lq}}{dt} = v_{qN} - v_{oq} - i_{Lq}r - \omega L_f i_{Ld}, \\ C_f \frac{dv_{od}}{dt} = i_{Ld} - i_{od} + \omega C_f v_{oq}, \\ C_f \frac{dv_{oq}}{dt} = i_{Lq} - i_{oq} - \omega C_f v_{od}. \end{cases} \tag{2}$$

On the *d*-axis, v_{dN} is the output of inverter before LC filter, v_{od} is the voltage of loads, i_{Ld} is the inductance current and i_{od} is the current of loads. And v_{qN}, v_{oq}, i_{Lq}, i_{oq} have the same definition on the *q*-axis.

Letting $i_{Ldq} = i_{Ld} + ji_{Lq}$, $v_{dqN} = v_{dN} + jv_{qN}$, $i_{odq} = i_{od} + ji_{oq}$, $v_{odq} = v_{od} + jv_{oq}$, form (2) can be rewritten as:

$$\begin{cases} L_f \frac{di_{Ldq}}{dt} = v_{dqN} - v_{odq} - i_{Ldq}r - j\omega L_f i_{Ldq}, \\ C_f \frac{dv_{odq}}{dt} = i_{Ldq} - i_{odq} - j\omega C_f v_{odq}. \end{cases} \tag{3}$$

From system (2), it can be seen that there are strong couplings between *d*-axis and *q*-axis. Any disturbance of one axis will affect the other axis by the coupling term, thus affecting the dynamic performance of the system. Therefore, control methods with decoupling functions are required in the *dq* synchronous reference frame, such as LADRC.

2.2. Model Simplification

The effect of filter capacitor can be disregarded in low frequency systems, hence the main response of the LC filter can be represented by an inductance L_f, the simplified circuit is shown in Figure 2. Where v_N is the voltage generated by the inverter and v_L is the voltage drop of filter inductance and parasitic resistance. i_o is the inverter output current, in which low-order harmonic components lead to the distortion of output voltage v_o. When the nonlinear loads are far away from the inverter, this distortion will be more serious due to the combined effect of line impedances and filter inductances.

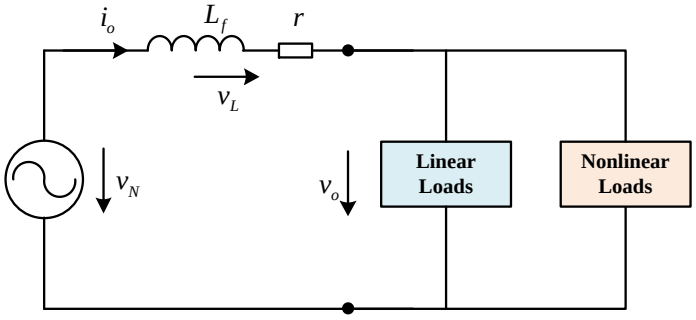


Figure 2. Equivalent circuit of the virtual harmonic impedance loop.

According to the equivalent circuit, v_o can be described as:

$$v_o(t) = v_N(t) - v_L(t) = v_N(t) - v_{L1}(t) - \sum_{n=2}^{h} v_{Ln}(t). \tag{4}$$

In Equation (4), v_{L1} and v_{Ln} are the fundamental component and harmonic components of v_L and n refers to the harnmonic order. The main implementation of virtual harmonic impedance loops is

to design virtual harmonic impedance value equal to the v_{Ln} at each frequency to be compensated. Hence, the compensation effect of virtual harmonic impedance loops is very sensitive to inductance value. In order to avoid this problem, a compensation strategy based on LADRC is proposed in this paper. In this strategy, inductance fluctuations are regarded as an unmodelled dynamic, which is estimated by extended state observer (ESO) and then be compensated. In this way, the sensitivity of virtual harmonic impedances to inductance values is reduced. In conclusion, compared with the traditional harmonic compensation strategies, the proposed method has two advantages: decoupling and disturbance rejection.

3. Proposed Control Method

Figure 1 shows the diagram of proposed control, it consists of a fundamental voltage control loop and some specific frequency harmonic compensation loops. The fundamental voltage control loop adopts the LADRC controller in the *dq* synchronous reference frame, and its output signal is v_f. Harmonic compensation loops works by shaping harmonic voltage drops v_h with harmonic currents and virtual harmonic impedances. The total output signal of controller is given as follows:

$$v_c = v_f - v_h. \tag{5}$$

3.1. Virtual Harmonic Impedance Dsign

In harmonic compensation loops, the nth harmonic component from the output current can be detected by Fourier transform. And then the nth harmonic voltage drop is obtained by multiplying the nth harmonic current by the nth virtual harmonic impedance:

$$v_{hn} = i_{hn} Z_{hn}, \tag{6}$$

where i_{hn} is the nth harmonic current and Z_{hn} is the nth virtual harmonic impedance to be designed. The harmonic voltage drop can be added to fundamental voltage control loop inversely. In this way, usually harmonics less than 50th can be compensated without additional compensation inverters.

In order to compensate the voltage drop across the output inductance of the inverter, the v_{hn} should have the same amplitude and opposite phase to v_{Ln}:

$$v_{hn} = -v_{Ln} = -i_{hn} Z_{Ln}, \tag{7}$$

where Z_{Ln} is the output inductance of nth harmonic. It consists of a filter inductor L_f and a parasitic resistance r:

$$Z_{Ln} = r + j\omega_n L_f, \tag{8}$$

where ω_n is the angular frequency of nth harmonic componet.

There are many models of virtual harmonic impedance, such as a resistance, a series RL, a parallel RC, a series RC, etc. In this paper, the virtual harmonic impedance will be modeled as a series RL. This model was chosen because of its simple structure and same form as the output inductance, which simplifies the design process. According to formula (8), the transfer function of a series RL is:

$$Z_{hn} = R_{hn} + j\omega_n L_{hn}, \tag{9}$$

where $R_{hn} = r$, $L_{hn} = L_f$, $\omega_n = 2n\pi f_1$, f_1 is the fundamental frequency. The amplitude and phase of virtual harmonic impedance denotes as K and θ:

$$K = |Z_{hn}(s)| = \sqrt{R_{hn}^2 + (\omega_n L_{hn})^2}, \tag{10}$$

$$\theta = arctan(\frac{\omega_n L_{hn}}{R_{hn}}). \tag{11}$$

Hence, the calculation process of the virtual harmonic voltage drop can be equivalent to using a virtual harmonic impedance to perform a K gain and θ phase shift on the harmonic current.

3.2. LADRC Controller Design

This paper proposes the application of LADRC in the fundamental voltage control loop to ensure good tracking of the output voltage reference and robust stability with respect to parametric variations and disturbance. Compared with the PI controller, the proposed strategy has two advantages. One is that it can decouple the model (3) and achieve better transient performance when the load changes. The other is to reject the internal parameter variation and disturbance of the physical system so as to weaken the sensitivity of virtual harmonic impedance effectiveness to output inductance fluctuation.

The first step of designing LADRC controller is to determine the relative order of the system. This section uses the shortest path method to obtain the relative order of the system, that is, to find a shortest path from the input to the output through the minimum number of integrators.

According to the system (3), the diagram of LC type inverter in s domain can be drawn, as shown in Figure 3. On d-axis, the input of this system is v_{dN}, the output is v_{od}, and the shortest path is shown in the red dotted line. There are two integrators on this path, so the the d-axis system is a two-order model. Similarly, the system on the q-axis is also a two-order model.

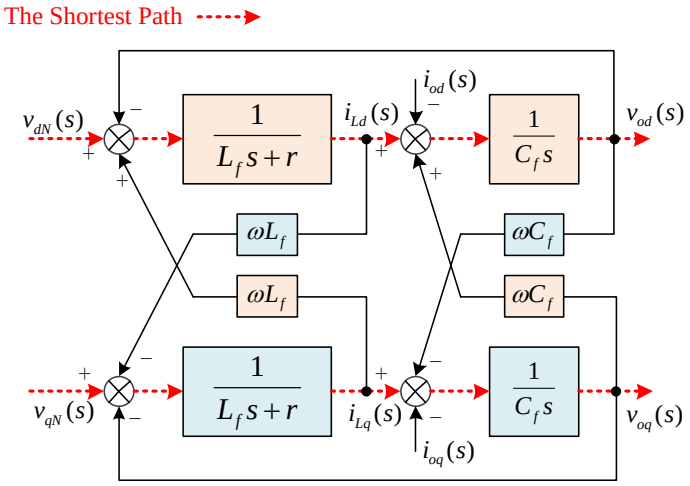


Figure 3. The shortest path of LC inverter model in s domain.

The system (3) can be written as a second-order plant in the time domain:

$$\begin{cases} \ddot{v}_{od} = bv_{dN} + f_d, \\ \ddot{v}_{oq} = bv_{qN} + f_q, \end{cases} \tag{12}$$

where $b = \frac{1}{L_f C_f}$, it is the input gain of two integrators; f_d and f_q are the contributions to the output of something other than the input on the shortest path, they be called as total disturbance. The total disturbance includes external disturbances and internal disturbances, such as device parameter fluctuation, load changes, unmodelled dynamics, etc.

In order to simplify ADRC structure, Zhiqiang Gao uses linear gain instead of nonlinear gain, namely LADRC. In this way, the number of parameters is reduced, greatly simplifying the tuning process and providing convenience for engineering applications.

For system (12), a two-order LADRC controller can be designed in Figure 1. LADRC consists of the linear extended state observer (LESO) and the linear state error feedback law (LSEF). LESO is responsible for accurately estimate the total disturbance. The LSEF is responsible for realization of the

desired signal by using a feedback controller, such as linear PD. Hence, the effect of LADRC largely depends on the estimation accuracy of the total disturbance.

The controller form of d-axis and q-axis is the same, so plant (12) can be rewritten as a universal two-order state space model:

$$\begin{cases} \dot{x}_1(t) = x_2(t), \\ \dot{x}_2(t) = bu(t) + f(t), \\ y(t) = x_1(t), \end{cases} \tag{13}$$

where $y(t)$ represents the output voltage v_{odq}, it is defined as the first state $x_1(t)$ as usual; the second state $x_2(t)$ is derivative of $x_1(t)$, which is $\dot{v}_{odq}$; $f(t)$ represents the total disturbance, which including the variations of the output inductance.

Letting a extended state $x_3(t) = f_{dq}(t)$, the extended state system can be obtained:

$$\begin{cases} \dot{x}_1(t) = x_2(t), \\ \dot{x}_2(t) = x_3(t) + bu(t), \\ \dot{x}_3(t) = \dot{f}(t), \\ y(t) = x_1(t). \end{cases} \tag{14}$$

Hence, the LESO can be written as:

$$\begin{cases} e(t) = z_1(t) - x_1(t), \\ \dot{z}_1(t) = z_2(t) - \beta_1 e(t), \\ \dot{z}_2(t) = z_3(t) - \beta_2 e(t) + bu(t), \\ \dot{z}_3(t) = -\beta_3 e(t), \end{cases} \tag{15}$$

where $z_i(t)$ is the estimated value of $x_i(t)$, β_i is the observer gain $(i = 1, 2, 3)$. With appropriate selection of β_i, the $z_i(t)$, will track $x_i(t)$. The transfer function of the three-order ESO is given by

$$\begin{cases} G_{eso1}(s) = \frac{z_1(s)}{y(s)} = \frac{\beta_1 s^2 + \beta_2 s + \beta_3}{s^3 + \beta_1 s^2 + \beta_2 s + \beta_3}, \\ G_{eso2}(s) = \frac{z_2(s)}{y(s)} = \frac{\beta_2 s^2 + \beta_3 s}{s^3 + \beta_1 s^2 + \beta_2 s + \beta_3}, \\ G_{eso3}(s) = \frac{z_3(s)}{y(s)} = \frac{\beta_3 s^2}{s^3 + \beta_1 s^2 + \beta_2 s + \beta_3}. \end{cases} \tag{16}$$

The observer gains can be selected by bandwidth-parameterization method [31], such that all the observer eigenvalues are placed at $-\omega_o$, then $\beta_1 = 3\omega_o$, $\beta_2 = 3\omega_o^2$, $\beta_3 = \omega_o^3$. Denote ω_o as the observer bandwidth.

Base on the estimation of the state of the system, the linear PD controller is used to track the reference value $r(t)$ and the estimation of the total disturbance is subtracted from PD control law to compensate the disturbance. Hence, in the s domain the transfer function of the LSEF can be expressed as:

$$u(s) = \frac{u_0(s) - z_3(s)}{b}, \tag{17}$$

$$u_0(s) = k_p[r(s) - z_1(s)] - k_d z_2(s). \tag{18}$$

The parameters k_p and k_d can also be selected by bandwidth-parameterization method, generally $k_p = 2\omega_c$, $k_d = \omega_c^2$. Denote ω_c as the observer bandwidth.

Substitute (15) into controlled plant results in:

$$\dot{x}_2 = u_0 - z_3 + f. \tag{19}$$

Thus, the total disturbance will be eliminated once z_3 is approximately equal to f.

To obtain the transfer function of the LADRC controller, combine (16)–(18):

$$u(s) = G_{ur}(s)r(s) - G_{uy}(s)y(s), \tag{20}$$

where

$$G_{ur}(s) = \frac{k_p}{b}, \tag{21}$$

$$G_{uy}(s) = \frac{k_p G_{eso1}(s) + k_d G_{eso2}(s) + G_{eso3}(s)}{b} \tag{22}$$

And then, the stability of LADRC controller and virtual harmonic impedance will be proved in the Section 4.

4. Stability and Disturbance Rejection Analysis

In this section, the stability of the fundamental voltage control loop and the harmonic compensation loop is proved. Furthermore, a disturbance rejection analysis regarding to variations of the output LC filter parameters is shown.

The block diagram of the fundamental voltage control loop transfer function under no load conditions is shown in Figure 4. Where $v_o(s)$ is the voltage of loads, which is $y(s)$ of transfer function (20). $r(s)$ is the reference voltage and $v_N(s)$ is the voltage generated by the inverter. The output signal of LADRC controller is denoted as $v_f(s)$ (d-axis has the same form as the q-axis), which is $u(s)$ of transfer function (20). $G_{LC}(S)$ is the LC filter transfer function, $G_{PWM}(s)$ is the relationship between $v_N(s)$ and $v_f(s)$. $G_{ur}(s)$ and $G_{uy}(s)$ are given by transfer function (21) and (22) respectively.

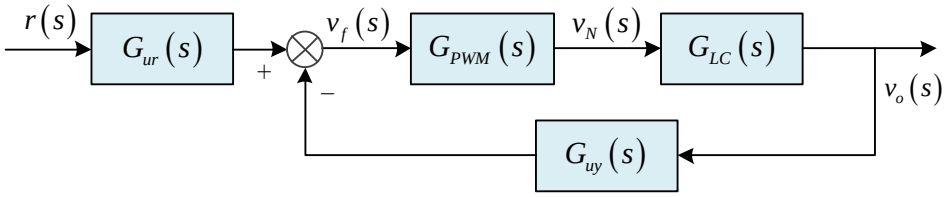


Figure 4. The transfer function of the fundamental voltage control loop.

Due to the no load conditions, the i_{ok} in the model (1) is equal to zero, then the transfer function between $v_o(s)$ and $v_N(s)$ can be written as:

$$G_{LC}(s) = \frac{v_o(s)}{v_N(s)} = \frac{1}{L_f C_f s^2 + r C_f s + 1}. \tag{23}$$

In this paper, according to the state space averaging method, the switching function of the IGBT is linearized, and the pulse width modulation method is adopted. The relationship between the modulation signals $v_f(s)$ and the inverter generated voltage $v_N(s)$ can be regarded as an one-order inertia unit:

$$G_{PWM}(s) = \frac{v_N(s)}{v_f(s)} \frac{v_{dc}}{2v_{tri}(Ts+1)}, \tag{24}$$

where v_{tri} is the amplitude of the triangle wave, v_{dc} is the DC voltage. By combining (21)–(24), the transfer function of the fundamental voltage control loop can be expressed as:

$$G_{sys1}(s) = \frac{v_o(s)}{r(s)} = \frac{G_r(s)}{1 + G_y(s)}, \tag{25}$$

where

$$G_r(s) = G_{ur}(s)G_{PWM}(s)G_{LC}(s), \tag{26}$$

$$G_y(s) = G_{uy}(s)G_{PWM}(s)G_{LC}(s). \tag{27}$$

Letting $L_f = 2.5$ mH, $C_f = 4.7$ µF, $r = 1.5$ Ω, $b = \frac{1}{L_f C_f}$, $k_p = \omega_c^2$, $k_d = 2\omega_c$, $\omega_c = 200$, $\beta_1 = 3\omega_o$, $\beta_2 = 3\omega_o^2$, $\beta_3 = \omega_o^3$, $\omega_o = 5\omega_c$, $v_{dc} = 30$ V, $v_{tri} = 12.5$ V, $T = 0.0001$ s . The frequency response of $G_{sys1}(s)$ can be obtained, as shown in Figure 5.

As can be seen from the Bode plot, the phase margin of $G_{sys1}(s)$ is 82 deg at 12.6 Hz and the amplitude margin is 42.4 dB at 390 Hz. Moreover, systems with phase margins greater than 45 deg in engineering experience have good dynamic performance. Therefore, the stability and dynamics of the fundamental voltage control loop are excellent.

The proposed strategy adds a virtual harmonic impedance branch to the fundamental voltage control loop, similar to the feedforward-feedback composite control method. Therefore, based on the stability analysis of the feedback loop, the frequency response of the feedforward loops needs to be analyzed.

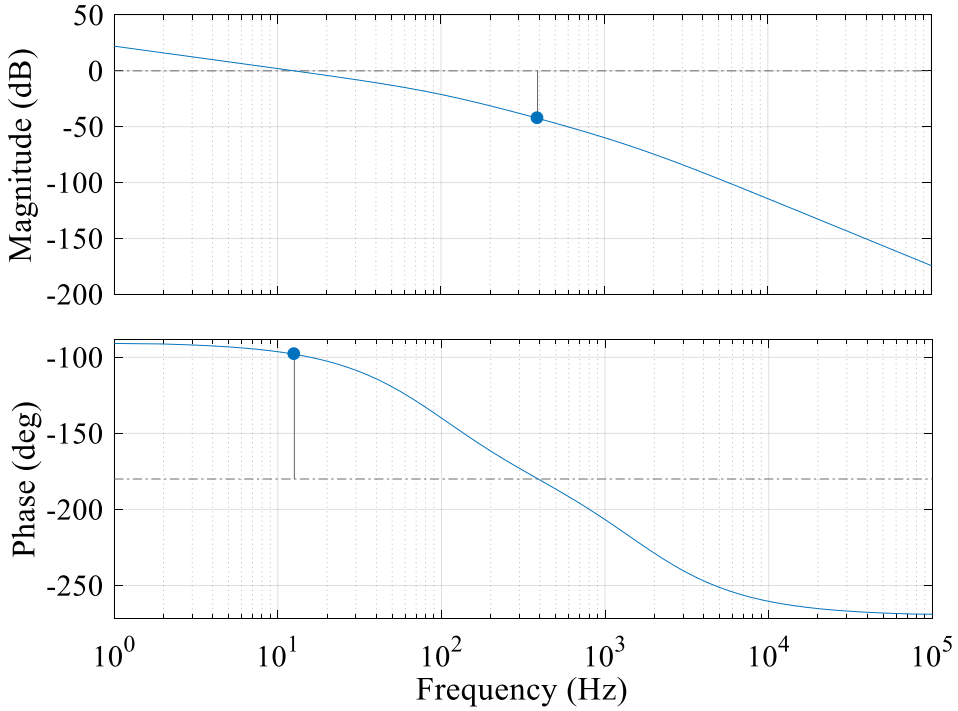


Figure 5. Bode plot of the transfer function of the fundamental voltage control loop.

The block diagram of the transfer function of multiple virtual harmonic impedances in parallel is shown in Figure 6, where v_h is the total harmonic voltage drop shaped by harmonic currents and virtual harmonic impedances, $Z_{hn}(s)$ is the nth virtual harmonic impedance.

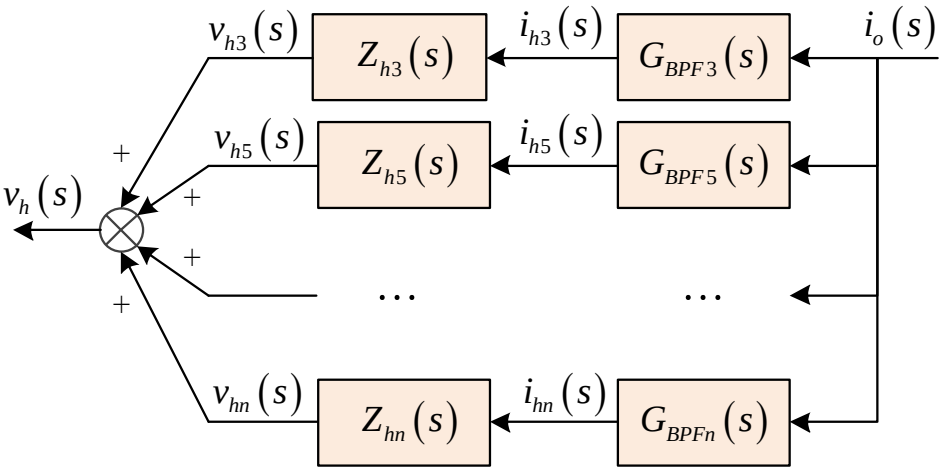


Figure 6. The transfer function of the harmonic compensation loop.

The premise of harmonic compensation using virtual harmonic impedance is the extraction of harmonic components in the current signal. To simplify the analysis, the extraction process is approximated as a bandpass filter $G_{BPFn}(s)$ designed at the harmonic frequencies ω_n that need to be compensated:

$$G_{BPFn}(s) = \frac{k\omega_n s}{Qs^2 + \omega_n s + Q\omega_n^2}, \tag{28}$$

where ω_n is the center frequency of the extracted harmonic components, k is the gain of center frequency, Q is the quality factor. The transfer function of the virtual harmonic impedance is G_{sys2}, which can characterize the relationship between $i_o(s)$ and $v_h(s)$. By combing (9) and (28), the transfer function of this loop can be obtained:

$$G_{sys2}(s) = \sum_{i=3}^{n} Z_{hi}(s) G_{BPFi}(s). \tag{29}$$

Due to the $6k \pm 1$ times harmonics are the main components of harmonic current under the nonlinear loads, and the harmonic content is attenuated with the increase of harmonic frequency, this paper selects the 5th, 7th, 11th and 13th harmonics for compensation.

Letting $k = 1.5$, $Q = 15$, $R_{h5} = R_{h7} = R_{h11} = R_{h13} = 1.5\ \Omega$, $L_{h5} = 3.927$ H, $L_{h7} = 5.498$ H, $L_{h11} = 8.639$ H, $L_{h13} = 10.210$ H. The frequency response of each individual virtual harmonic impedance is shown in Figure 7. It can be seen that the designed virtual harmonic impedance (including the extraction units) has a high positive gain at 250 Hz, 350 Hz, 550 Hz, and 650 Hz, respectively.

Frequency responses of (29) ($i = 5, 7, 11, 13$) and proposed method are shown in Figure 8. It can be seen from Figure 8b that the whole system exhibits a larger negative gain at the selected frequency, which reduces the equivalent output impedance of the system, so the harmonic voltage drop generated by the harmonic current is reduced. This conclusion proves the validity of the feedforward loop.

Furthermore, as virtual harmonic impedance effectiveness depends on the real inductance value L_f', in this section a sensitivity analysis regarding to variations of the output LC filter parameters is shown in Figure 9. It can be seen that compared with PI, the use of LADRC makes the output inductance fluctuation have less influence on the harmonic compensation effect. Authors in [21] indicates that the value of parasitic resistance has a weak influence on the virtual harmonic impedance, so the influence of parasitic resistance in this paper is not studied.

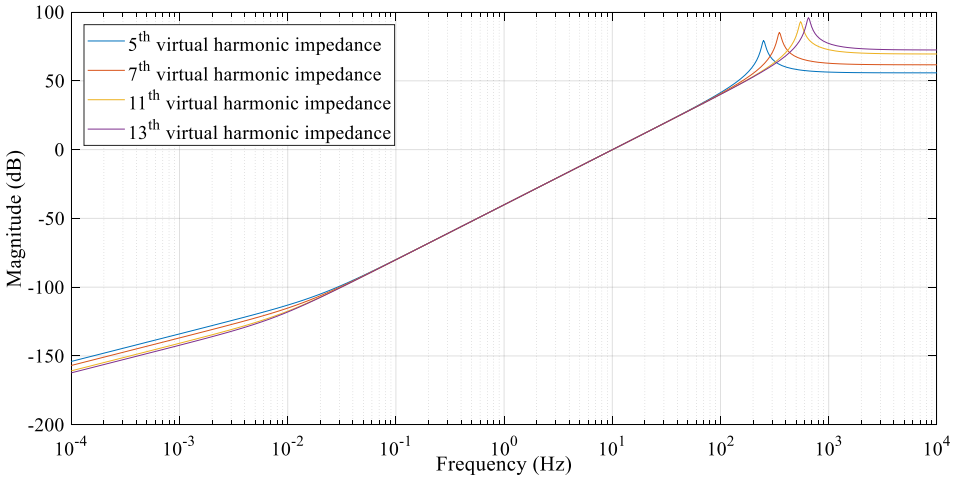


Figure 7. Frequency response of virtual harmonic impedance.

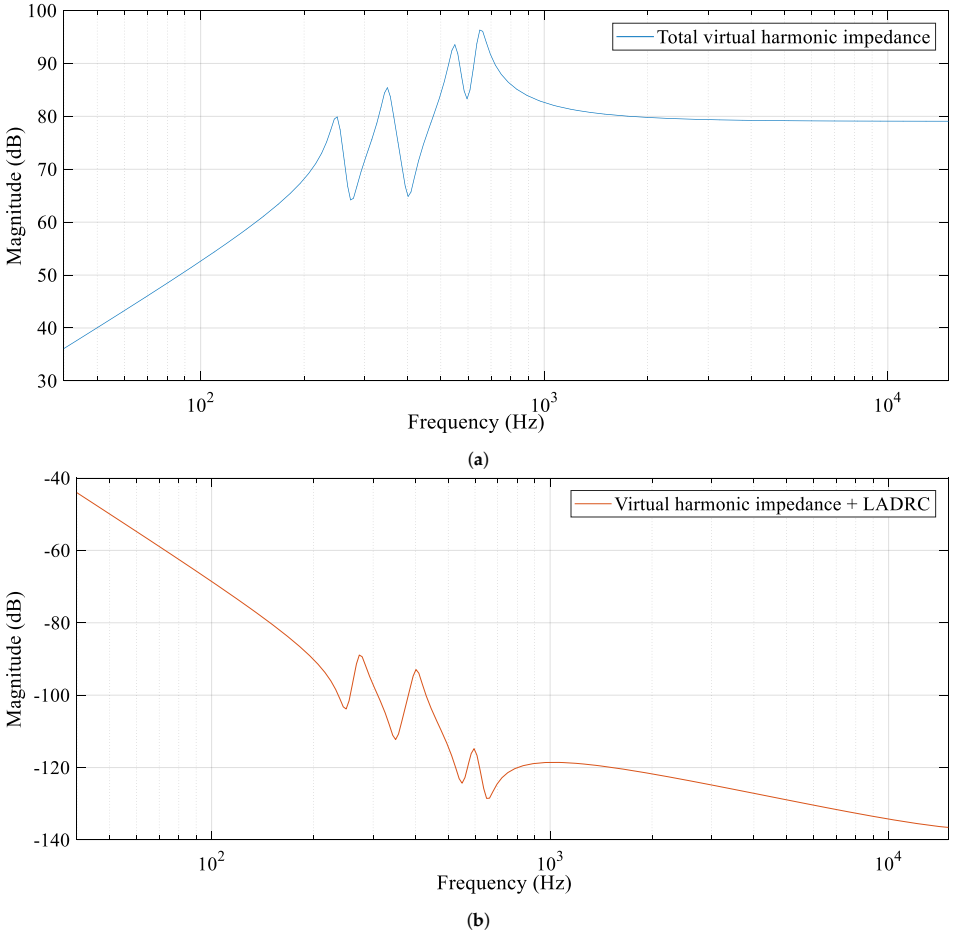


Figure 8. (**a**) Frequency response of total virtual harmonic impedance. (**b**) Frequency response of proposed method.

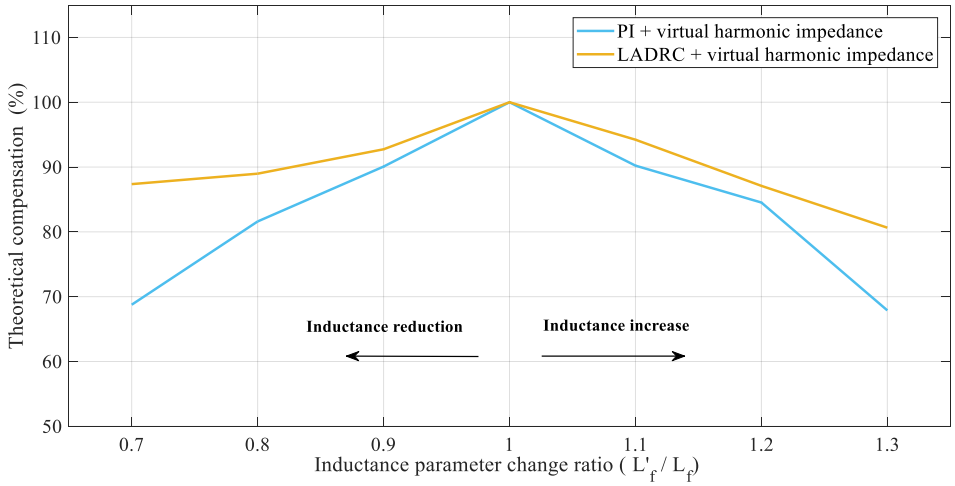


Figure 9. The relationship between theoretical compensation degree and parameter variation.

5. Simulation and Experimental Results

In order to verify the performances of the proposed strategy, simulations and experiments are designed in this section. A LC type three-phase three-leg inverter of Figure 1 is used, and a resistive linear load and a non-linear load are respectively connected to the output terminals. The nonlinear load consists of a three-phase full-bridge rectifier and a series resistive and inductive load. In order to ensure the reasonableness of the comparison, when the virtual harmonic impedance parameters of the design are unchanged, the PI and LADRC algorithms are used in the fundamental voltage control loop respectively.

5.1. Simulation Results

The circuit parameters and controller parameters in the simulation are shown in Tables 1 and 2. In order to prove the performance of the proposed strategy, two comparative simulations were designed, as shown in Tables 3, and the results are shown in Figure 10. It can be seen that the transient response speed of LADRC is faster than PI. The transition time with PI is 0.07 s (3.5 periods), while the transition time with LADRC is 0.03 s (1.5 periods), and the rapidity of the system is increased by 57.1%. This is mainly because there are two coupling terms in the dual-loop PI control strategy in the *dq* synchronous reference frame. When the system state changes, the *d*-axis and the *q*-axis will affect each other. However, the LADRC controller puts coupling terms into the total disturbance to achieve decoupling and improve response speed.

Table 1. Circuit Parameters.

Symbol	Quantity	Value
f_s	Switching frequency	10 kHz
f_1	Fundamental frequency	50 Hz
L_f	Filter inductance	2.5 mH
r	Parasitic resistance	1.5 Ω
C_f	Filter capacitance	4.7 μF
L_{nl}	Inductance of nonlinear load	9 mH
R_{nl}	Resistance of nonlinear load	28 Ω
R_l	Resistance of linear load	73 Ω

Table 2. Controller Parameters in Simulations.

Virtual Harmonic Impedance				LADRC				Dual-Loop PI Control	
Symbol	**Value**	**Symbol**	**Value**	**Symbol**	**Value**	**Symbol**	**Value**	**Symbol**	**Value**
L_{h5}	3.927 H	R_{h5}	1.5 Ω	ω_c	2500	ω_o	1.25×10^4	$k_{p-innerloop}$	1
L_{h7}	5.498 H	R_{h7}	1.5 Ω	k_p	6.25×10^6	k_d	5000	$k_{i-innerloop}$	10
L_{h11}	8.639 H	R_{h11}	1.5 Ω	β_1	3.75×10^4	β_2	4.69×10^8	$k_{p-outerloop}$	1.5
L_{h13}	10.210 H	R_{h13}	1.5 Ω	β_3	1.95×10^{12}	b	8.51×10^7	$k_{i-outerloop}$	10

Table 3. The Design of Simulations.

No.	0–0.05 s	0.05–0.20 s
Simulation 1	Open loop	PI + virtual harmonic impedance
Simulation 2	Open loop	LADRC + virtual harmonic impedance

In addition, in the condition of open loop and two strategies, harmonic contents are shown in Table 4. It can be seen that when open loop control, THD (only the first 20 harmonics are counted) is 9.35%, and the 5th, 7th, 11th, and 13th harmonic contents are 5.00%, 3.50%, 2.90%, and 2.95%, respectively. With the proposed strategy, the THD is reduced to 2.30%, the harmonic compensation is up to 75.4%, and each compensated component is reduced to less than 1% (the 5th, 7th, 11th, and 13th harmonic contents is reduced to 0.87%, 0.60%, 0.85%, and 0.74%, respectively). If PI control is used in the fundamental voltage control loop, the THD drops to 2.50%, and the compensated harmonic components are also significantly reduced. It can be confirmed that the virtual harmonic impedance designed in this paper can effectively compensate for harmonics at selected frequencies.

Although PI and LADRC have almost the same suppression of selected harmonics, it can be seen from Figure 10a that when PI is used, there are many high-frequency components in the output voltage. Larger inductance parameters are often used to eliminate this ripple, but the inductance is proportional to its volume, which takes up more space and results in additional power loss and expense.

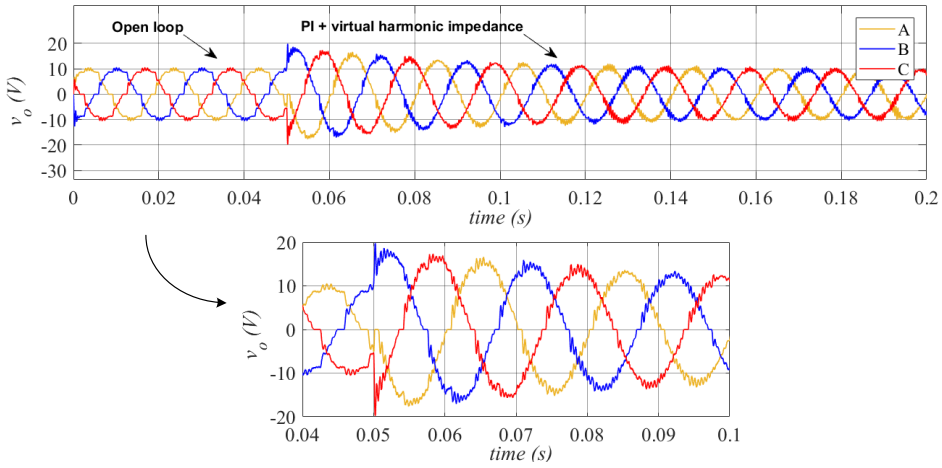
Table 4. HarmonicContents.

Harmonic Order	without Compensation	Simulation 1	Simulation 2
THD	9.35%	2.58%	2.30%
5th	5.00%	1.08%	0.87%
7th	3.50%	0.74%	0.60%
11th	2.90%	0.91%	0.85%
13th	2.95%	0.79%	0.74%

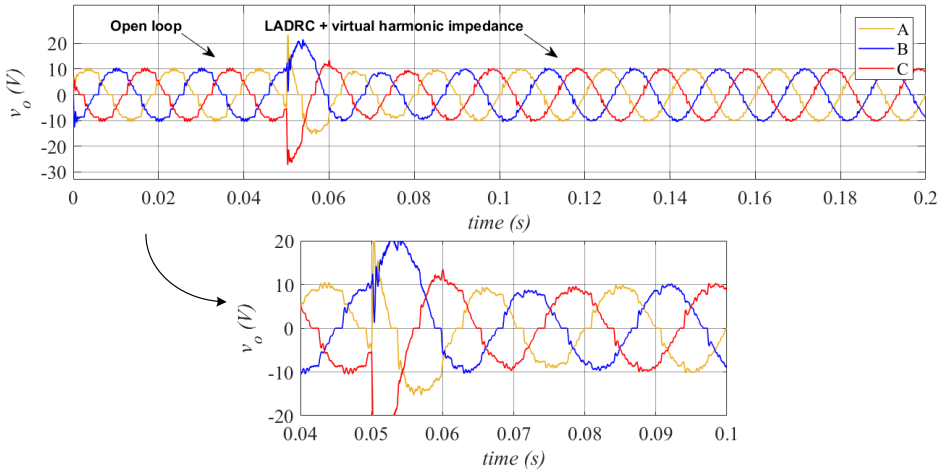
5.2. Experimental Results

Compared with the controller without disturbance rejection function, the advantage of LADRC is mainly reflected in the fact that the fluctuation of the filter inductance parameter has less influence on the compensation effect of virtual harmonic impedance loops. This feature of LADRC is not significant in the ideal environment for simulation. However, since the actual physical system is a non-ideal system, the fluctuation of the inductance L_f cannot be eliminated, so this feature is meaningful in the physical experiment.

In this paper, an experimental platform is built (shown in Figure 11), which includes an LC type three-phase three-leg inverter, a Speedgoat real-time controller, a Faith DC power source, a three-phase linear Load, a nonlinear load, a Hioki power quality analyzer and a four-channel oscilloscope. The Speedgoat real-time controller consists of a real-time target machine, an input module and an output module. The hardware circuit topology and parameter selection of inverter are the same as those in Section 5.1. The circuit parameters and the controller parameters are shown in Tables 1 and 5, respectively.



(**a**)



(**b**)

Figure 10. (**a**) The output voltage with PI and virtual harmonic impedance. (**b**) The output voltage with LADRC and virtual harmonic impedance.

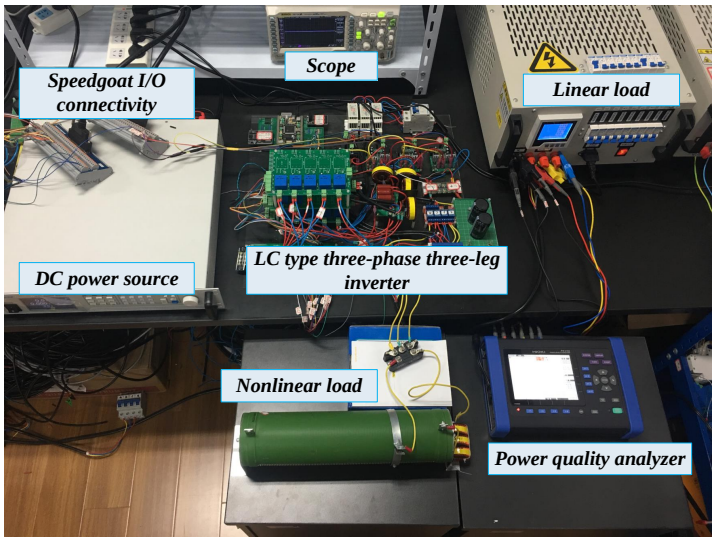


Figure 11. Experimental platform.

Table 5. Controller Parameters in Experiments.

Virtual Harmonic Impedance				LADRC				Dual-Loop PI Control	
Symbol	**Value**	**Symbol**	**Value**	**Symbol**	**Value**	**Symbol**	**Value**	**Symbol**	**Value**
L_{h5}	3.797 H	R_{h5}	1.257 Ω	ω_c	400	ω_o	2000	$k_{p-innerloop}$	3
L_{h7}	7.878 H	R_{h7}	1.389 Ω	k_p	1.60×10^5	k_d	800	$k_{i-innerloop}$	5
L_{h11}	9.880 H	R_{h11}	1.488 Ω	β_1	6000	β_2	1.20×10^7	$k_{p-outerloop}$	0.2
L_{h13}	13.880 H	R_{h13}	1.769 Ω	β_3	8.00×10^9	b	8.51×10^7	$k_{i-outerloop}$	10

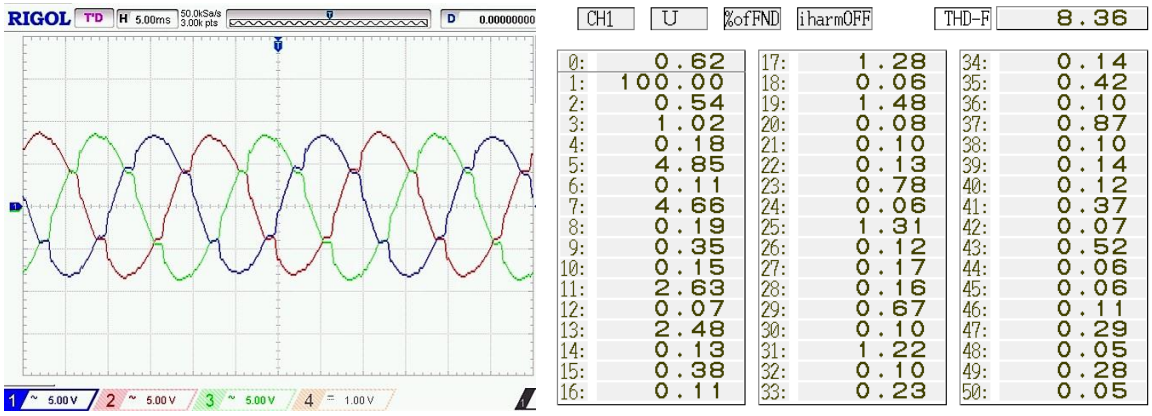
Three sets of experiments were designed for comparison in this section, as shown in Table 6.

Table 6. The Design of Experiments.

No.	Fundamental Voltage Control Loop	Harmonic Compensation Loops
Experiment 1	Open loop	Open loop
Experiment 2	Dual-loop PI control	Virtual harmonic impedance
Experiment 3	LADRC	Virtual harmonic impedance

As shown in Figure 12a, there is a significant distortion of the output voltage waveforms under the open loop control. In addition, due to the non-ideality of the three-phase linear load, there is a slight unbalance in the output voltage. Figure 12c shows the output voltage waveforms under the control of the dual-loop PI at the fundamental voltage control loop. As can be seen from this figure, the harmonics in the output voltage are partially compensated, but there are still significant distortions. Moreover, the three-phase unbalance has not improved. Figure 12e shows the output voltage waveforms under the proposed control strategy. It can be seen that the harmonics of the output voltage are significantly compensated. Moreover, the three-phase unbalance problem has also been improved. The reason for this effect is that LADRC can estimate and compensate for disturbances in the system and unmodelled dynamics (i.e., total disturbance f), thereby improving power quality.

The compensation effect of the three experiments can be measured by the power quality analyzer, as shown in Figure 12b,d,f. It can be seen that although experiment 2 has some compensation on the 5th, 7th, 11th and 13th harmonics, it raises the distortion content near the compensated harmonics, for example, 6th, 8th, and 12th. The main reason is that the inductance value fluctuates during the operation of the physical system, which results in the virtual harmonic impedance compensation effect are not ideal. Since LADRC estimates and compensates for the parameter fluctuation of the filter inductor, the effect of the virtual harmonic impedance is less sensitive to the inductance variation. The proposed strategy shows better harmonic compensation effect. The proposed control strategy reduced THD from 8.36% to 4.37%, and the 5th, 7th, 11th and 13th harmonics decreased from 4.85%, 4.66%, 2.63%, and 2.48% to 0.90%, 0.94%, 0.85%, and 0.81%, respectively.



(**a**) (**b**)

Figure 12. *Cont.*

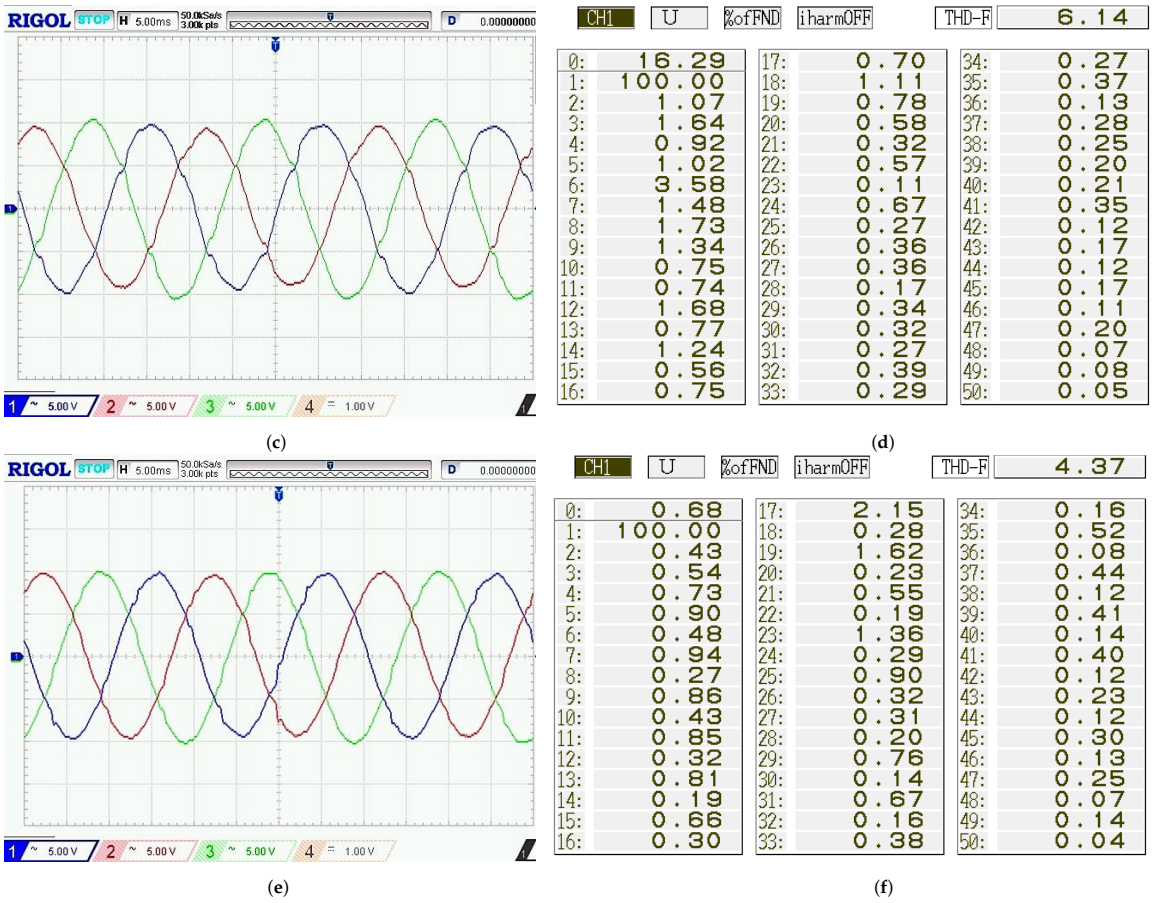


Figure 12. (**a**) Output voltage waveforms for experiment 1. (**b**) THD for experiment 1. (**c**) Output voltage waveforms for experiment 2. (**d**) THD for experiment 2. (**e**) Output voltage waveforms for experiment 3. (**f**) THD for experiment 3.

6. Discussion

This paper proposes a harmonic compensation strategy based on LADRC and virtual harmonic impedance for LC type three-phase three-leg inverter.

Firstly, the proposed strategy considers the fluctuation of the filter inductance as the unmodelled dynamics of the system and reduces the sensitivity of the virtual harmonic impedance to the filter inductance through the observation and compensation of LADRC, which is shown in Figure 9. Therefore, when the filter inductance fluctuates in actual engineering, the proposed control strategy has better harmonic compensation effect. In Section 5.2 demonstrates this advantage through physical experiments.

Secondly, the proposed method does not require additional compensation devices, which reduces power loss and cost, and has higher economic and application value. As the harmonic compensation loops increases, the computational complexity of the method will increase, but this method is a flexible and effective strategy for specific compensation of harmonic components with higher content in the output voltage.

Finally, the proposed strategy can decouple the system model and eliminate the interaction between the d-axis and the q-axis to improve the transient recovery speed. Decoupling the model reduces the number of sensors in physical experiments, from 9 sensors (with PI controllers) to 6 sensors (with LADRC controllers).

In summary, the proposed method has better control performance and engineering applicability, which is verified by simulations and experiments. However, as the number of harmonics that need to

be compensated increases, the amount of calculation also increases. In the next studies, a harmonic full compensation strategy with less computational complexity can be studied.

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