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A Full-bridge Director Switches based Multilevel Converter with DC Fault Blocking Capability and Its Predictive Control Strategy

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Abstract: Voltage source converter-based high-voltage direct current transmission system (VSC-HVDC) technology has been widely used. However, traditional half-bridge sub module (HBSM)-based module multilevel converter (MMC) cannot block a DC fault current. This paper proposes that a full-bridge director switches based multi-level converter can offer features such as DC side fault blocking capability and is more compact and lower cost than other existing MMC topologies. A suitable predictive control strategy is proposed to minimize the error of the output AC current and the capacitor voltage of the sub-module while the director switches are operated in low-frequency mode. The validity of the proposed topology and control method is demonstrated based on simulation and experimental studies.

Keywords: multilevel converter; DC side fault blocking; predictive control

1. Introduction

The modular multilevel converter (MMC) has been accepted as a suitable solution for high-voltage and high-power application fields due to several inherent features [1–8]. However, blocking the DC fault current becomes a difficult problem because the anti-parallel diodes are still conducting after the insulated-gate bipolar transistors (IGBTs) of HBSM are turned off [9].

To solve this problem, recent research has highlighted a number of interesting converter topologies which combine the features of the multilevel output AC voltage waveform and DC fault blocking capacity [9–22]. Full-bridge sub-module (FBSM) based MMC (F-MMC) is a basic configuration with DC fault current blocking capacity [10,11]. However, the DC fault current blocking capability comes at a cost of nearly doubling power losses and number of semiconductor devices. Some other type of sub-module is proposed instead of FBSM to make a further optimization in reducing the number of IGBTs, such as a clamp double sub-module (CDSM) proposed in [14,15] and a three-level cross-connected sub-module (TCSM) proposed in [16]. Several hybrid MMC topologies are also proposed, based on HBSM and those various types of sub-module [9,12,13,16–19,23], for further reducing the cost and loss on the premise of having the DC fault blocking capacity, such as hybrid MMC based on CDSM and HBSM (CH-MMC). However, there are still some drawbacks, for example, as they are composed of a large number of sub-modules, the system needs to be more complicated and the converter station bulkier.

The alternate-arm multilevel converter (AAMC) based on the hybrid topology of HBSM and director switches is proposed in [20–22]. The AAMC further improves the traditional MMC topology by cutting the number of sub-modules, reducing DC bus voltage, and gaining the ability to block DC fault currents [22]. However, some features still have the possibility for further

optimization, such as the size and cost of the overall system. One of the main technical challenges associated with the control of such a director switches based multilevel converter is to simultaneously keep the capacitor voltages balanced and provide good output current tracking performance, while the director switches keep switching in low frequency.

In order to further optimize the size and cost of the voltage source converter-based high-voltage direct current transmission system (VSC-HVDC) converter with the blocking ability of DC faults, this paper proposes a full bridge director switches based alternate-arm multi-level converter (FA-MMC) and a corresponding control strategy:

1. The size and cost of the overall system can be significantly reduced by reducing the number of SM capacitors, IGBTs, and other related devices. In addition, an FA-MMC retains the ability to block DC-side faults since it uses H-bridge SMs as the AAMC.
2. Similar to AAMC, a systematic multi-objective control method is needed for this kind of topology to minimize the error of output AC current and the capacitor voltage of the sub-module while the director switches are operated in low-frequency mode. A suitable predictive control strategy for this kind of topology is presented in this paper to achieve the flexibility to include the previously mentioned multiple system requirements.

2. Proposed Topology

2.1. Structure and Basic Operation

The basic circuit configuration of full-bridge director switches based modular multi-Level converter (FA-MMC) proposed in this paper is shown in Figure 1b. The proposed topology consists of a stack of H-bridge SMs and four director switches (S_1 – S_4) made of series IGBTs or IGCTs. The ability of DC-side fault blocking is still retained since the H-bridge SMs structure is the same as the AAMC.

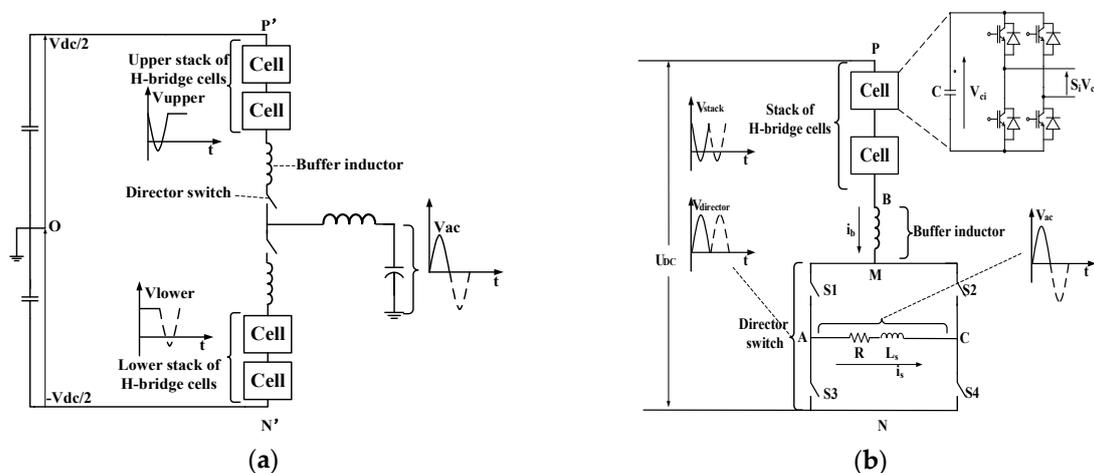


Figure 1. Schematic representation of the two topologies: (a) alternate-arm multilevel converter (AAMC); (b) full bridge director switches based alternate-arm multi-level converter (FA-MMC).

The voltage of the director switches ($U_{director}$ in Figure 1b) is equal to the DC voltage (U_{DC} in Figure 2) plus the voltage produced by the stack of H-bridge SMs which can be considered as only one controllable voltage source. Therefore, the voltage of director switches can be adjusted flexibly so that the switching of S_1 – S_4 can switch at near to zero voltage. The ideal voltage waveform is shown in Figure 2a.

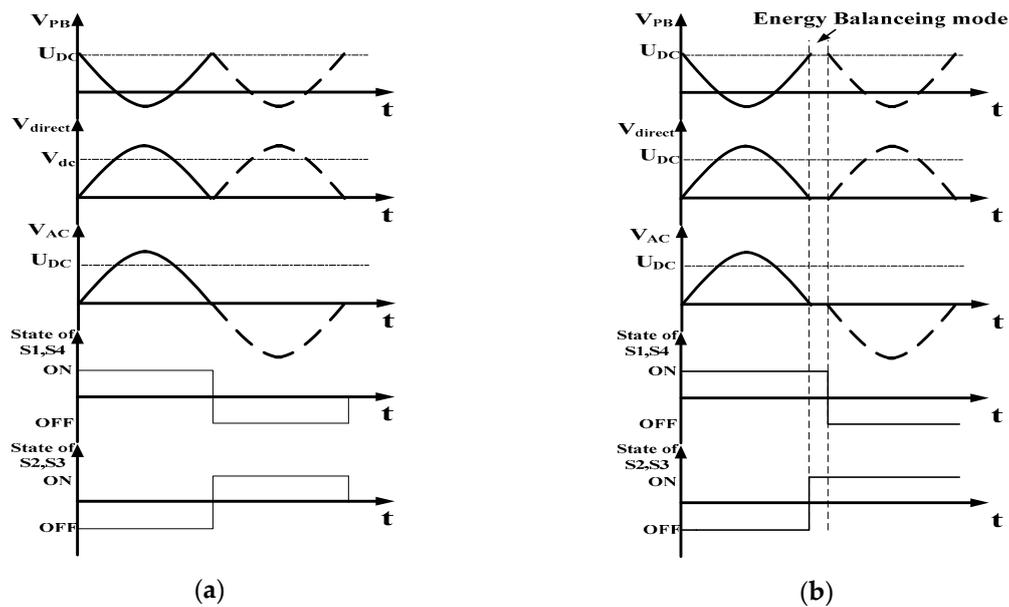


Figure 2. The voltage waveform and state of S1–S4: (a) without energy balance mode; (b) with energy balance mode.

The working cycle of S₁–S₄ is synchronized with the output AC voltage. S₁ and S₄ are conducting and S₂ and S₃ are turned off while the output AC voltage (U_{ac} in Figure 1b is in its positive half-cycle, in contrast, S₂ and S₃ are conducting and S₁ and S₄ are turned off while the output AC voltage is in its negative half-cycle. This ensures that the four director switches can switch at low-frequency and at the point of zero-voltage-crossing as shown in Figure 2a. These features lead to low switching losses, and low demand for dynamic voltage sharing at the switching instant of the series switches, so that the system design has been simplified.

2.2. Energy Balance

When the AC current flows through the stack of H-bridge sub module. In order to ensure the continuous operation of the system, the energy balance of the stack of H-bridges should be guaranteed. The amount of energy transferred from the AC side (E_{AC}) and going to the DC side (E_{DC}) should be equal over half the fundamental period and is given as

$$E_{AC} = \frac{3}{2} \frac{\hat{V}_{AC} \hat{I}_{AC}}{\omega} \pi \cos(\varphi), \tag{1}$$

$$E_{DC} = \frac{6U_{DC} \hat{I}_{AC}}{\omega} \cos(\varphi), \tag{2}$$

For E_{AC} to equal E_{DC} , the relationship between the DC voltage magnitudes and AC voltage magnitudes mentioned in Equations (1) and (2) can be given as

$$U_{DC} = \frac{\pi}{4} \hat{V}_{AC}, \tag{3}$$

However, since the converters can't operate in the perfect given by Equation (3), an energy balancing strategy should be used.

Reference [22] presented two methods to achieve energy balance for AAMCs that can also be used in this topology: Overlap current and third harmonic current injection. In this paper the overlap current method is used to extend the period when the current directed from S₁ and S₄ to S₂ and S₃ is extended and S₁–S₄ are all conducting. The overlap current is used to exchange power between

the sub module capacitors and the DC bus. The load current is only slightly affected, since the overlap time is very short and the inductance can smooth the change in current. Considering its effect on the grid current, the overlap time is determined to be less than 0.8 ms.

3. Predictive Control Strategy

The control strategy of the proposed topology requires minimizing the error of the output current and DC voltage in each sub module, and, meanwhile, the director switches switching should be operated in low-frequency and zero-voltage switching mode.

3.1. Dynamic Modeling

Based on Figure 2, the governing equations of the single-phase FA-MMC can be shown as follows:

$$U_{DC} - V_{PB} - L_b \frac{di_b}{dt} = V_{MN} \quad (4)$$

$$V_{AC} = L_s \frac{di_s}{dt} + Ri_s \quad (5)$$

$$V_{AC} = S_d V_{MN} \quad (6)$$

As presented in Section 2, the value of L_b is small and the voltage on it can be ignored; S_1 – S_4 have five switching state combinations depending on a switching function S_d as shown in Table 1.

Table 1. Switching states of director switches.

Mode	S_d	S_1	S_2	S_3	S_4	Output Voltage (V_{AC})
Basic Operating Mode	1	ON	OFF	OFF	ON	V_{MN}
	−1	OFF	ON	ON	OFF	$−V_{MN}$
	0	ON	ON	ON	ON	0
Energy Balancing Mode	0	ON	ON	OFF	OFF	0
	0	OFF	OFF	ON	ON	0

The output voltage of each H-bridge sub module is equal to V_{ci} (capacitor voltage of the i th sub module ($i = 1, 2, \dots, n$)), $−V_{ci}$, or zero, depending on the switching states, and depends on a switching function S_i

$$S_i = \begin{cases} 1 \\ 0 \\ -1 \end{cases} \quad (i = 1, 2, \dots, n). \quad (7)$$

The relationship between V_{ci} and U_{DC} is formalized as

$$\sum_{i=1}^n V_{ci} \approx U_{DC} \quad (8)$$

Based on Equation (16) and the basic principle, V_{PB} is formalized as

$$\sum_{i=1}^n S_i V_{ci} = V_{PB} \quad (9)$$

The dynamic capacitor voltage of the cells of the H-bridge sub module in Figure 1b is formalized as

$$S_i i_b = C \frac{dV_{ci}}{dt} \quad (10)$$

The relationship of currents is and i_b in Figure 1b, which was also indicated by the switching function S_d according to Table 1, is expressed as

$$i_b = S_d i_s \quad (S_d = 1 \text{ or } -1) \quad (11a)$$

$$L \frac{di_b}{dt} = U_{DC} - \sum_{i=1}^n S_i V_{ci} \quad (S_d = 0) \quad (11b)$$

The switching states of director switches operate in an energy balancing mode, as mentioned in Table 1. As discussed previously, the current i_b flows through the stack of H-bridge sub modules, buffer inductor, and director switch to the DC side, charging or discharging the capacitor of the H-bridge sub modules.

Only considering the basic operating mode, substituting Equations (5), (6), (9), and (11a) into (4), a dynamic model of the single-phase proposed topology in basic operating mode can be expressed as

$$S_d (U_{DC} - \sum_{i=0}^n S_i V_{ci} - S_d L_b \frac{di_s}{dt}) = L_s \frac{di_s}{dt} + R i_s \quad (12)$$

where $S_d = 1$ or -1 . Equation (12) can be simplified as

$$L \frac{di_s}{dt} = S_d (U_{DC} - \sum_{i=0}^n S_i V_{ci}) - R i_s \quad (13)$$

where $L = L_b + L_s$.

3.2. Proposed Predictive Control

The predictive control strategy is proposed in this section based on the dynamic model of the FA-MMC presented above, the three primary targets of the predictive control strategy is achieved as follows:

3.2.1. AC-Side Current Control

Assuming a sampling period of T_s , a discrete-time model of the FA-MMC AC-side current in basic operating mode based on Equation (3) is calculated by

$$\frac{L}{T_s} (i_s(k+1) - i_s(k)) = S_d(k) (U_{DC}(k) - \sum_{i=0}^n S_i(k) V_{ci}(k)) - R i_s(k) \quad (14)$$

the value of S_d could be assumed as a constant value during a short sampling period of T_s . $i_s(k)$ is the actual AC current at time k and $i_s(k+1)$ is the predicted AC current at time $k+1$, $U_{DC}(k)$ can be considered as a constant value if the DC side voltage is controlled. Finally, $V_{ci}(k)$ is the capacitor voltage of the sub module i at time k .

To reduce the error between the predicted current and the reference current, a cost function associated with the current error is defined as

$$J_i = \left| i_{sref}(k+1) - i_s(k+1) \right| \quad (15)$$

where i_{sref} is the reference current and $i_s(k+1)$ is the predicted current obtained from Equation (14). Ideally, J_i will be equal to its minimum value of ($J_{min} = 0$ in Figure 4) if the AC-side current is controlled well.

3.2.2. Capacitor Voltage Balancing

Based on Equations (10) and (11), $V_{ci}(k+1)$ can be deduced as

$$V_{ci}(k+1) = V_{ci}(k) + \frac{S_i(k)S_d(k)i_s(k)}{C}T_s \quad (16)$$

where $V_{ci}(k)$ can be measured in real time. Another cost function for balancing the capacitor voltage of sub modules is given as

$$J_{vc} = \sum_{i=1}^n |V_{ci}(k+1) - V_{ciref}(k+1)| \quad (17)$$

where $V_{ciref}(k+1)$ is the reference DC capacitor voltage of sub module i (with i between 1 and n),

which can be equal to the average voltage of all cells (given as $\frac{\sum_{i=1}^n V_{ci}(k+1)}{n}$), and $V_{ci}(k+1)$ is a predicted value, which can be obtained from Equation (16).

Consequently, by adding the above cost function together a combined cost function, which can simultaneously achieve the two main control objectives mentioned above is given as the linear combination

$$J_{all} = \alpha J_i + \beta J_{vc} \quad (18)$$

where α and β are weighing factors, α is adjusted based on the cost contribution allocated to the error of AC-Side current, and β is adjusted based on the cost contribution allocated to the voltage deviations of sub module capacitors. The empirical method to determine the value of cost function is presented in [24].

Within each sampling and computing period T_s , the combined cost function J_{all} is re-calculated, and the best switching indicated to the minimum value for Equation (18) will be adopted for the current control cycle.

3.2.3. Director Switch Control

As presented in Figure 2a in Section 2.1, the state of director switches S_1 – S_4 at the next step should depend on the value of V_{AC} . According to Equation (5), the necessary value of V_{AC} at the current step can be expressed as

$$V_{AC}(k+1) = Ri_{sref}(k+1) + \frac{L_s}{T_s}(i_{sref}(k+1) - i_s(k)) \quad (19)$$

However, the fluctuation of $V_{AC}(k+1)$ due to differences between $i_{sref}(k+1)$ and $i_s(k)$ during zero voltage crossings will lead to high frequency repeated switching of S_1 – S_4 , resulting in an increase of switching losses.

Therefore, a director switch control strategy should be taken considering the need to

1. Add the energy-balancing mode ($S_d = 0$ in Table 1) in to achieve energy balancing of the stack of H-bridge by exchanging power with DC bus.
2. Avoid repeated switching of the director switches.

Replacing $i_s(k)$ by $i_{sref}(k)$, the necessary value of V_{AC} at the current step can be expressed as

$$V_{ACref}(k+1) = Ri_{sref}(k+1) + \frac{L}{T_s}(i_{sref}(k+1) - i_{sref}(k)) \quad (20)$$

where $i_{sref}(k)$ is the reference value of the current of the current step. Voltage $V_{ACref}(k+1)$, obtained by Equation (20), is a standard sine wave, which can avoid the fluctuation of $V_{AC}(k+1)$ due to differences between $i_{sref}(k+1)$ and $i_s(k)$ during zero voltage crossings. Finally, the implementation procedure of the proposed director switch control strategy is summarized in Part I of Figure 4. The schematic diagram of the control system is shown in Figure 3.

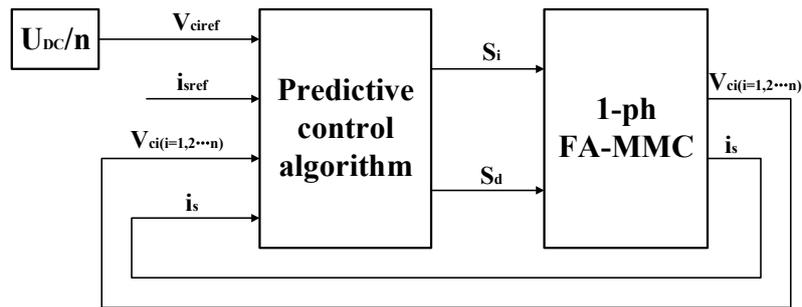


Figure 3. Schematic diagram of the control system.

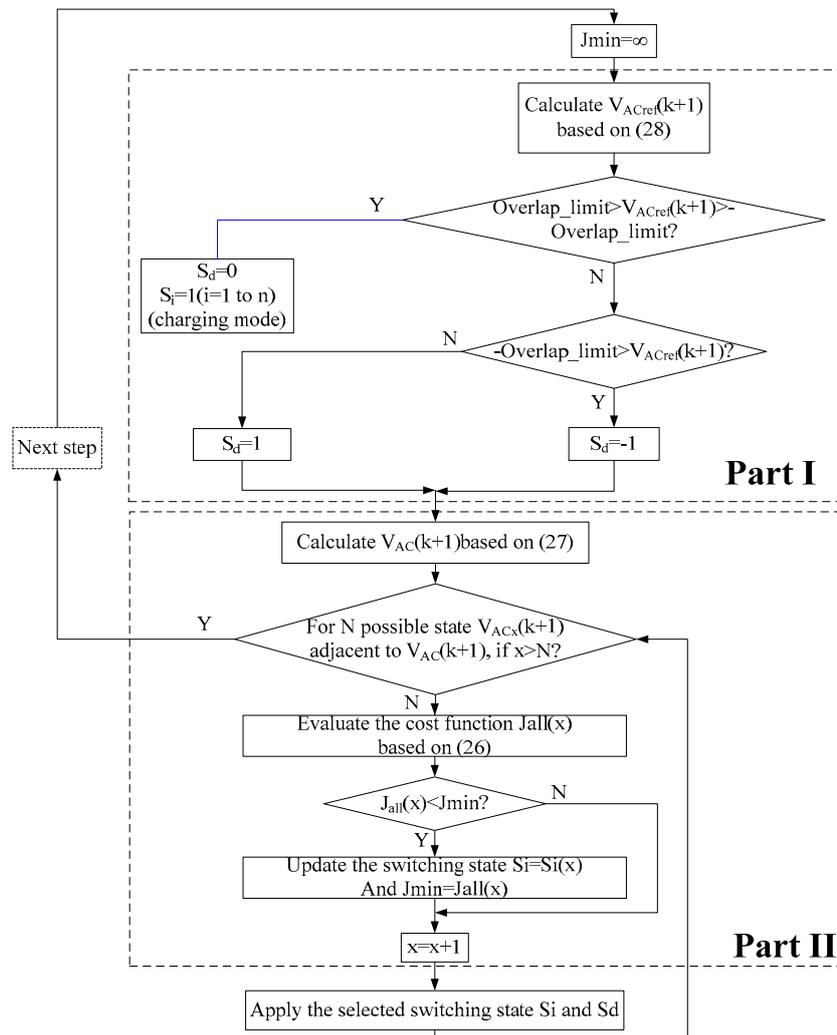


Figure 4. Block diagram of the predictive control strategy

4. Simulation Results

This section evaluates the performance of the proposed FA-MMC and control method with a simulation. The simulation parameters are given in Table 2.

Table 2. Parameters of the study system of Figure 1b.

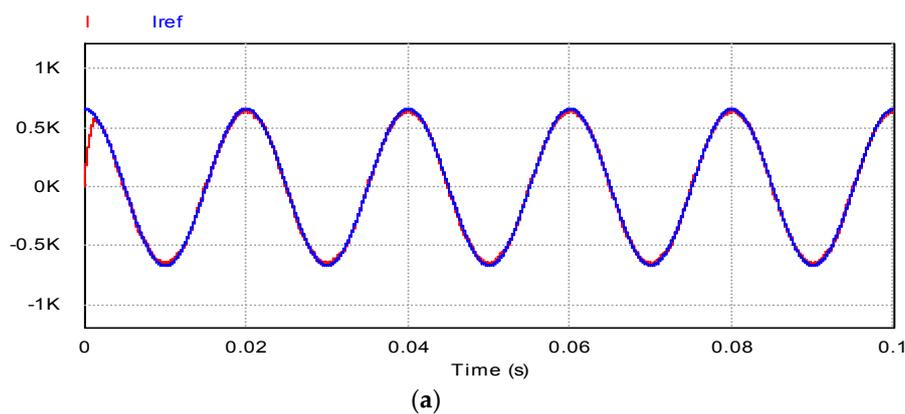
DC voltage U_{DC}	3000 V
Submodule capacitor C	3300 μ F
Load inductance L_s	3 mH
Buffer inductors L_b	0.1 mH
Load inductance R	6
Sampling period T_s	100 μ s
Nominal frequencies f	50 Hz
No. of cell in the stack of H-bridge cells	2

4.1. Operating Performance under a Steady-State Condition

Figure 5 shows the voltage of the stack of H-bridges cells, the voltage across the director switches S_1 – S_4 , and the AC output voltage while the load current tracks the reference in steady-state operation. The simulation results are consistent with the working principle of the topology described in Figure 1b of Section 2. The voltage waveforms appear staircased because there are only two cells, while they would more closely resemble a sine curve with an increase in the number of cells. Figure 6 shows that the capacitor voltages in the two cells are averaged well and mostly under the control of MPC in basic operating mode. Further, they get closer to the given value U_{DC}/n_{cell_FA} in energy-balancing mode.

Figure 7 shows the director switch control signal of S_1 – S_4 . It can be seen in Figure 7a that they all operated at a frequency of 100 Hz and achieved zero voltage switching under the director switch control strategy described in Part I of Figure 4. In contrast, when Part I of Figure 4 is removed, the director switch control signal, which is only determined by $V_{AC}(k+1)$, is shown in Figure 6b. The difference in responses occurs because $V_{ACref}(k+1)$ in Equation (20) is obviously a standard sine wave while the $V_{AC}(k+1)$ is repeatedly crossing the zero voltage point as shown in Figure 8. This demonstrates the effectiveness of the director switch control strategy.

Figure 9 reveals that the relation of the current across L_b (I_b in Figure 9) and the load current (I_s in Figure 9) is similar to Equation (11a) in basic operating mode. The current across L_b (I_b in Figure 9) becomes an overlap current that charges or discharges the capacitor of the cells when S_1 – S_4 are all conducting in energy balancing mode.

**Figure 5.** Cont.

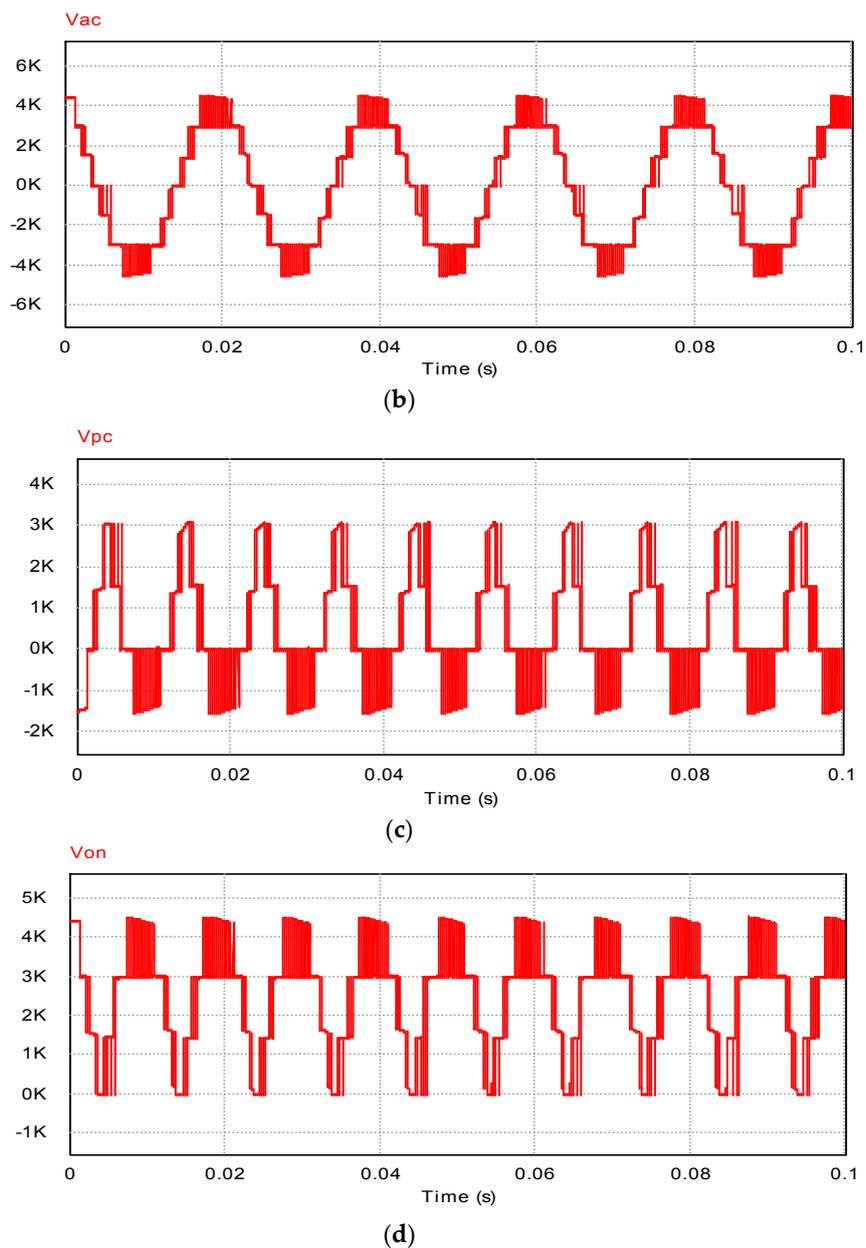


Figure 5. Simulation waveform of the single-phase FA-MMC in steady state operation: (a) Load current and reference current; (b) output AC voltage; (c) voltage of the stack of H-bridges; (d) voltage across the director switches S_1 – S_4 .

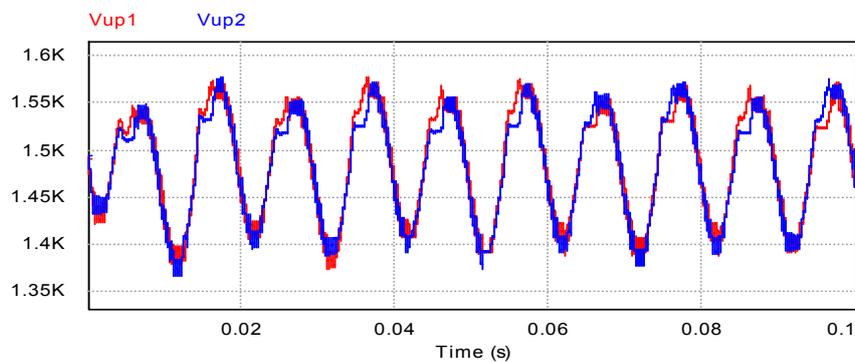


Figure 6. Capacitor voltages of the cells.

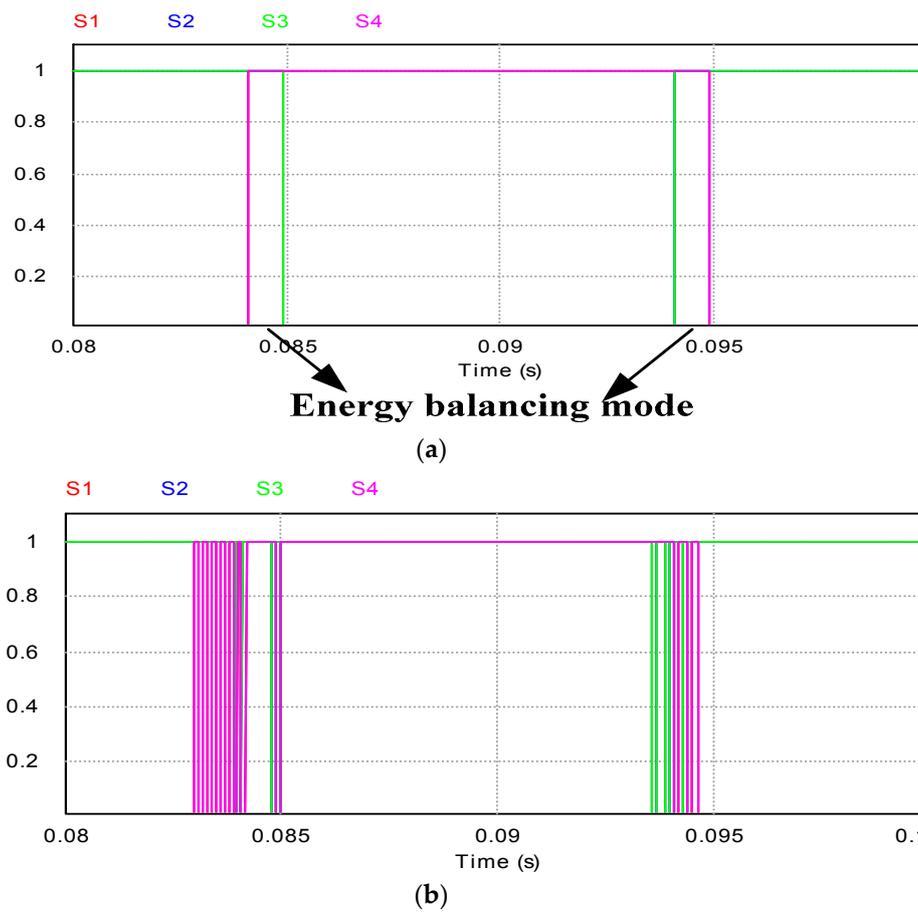


Figure 7. Director switch control signal of S₁–S₄: (a) Control signal based on $V_{acref}(t+T_s)$; (b) control signal based on $V_{ac}(t + T_s)$.

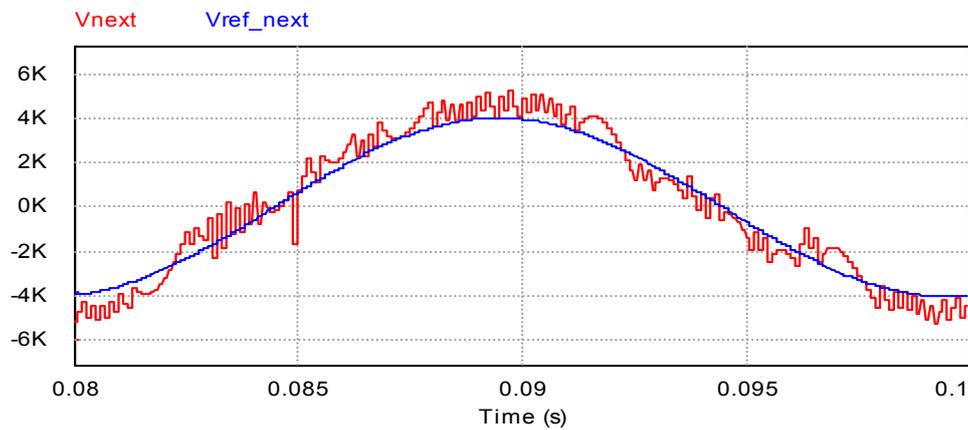


Figure 8. The waveforms of V_{ac} and V_{acref} .

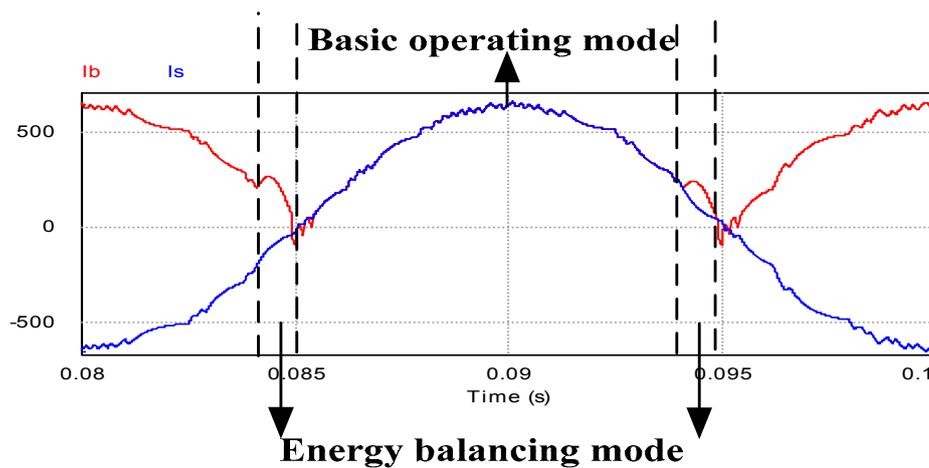


Figure 9. The waveforms of V_{ac} and V_{acref} .

4.2. Operating Performance under a Transient-State Condition

To test the dynamic performance, a sudden change in the reference current is set at 0.04 s, and the behavior of the system is shown in Figure 10. It can be seen that the current tracked the reference value well. The time of reference tracking (from 600 A to -600 A) is less than 0.01 ms as shown in Figure 10b, and the output AC voltage waveform is shown in Figure 11.

The capacitor voltage is shown in Figure 12. It can be seen that the capacitor voltage of the two sub-module remains balanced after a sudden change of load current. Figure 12b shows that there is a deviation in the beginning, but is averaged well immediately by the predictive control strategy after 1 ms.

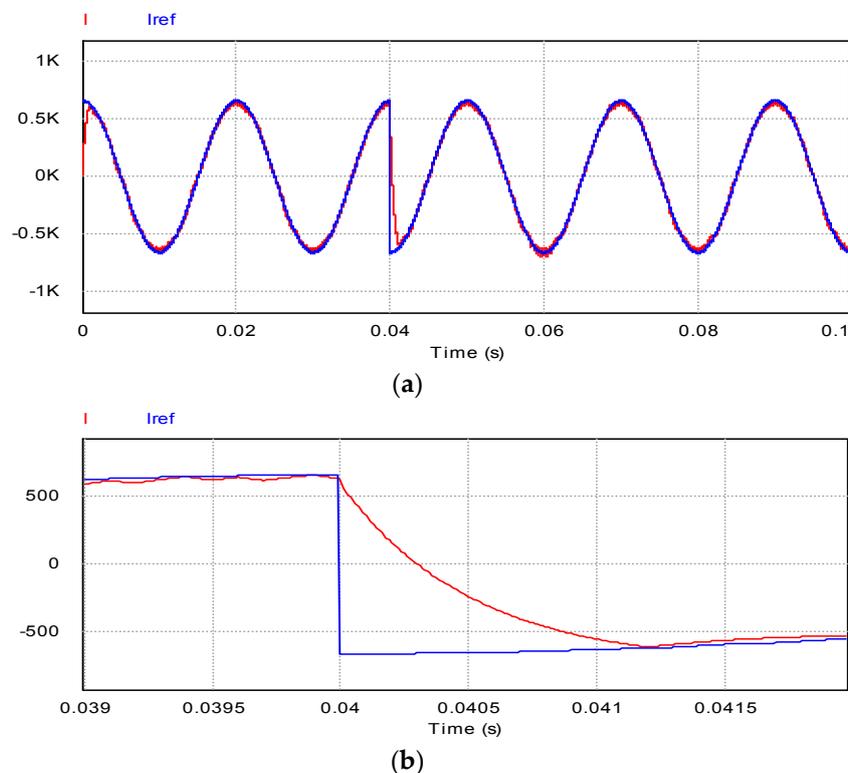
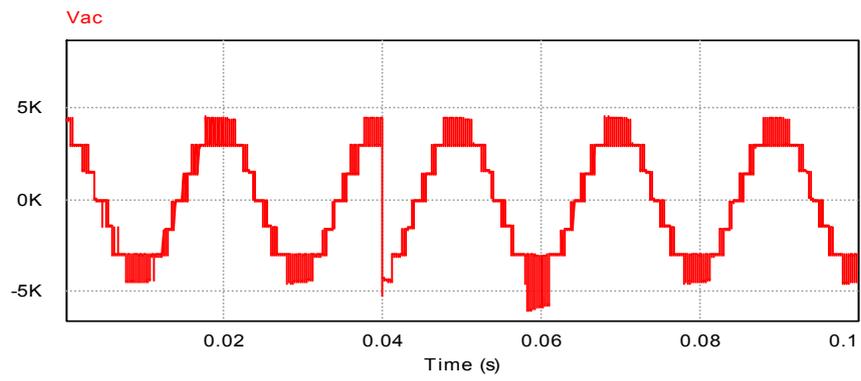
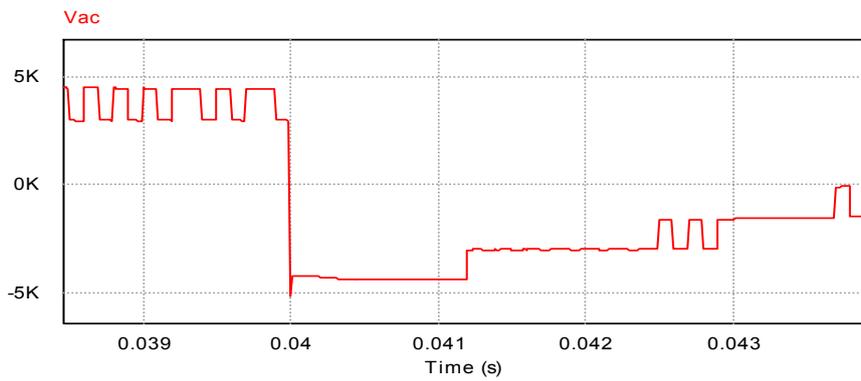


Figure 10. Load current for a sudden change: (a) reference current and actual load current; (b) Detail of the reference current and actual load current at the instant.

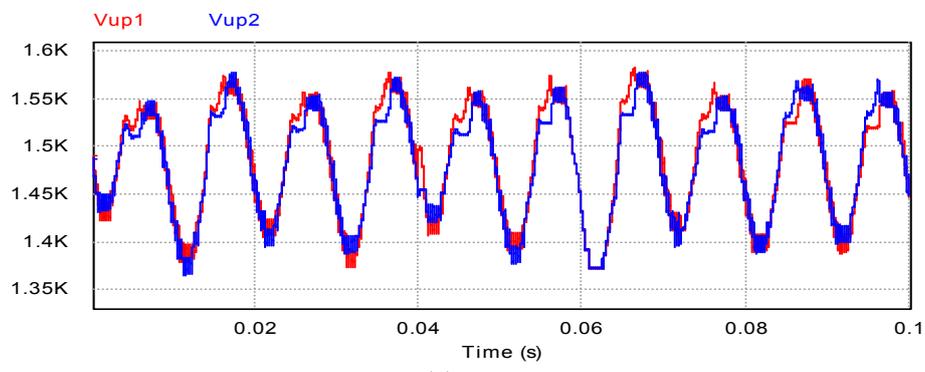


(a)

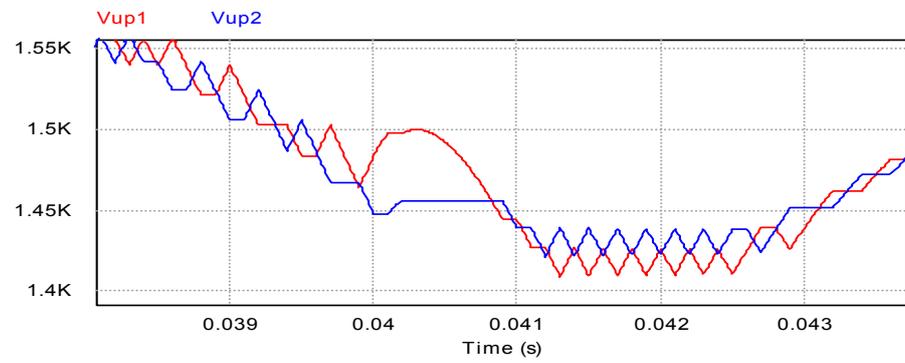


(b)

Figure 11. Output AC voltage waveforms: (a) Output AC voltage ; (b) detail of the output AC voltage at the instant.



(a)



(b)

Figure 12. Capacitor voltages of the sub-module.

Figure 13 shows the states of the director switches at the instant of the sudden change of load current, demonstrating that the director switches are controlled well and operated in low-frequency mode.

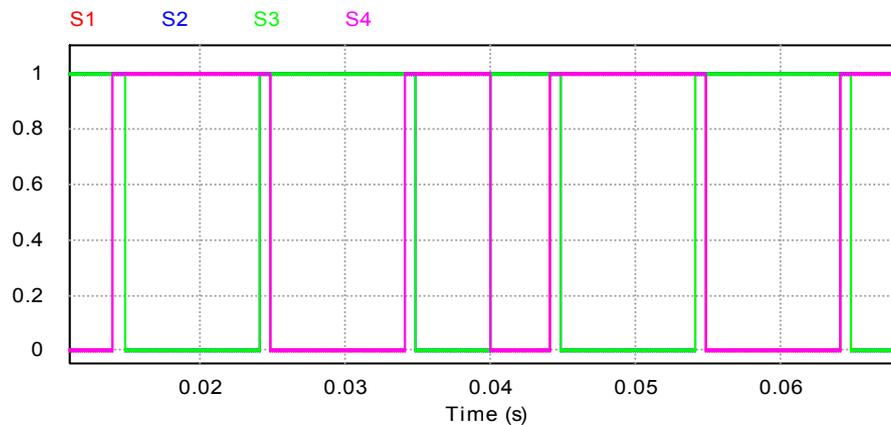


Figure 13. Control signal of S_1 – S_4 .

4.3. Operating Performance under a DC Fault

Having verified the normal operation of the converter, the model was tested under a DC fault. A three-phase model was built, and a DC fault was induced at 0.04 s. The blocking time is set to be 3 ms after the fault current is detected considering the sensor delay time. Figure 14 shows that the voltage of the cell capacitor is kept at 1.5 kV and the AC current follows the given value before 0.04 s. When a DC short-circuit happens at 0.04 s, the direction of current is reversed and the AC side current rises at first because during the sensor delay, the capacitors discharge and current flows from the AC side to the DC side. After 3 ms, when the converter station is blocked, the DC and AC side currents gradually reduce to zero along with the charging of the capacitor.

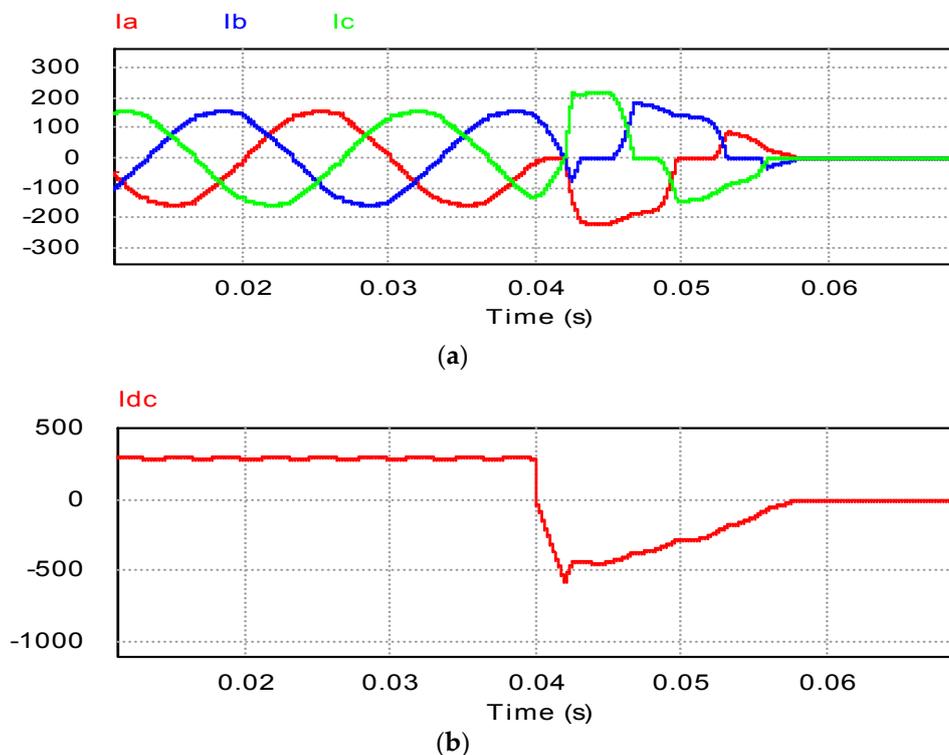


Figure 14. Cont.

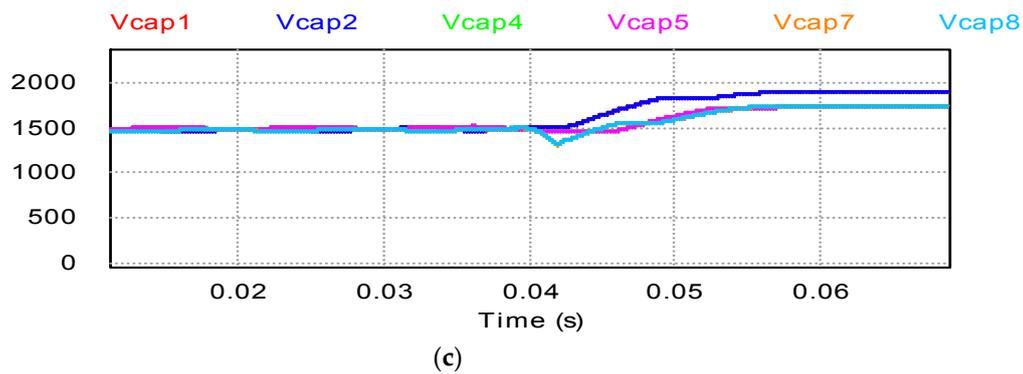


Figure 14. Current and voltage simulation waveforms of a DC fault: (a) AC current; (b) DC current; (c) capacitor voltages.

5. Experimental Results

Experiments on an FA-MMC-based inverter were also carried out to verify the proposed topology and test the predictive control strategy. The parameters for the experiment are listed in Table 3. A photo of the inverter is shown in Figure 15 and an IGBT is utilized as the power switch. The main control algorithms were implemented in a combination of a DSP and FPGA. The DC-link voltage was obtained via a three-phase autotransformer.

Table 3. Experiment parameters.

DC voltage U_{DC}	100 V
Submodule capacitor C	3300 μ F
Load inductance L_s	3 mH
Buffer inductors L_b	0.1 mH
Load inductance R	6
Sampling period T_s	100 μ s
Nominal frequencies f	50 Hz
No. of cell in the stack of H-bridge cells	2

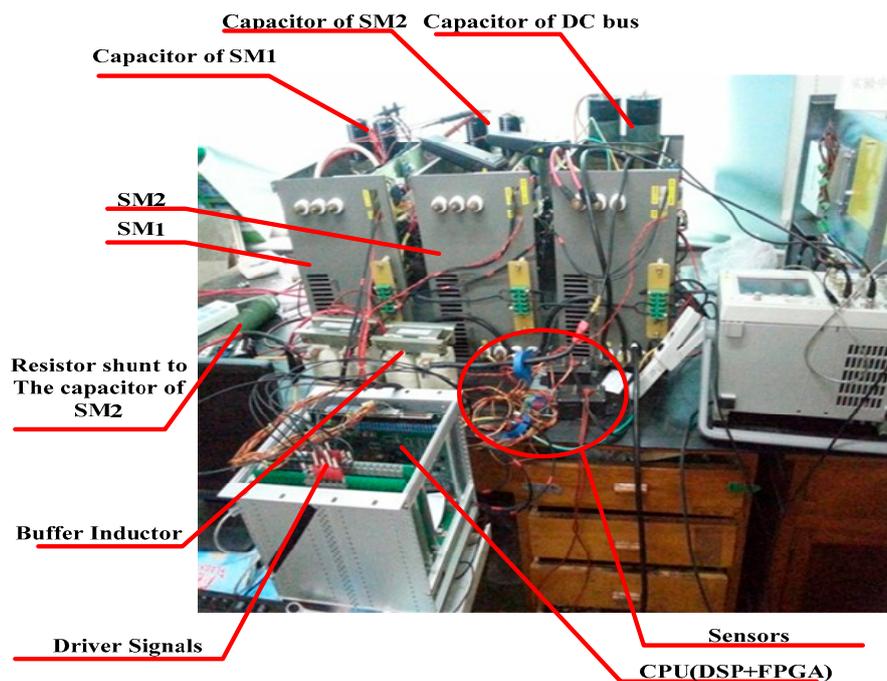


Figure 15. Photo of the modular multilevel converter (MMC)-based inverter for the experiment.

To test the system balance ability, a $100\ \Omega$ resistor was shunted to capacitor SM2. The topology worked in this unbalanced condition by appropriately setting the value of the weighting factor β , which is used to balance the capacitor voltage of the two SMs to zero. In this paper, we set the weighting factor α to a fixed value of 50, and set weighting factor β to 0 or 100 to compare the waveforms. Figure 16 shows the capacitor voltages of the two SMs. At first, the capacitor voltage of SM1 is lower than SM2, and the fluctuation is larger due to the unbalanced condition. After giving a suitable value to weighting factor β , each cell capacitor voltage is well regulated to their reference value and the fluctuation of the two cells is also the same.

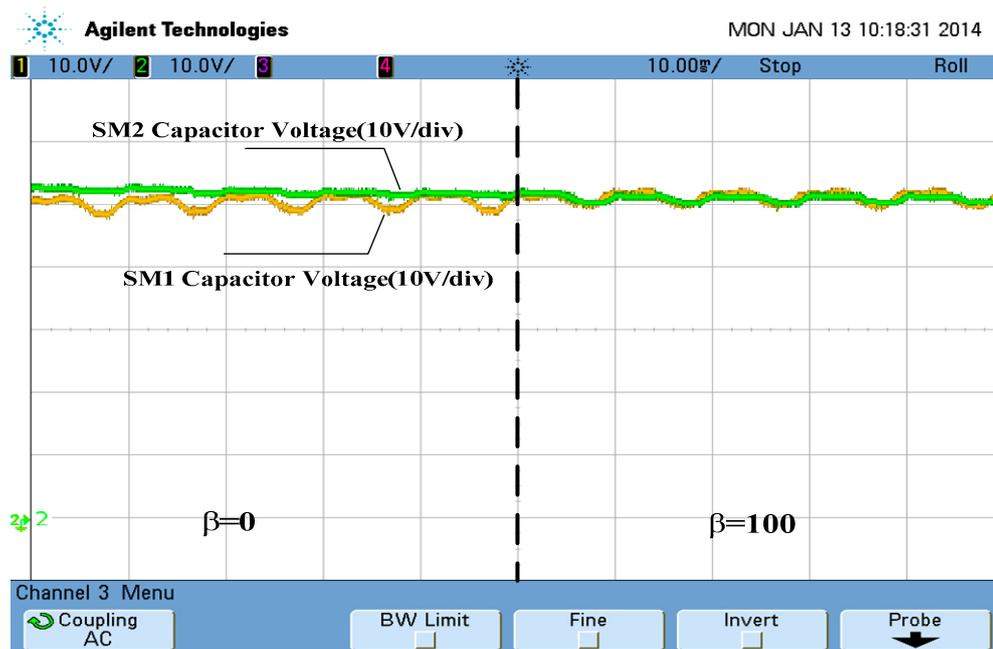


Figure 16. weighting factor β 's effects on the capacitor voltages.

Figures 17 and 18 show the output current and voltage of this topology, which are both measured during balanced and unbalanced operation. From Figure 18 we can see that the voltage ripple of the two cell capacitors does not affect the current, apparently due to the robustness of the predictive control. When the weighting factor β is set to 100, meaning that the capacitor voltage balance is considered as a control goal, only a slight distortion is introduced into the output current.

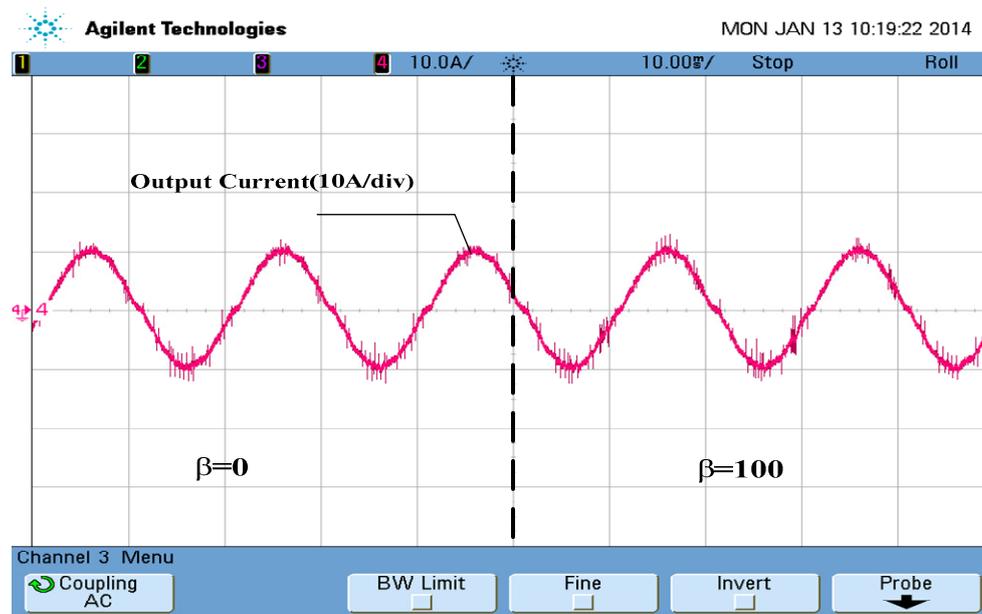


Figure 17. The waveform of the output current under balanced and unbalanced conditions.

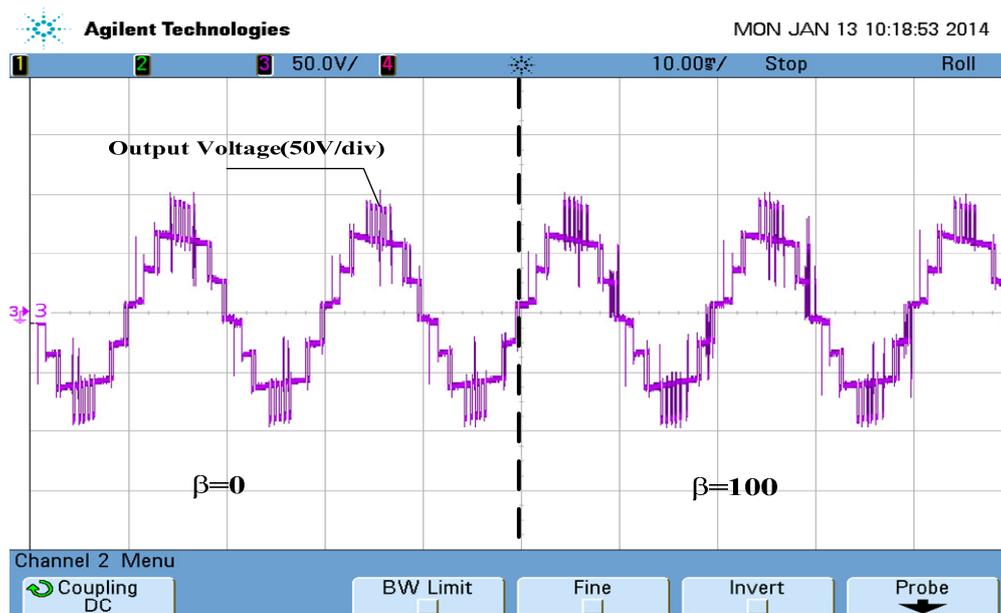


Figure 18. The waveform of the output voltage under balanced and unbalanced conditions.

To test the dynamic performance, the behavior of the FA-MMC and corresponding control method for a step in the angle of the reference current is shown in Figure 19. The waveforms show that the voltage changed quickly to drive the current to its new reference value and that the current is well-tracked. Figure 19 also shows that the dynamic capacitor voltage waveform is not influenced by the step in the angle of the reference current. Figure 20 shows a detailed view of the output voltage and current for a step in the angle of the reference current. The reference tracking of the proposed method that considered the possible switching states adjacent to $V_{AC}(k + 1)$ is fast, because extreme voltage changes are possible. The results are similar to simulation results.

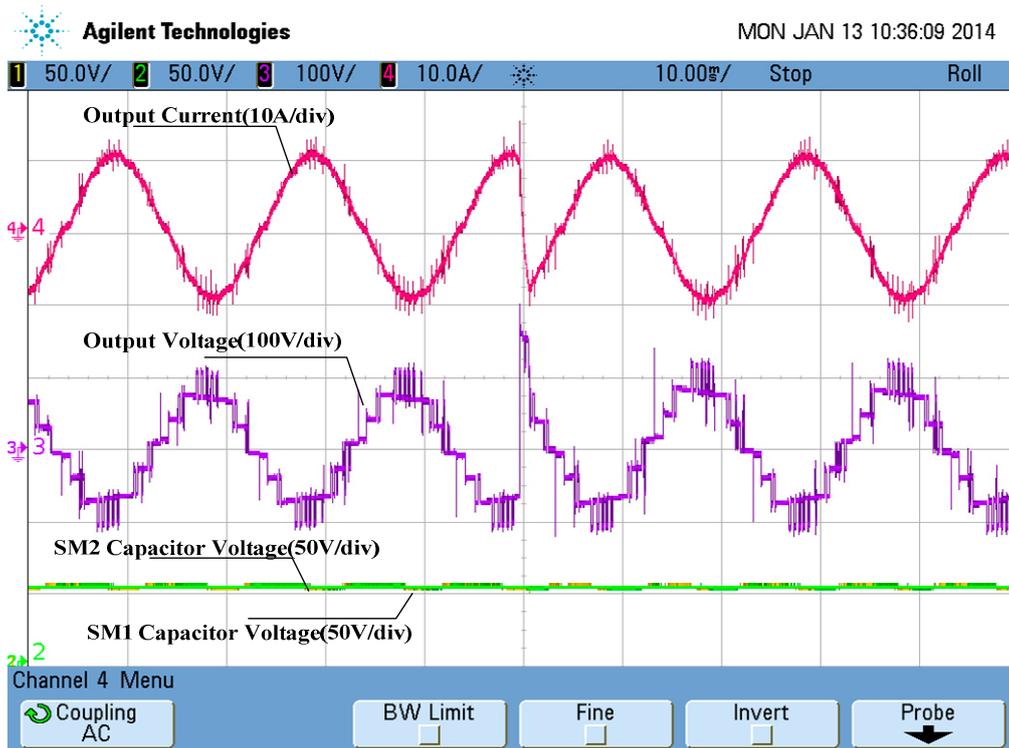


Figure 19. Waveform of the voltage and current for a step in the angle of the reference current.

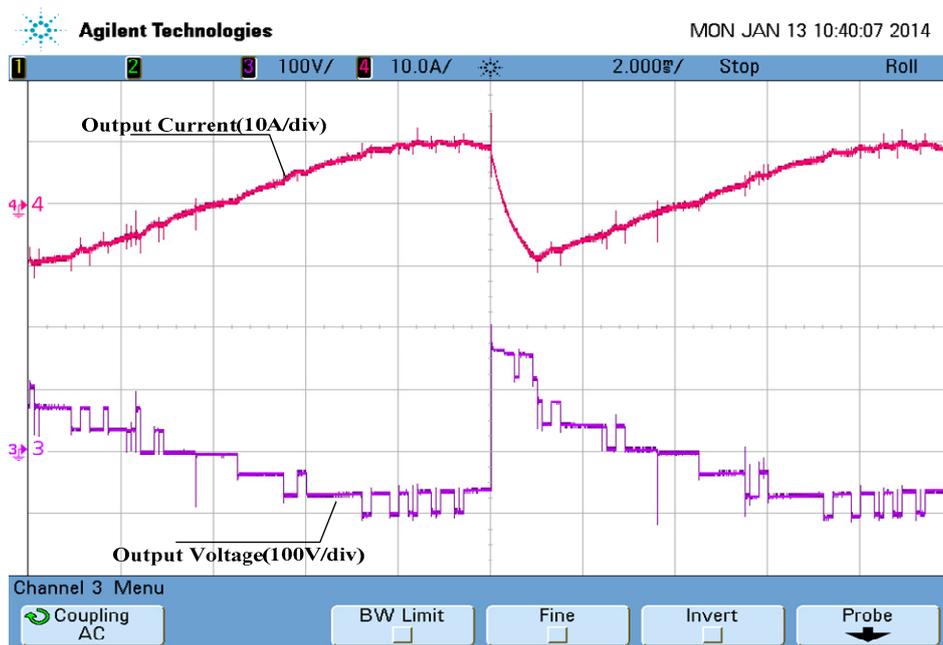


Figure 20. Detail of the output voltage and current for a step in the angle of the reference current.

6. Characteristic Analysis and Comparison with Other Topologies

6.1. DC Fault Blocking Capacity

When a DC-side short-circuit happens, with all IGBTs turned off, the director switches and stack of H-bridges behave as a number of uncontrolled diodes connecting with all DC capacitors in the cells

connected in series, as shown in Figure 21. The equivalent capacitor value in Figure 21 can be expressed as

$$C_e = C/n_{cell_FA} \quad (21)$$

where C is the capacitance of the capacitor in each cell and n_{cell_FA} is the number of cells in one phase of the FA-MMC. The AC source charges the equivalent capacitor and inductors (including the L_s , L_b , L_d) through the DC fault current, thus, limiting the rising rate of the fault current. Consequently, the value of U_{ce} will rise rapidly, and the DC fault current will be blocked.

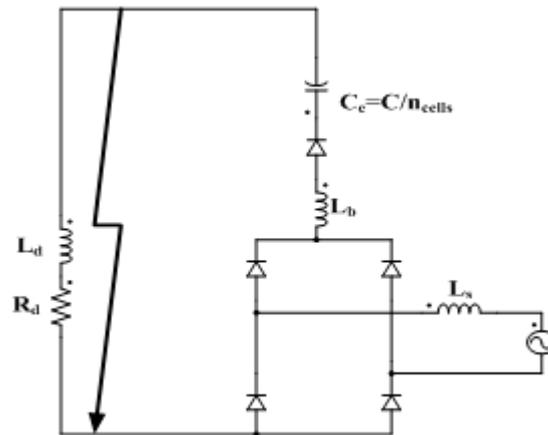


Figure 21. The equivalent circuit of the insulated-gate bipolar transistors (IGBTs) blocking when a DC fault occurs.

6.2. Number of Sub-module and IGBTs

Equation (3) shows that the DC bus voltage is lower than the peak value of output AC voltage by 27% in FA-MMC topology. This implies that the voltage rating of the director switches should be at least equal to the peak value of output AC voltage since they have to support higher voltages.

Assuming that the maximum allowable working voltage rating of the IGBTs is equal to the voltage rating of the DC capacitors in the sub-modules, the number of sub-modules of the proposed FA-MMC is given by

$$n_{cell_FA} = \frac{\hat{U}_{AC}}{U_{RATED}} \quad (22)$$

where U_{RATED} is the voltage rating of the IGBTs. The number of IGBTs of each phase of the FA-MMC is given by

$$n_{IGBT1} = 4n_{cell_FA} + 4n_s = \frac{8\hat{U}_{AC}}{U_{RATED}} \quad (23)$$

where n_s , the number of IGBT in S_1 – S_4 , is given by

$$n_s = \frac{\hat{V}_{MN}}{U_{RATED}} = \frac{\hat{U}_{AC}}{U_{RATED}} \quad (24)$$

Given the same AC output voltage, we also can deduce the DC voltage, number of cells, and IGBTs needed in an AAMC. The relationship between DC and AC voltage magnitudes in an AAMC, which has been derived in [22], can be expressed as

$$V_{dc} = \frac{\pi}{2} \hat{V}_{AC} \quad (25)$$

It can be seen from Equation (3) and (25) that the FA-MMC can reduce the DC bus voltage by half with the same AC output voltage and same active/reactive power flow compared with an AAMC.

Considering the sum of the sub-module capacitor voltage must be greater than the peak value of the line-to-line voltage to achieve DC current blocking capability, the number of sub-modules of an AAMC can be expressed as

$$n_{cell_AA} = \frac{\sqrt{3}\hat{U}_{AC}}{U_{RATED}} \quad (26)$$

But, it only has two direct switches, so considering Equation (24) and (26), the number of IGBTs of a single-phase AAMC is given by

$$n_{IGBT2} = 4n_{cell_AA} + 2n_S = \frac{(4\sqrt{3} + 2)\hat{U}_{AC}}{U_{RATED}} \quad (27)$$

To summarize, the number of IGBTs of the FA-MMC is less than that of the AAMC, and the DC voltage and number of sub-modules of the FA-MMC is nearly half those of the AAMC, leading to smaller size, less need for insulation, and lower cost. And the comparison results of the number of IGBTs and sub-module capacitors between FA-MMC, AAMC and various MMC topologies mentioned in the introduction is shown in Table 4.

Table 4. Number of semiconductor devices and sub-module capacitors.

Topology	Number of Sub-Module Capacitor	Number of IGBTs	Number of Diodes
H-MMC	N	2 N	0
F-MMC	N	4 N	0
CH-MMC	N	2.35 N	0.7 N
AAMC	0.34 N	1.8 N	0
FA-MMC	0.2 N	1.6 N	0

6.3. Efficiency Analysis

To evaluate the power losses of the FA-MMC and AAMC, a simple loss calculation method for module multilevel converter is adopted [25]. And the result is shown in Table 5. To summarize, the losses of FA2MC increases slightly compared with AAMC, but it is still significantly lower than other types of MMC topologies.

Table 5. Losses calculation results

Topology	Switching Losses	Conduction Losses	Total Losses
H-MMC	0.29%	0.82%	1.11%
F-MMC	0.29%	1.88%	2.18%
CH-MMC	0.29%	1.19%	1.48%
AAMC	0.16%	0.47%	0.63%
FA-MMC	0.16%	0.66%	0.82%

6.4. Comprehensive Comparison with Other Topological Structures

According to the above analysis, a comprehensive comparison between the full-bridge MMC, half-bridge MMC, CH-MMC, A2MC, and FA-MMC is summarized in Table 6, where more “+” means the corresponding topology performs better in the corresponding characteristic. It can be seen in Table 6 that the FA-MMC has advantages in several aspects compared with the other topologies.

Table 6. Comprehensive comparison with other various topology

Topology	Economy	Efficiency	Volume	DC Fault Blocking Capacity	Demand for Insulation
H-MMC	+++	+++	+	+	+
F-MMC	+	+	+	++	+
CH-MMC	++	++	+	++	+
AAMC	++++	+++++	++	++	++
FA-MMC	+++++	++++	+++	++	+++

7. Conclusions

In this paper, a FA-MMC topology and its predictive control scheme have been proposed. The effectiveness of the proposed topology and proposed control strategy under various operating conditions are evaluated based on simulation studies in the PowerSIM environment and experiments, and the comparisons with other topological structures are also given. Through the analysis and demonstration mentioned above, the characteristics of this topology and its predictive control strategy are summarized as follows:

- (1) The sub-module capacitor number of FA-MMC reduce significantly while connecting to the same AC voltage level and power level, results in a more compact structure;
- (2) Further, it reduces the number of needed IGBTs while retaining the ability to block a DC-side fault compared with other topologies, so that the cost of the system is reduced;
- (3) The algorithm the algorithm has been proved to be able to achieve multiple control objectives of FA-MMC simultaneously (i.e., capacitor voltages balancing and ac-side currents control). The developed control strategy also contains a director switch control function so that the director switch maintains operation in low-frequency and zero voltage switching mode.

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Glossary of Terms

E_{AC}	The amount of energy transferred from AC side over half the fundamental period
E_{DC}	The amount of energy going to DC side over half the fundamental period.
V_{AC}	Output ac voltage
I_{AC}	AC current
U_{DC}	DC voltage of FA MMC
C_e	Equivalent capacitance while all capacitors in cells connected in series
U_{ce_int}	Initial voltage of C_e when dc fault blocking
φ	Angular position of AC current
n_{cell_FA}	Number of cells of FA-MMC each phase
U_{RATED}	The rated voltage of IGBT
n_{IGBT1}	The needed number of IGBTs of FA-MMC each phase
n	The needed number of IGBTs of S1–S4
n_{cell_AA}	The needed number of cells of AAMC each phase
n_{IGBT2}	The needed number of IGBTs of AAMC each phase
V_{dc}	DC voltage of AAMC while the output AC voltage is equal to FA MMC
V_{PB}	The voltage produced by the stack of H-bridge cells of FA MMC
S_i	Switching function of the i th cell
V_{ci}	The capacitor voltage of the i th cell

L_b	Buffer inductor
I_b	The current through L_b
C	The capacitor value of cell
S_d	Switching function of director switch
L_s	Filter inductor
I_s	The current through L_s
T_s	Sampling period
J_{all}, J_i, J_{vc}	Cost function
α, β	Weighting factor

References

1. Wang, Y.; Yang, B.; Zuo, H.; Liu, H.; Yan, H. A DC Short-Circuit Fault Ride Through Strategy of MMC-HVDC Based on the Cascaded Star Converter. *Energies* **2018**, *11*, 2079. [[CrossRef](#)]
2. Xiao, L.; Li, Y.; Xiao, H.; Zhang, Z.; Xu, Z. Electromechanical Transient Modeling of Line Commutated Converter-Modular Multilevel Converter-Based Hybrid Multi-Terminal High Voltage Direct Current Transmission Systems. *Energies* **2018**, *11*, 2102. [[CrossRef](#)]
3. Wu, Z.; Chu, J.; Gu, W.; Huang, Q.; Chen, L.; Yuan, X. Hybrid Modulated Model Predictive Control in a Modular Multilevel Converter for Multi-Terminal Direct Current Systems. *Energies* **2018**, *11*, 1861. [[CrossRef](#)]
4. Li, Z.; Tan, G. A Black Start Scheme Based on Modular Multilevel Control-High Voltage Direct Current. *Energies* **2018**, *11*, 1715. [[CrossRef](#)]
5. Pouesmaeil, E.; Mehrasa, M.; Rodrigues, E.; Godina, R.; Catalão, J.P.S. Control of Modular Multilevel Converters Under Loading Variations in Distributed Generation Applications. In Proceedings of the 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I CPS Europe), Palermo, Italy, 12–15 June 2018; pp. 1–6.
6. Hakimi, S.M.; Hajizadeh, A. Integration of Photovoltaic Power Units to Power Distribution System through Modular Multilevel Converter. *Energies* **2018**, *11*, 2753. [[CrossRef](#)]
7. Jafarishiadeh, M.; Ahmadi, R. Two-and-One Set of Arms MMC-Based Multilevel Converter with Reduced Submodule Counts. In Proceedings of the 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, USA, 13–15 June 2018; pp. 779–782.
8. Yang, D.; Yin, L.; Xu, S.; Wu, N. Power and Voltage Control for Single-Phase Cascaded H-Bridge Multilevel Converters under Unbalanced Loads. *Energies* **2018**, *11*, 2435. [[CrossRef](#)]
9. Zhang, J.; Zhao, C. The Research of SM Topology with DC Fault Tolerance in MMC-HVDC. *IEEE Trans. Power Deliv.* **2015**, *30*, 1561–1568. [[CrossRef](#)]
10. Dong, S.; He, H.; Yuan, Z.; Yang, Y.; He, J.; He, H. Transient over-voltage of the full-bridge MMC HVDC system with overhead line fault. In Proceedings of the 2016 Power Systems Computation Conference, Chengdu, China, 19–22 September 2016; pp. 1–4.
11. Lin, W.; Jovicic, D.; Nguefeu, S.; Saad, H. Protection of full bridge MMC DC grid employing mechanical DC circuit breakers. In Proceedings of the 2017 IEEE Power Energy Society General Meeting, Chicago, IL, USA, 16–20 July 2017; pp. 1–5.
12. Zeng, R.; Xu, L.; Yao, L.; Williams, B.W. Design and Operation of a Hybrid Modular Multilevel Converter. *IEEE Trans. Power Electron.* **2015**, *30*, 1137–1146. [[CrossRef](#)]
13. Li, R.; Adam, G.P.; Holliday, D.; Fletcher, J.E.; Williams, B.W. Hybrid Cascaded Modular Multilevel Converter with DC Fault Ride-Through Capability for the HVDC Transmission System. *IEEE Trans. Power Deliv.* **2015**, *30*, 1853–1862. [[CrossRef](#)]
14. Marquardt, R. Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications. In Proceedings of the 2010 International Power Electronics Conference, Sapporo, Japan, 21–24 June 2010; pp. 502–507.
15. Marquardt, R. Modular Multilevel Converter topologies with DC-Short circuit current limitation. In Proceedings of the 8th International Conference on Power Electronics, Jeju, South Korea, 30 May–3 June 2011; pp. 1425–1431.

16. Qin, J.; Saeedifard, M.; Rockhill, A.; Zhou, R. Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits. *IEEE Trans. Power Deliv.* **2015**, *30*, 385–394. [[CrossRef](#)]
17. Li, R.; Fletcher, J.E.; Xu, L. A Hybrid Modular Multilevel Converter with Novel Three-level Cells for DC Fault Blocking Capability. *IEEE Trans. Power Deliv.* **2015**, *30*, 2017–2026. [[CrossRef](#)]
18. Zeng, R.; Xu, L.; Yao, L. An improved modular multilevel converter with DC fault blocking capability. In Proceedings of the 2014 IEEE PES General Meeting, National Harbor, MD, USA, 27–31 July 2014; pp. 1–5.
19. Xu, J.; Zhao, P.; Zhao, C. Reliability Analysis and Redundancy Configuration of MMC with Hybrid Sub-Module Topologies. *IEEE Trans. Power Electron.* **2016**, *31*, 2020–2029. [[CrossRef](#)]
20. Davidson, C.C.; Trainer, D.R. Innovative concepts for hybrid multi-level converters for HVDC power transmission. In Proceedings of the 9th IET International Conference an AC and DC Power Transmission, London, UK, 19–21 October 2010; pp. 1–5.
21. Cross, A.M.; Trainer, D.R.; Crookes, R.W. Chain-link based HVDC Voltage Source Converter using current injection. In Proceedings of the 9th IET International Conference an AC and DC Power Transmission, London, UK, 19–21 October 2010; pp. 1–5.
22. Merlin, M.M.C.; Green, T.C.; Mitcheson, P.D.; Trainer, D.R.; Critchley, D.R.; Crookes, R.W. A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability. In Proceedings of the 9th IET International Conference an AC and DC Power Transmission, London, UK, 19–21 October 2010; pp. 1–5.
23. Lee, H.Y.; Asif, M.; Park, K.H.; Lee, B.W. Assessment of Appropriate MMC Topology Considering DC Fault Handling Performance of Fault Protection Devices. *Appl. Sci.* **2018**, *8*, 1834. [[CrossRef](#)]
24. Cortes, P.; Kouro, S.; Rocca, B.L.; Vargas, R.; Rodriguez, J.; Leon, J.I.; Vazquez, S.; Franquelo, L.G. Guidelines for weighting factors design in Model Predictive Control of power converters and drives. In Proceedings of the 2009 IEEE International Conference on Industrial Technology, Gippsland, Australia, 10–13 February 2009; pp. 1–7.
25. Zhang, Z.; Xu, Z.; Xue, Y. Valve Losses Evaluation Based on Piecewise Analytical Method for MMC–HVDC Links. *IEEE Trans. Power Deliv.* **2014**, *29*, 1354–1362. [[CrossRef](#)]



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