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Design and Analysis of a Repetitive Current Controller for a Single-Phase Bridgeless SEPIC PFC Converter

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Abstract: This paper studies a repetitive controller design scheme for a bridgeless single-ended primary inductor converter (SEPIC) power factor correction (PFC) converter to mitigate input current distortions. A small signal modeling of the converter is performed by a fifth-order model. Since the fifth-order model is complex to be applied in designing a current controller, the model is approximated to a third-order model. Using the third-order model, the repetitive controller is designed to reduce the input current distortion. Then, the stability of the repetitive controller is verified with an error transfer function. The proposed controller performance is validated by simulation, and the experiment results show that the input current total harmonic distortion (THD) is improved by applying the proposed controller for an 800 W bridgeless SEPIC PFC converter prototype.

Keywords: AC-DC converters; bridgeless SEPIC PFC converter; repetitive controller; current distortion; current controller design

1. Introduction

Until now, many power conversion systems (PCS) are connected to grid and harmonic pollution becomes an issue [1,2]. General PCS needs AC-DC conversion to operate with the grid, and the easiest way is using a diode rectifier. However, it can decrease the power quality due to harmonics of the input current of the diode rectifier [3]. Thus, to improve the quality of the input current, the grid-tied power factor correction (PFC) converter can be applied. The PFC converter can achieve a unity power factor operation with the sinusoidal input current, which has low harmonics. Generally, the boost PFC converter is used, due to the simplicity, efficiency and low cost [4–6].

There are many systems using the PFC converter, such as switching mode power supply (SMPS) and LED applications, etc. [7–9]. These applications demand a low DC output voltage while the input voltage is relatively high. However, the general boost PFC converter only generates higher output voltage than the grid peak-voltage, and it needs two stages for step-down operation. It is difficult to expect the high efficiency because the number of PCS has been increased. In this case, the step-down PFC converter which has only one stage can be used. There are step-down PFC converters such as buck, buck-boost, Cuk and single-ended primary inductor converter (SEPIC) [10–28]. The buck PFC converter is simple as boost PFC converter with high efficiency, but it only can generate the lower voltage than the input voltage and does not create the input current around in zero-crossing point. On the other hand, the buck-boost, Cuk, and SEPIC have no limit to generate the input current and can operate in both step-up and step-down modes. So, the output voltage with wide range can be generated.

Recently, there have been continuing researches of the buck-boost, Cuk, and SEPIC PFC converters. The buck-boost PFC converter needs an input filter due to pulsating input current. On the contrary, the Cuk and SEPIC converters generate the continuous input current, and do not need an additional input filter which can decrease the efficiency of the system. However, the Cuk converter's output voltage is inversed comparable table [19].

In [20–22], SEPIC and Cuk PFC converter topologies utilize the diode bridge at input side, which causes additional conduction losses. On the other hand, bridgeless SEPIC and Cuk PFC converter topologies are proposed in [23–28]. A Cuk PFC converter in [23,24] consists of 2 switches and 3 diodes. A SEPIC PFC converter in [25,26] has 2 switches and 3 diodes. The circuits using more switches have also been introduced in [27,28]. In this paper, a bridgeless SEPIC PFC converter with single switch and 5 diodes is utilized in Figure 1 [29]. Accordingly, the converter has low switching loss.

In general, the PFC converter has a unidirectional power transfer characteristic, because it is operated in unity power factor condition. Therefore, the PFC converter works in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The DCM operation is the cause of the input current distortion in low power condition. The input current distortion due to the DCM operation includes high-order harmonics, which are higher than the bandwidth of a typical current controller such as a proportional-integral (PI) controller or a proportional-resonant (PR) controller. To reduce the input current distortion, the current controller should be designed considering the plant model in DCM as well as in CCM [27,30,31]. In [27], the feed-forward is utilized in the SEPIC PFC converter for compensating the input current distortion. However, deriving an accurate DCM model is more difficult than a CCM model, which is relatively easy to interpret.

A repetitive controller can be applied to compensate the harmonic components caused by DCM operation. The repetitive controller has a high gain for the harmonics corresponding to multiples of the fundamental frequency [32–35]. Thus, if a stable repetitive controller design is guaranteed, the current distortion can be improved without the complicated analysis under DCM condition. In this paper, the design method of the current controller with repetitive controller is introduced. Also, a simplified third-order model of the SEPIC PFC converter is proposed.

This paper is organized as follows. Section 2 provides an analysis of the operating modes and the transfer function of the bridgeless SEPIC PFC converter. In Section 3, the proposed current controller design is described. The results of the simulations and the experiments are presented in Sections 4 and 5 to verify the performance of the proposed current controller.

2. Bridgeless SEPIC PFC Converter with RC Damping Circuits

2.1. Circuit Structure and Mode Analysis

Figure 1 shows the bridgeless SEPIC PFC converter dealt in this paper. A RC damping circuit is equipped to suppress the high-order resonance of the converter which will be described in a later section. Compared to a traditional SEPIC DC–DC converter, the bridgeless SEPIC PFC converter contains the blocking diodes, D_1 and D_2, and the freewheeling diodes, D_p and D_n. With this configuration, only the single switching device S_c can be utilized for both positive and negative input voltage cycles.

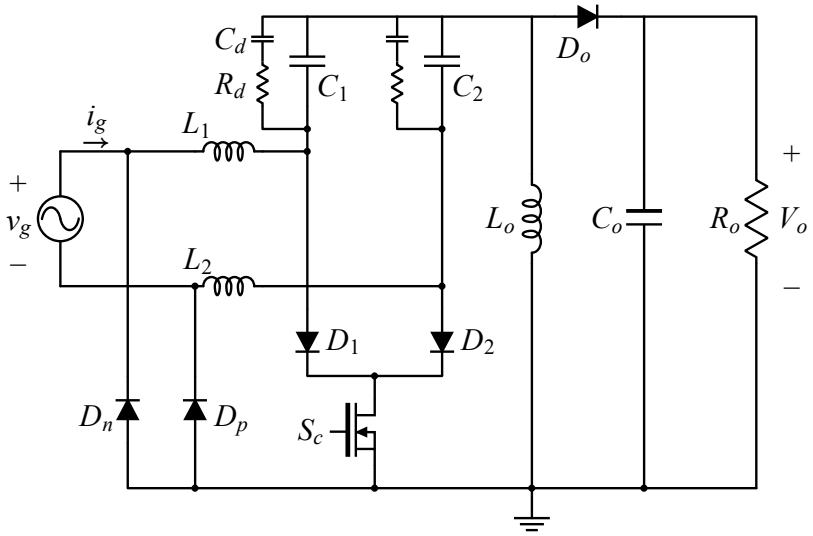
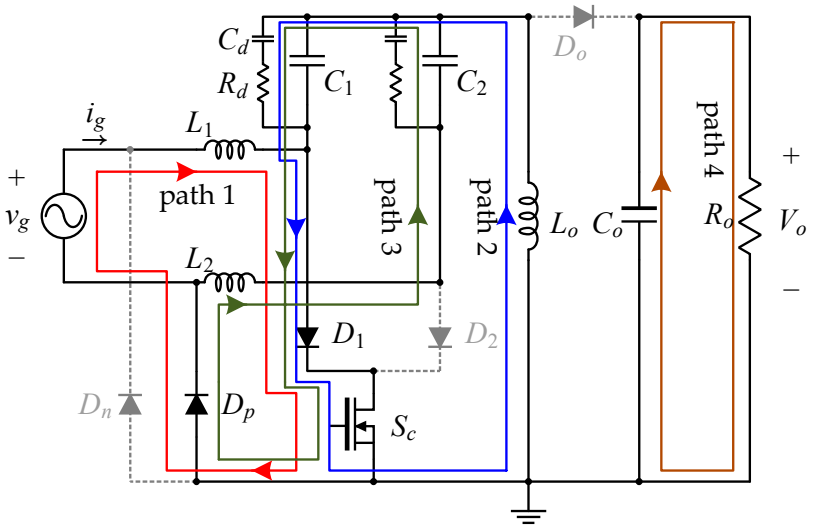


Figure 1. Topology of the bridgeless SEPIC PFC converter with the RC damping circuits. SEPIC: single-ended primary inductor converter; PFC: power factor correction.

Figure 2 represents the operation mode analysis of the bridgeless SEPIC PFC converter under a positive input voltage cycle. In Figure 2a, the current conduction paths are indicated when S_c turns on. In this case, D_n, D_2, and D_o are biased reversely. In this case, four paths are existent. Path 1 consists of the input source, L_1, D_1, S_c, and D_p. In this path, the input energy is stored in L_1. Through path 2, C_1 is charged by the energy stored in L_o. The RC damping circuit existing in this path dampens the resonant peak caused by C_1, L_1, and L_o. So, it can increase the stability of the circuit in the control viewpoint. For path 3, the energy exchange occurs between C_1, C_2, and L_2. Again, C_1 is charged while C_2 is discharged. Unlike L_o, the input source does not contribute charging of the energy for L_2. In this interval, the load R_o is supplied by C_o via path 4. When S_c is opened, the current conduction paths change as shown in Figure 2b. In this case, D_o turns on, and D_1, D_2, S_c, and D_n are blocked and the energy stored in L_1, L_2, C_1, C_2, and L_o is transferred to the load side including C_o and R_o. Similarly, the analyses for negative input voltage cycles which are not discussed here can be also performed.



(**a**)

Figure 2. *Cont.*

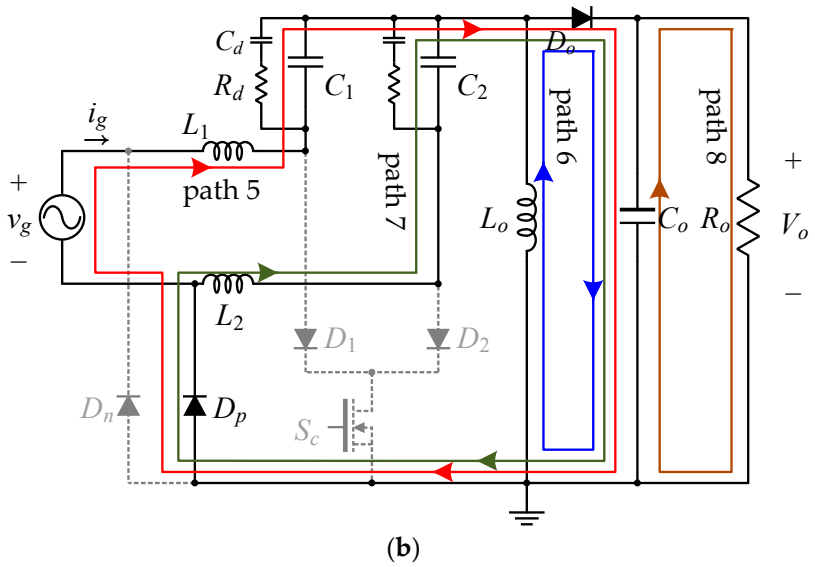


Figure 2. Operation modes of the bridgeless SEPIC PFC converter under positive voltage cycles: (**a**) when S_c is turned on; (**b**) when S_c is turned off.

2.2. Control Model Derivation of the Bridgeless SEPIC PFC Converter

Figure 3 illustrates the equivalent circuits of the bridgeless SEPIC PFC converter with the damping circuit according to the switching operations. Since paths 3 and 7 are the leakage current paths and the leakage current is very smaller than the input current, it can be ignored. So, the operation of the converter is basically identical to traditional SEPIC PFC converters except the RC damping circuit is included. In order to see the effect of the damping circuit and design the controller, the control-to-inductor current model for the SEPIC PFC converter is derived.

When S_c is turned on, the following equations can be obtained. At this moment, the voltages of L_1 and L_o are derived as follows:

$$V_{in} = L_1 \frac{di_{L1}}{dt} \tag{1}$$

$$v_{C1} = L_o \frac{di_{Lo}}{dt} \tag{2}$$

The capacitor currents i_{C1}, i_{Co} and i_{Cd} are represented as follows:

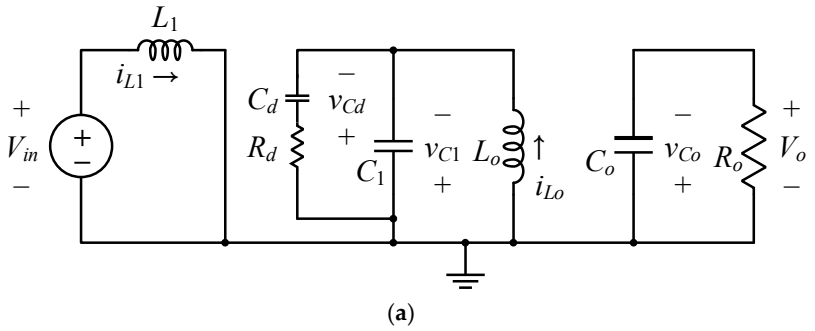


Figure 3. *Cont.*

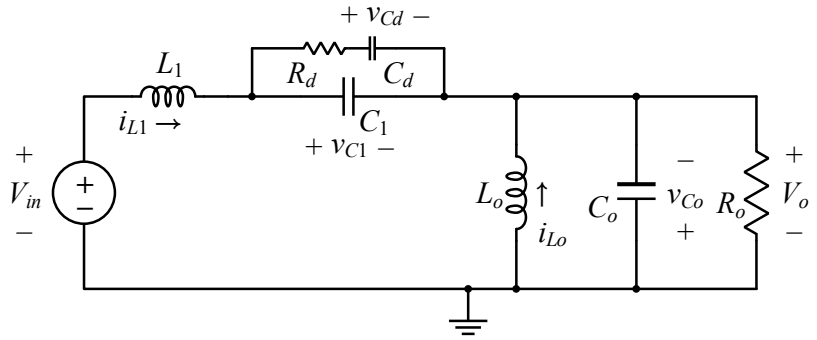


Figure 3. Equivalent circuits of the bridgeless SEPIC PFC converter with the damping circuit: (**a**) when S_c is turned on; (**b**) when S_c is turned off.

$$-i_{Lo} - \frac{v_{C1} - v_{Cd}}{R_d} = C_1 \frac{dv_{C1}}{dt} \tag{3}$$

$$\frac{v_{C1} - v_{Cd}}{R_d} = C_d \frac{dv_{Cd}}{dt} \tag{4}$$

$$-\frac{v_{Co}}{R_o} = C_o \frac{dv_{Co}}{dt} = -\frac{V_o}{R_o} \tag{5}$$

When S_c is turned off, the voltages of L_1 and L_o are expressed as below:

$$V_{in} - v_{C1} - v_{Co} = L_1 \frac{di_{L1}}{dt} \tag{6}$$

$$-v_{Co} = L_o \frac{di_{Lo}}{dt} \tag{7}$$

and the currents of C_1, C_d and C_o are written as:

$$i_{L1} - \frac{v_{C1} - v_{Cd}}{R_d} = C_1 \frac{dv_{C1}}{dt} \tag{8}$$

$$\frac{v_{C1} - v_{Cd}}{R_d} = C_d \frac{dv_{Cd}}{dt} \tag{9}$$

$$i_{L1} + i_{Lo} - \frac{V_{Co}}{R_o} = C_o \frac{dv_{Co}}{dt} \tag{10}$$

Using Equations (1)–(5), then state–space matrix for S_c on time can be rewritten as follows:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_o} & 0 & 0 \\ 0 & -\frac{1}{C_o} & -\frac{1}{R_d C_1} & \frac{1}{R_d C_1} & 0 \\ 0 & 0 & \frac{1}{R_d C_d} & -\frac{1}{R_d C_d} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{R_o C_o} \end{bmatrix} B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{11}$$

and, the state–space matrix for S_c off time can be derived as below:

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 & 0 & -\frac{1}{L_o} \\ \frac{1}{C_1} & 0 & -\frac{1}{R_d C_1} & \frac{1}{R_d C_1} & 0 \\ 0 & 0 & \frac{1}{R_d C_d} & -\frac{1}{R_d C_d} & 0 \\ \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 & -\frac{1}{R_o C_o} \end{bmatrix} B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{12}$$

$$x = \begin{bmatrix} i_{L1} \\ i_{Lo} \\ v_{C1} \\ v_{Cd} \\ v_{Co} \end{bmatrix} \quad u = [V_{in}] \quad \dot{x} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{Lo}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{Cd}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} \tag{13}$$

$$\frac{x(s)}{d(s)} = (sI - A)^{-1}\{(A_1 - A_2)X + (B_1 - B_2)V_{in}\} \tag{14}$$

The control-to-inductor current model can be obtained by Equations (11)–(14) as a fifth-order model. Similarly, the control-to-inductor current model without the RC damping also can be derived as a fourth-order model [29]. Figure 4 compares the control models of the bridgeless SEPIC PFC converters with the RC damping and without damping in frequency domain with parameters in Table 1. The model with the RC damping has only one resonant frequency in 800 Hz and the resonance at higher frequency is damped. On the contrary, the model without the RC damping has two resonance points in about 800 Hz and 5 kHz with high Q factor. This second resonance point with high frequency which is over than the current control bandwidth cannot be controlled and oscillates the system current unexpectedly. Therefore, the RC damping should be included to damp the second resonant peak.

Table 1. System Parameters.

Parameters	Values
Switching frequency (f_{sw})	72 kHz
Sampling frequency (f_s)	24 kHz
Input root mean square (RMS) voltage (v_g)	120 V/60 Hz
Output voltage (V_o) (buck/boost)	80 V/220 V
Input filter inductance (L_1, L_2)	1 mH
Output inductance (L_o)	1 mH
Damping resistance (R_d)	60 Ω
Energy transfer capacitance (C_1, C_2)	0.47 μF
Damping capacitance (C_d)	2.2 μF
Output capacitance (C_o)	2.6 mF

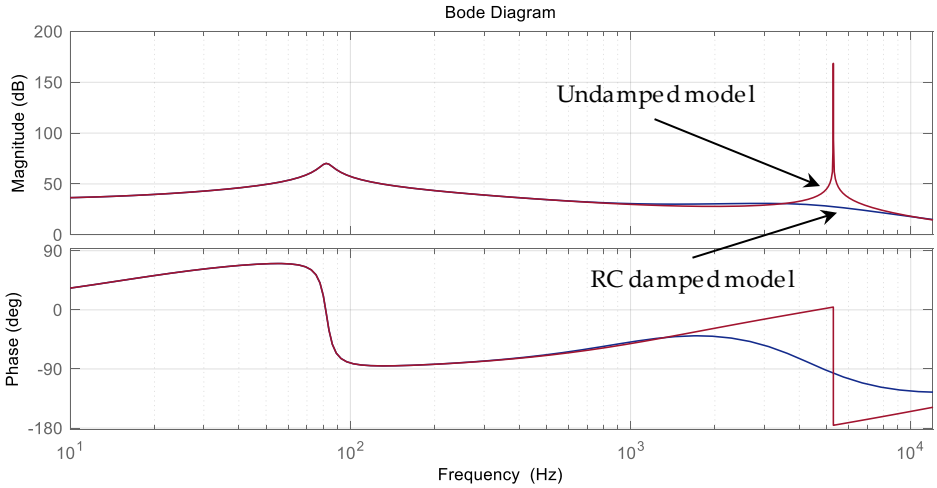


Figure 4. Frequency responses of the RC damped and the undamped models.

2.3. Control Model Approximation of the Bridgeless SEPIC PFC Converter

The control-to-inductor current model with the RC damping is the fifth-order model. Since the original undamped model is the fourth model, it became more complexed than the original undamped model. Thus, it is difficult to analyze the frequency response of the controller with the fifth model so, approximation needs to be adapted to design the controller easily. Since the capacitance of C_1 and C_d

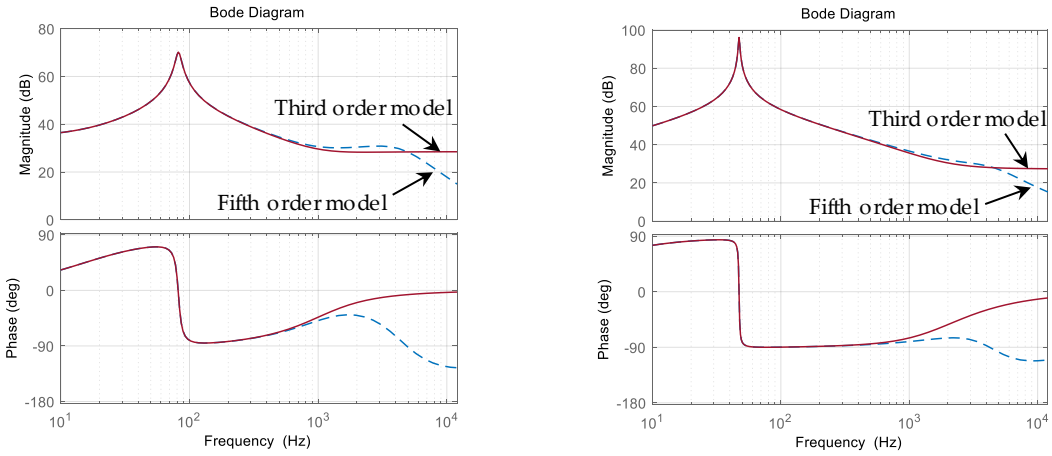
is much lower value than the other components, the multiple of C_1 and C_d is sufficiently small to be ignored. Similarly, the multiple of the L_1 and L_o is low value as C_d or C_1, so $C_1L_1L_o$ and $C_dL_1L_o$ also can be substituted with zero. With these processes, the approximate model can be represented as follows:

$$G_{id}(s) = \frac{i_g(s)}{d(s)} = \frac{N_1 s^3 + N_2 s^2 + N_3 s + N_4}{D_1 s^3 + D_2 s^2 + D_3 s + D_4} \tag{15}$$

$$\begin{aligned} N_1 &= C_o L_o R_o \{(C_1 + C_d)(V_{C1} + V_{Co}) + C_d R_d D'(I_{L1} + I_{Lo})\} \\ N_3 &= L_o D'(I_{L1} + I_{Lo}) + D(C_d R_d + C_o R_o)(V_{C1} + V_{Co}) + C_d R_d R_o D'(I_{L1} + I_{Lo}) \\ N_3 &= L_o D'(I_{L1} + I_{Lo}) + D(C_d R_d + C_o R_o)(V_{C1} + V_{Co}) + C_d R_d R_o D'(I_{L1} + I_{Lo}) \\ N_4 &= D(V_{C1} + V_{Co}) + R_o D'(I_{L1} + I_{Lo}) \end{aligned} \tag{16}$$

$$\begin{aligned} D_1 &= C_d C_o R_d R_o \{L_o(1-2D) + D^2(L_1 + L_o)\} \\ D_2 &= R_o(L_1 D^2 + L_o D'^2)(C_1 + C_d + C_o) + L_1 R_o(1-2D)(C_1 + C_d) + C_d R_d \{L_o(1-2D) + D^2(L_1 + L_o)\} \\ D_3 &= L_o(1-2D) + D^2(L_1 + L_o) + C_d R_d R_o D'^2 \\ D_4 &= R_o D'^2 \\ D' &= 1 - D \end{aligned} \tag{17}$$

The frequency responses of the original fifth-order model and the approximated third-order model in buck and boost modes are represented in Figure 5. As can be seen, the third-order model is very well matched with the fifth-order model until 600 Hz. Where the frequency is beyond 600 Hz, the fifth-order model contains the damped resonance and phase delay, which do not appear in the third-order model. However, the third-order model is enough to design the current controller, because the current control bandwidth is not very high.



(**a**) (**b**)

Figure 5. Frequency responses of the third- and the fifth-order RC damped models: (**a**) Buck mode; (**b**) Boost mode.

3. Proposed Current Controller

3.1. Traditional Current Controller Design

In order to control the bridgeless SEPIC PFC converter, a digital controller is implemented. Therefore, the approximated $G_{id}(s)$ is transformed on the z-domain and delays due to unit calculation and digital pulse-width modulation (PWM) update should be also considered [36]. The z-domain control-to-inductor current model $G_{id}(z)$ is derived as follows:

$$G_{id}(z) = z^{-1} G_{id}(s)|_{s=(z-1)/T_s} \tag{18}$$

where T_s is the sampling period. The digital delay is represented by a unit delay.

The controller structure for regulating the current is shown in Figure 6. The input current reference i_g^* and the input current i_g are input to the controller as absolute values. The duty reference d_{ref} is generated by the current controller $G_{cc}(z)$ and the feed-forward duty d_{ff}. The feed-forward duty compensates for the disturbance caused by the input voltage [37], and is calculated as below:

$$d_{ff} = \frac{V_o}{|v_g| + V_o} \tag{19}$$

where v_g is the input voltage, and V_o is the output voltage.

For the stable current controller design, the frequency response of the open-loop gain $T_i(z)$ consisting of $G_{cc}(z)$ and $G_{id}(z)$ should be analyzed. The open-loop gain $T_{i,P}(z)$ and $T_{i,PI}(z)$ of a proportional (P) controller and a proportional-integral (PI) controller are obtained as:

$$T_{i,P}(z) = K_p G_{id}(z) \tag{20}$$

$$T_{i,PI}(z) = \left(K_p + K_i \frac{T_s z}{z-1}\right) G_{id}(z) \tag{21}$$

where K_p is a proportional gain, and K_i is an integral gain. Since the approximated $G_{id}(s)$ is consistent with the original fifth-order model up to about 600 Hz, the controller is designed accordingly. Figure 7 shows the frequency response of $T_{i,P}(z)$ and $T_{i,PI}(z)$ when K_p and K_i are selected as 0.01 and 60, respectively. In the buck mode, the crossover frequency of $T_{i,P}(z)$ is 269 Hz, which is the bandwidth of the controller. The phase margin Φ_{pm} at the crossover frequency is 96.7 deg. For $T_{i,PI}(z)$, the crossover frequency is 530 Hz and the phase margin is 45.3 deg. Thus, both controllers designed are stable in the buck mode. Also, $T_{i,p}(z)$ and $T_{i,PI}(z)$ of the boost mode are stable, but the crossover frequency is wider than the buck mode. As a result, characteristic of the controller can be superior in the boost mode.

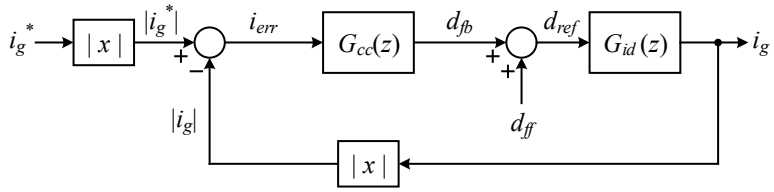
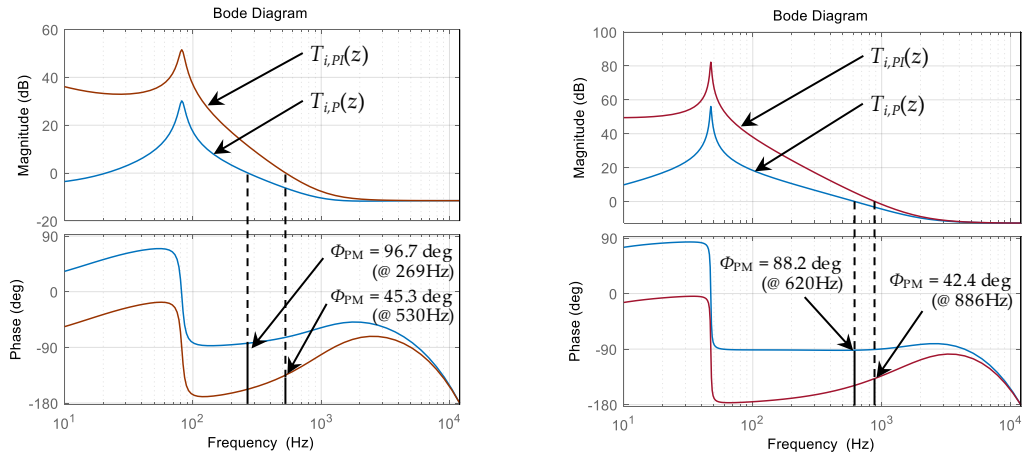


Figure 6. Current controller structure.



(**a**) (**b**)

Figure 7. Frequency response of $T_i(z)$: (**a**) Buck mode; (**b**) Boost mode.

3.2. Repetitive Controller Design

The repetitive controller has excellent performance in eliminating periodic errors [32–35]. The proposed current controller is shown in Figure 8, which consists of the repetitive controller and the P controller in parallel. The repetitive controller is composed of repetitive controller gain K_{rp}, the number of samples N, the number of samples for phase leading L, and stabilization filter $q(z)$. The transfer function of the repetitive controller is derived as below:

$$G_{rp}(z) = \frac{d_{rp}}{i_{err}} = K_{rp}\frac{z^L}{z^N - q(z)} \tag{22}$$

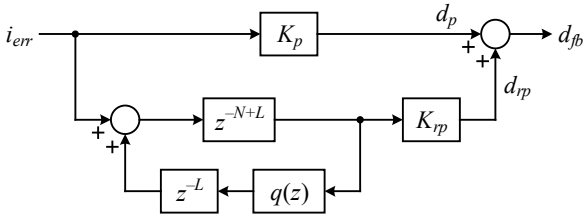


Figure 8. Proposed current controller.

The number of samples N of the repetitive controller is determined by the fundamental frequency f_r of the current reference to be controlled and the sampling frequency f_s as follows:

$$N = \frac{f_s}{f_r} \tag{23}$$

As shown in Figure 6, the current controller regulates the absolute value of the input current. Thus, compared with the frequency of the input current reference, the fundamental frequency of the repetitive controller is doubled. The number of samples for phase leading L is chosen as 2 to compensate for the digital delay of 1.5 T_s. The stabilization filter $q(z)$ is used to ensure the stability of the repetitive controller for the very high order harmonics that cannot be regulated [32]. In general, the following zero-phase delay low pass filter is selected as $q(z)$:

$$q(z) = 0.25z^{-1} + 0.5 + 0.25z \tag{24}$$

The remaining parameter of the repetitive controller is K_{rp}, which determines the stability of the repetitive controller. In order to select K_{rp}, the transfer function of the input current reference to error $G_e(z)$ should be considered, and it is obtained as:

$$G_e(z) = \frac{i_{err}}{i_g^*} = G_{ep}(z)G_{erp}(z) \tag{25}$$

where $G_{ep}(z)$ and $G_{erp}(z)$ are expressed as below:

$$G_{ep}(z) = \frac{1}{1 + T_{i,P}(z)} \tag{26}$$

$$G_{erp}(z) = \frac{z^N - q(z)}{z^N - H(z)} \tag{27}$$

where $H(z)$ is defined as follows:

$$H(z) = q(z) - K_{rp}z^L\frac{G_{id}(z)}{1 + T_{i,P}(z)} \tag{28}$$

For $G_e(z)$ to be stable, all poles must be located within the unit circle in the z-domain. If the P controller is designed to be stable, the poles of $G_{ep}(z)$ are in the unit circle. It can be ensured by selecting an appropriate K_p through the open-loop gain analysis as described above. Therefore, in order for $G_e(z)$ to be stable, the stability of $G_{erp}(z)$ must be guaranteed. According to the small gain theorem, $G_{erp}(z)$ is stable if the magnitude of $H(z)$ is less than 1 [35]. Figure 9 shows the root trajectories of $H(z)$ depending on K_{rp} up to the Nyquist frequency in buck and boost modes. When K_{rp} is 0.021, $G_{erp}(z)$ is unstable because the root trajectories of $H(z)$ deviate from the unit circle in both modes. When K_{rp} is 0.02, the magnitude of $H(z)$ is smaller than 1 in buck mode, but not in boost mode. Therefore, K_{rp} must be less than 0.02 for $G_e(z)$ to be stable in both modes. The frequency response of $G_e(z)$ is illustrated in Figure 10 when K_{rp} is 0.01. Since the fundamental frequency is 120 Hz, it can be seen that the errors of the multiples of fundamental frequency are removed.

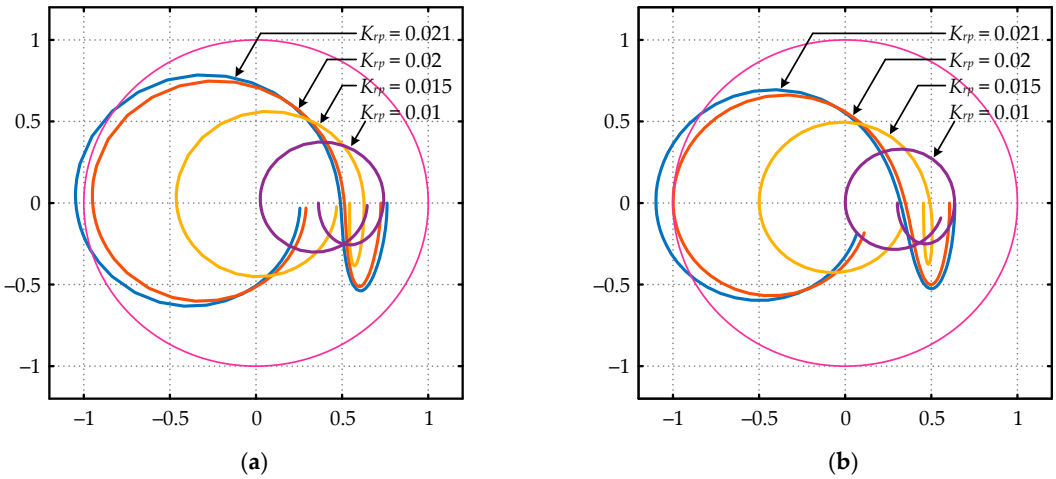


Figure 9. Root trajectories of $H(z)$: (**a**) Buck mode; (**b**) Boost mode.

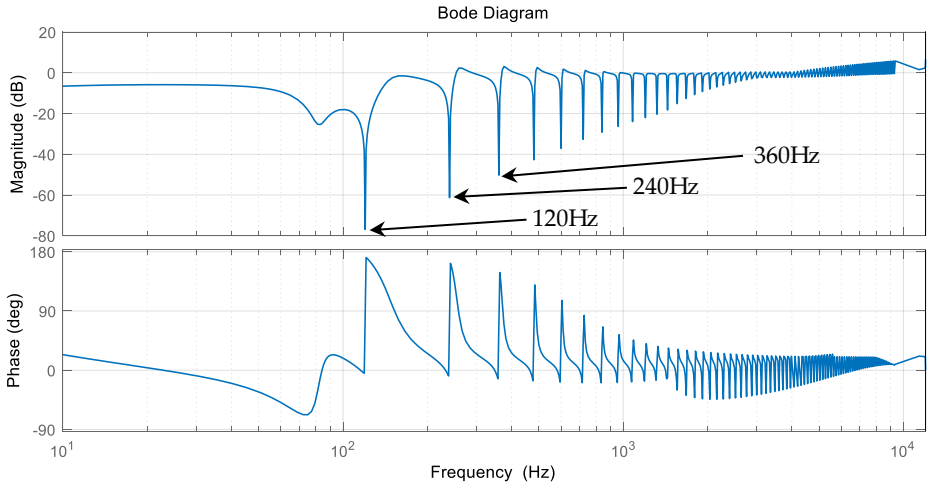


Figure 10. Frequency response of $G_e(z)$.

4. Simulation Results

In order to verify the performance of the proposed controller, the simulation studies have been performed using the simulation software package PSIM. All parameters used in the simulation are shown in Table 1.

Figures 11 and 12 show the input current and the current error when operating in buck mode and boost mode at the full load condition under 800 W and light load condition under 100 W.

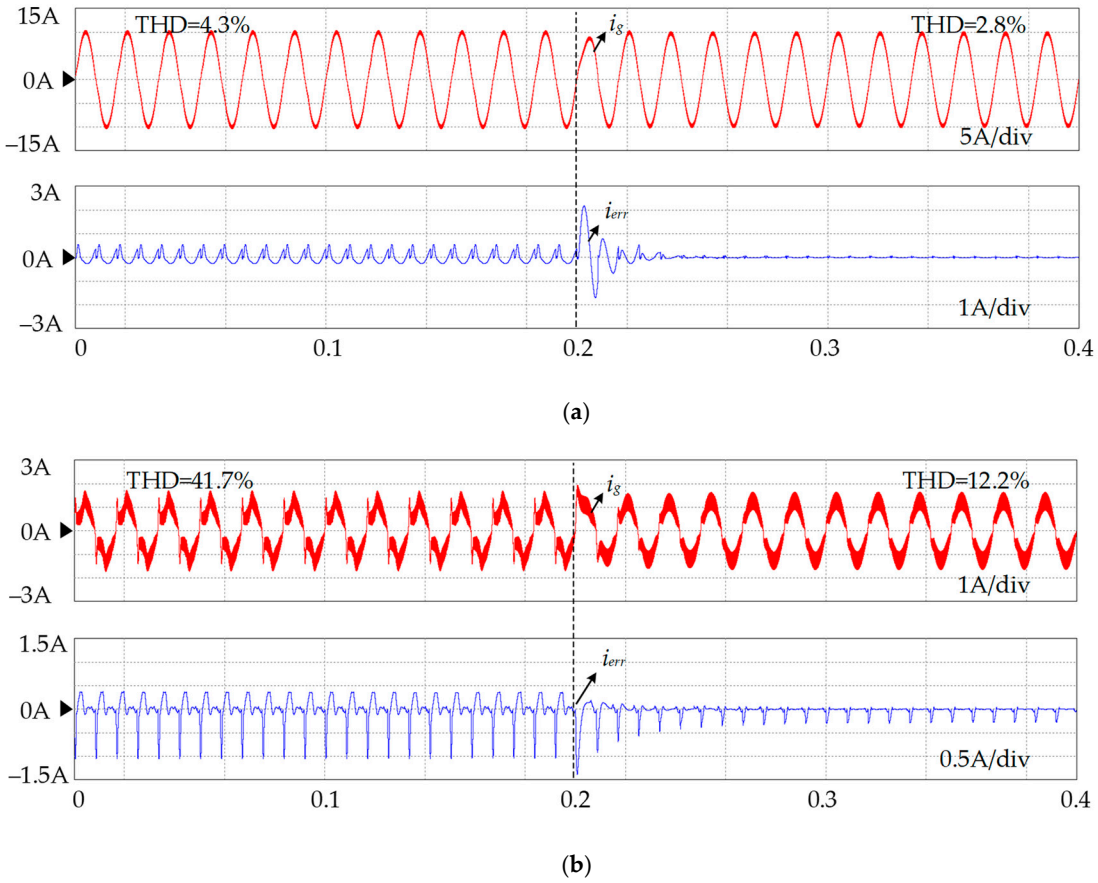


Figure 11. Simulation results applying repetitive controller at 0.2 s in buck mode: (**a**) Input current and current error at load = 800 W; (**b**) Input current and current error at load = 100 W.

Before t = 0.2 s, the input current is regulated with the PI controller. At t = 0.2 s, the PI controller is substituted with the repetitive controller in parallel with P controller. In Figure 11, before applying the repetitive controller, the magnitude of the current error is less than 1 A. However, after applying the repetitive controller, the magnitude of the current error is limited to 0.5 A. The current errors considerably decrease after t = 0.2 s in both load conditions. Especially, under the light load condition, the distortion of the input current is significantly reduced. Also, the total harmonic distortion (THD) of the input current is improved from 4.3% to 2.8% at the full load condition and from 41.7% to 12.2% at light load condition.

Figure 12 depicts the input current and the current error when operating in boost mode at the full load condition under 800 W and light load condition under 100 W. In boost mode, after applying the repetitive controller the magnitude of the input current error is similar with that in buck mode. The THD of the input current under heavy and light load conditions improved 4.4% to 4.3% and 45.8% to 34.8%, respectively. In boost mode, the input current ripple is larger than in buck mode, because the voltage across L_1 is higher due to output voltage according to Equation (6). So, the THD of the input current is higher than in buck mode.

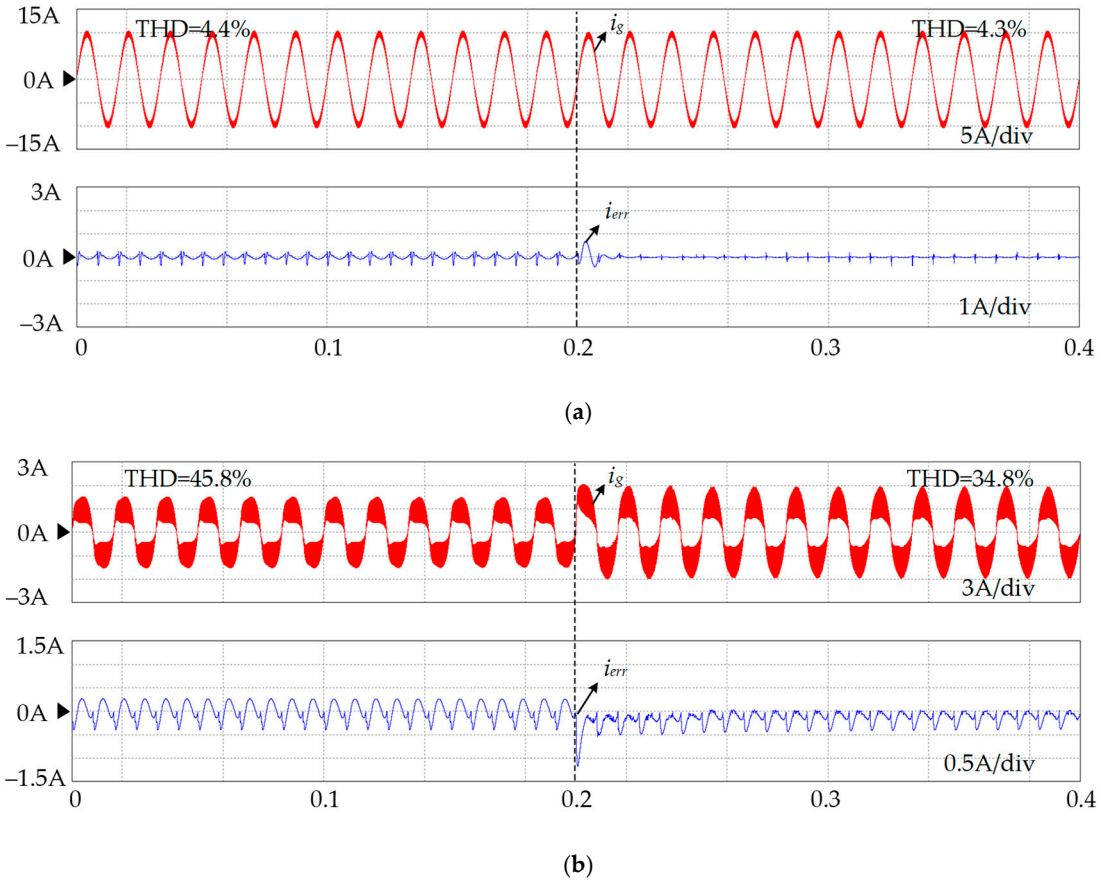


Figure 12. Simulation results applying repetitive controller at 0.2 s in boost mode: (**a**) Input current and current error at load = 800 W; (**b**) Input current and current error at load = 100 W.

5. Experimental Results

The parameter values for hardware are the same values in Figure 1, and a TMS320F28335 digital signal processor (DSP) of Texas Instruments (Dallas, TX, USA) was adopted to implement the digital controller. The bridgeless SEPIC PFC converter consists of a silicon carbide (SiC) MOSFET C2M004120D and four SiC schottky diodes C4D20120D, C3D16065A which are manufactured from Cree. The input voltage of the converter is supplied by Programmable AC power source model 61704. The SEPIC PFC prototype system has been tested from 100 W to 800 W in both buck and boost mode. The output voltages of buck and boost mode are 80 V and 220 V each.

Figures 13 and 14 illustrate the experimental results without the repetitive controller and with the repetitive controller. Figure 13 shows the input current and the current error under 100 W load condition in buck mode and in boost mode. In Figure 13a, without the repetitive controller, the input current is regulated in phase with the input voltage. However, there is the current distortion near the zero-crossing point of the input current, and the peak-to-peak value of the current error is less than 1.8 A. On the other hand, with the repetitive controller the current error is reduced to 0.39 A and the waveform of the input current is significantly improved in Figure 13b. Figure 13c,d shows the experimental results in boost mode without and with the repetitive controller, respectively. In boost mode, the magnitude of current error is 1.53 A without the repetitive controller, but only 0.47 A is measured by applying the repetitive controller.

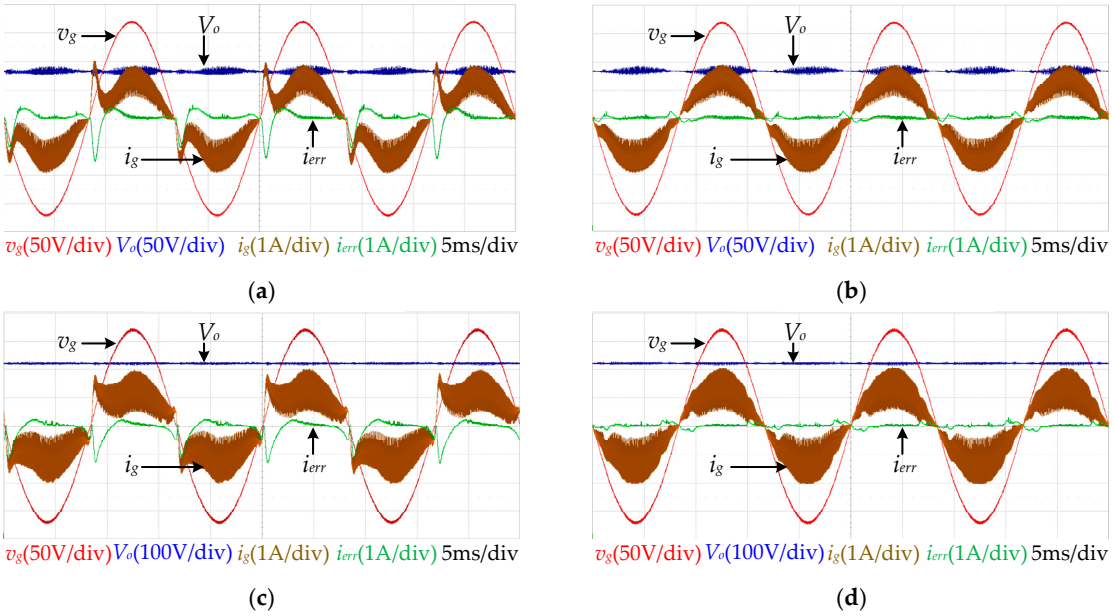


Figure 13. Experimental results under the 100 W condition in buck/boost mode under v_g = 120 V_{rms}, V_o = 80 V(buck)/V_o = 220 V(boost): (**a**) without the repetitive controller in buck mode; (**b**) with the repetitive controller in buck mode; (**c**) without the repetitive controller in boost mode; (**d**) with the repetitive controller in boost mode.

Figure 14 represents the input current and the current error under 800 W load condition in buck mode and boost mode. Figure 14a,c shows that the PI controller works well, and the addition of repetitive controller can be seen to reduce both size of current error and the input current THD as shown in Figure 14b,d. In Figure 14a that is buck mode operation, the current error is 1.35 A but after adding the repetitive controller, the current error is changed to 1.32 A as shown in Figure 14b. Similarly, Figure 14c which is the boost mode shows the current error magnitude of 1.94 A. But in Figure 14d, when the repetitive controller is applied, the current error was read as 1.12 A. Accordingly, Figures 13 and 14 show that the proposed repetitive control method improves the input current quality.

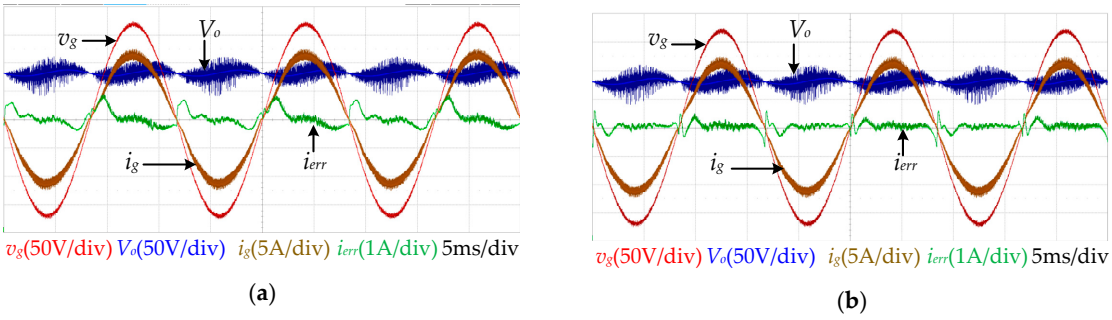


Figure 14. *Cont.*

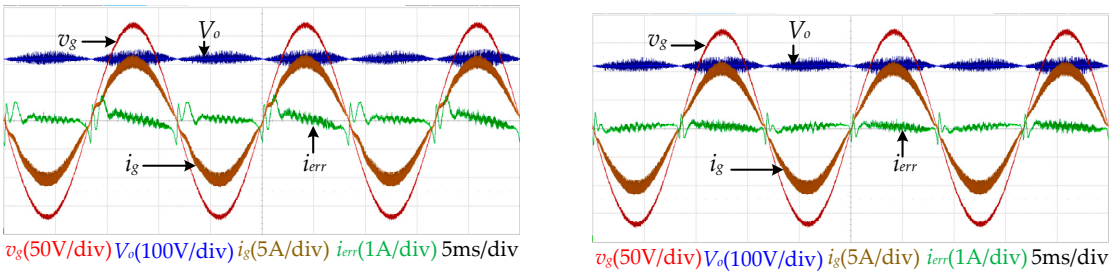
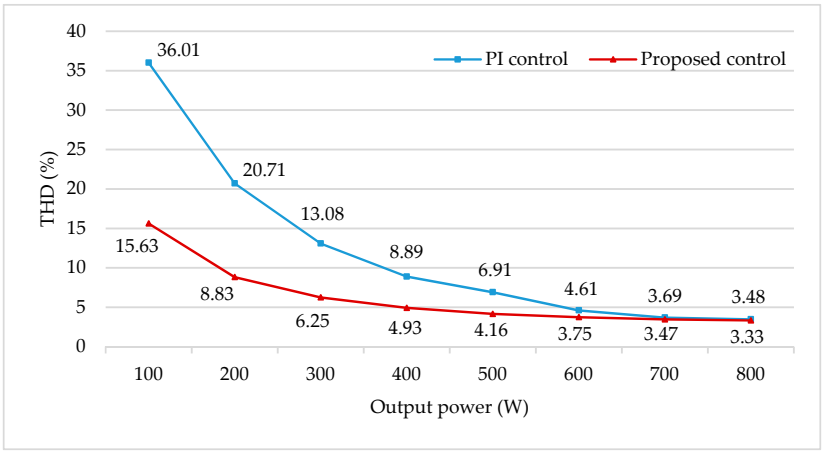
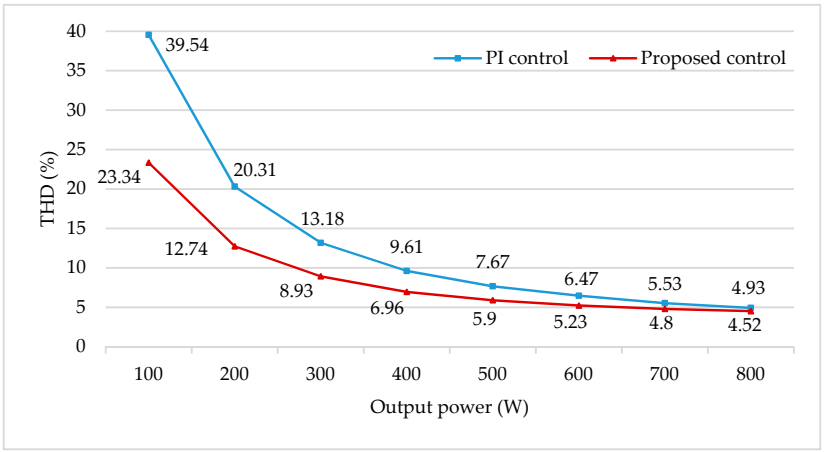


Figure 14. Experimental results under the 800 W condition in buck/boost mode under v_g = 120 V_{rms}, V_o = 80 V(buck)/V_o = 220 V(boost): (**a**) without the repetitive controller in buck mode; (**b**) with the repetitive controller in buck mode; (**c**) without the repetitive controller in boost mode; (**d**) with the repetitive controller in boost mode.

Under various load conditions, the input current THD comparisons between the conventional PI controller and the proposed control scheme are shown in Figure 15. Figure 15a shows the buck operation mode and Figure 15b shows the boost operation mode in the bridgeless SEPIC PFC converter. It also shows that the proposed repetitive controller has much improved THD than the conventional PI controller.



(**a**)



(**b**)

Figure 15. Input current total harmonic distortion comparison results at different load conditions: (**a**) THDs in buck mode; (**b**) THDs in boost mode.

6. Conclusions

The general PFC converters have been studied to boost the output voltage. On the other hand, it only can operate in boost mode, not in buck mode. To step down the output voltage, the general PFC converters must operate with the DC–DC converters. However, the SEPIC PFC converter can operate in buck and boost mode itself, without another system. In this paper, the bridgeless SEPIC PFC converter with RC damping topology has been discussed. The operation modes of the SEPIC converter and the control-to-inductor current model are described in detail. Also, the approximation of the current control model was proceeded, and it has been used to design and to analyze the stability of the current controller. By using this approximation model, the repetitive control scheme was evaluated with the error transfer function. The repetitive control parameters were derived by these analyses and the implementation of the digital controller is also discussed. The simulation and the experimental results verified the repetitive controller performance in 100 W to 800 W load conditions in buck mode and boost mode. As a result, the THDs of the input current are significantly decreased by the proposed repetitive controller in both buck and boost modes. Also, the experimental result shows that the controller based on simplified model is well designed.

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