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A Simplified Minimum DC-Link Voltage Control Strategy for Shunt Active Power Filters

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Abstract: The active power filter (APF) is a popular electrical device to eliminate harmonics in power systems. The rational design and effective control of DC-link capacitor voltage are important for implementing APF functions. In this study, the influences from the DC-link voltage on the APF compensating current characteristic and compensation performance are analyzed, and the reason to maintain DC-link voltage at a minimum value is investigated. On this basis, a simplified minimum DC-link voltage control strategy for APF is proposed. Compared with the existing DC-link voltage control strategies, the minimum DC-link voltage value in proposed strategy is only determined by the grid voltage and modulation ratio, reducing the calculation burden and the implementation difficulty in application, avoiding the interference from external parameters on the compensation effect. Additionally, the reference DC-link voltage varies at different values according to the grid voltage and modulation ratio. A shunt APF prototype is established and the experimental results verify the correctness and effectiveness of the analysis and proposed strategy.

Keywords: active power filter; minimum DC-link voltage; compensating current characteristic; compensation performance; simplified DC-link voltage control strategy

1. Introduction

With the rapid development of power technology, a large amount of nonlinear loads are widely installed in power grids. Nowadays, with the utilization and popularization of renewable energy, including wind power, solar photovoltaic power, and electric vehicles, new harmonic sources have emerged in modern grids. Therefore, a great many harmonics are generated and injected into the power grid, deteriorating the power quality and bringing great harm to the equipment and grid [1,2]. Therefore, he harmonic elimination has been of extensive concern and investigated. To eliminate harmonic pollution, passive filters were applied. However, they did not achieve an ideal compensation effect [3,4]. The active power filter (APF) is an attractive solution to eliminate the harmonics for power system. Additionally, APF has many advantages, such as high filtering accuracy, superior dynamic response, modularity and scalability, making it an ideal devices to compensate harmonics and improve power quality [5–7].

To improve APF performance, the existing literature mainly focuses on the topology, harmonic detection method, compensating current control, DC-link voltage control, modulation strategy, etc. [8–12]. The APF compensating currents are generated by the inductor voltage which is the voltage difference between grid source and DC-link capacitor, and the DC-link voltage mainly determines the current-generating capability in APF. Therefore, the DC-link voltage should be maintained at a high enough value, ensuring the APF produce the compensating currents and achieving an ideal

compensation performance [13–15]. Therefore, the value design and stable control in APF DC-link voltage are important works, and they need detailed analysis and optimized designed.

Fortunately, there are literature investigate the DC-link voltage control in APF specifically. Zhao et al. [16] analyzed the influence from the DC-link voltage on APF performance based on the Fourier transform and presents a design of DC-link voltage reference value. Cui et al. [17] analyzed the DC-link voltage control in hybrid APF under current-mode scheme, improving the DC-link voltage control during the start-up process. Hoon et al. [18] enhanced the DC-link voltage control in a three-level neutral-point diode clamped inverter based shunt APF by combining an inverted error deviation control. Luo et al. [19] proposed a hysteretic control and a controllable pulse width modulation rectifier to overcome the DC-link voltage instability in hybrid APF. Choi et al. [20] investigated the various DC-link voltage control strategies in a LC coupling hybrid APF for reactive power compensation. Mannen et al. [21] proposed a new control method with *k*-step compensator in three-phase APF to reduce the fluctuation in DC-kink voltage during load variation. Zainuri et al. [22] presented a new self-charging strategy with step size error cancellation to improve the DC-link voltage control in a shunt APF. Mannen et al. [23] proposed a novel DC-link voltage control strategy for APF with a small DC capacitor to obtain a high feedback gain for reducing the capacitor voltage fluctuation and ensuring harmonic compensation performance.

Moreover, a sufficient DC-link voltage ensures satisfactory APF compensation performance, however, a higher DC-link voltage leads to larger switching loss and noise in the APF, and vice versa [24]. Therefore, to obtain a satisfactory compensation effect with lower switching loss and noise, the minimum DC-link voltage value and the corresponding control strategies were discussed in [25,26]. The existing literature investigated the minimum DC-link voltage design based on reactive power for power quality compensator and APF, decreasing the device capacity, power consumption, and installation cost. However, the relationship between DC-link voltage and compensating current characteristic including the switching frequency harmonic current and harmonic compensating currents had not been concerned yet. Although the switching frequency harmonic current can be attenuated by applying the optimized pulse width modulation strategy and LCL filter, the above methods cannot guarantee to eliminate the switching frequency harmonic current completely under varied working conditions, and the implementation process are complicated. Thus, the switching frequency harmonic current should be considered during the compensation performance analysis, and the reason to maintain the DC-link voltage at the minimum value also needs to be discussed in detail.

Based on the analysis of minimum DC-link voltage, the controllers to maintain DC-link voltage at the minimum value were proposed. Lam et al. [27] investigated the relationship between the reactive power compensation and DC-link voltage in LC coupling hybrid APF was deduced, and proposed a minimum DC-link voltage controlled to reduce switching loss under reactive power compensation. However, the harmonic currents were not considered in this work. Then, Lam et al. [28] deduced the minimum DC-link voltage value based on harmonic currents and dynamic reactive power in LC coupling hybrid APF, and presented a minimum DC-link voltage controlled obtained the least switching loss and best compensating effect. However, the minimum DC-link voltage is determined by grid voltage, harmonic currents, reactive power and equivalent circuit parameters in APF, leading to the complicated analysis and calculation process. Moreover, the harmonic currents, reactive power and equivalent circuit parameters frequently vary in the practical applications, and the randomly variation may cause a frequent fluctuation in DC-link voltage value calculation, resulting in the deterioration and unreliability in DC-link voltage control in APF.

Thus, the relationship between the DC-link voltage and the switching frequency harmonic current and compensation performance is studied in this paper, and the reason to maintain the DC-link voltage at the minimum value is presented. Additionally, to address the shortcomings in the existing minimum DC-link voltage strategies, this paper proposed a simplified minimum DC-link voltage control strategy. The DC-link voltage value under the proposed strategy is only determined by the grid voltage and modulation index, avoiding the complex calculation of the harmonic currents,

reactive power, and equivalent circuit parameters, significantly reducing the number of calculation steps and computational burden, improving the real-time characteristic and reliability of the APF in practical implementation. Furthermore, the DC-link voltage value can vary at different levels according to the varied grid voltage, maintaining the DC-link voltage at the minimum value in varied operating conditions. Moreover, the proposed control strategy can also be applied for unbalance load compensation, enhancing the applicability of APF.

The structure of this paper is organized as follows: the relationships between the DC-link voltage, compensating current characteristic, and compensation performance are analyzed in Section 2. Based on the analysis, a simplified minimum DC-link voltage control strategy is proposed in Section 3. To verify the correctness and feasibility of the analysis and the proposed strategy, the experimental results in a shunt APF prototype are presented in Section 4. Finally, the conclusion of this study and the outlook for future work are presented in Section 5.

2. Influences of DC-Link Voltage on APF Compensation Performance

Figure 1 presents the topology of three-phase four-wire center-split shunt APF. From the figure, u_{sx} is the grid voltage, and u_{cx} is the inverter output voltage. Besides, i_{sa}, i_{sb} and i_{sc} are grid currents, i_{ca}, i_{cb} and i_{cc} are compensating currents, and i_{La}, i_{Lb} and i_{Lc} are load currents, and C_{dc} is the DC-link capacitor. U_{dc} is the DC-link voltage, where $U_{dcU} = U_{dcL} = 0.5U_{dc}$. R is the equivalent resistance of inductor. A resistance R_L and a three-phase full bridge rectifier constitute the non-linear load. The LCL filter is consisted of L_C, L_G, C_F, and the LCL filter is simplified to be an inductor with the value $L = L_C + L_G$.

From Figure 1, the single-phase equivalent circuit for each phase is presented in Figure 2. From the figure, the inverter output voltage is:

$$u_{cx} = u_{sx} + u_{Lx} = u_{sx} + R \times i_{cx} + L \times \frac{di_{cx}}{dt} \quad (1)$$

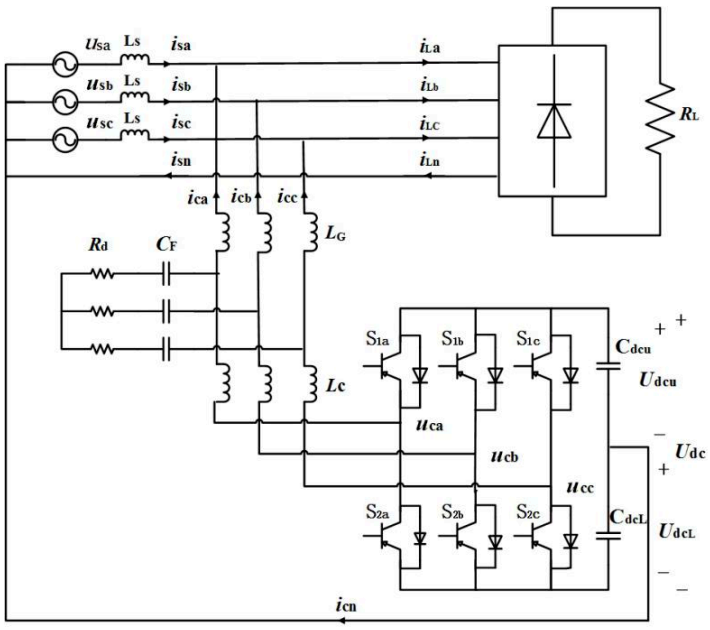


Figure 1. Topology of three-phase four-wire center-split shunt APF.

From Equation (1), the inverter voltage in APF can be calculated by grid voltage, equivalent inductance, equivalent resistance, and compensating current.

Generally, the non-linear load currents i_{L} contains the fundamental current i_{L1} and harmonic currents i_{Lh}:

$$i_{\mathrm{L}x} = i_{\mathrm{L1}x} + i_{\mathrm{Lh}x} = I_{\mathrm{L1}x}\cos(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_{\mathrm{Ln}x}\cos(n\omega t + \theta_n) \tag{2}$$

where $I_{\mathrm{L1}x}$ and $I_{\mathrm{Lh}x}$ are the effective values of i_{L1} and $i_{\mathrm{Lh}x}$.

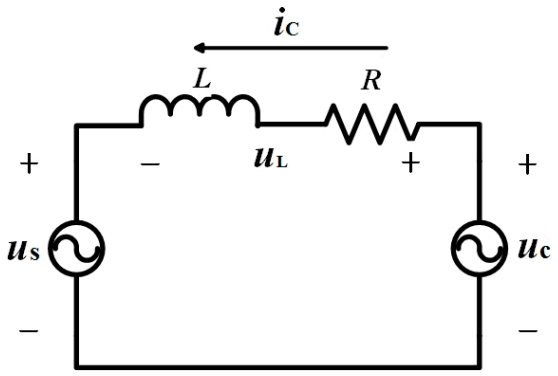


Figure 2. The single-phase equivalent circuit of APF.

Actually, APF compensating current i_{c} contains the fundamental component i_{c1}, the harmonic component i_{ch} and also the switching frequency harmonic current i_{csw}:

$$i_{\mathrm{c}x} = i_{\mathrm{c1}x} + i_{\mathrm{ch}x} + i_{\mathrm{csw}x} \tag{3}$$

In Equation (3), the fundamental current i_{c1}, which compensates system power loss and maintains the DC-link voltage, is very small during a steady-state situation, and it is neglected during a steady-state operation.

Additionally, to compensate the load harmonics, the compensation component in compensating current is equaled to the harmonic components in load current presented in Equation (2). Thus, the compensating current i_{ch} is:

$$\begin{cases} i_{\mathrm{cha}} = i_{\mathrm{Lha}} = \sum\limits_{n=2}^{\infty} I_{\mathrm{L}n}\cos(n\omega t + \theta_n) \\ i_{\mathrm{chb}} = i_{\mathrm{Lhb}} = \sum\limits_{n=2}^{\infty} I_{\mathrm{L}n}\cos[n(\omega t - 2\pi/3) + \theta_n] \\ i_{\mathrm{chc}} = i_{\mathrm{Lhc}} = \sum\limits_{n=2}^{\infty} I_{\mathrm{L}n}\cos[n(\omega t + 2\pi/3) + \theta_n] \end{cases} \tag{4}$$

Moreover, since the APF usually uses pulse width modulation (PWM) technology to generate the compensating currents, the compensating currents not only contain the required compensation component, but also contain the switching frequency harmonic current i_{csw}. Generally, the i_{csw} can be attenuated by applying the composite current tracking method, the space vector pulse width modulation (SVPWM), and optimized designed LCL filter. However, the above methods cannot guarantee eliminating the switching frequency harmonic current completely under varied working conditions, and their implementation processes are also complicated. Therefore, the switching frequency harmonic current i_{csw} should be considered during the compensating current analysis, and the switching frequency harmonic current i_{csw} can be described as:

$$i_{\mathrm{csw}x} = I_{\mathrm{csw}x}\cos(b\omega t + \theta_{\mathrm{sw}}) \tag{5}$$

where I_{csw} is the effective value of switching frequency harmonic current, and $b = f_{\mathrm{sw}}/f$.

Substituting Equations (4) and (5) into Equation (3), the APF compensating current i_c can be described as:

$$i_{cx} = i_{c1x} + i_{chx} + i_{cswx} = \sum_{n=2}^{\infty} I_{Lnx}\cos(n\omega t + \theta_n) + I_{cswx}\cos(b\omega t + \theta_{sw}) \tag{6}$$

Then, in a three-phase symmetrical power system, the grid voltages are:

$$\begin{cases} u_{sa} = \sqrt{2}U_{sn}\cos(\omega t) \\ u_{sb} = \sqrt{2}U_{sn}\cos(\omega t - 2\pi/3) \\ u_{sc} = \sqrt{2}U_{sn}\cos(\omega t + 2\pi/3) \end{cases} \tag{7}$$

where U_{sn} is the effective value of u_{sa}, u_{sb} and u_{sc}, and w is the fundamental angular frequency.

Substituting Equations (4) and (7) into Equation (1), the inverter voltages can be described as:

$$\begin{cases} u_{ca} = \sqrt{2}U_{sn} + \sum\limits_{n=1}^{\infty} I_{Ln}[R\cos(n\omega t + \theta_n) - n\omega L\sin(n\omega t + \theta_n)] \\ u_{cb} = \sqrt{2}U_{sn} + \sum\limits_{n=1}^{\infty} I_{Ln}\{R\cos[n(\omega t - \frac{2\pi}{3}) + \theta_n] - n\omega L\sin[n(\omega t - \frac{2\pi}{3}) + \theta_n]\} \\ u_{cc} = \sqrt{2}U_{sn} + \sum\limits_{n=1}^{\infty} I_{Ln}\{R\cos[n(\omega t + \frac{2\pi}{3}) + \theta_n] - n\omega L\sin[n(\omega t + \frac{2\pi}{3}) + \theta_n]\} \end{cases} \tag{8}$$

Therefore, the inverter voltage can also be expressed as:

$$u_c = u_{c1} + u_{ch} + u_{csw} = U_{c1}\cos(\omega t + \varphi_1) + \sum_{n=2}^{\infty} U_{cn}\cos(n\omega t + \varphi_n) + U_{sw}\cos(b\omega t + \varphi_n) \tag{9}$$

where u_{c1} is the fundamental component of u_c, u_{ch} is used to produce compensating currents compensating load harmonics, and u_{csw} is the inverter voltage at switching frequency.

Then, the mold length of inverter voltage vector is:

$$U_c = \| U_{c1}e^{j(\omega t+\varphi_1)} + \sum_{n=2}^{\infty} U_{cn}e^{j(n\omega t+\varphi_n)} + U_{sw}e^{j(b\omega t+\varphi_n)} \| \tag{10}$$

From Equations (7)–(10), the maximal value of inverter voltage mold is:

$$U_{c-max} = U_{c1} + \sum_{n=2}^{\infty} U_{cn} + U_{sw} = \sqrt{2}U_{sn} + R \times \sum_{n=2}^{\infty}(I_{cn} + I_{csw}) + \omega L \times \sum_{n=2}^{\infty}(nI_{cn} + I_{csw}) \tag{11}$$

To provide the sufficient DC-link voltage to generate compensating currents, the following equation needs to be satisfied:

$$U_{c\_max} = \frac{m}{2}U_{dc} \tag{12}$$

where m is modulation index.

To compensate harmonic currents, the APF needs to produce a voltage exceed the maximal value of inverter voltage vector mold. From Equation (12), the minimum DC-link voltage can be obtained:

$$U_{dc\_min} = \frac{2}{m}U_{c-max} \tag{13}$$

During the steady-state operation, the DC-link voltage maintains at minimum value, and APF generates compensating currents to compensate the load harmonics. When the DC-link voltage becomes larger than the minimum value, the effective value of inverter output voltage increases. From

Equations (11)–(13), the DC-link voltage determines the ability of producing compensating currents, and following equations can be obtained:

$$\frac{m}{2}U_{\mathrm{dc}} = \sqrt{2}U_{\mathrm{sn}} + R \times \sum_{n=2}^{\infty}(I_{\mathrm{c}n} + I_{\mathrm{csw}}) + \omega L \times \sum_{n=2}^{\infty}(nI_{\mathrm{c}n} + I_{\mathrm{csw}}) \tag{14}$$

Generally, the effective value of harmonic currents I_{ch} are determined by harmonic detection algorithm calculated from the load currents, and they remain stable during steady-state operation. From Equation (14), the switching frequency harmonic current I_{sw} can be described as:

$$I_{\mathrm{csw}} = \frac{\frac{m}{2}U_{\mathrm{dc}} - \sqrt{2}U_{\mathrm{sn}} - R\sum_{n=2}^{\infty}I_{\mathrm{c}n} - \omega L\sum_{n=2}^{\infty}nI_{\mathrm{c}n}}{R + \omega L} \tag{15}$$

According to Equation (15), with the stable effective value of grid voltage U_{sn}, equivalent inductance L, equivalent resistance R and compensating harmonic currents I_{ch} calculated from load currents, the increase of DC-link voltage U_{dc} may lead to the increase in effective value of switching frequency harmonic current I_{csw}.

Generally, the total harmonic distortion (THD) is an important indicator of compensation performance, and it can be expressed as:

$$\mathrm{THD} = \sqrt{\sum_{n=2}^{\infty}\frac{{I_n}^2 + {I_{\mathrm{sw}}}^2}{{I_1}^2}} \tag{16}$$

As can be seen from Equation (16), the THD is not only affected by the nth harmonic currents I_n, but also affected by the switching frequency harmonic current I_{sw}.

Therefore, according to Equations (15) and (16), the increase of DC-link voltage U_{dc} leads to the increase of switching frequency harmonic current I_{csw}, thereby raising the THD value and deteriorate the compensation performance. Therefore, to prevent the increase of the DC-link voltage from deteriorating the compensation performance, the DC-link voltage should be maintained at the minimum value.

3. Proposed Simplified Minimum DC-Link Voltage Control Strategy

Substituting Equations (7) and (8) into Equation (1), the inverter voltage can be described as:

$$\begin{cases} u_{\mathrm{ca}} = \sqrt{2}U_{\mathrm{sn}} + \sum_{n=2}^{\infty} I_{\mathrm{L}n}[R\cos(n\omega t + \theta_n) - n\omega L\sin(n\omega t + \theta_n)] \\ u_{\mathrm{cb}} = \sqrt{2}U_{\mathrm{sn}} + \sum_{n=2}^{\infty} I_{\mathrm{L}n}\{R\cos[n(\omega t - \frac{2\pi}{3}) + \theta_n] - n\omega L\sin[n(\omega t - \frac{2\pi}{3}) + \theta_n]\} \\ u_{\mathrm{cc}} = \sqrt{2}U_{\mathrm{sn}} + \sum_{n=2}^{\infty} I_{\mathrm{L}n}\{R\cos[n(\omega t + \frac{2\pi}{3}) + \theta_n] - n\omega L\sin[n(\omega t + \frac{2\pi}{3}) + \theta_n]\} \end{cases} \tag{17}$$

Make the transformation of the inverter voltages from the stationary abc coordinate system to the stationary α-β coordinate system with coordinate transformation formula $\mathrm{T}_{\mathrm{abc}\text{-}\alpha\beta}$:

$$\begin{bmatrix} u_{\mathrm{c}\alpha} \\ u_{\mathrm{c}\beta} \end{bmatrix} = \mathrm{T}_{\mathrm{abc}-\alpha\beta}\begin{bmatrix} u_{\mathrm{ca}} \\ u_{\mathrm{cb}} \\ u_{\mathrm{cc}} \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_{\mathrm{ca}} \\ u_{\mathrm{cb}} \\ u_{\mathrm{cc}} \end{bmatrix} \tag{18}$$

Substituting Equation (17) into Equation (18), the inverter voltages in the stationary α-β coordinate are:

$$\begin{cases} u_{c\alpha} = \sqrt{2}U_{sn} + \sum_{n=2}^{\infty} I_{Ln}[R\cos(n\omega t + \theta_n) - n\omega L\sin(n\omega t + \theta_n)] \\ u_{c\beta} = \frac{1}{\sqrt{3}}\{3\sqrt{2}U_{sn} + R\sum_{n=2}^{\infty} I_{Ln}[\cos(n\omega t + \theta_n) + 2\cos[n(\omega t - \frac{2\pi}{3}) + \theta_n] - n\omega L\sum_{n=2}^{\infty} I_{Ln}[\sin(n\omega t + \theta_n) + 2\sin[n(\omega t - \frac{2\pi}{3}) + \theta_n]\} \end{cases} \quad (19)$$

In Equation (19), since the values of harmonic components and their arithmetic combinations are small compared with effective value of grid voltage U_{sn}, they can be ignored to simplify the calculation. Therefore, the mold length of the inverter output voltage vector is:

$$|U_c| = \sqrt{u_{c\alpha}^2 + u_{c\beta}^2} = \sqrt{2}U_{sn} \quad (20)$$

To produce compensating currents to eliminate the load harmonics, the APF inverter voltage exceeds the maximal value of inverter voltage vector. Substituting Equation (20) into Equation (13), the following equation is obtained:

$$U_{dc\_min} = \frac{2}{m}\sqrt{2}U_{sn} + U_{mar} \quad (21)$$

where U_{mar} is the voltage margin with a small value to control the switching frequency harmonic current and other factors.

The control diagram of the proposed strategy is presented in Figure 3. From the figure, the DC-link voltage reference value is initially set to be a minimum value calculated by the grid voltage and modulation index according to Equation (21), reducing the power consumption and switching loss. Additionally, the grid voltage may vary occasionally in practical application, leading to the frequent change of DC-link voltage reference value. To solve this issue, the DC-link voltage value under the proposed strategy is classified into certain levels according to different ranges of the grid voltage for selection. Thus, the reference DC-link voltage maintains at a constant value within a specific range. Furthermore, the DC-link voltage reference value under proposed strategy varies adaptively with the change of grid voltage, maintaining DC-link voltage at the minimum value in varied operating conditions.

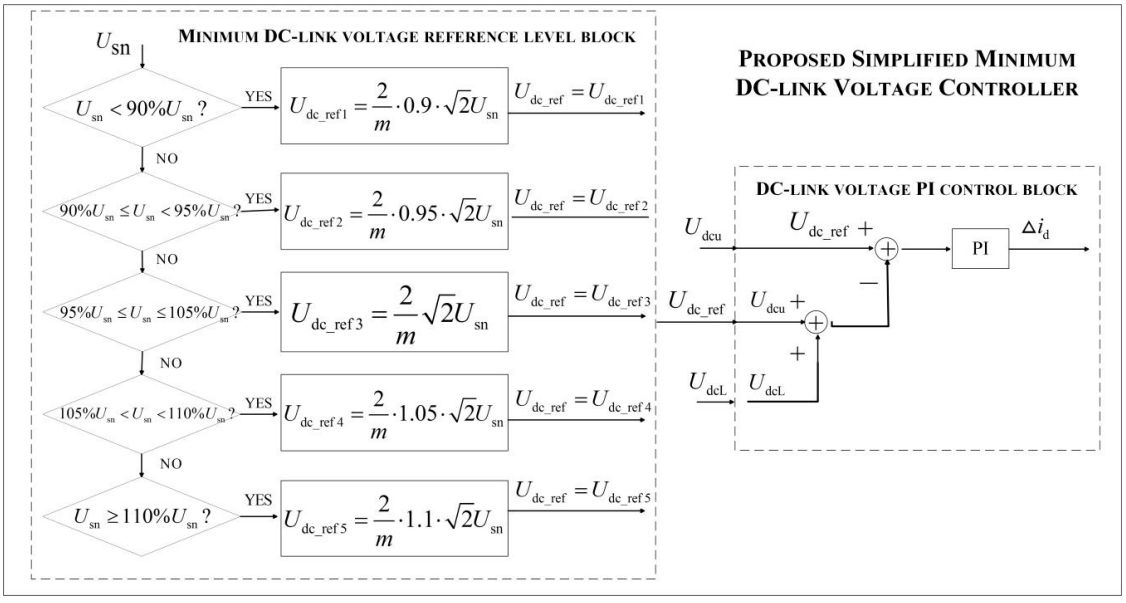


Figure 3. The control block of proposed simplified minimum DC-link voltage control strategy.

Compared with the existing minimum DC-link voltage control strategy, the proposed minimum DC-link voltage is only determined by the grid voltage and modulation index, avoiding the influence from variations of equivalent parameters, reactive power and harmonic currents, thus improving the stability, reliability, and real-time characteristic of APF. Additionally, the proposed DC-link voltage minimum value avoids complex calculation of equivalent parameters, harmonic currents, and reactive power, reducing the calculation burden of processor. The comparison of calculation burden between the conventional and the proposed minimum DC-link voltage control strategy is listed in Table 1. The minimum DC-link voltage calculation in [27] contains four additions and subtractions and 16 multiplications and divisions, and the calculation in [28] contains 20 additions and subtractions and eight multiplications and divisions. This brings a large calculation burden to the processor. By applying the proposed strategy, the addition and subtraction calculations are not needed, and the number of the multiplication and division reduces to three, thus reducing the calculation burden on processor and improving the real-time characteristics for APF.

Table 1. Comparison of calculation burden under proposed and conventional strategies.

Minimum DC-Link Voltage Strategy	Addition and Subtraction Times (Within the 20th Harmonics)	Multiplication and Division Times (Within the 20th Harmonics)
Strategy in Ref. [27]	4	16
Strategy in Ref. [28]	20	8
Proposed Strategy	0	3

4. Experiment Verification

Figure 4 presents a shunt APF prototype established in laboratory, and the parameters are shown in Table 2. Without APF, the grid current contains a large number of harmonics, and the THD of the experimental grid current is 23.63%. Based on the deduction, the APF minimum DC-link voltage under the proposed simplified strategy can be calculated from Equation (21). Thus, with the grid voltage U_{sn} = 220 V, the minimum DC-link voltage $U_{dc\text{-}ref}$ = 630 V. When the U_{dc} = 620 V, lower than minimum value 630 V, the experimental results are shown in Figure 5. From the figure, the grid current after compensation still contains a large number of harmonics, and it is not an ideal sine waveform. Furthermore, the grid current THD after compensation is 11.05%, and it does not ideally compensate performance. The results illustrate that, when U_{dc} is lower than the minimum value, APF cannot largely compensate the harmonics and achieve an ideal compensation performance.

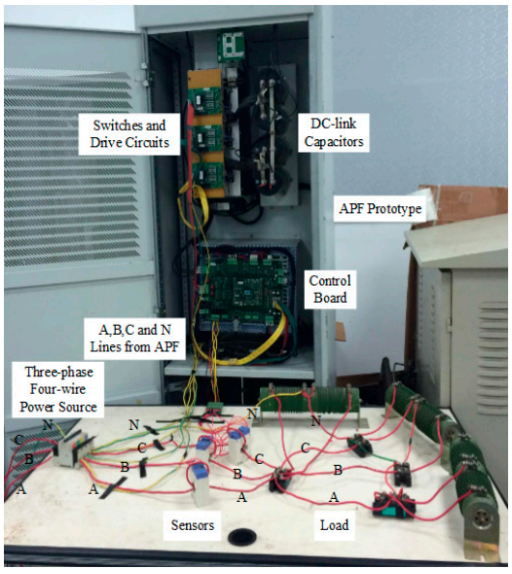


Figure 4. The APF prototype.

Table 2. Parameters of APF prototype and experimental setup.

Parameters	Symbol	Value
Grid Voltage	U_{sn}	220 V
Grid Frequency	f	50 Hz
Switching Frequency	f_{sw}	9.6 kHz
Equivalent Inductance	L	0.45 mH
Equivalent Resistance	R	0.2 ohm
DC-link Capacitance	C_{dcu}, C_{dcL}	10,000 uF

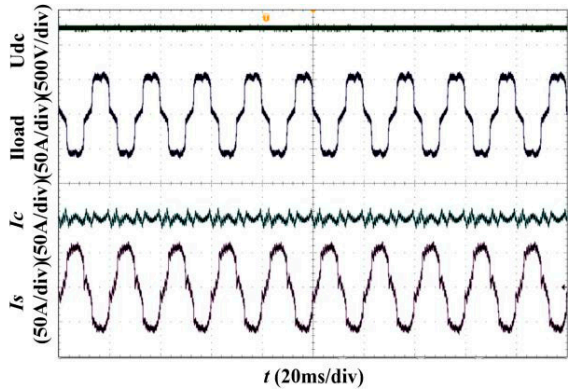


Figure 5. Voltage and current waveforms when U_{sn} = 220 V and $U_{dc\text{-}ref}$ = 620 V.

Then, when U_{dc} = 640 V, higher than the minimum value 630 V, the experimental results are shown in Figure 6a. The load harmonics are greatly compensated, and the grid currents are nearly sinusoidal waveforms. Additionally, the grid current distortions are almost eliminated, and the grid current THD after compensation is 5.65%, thus satisfying the international standards. In addition, the experimental voltages and currents with U_{dc} = 660 V are shown in Figure 6b. Compared with the voltages and currents with U_{dc} = 640 V and U_{dc} = 660 V, the grid currents after compensation are both nearly sinusoidal waveforms, and harmonic components are largely compensated. Therefore, when the DC-link voltage becomes higher than the minimum value, the APF achieves an ideal compensation performance.

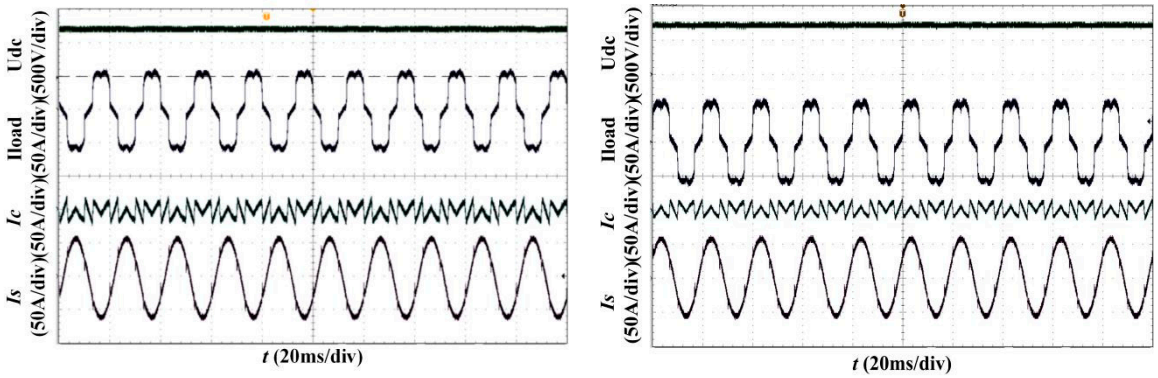


Figure 6. Voltage and current waveforms when U_{sn} = 220 V, $U_{dc\text{-}ref}$ = 640 V and 660 V. (**a**) $U_{dc\text{-}ref}$ = 640 V; and (**b**) $U_{dc\text{-}ref}$ = 660 V.

With the increase of DC-link voltage value, the THD values of simulation and experiment grid current after compensation with the different U_{dc} are presented in Table 3, and the THDs with different DC-link voltages are presented in Figure 7. The results illustrate that, when the DC-link voltage becomes lower than the minimum value, APF cannot compensate harmonics completely, and the

compensation performance even deteriorates with the decrease of DC-link voltage. Additionally, when the DC-link voltage becomes larger than the minimum value, the increase of DC-link voltage cannot improve the APF compensation performance, but increases the THD of grid current and deteriorates the compensation effect.

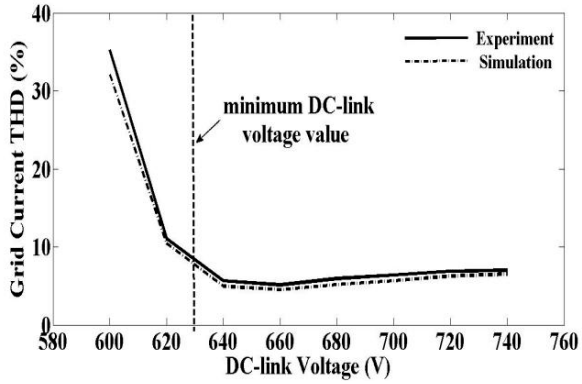


Figure 7. The grid current THD value with the variation of the DC-link voltage.

Although the THDs of grid currents with varied DC-link voltages are different, it is difficult to recognize from the voltage and current waveforms. Thus, the values of compensating current in each order with varied DC-link voltages are presented in Table 4. From the table, with the increase of the DC-link voltage, the values of each order in compensating currents vary slightly, due to the compensating currents strictly following the reference compensating currents obtained from the harmonic detection section. However, the switching frequency harmonic current increase obviously with the increase of the DC-link voltage. As mentioned above, the THD is calculated with every order in compensating the current, including the switching frequency harmonic current. Therefore, the increase of the DC-link voltage leads to the increase of the switching frequency harmonic current, leading to the increase of the THD value, but not the improvement of the compensation effect, and the influence becomes more serious with the further increase of the DC-link voltage. Therefore, when the DC-link voltage is higher than the minimum value, the increase of the DC-link voltage cannot improve, but brings the deterioration in the compensation effect. To avoid the deterioration in the compensation and achieve an ideal compensation performance, the DC-link voltage should be maintained at a minimum value.

Moreover, when the effective value of grid voltage varies form U_{sn} = 220 V to 198 V, the required minimum DC-link voltage value changes to $U_{dc\text{-}ref}$ = 575 V accordingly. Under the proposed strategy, the DC-link voltage varies adaptively and maintains at a new minimum value, as shown in Figure 8. Additionally, the dynamic behavior of currents during the transient is not obvious. This is because the transient is not caused by a variation of the load, but caused by a variation of the grid voltage, resulting in a variation of the DC-link voltage. In the APF, the dynamic in current control loop is much faster than that in voltage control loop, thus the disturbance from the voltage loop causes a very small current distortion during the transient. Thus, with the DC-link voltage obtained by the proposed strategy, the load harmonic currents are still significantly compensated and the grid current distortion is almost eliminated. After compensation, the THD of the grid current is 5.52%. The results verify that, under the proposed strategy, the DC-link voltage can vary adaptively to maintain the minimum value with the varied grid voltage situation and ensure the ideal APF compensation performance.

Table 3. Comparison of THD values with different DC-link voltages.

Cases		THD Value	
		Simulation	**Experiment**
Without APF		22.39%	23.63%
DC-link Voltage	600 V	32.08%	35.25%
	620 V	10.42%	11.05%
	640 V	4.94%	5.65%
	660 V	4.53%	5.52%
	680 V	5.08%	5.82%
	700 V	5.47%	6.17%
	720 V	5.96%	6.58%
	740 V	6.22%	6.82%

Table 4. The values of compensating current in each order with varied DC-link voltages.

Current Orders	640 V	660 V	680 V	740 V
Fundamental	45.88 A	46.85 A	46.55 A	46.87 A
5th	8.57 A	8.59 A	8.58 A	8.59 A
7th	4.25 A	4.32 A	4.30 A	4.32 A
11th	3.41 A	3.43 A	3.43 A	3.35 A
13th	2.39 A	2.45 A	2.39 A	2.41 A
17th	2.21 A	2.22 A	2.22 A	2.21 A
19th	1.65 A	1.68 A	1.65 A	1.68 A
23rd	1.55 A	1.56 A	1.57 A	1.57 A
25th	1.30 A	1.32 A	1.31 A	1.31 A
29th	1.18 A	1.20 A	1.19 A	1.20 A
Switching Frequency	0.55 A	0.73 A	0.82 A	0.95 A

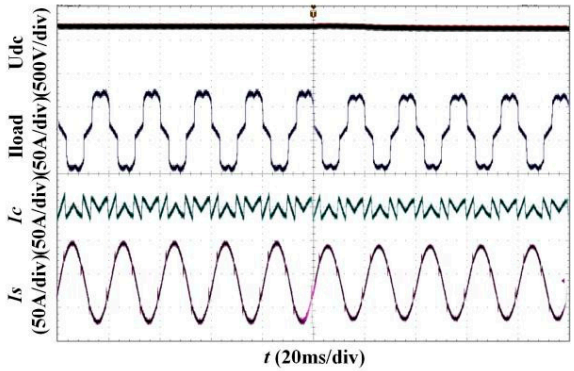
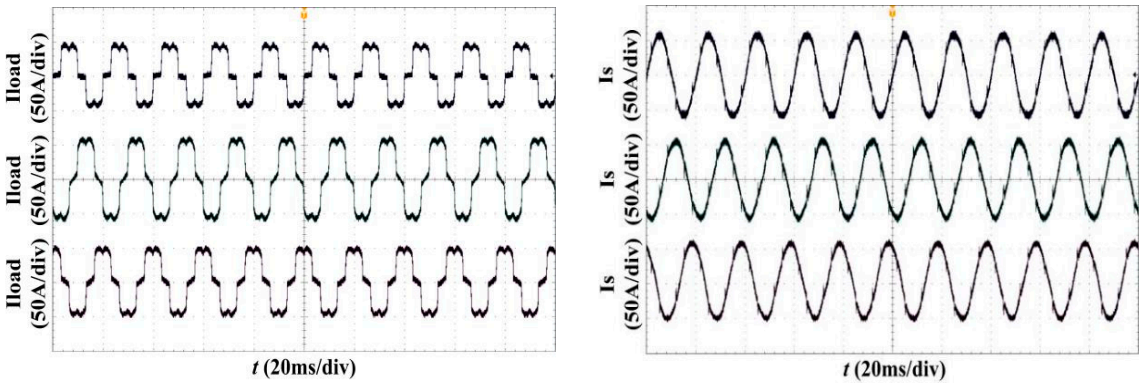


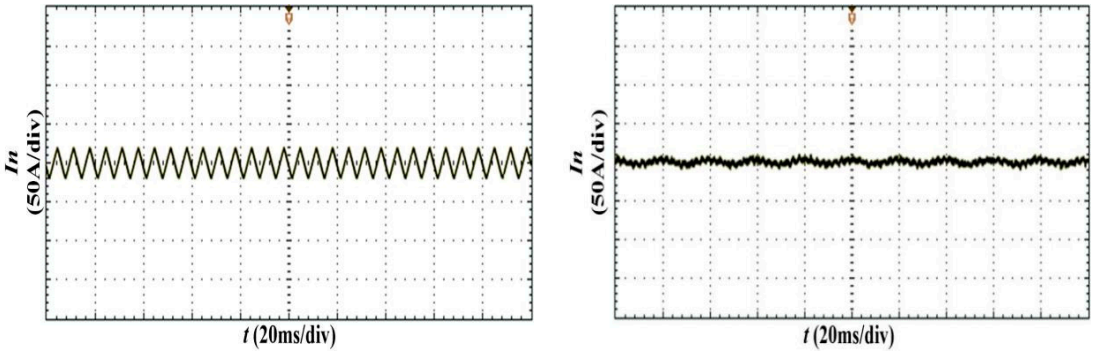
Figure 8. Voltage and current waveforms when the grid voltage U_{sn} varies from 220 V to 198 V.

Furthermore, the experiment results in an unbalanced load are shown in Figure 9. From the figures, the grid current in a, b, and c phases before compensation are 35.8 A, 45.3 A, and 37.8 A, respectively. When applying the proposed strategy in APF, the load harmonics are greatly compensated, and the grid currents are all sinusoidal waveforms and 45.2 A, 46.8 A, and 45.8 A in a, b, and c phase, respectively. Moreover, the neutral line current is i_n = 11.2 A with the unbalance load, as shown in Figure 10a. After compensation by the APF under the proposed the DC-link voltage strategy, the neutral current drops to about i_n = 1.7 A, as shown in Figure 10b. The experimental results show that the APF under proposed DC-link voltage strategy can also compensate the neutral current in unbalanced load application, reducing the influence from neutral current to the system, and the unbalanced load phenomenon is eliminated effectively. Therefore, the proposed strategy can be applied in the unbalanced load situation and also achieves an ideal APF compensation performance.



(**a**) (**b**)

Figure 9. Three-phase load and grid currents with the unbalance load when U_{sn} = 220 V and $U_{dc\text{-}ref}$ = 640 V. (**a**) Before compensation; and (**b**) after compensation.



(**a**) (**b**)

Figure 10. Neutral line current with the unbalance load when U_{sn} = 220 V and $U_{dc\text{-}ref}$ = 640 V. (**a**) Without compensation; and (**b**) with compensation.

5. Conclusions

This paper analyzes the influence from DC-link voltage on the APF compensating current characteristic and compensation performance, and establishes the relationships between the DC-link voltage and switching frequency harmonic current is established. The increase of the DC-link voltage may lead to the increase of the switching frequency harmonic current, thus raising the THD value and deteriorating the compensation performance. Thus, to achieve an ideal compensation performance, and to reduce switching loss and power consumption in the APF, the DC-link voltage should be maintained at the minimum value level.

On this basis, a simplified minimum DC-link voltage control strategy for the APF is proposed. Compared with the existing minimum DC-link voltage strategies, the reference DC-link voltage in the proposed strategy is only determined by the grid voltage and the modulation ratio, avoiding the complex calculation of harmonic currents, reactive power, and equivalent parameters, reducing the calculation burden of the processor and improving the real-time characteristic and reliability of the APF in practical implement. Therefore, the proposed strategy can be an optimized solution for the APF in practical application.

Author Contributions: All authors contributed improving the quality of the manuscript. Specifically, Y.W. conceptualized the idea of this research, carried out the theoretical analysis, and performed the experiments. Y.W. contributed to the design of the methodology and experiments, writing, and revising the paper. S.C. provided important comments on the structure, language, and format of the paper. G.Z. designed the methodology and experiment setup. Y.Z. contributed to the writing and revising the paper.

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