

Article

Conducted EMI Prediction and Mitigation Strategy Based on Transfer Function for a High-Low Voltage DC-DC Converter in Electric Vehicle

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Abstract: The high dv/dt and di/dt outputs from power devices in a high-low voltage DC-DC converter on electric vehicles (EVs) can always introduce the unwanted conducted electromagnetic interference (EMI) emissions. A conducted EMI prediction and mitigation strategy that is based on transfer function for the high-low voltage DC-DC converter in EVs are proposed. A complete test for the DC-DC converter is conducted to obtain the conducted EMI from DC power cables in the frequency band of 150 kHz-108 MHz. The equivalent circuit with high-frequency parasitic parameters of the DC-DC converter is built'1 based on the measurement results to acquire the characteristics of the conducted EMI of the DC power cables. The common mode (CM) and differential mode (DM) propagation coupling paths are determined, and the corresponding transfer functions of the DM interference and CM interference are established. The simulation results of the conducted EMI can be obtained by software Matlab and Computer Simulation Technology (CST). By analyzing the transfer functions and the simulation results, the dominated interference is the CM interference, which is the main factor of the conducted EMI. A mitigation strategy for the design of the CM interference filter based on the dominated CM interference is proposed. Finally, the mitigation strategy of the conducted EMI is verified by performing the conducted voltage experiment. From the experiment results, the conducted voltage of the DC power cables is decreased, respectively, by 58 dBµV, 55 dBµV, 65 dBµV, 53 dBµV, and 54 dBµV at frequency 200 kHz, 400 kHz, 600 kHz, 1.4 MHz, and 50 MHz. The conduced voltage in the frequency band of 150 kHz-108 MHz can be mitigated by adding the CM interference filters, and the values are lower than the limit level-3 of CISPR25 standard (GB/T 18655-2010).

Keywords: electric vehicle; high-low voltage DC-DC converter; conducted EMI; transfer function; EMI filter design

1. Introduction

Electric vehicles, as the new energy products of energy conservation and environmental protection, have gradually become the focus of consumers' attention [1]. With the development of modern science and technology, more and more electrical and electronics equipment have been used in electric vehicles (EVs). Especially, in the narrow space of EVs, not only the high-voltage system, including the motor drive system, DC-DC converter system, and on-board charger, etc., but also the low-voltage system,



such as the battery management system (BMS), the vehicle control units (VCU), and malfunction detecting and recording instrument are applied [2]. Therefore, electromagnetic compatibility (EMC) for EVs becomes more and more important.

The fast switching of these power semiconductor devices like MOSFET, IGBT, used in the high-low voltage DC-DC converter is controlled by pulse width modulation (PWM), resulting in the conducted electromagnetic interference (EMI) of EVs. Besides, the conducted-EMI may generate some radiated EMI to influence or even damage a part of onboard components, such as wireless devices, analog devices, sensors of EVs, etc. Therefore, predicting and suppressing the conducted-EMI is very significant for the high-low voltage DC-DC converter of the EVs.

At present, for radio disturbance characteristics, CISPR25 standard has defined the limits and the methods of measurement for the protection of on-board receivers [3]. The design and verification of the products for EVs should comply CISPR25 standard to ensure the EMC of the whole vehicle. A large number of tests for the low voltage systems on-board have been carried out, till 2012, the high voltage components in frequency band of 150 kHz–108 MHz can be tested by the CISPR25 standard. Unfortunately, many of the experimental results for the high voltage system cannot satisfy the requirements of CISPR25 standard. From the results and analysis of the measurements, the conducted voltage can exceed the limit level of CISPR25 standard due to the operation of the motor drive system and the DC-DC converter [4]. Although some studies about the conducted EMI from the high-voltage systems in EVs, such as the motor drive system have been carried out [5–9], few researches on the conducted-EMI for the high-low voltage DC-DC converter was presented previously to study the characteristics of the conducted-EMI and the models.

In industry application, the analysis and measurement of EMC for DC-DC converters used in switching over have been presented [10]. The design of the EMC filter on PCB boards in switching power is only used to mitigate the conducted EMI from PCB [11,12]. However, the DC-DC converter that is used in industry is different from that in EVs at the environment and operation characteristics, like voltage and frequency, and so on.

In the field of EVs, most of the conducted EMI researches are also carried out for low voltage DC-DC converters integrated on PCB boards of various ECUs. The modeling and the measurement for conduction emission based on MIL-STD-461F method have been presented [13]. The conducted EMI for DC-DC converter of PCB board mainly includes the influence of parasitic parameters, switching technology, and optimization layout based on port network theory [14–19]. However, the existence of difference are found between the high-low voltage DC-DC converter of the high voltage system and the low voltage DC-DC converter of PCB, which are both used in electric vehicles, is described as below: First, the input voltage of the high-low voltage DC-DC converter can reach a few hundred volts from 300 V to 600 V, and the output is 12 V to 24 V to power the low-voltage on-board equipment. But, the input or output voltage of the DC-DC converter on the PCB is usually from 12 V to 24 V. Second, when comparing with the DC-DC converters on PCB, the voltage, the current and the power of the power device used in the high-low voltage DC-DC converters are larger. Third, the electrical load of high-low voltage DC-DC converters varies greatly in real time. Finally, the topological structure and the geometry size are also different. Therefore, to predict and suppress the conducted-EMI of the high-low voltage DC-DC converters is pretty significant.

Although there are many researches on the EMI mechanism and the modeling of high-low voltage DC-DC converter, their models for EMC are established based on port network theory and black box theory. In addition, the detailed model with high frequency parasitic parameters is not established [20–22]. Then, it is hard to determine the conducted interference paths of the common mode (CM) and differential mode (DM) in detailed due to no model. In addition, most of the design method and the analysis for EMI filtering are based on the source impedance and the load impedance, but these impedances are not constant in practice [23–25]. The impedance mismatch may result in the inadequate mitigation and generation of new resonance.

Based on the problems proposed above, first of all, it is necessary to establish an equivalent circuit with high-frequency parasitic parameters of the high-low zero-voltage-switching (ZVS) DC-DC converter for EV to predict the conducted-EMI. Equivalent circuits with high-frequency distributed parameters of the DM interference and the CM interference are built, in order to predict the conducted voltage and to analyze the forming mechanism of the conducted interference, where the impedance of the practical EMI source and the load can be taken into consideration. Then, establishing the transfer functions of the DM interference and the CM interference to predict and determine the dominated interference mode that is responsible for EMI from the high-low DC-DC converter in EVs. Meanwhile, the simulation results' comparison between CM, DM, and CM+DM interference is performed to find the dominated interference mode for conducted EMI. Lastly, a strategy to determine the dominated interference mode is proposed for designing filter.

This paper is organized as follows: Section 2 presents a full test for high-low voltage DC-DC converter to obtain the conducted interference voltage in range of 150 kHz–108 MHz, and sets up a high frequency circuit model to analyze the paths of CM and DM interference. Section 3 predicts and analyzes the conducted interference through the transfer functions and the simulation results of CM, DM, and their hybrid mode. Next, Section 4 designs the filter and simulates its suppression effect. The experiment for DC-DC converter and the test for conducted voltage are presented in Section 5 to verify the theory correctness of high frequency circuit model and the efficiency of the designed filter. Finally, in Section 6, conclusions and the next work are drawn.

2. EMI Test and Modeling Analysis for Isolated Full-Bridge DC-DC Converter

2.1. The Construction of the Onboard DC-DC Converter System

As the indispensable part of EVs, DC-DC converter is used to convert the high dc voltage of the power battery into the low dc voltage to provide power for the low voltage electrical loads. This high-low voltage DC-DC converter system mainly consists of the following parts: high-voltage power battery of EV, DC-DC converter, low-voltage storage battery, and low-voltage load of EV. The Figure 1 below shows the topology of the isolated full-bridge DC-DC converter.

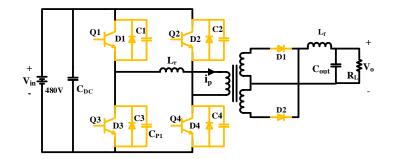


Figure 1. Topology diagram of zero-voltage-switching (ZVS) isolated full-bridge DC-DC converter.

The control mode of phase-shifting PWM is adopted in this topological structure to convert 480 V dc voltage from the power battery into 12 V dc voltage. When considering the high voltage and high frequency characteristics of the DC-DC converter, four MOSFETs, IPP65R150CFDA, with 650 dc voltage are adopted in the full-bridge topology of DC-DC converter. The rising time and falling time of the MOSFET are 7.6 ns and 5.6 ns, respectively.

2.2. Setup for Conducted-EMI Emission Test

What shown in Figure 2 is a complete test setup in an EMI laboratory to test the conducted-EMI emissions of the high-low voltage DC-DC converter. It is mainly consisted by a DC voltage source, DC power cables, and standard line impedance stabilization networks (LISNs), full-bridge DC-DC

converter, low voltage load, and an EMI receiver. What is shown in Table 1 is the conducted EMI emission limits from 150 kHz to 108 MHz for vehicle components, which is described in standard CISPR 25 (GB/T 18655-2010) complied by measurements. Two LISNs terminated with 50 Ω resistances provide DC power from a DC voltage source to the full-bridge DC-DC converter using two shielded cables (1.5 m). The full-bridge DC-DC converter with 480 V DC input is connected to the low voltage load using two shielded cables (1 m). The DC-DC converter operates at a frequency of 100 kHz. A battery with 12 dc voltage is used as the low voltage. With this configuration, the total conducted-EMI noise voltage signals of DC cables can be obtained through any one of the LISNs that is connected to an EMI receiver.

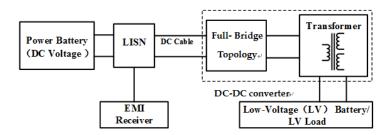


Figure 2. Test layout for the conducted electromagnetic interference (EMI) of ZVS isolated full-bridge DC-DC converter.

2.3. Experiment Results of the Conducted EMI

The test platform is set up, as shown in Figure 3. Figure 4 shows the experimental results and it can be found that the conducted-EMI noise voltage of the DC-DC converter is dominant in 150 kHz–108 MHz and does not comply with CISPR25(GB/T 18655), as shown in Table 1. In Figure 4, the blue line represents the peak value of the conduction voltage, the green line represents the mean value of the conduction voltage, and the yellow line represents the limit value of standard Level 3. From Figure 4, it can be seen that the frequency bands with excessive conducted voltage are 0.53–1.8 MHz, 5.9–6.2 MHz, 41–88 MHz and 76–108 MHz, and it also includes 200 kHz, 500 kHz–2 MHz, and 30 MHz–108 MHz. Therefore, in order to analyze the source and the paths of the conducted-EMI, the buildup of a high frequency circuit model is necessary, and then the conducted-EMI emissions can be predicted.

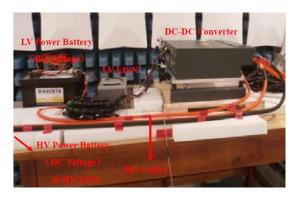


Figure 3. The conducted emission test platform for DC-DC converter.

Table 1. CISPR25 class3-average limits for conducted voltage.

Band	Frequency/MHz	Electrical Level/dB(µV)
LW	0.15-0.30	70
MW	0.53-1.8	50
SW	5.9-6.2	45
FW	76-108	30
TV Band I	41-88	36

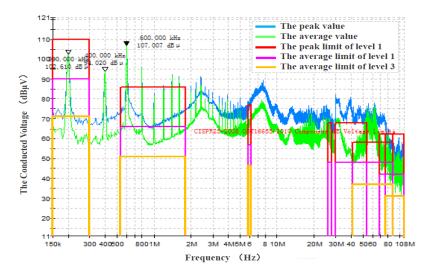


Figure 4. The experimental result of the conducted interference of DC-DC converter.

2.4. Modeling Analysis of the Onboard DC-DC Converter System

2.4.1. Noise Source

The MOSFETs of the DC-DC converter can switch fast and will cause large dv/dt and di/dt, which can introduce the conducted-EMI emissions. Therefore, the noise source signals of CM interference and DM interference can be obtained from the DC-DC converter legs by measurement. The CM interference voltage source U_{CM} and the DM interference voltage source U_{DM} will be described in detail in the next section.

2.4.2. Main Parasitic Parameter

From Figures 5 and 6, there are some parasitic parameters in the DC-DC converter system. It is necessary to extract and determine the parasitic parameters, so that the DC-DC converter for the conducted-EMI can be modeled. Some measurements for Z parameters and S parameters were made with a vector network analyzer and time-domain reflectometry. In order to obtain the high-frequency circuit model of element and system, a modeling method, which is based on a measurement-based model of the electromagnetic emissions, needs to be used. By comparing Z parameters and S parameters of the simulation and measurement, the values of elements, like inductance or capacitance, can be regulated and determined, as shown in Table 2, where, $C_{Q1}-C_{Q4}$ represent the resonant capacitance that is in parallel with MOSFETs Q1–Q4 respectively to achieve ZVS, L_r represents the resonant inductance to achieve ZVS, C_{DC} , L_f , and C_{out} are all filtering elements, R_1 , R_2 , L_1 , L_2 , C_1 – C_4 represent the components of LISN, R_L represent the equivalent resistance of the load, L_s and R_s are the high-frequency parasitic parameters of C_{DC} , C_{p1} , and C_{p2} called the distributed capacitance between the chassis and the midpoints of the leading leg and the lagging leg, C_{ps1} and C_{ps2} represent the chassis. All of these parameters are labeled in Figures 5 and 6.

2.4.3. High Frequency Parasitic Parameters of Common Mode EMI

The common mode noise is generated by the displacement current, flowing from the CM interference voltage source U_{CM} to the DC power cables by the parasitic parameters that were connected with the chassis. C_{p1} , C_{ps1} , C_{ps2} , and C_L are the dominated parasitic parameters, which result in CM interference. The main CM paths are shown in Figure 5a. According to Figure 5a, CM paths of U_{CM1} and U_{CM2} have similar structures, so only the equivalent circuits of U_{CM1} are shown in

Figure 5b. The four loops for the CM EMI propagation paths through the components can be listed, as follows:

- Loop 1 for CM1: $U_{CM1} \rightarrow C_{p1} \rightarrow U_{CM1}$ •
- Loop 1 for CM2: $U_{CM2} \rightarrow C_{p2} \rightarrow U_{CM2}$
- Loop 1 for CM2: $U_{CM2} \rightarrow C_{p2} \rightarrow U_{CM2}$ Loop 2 for CM1: $U_{CM1} \rightarrow C_L \rightarrow \binom{C_{out}}{R_L} \rightarrow L_f \rightarrow C_{ps1} \rightarrow L_r \rightarrow U_{CM1}$ Loop 2 for CM2: $U_{CM2} \rightarrow C_L \rightarrow \binom{C_{out}}{R_L} \rightarrow L_f \rightarrow C_{ps2} \rightarrow U_{CM2}$ Loop 3 for CM1: $U_{CM1} \rightarrow \binom{C_3 \rightarrow R_1}{C_1 \rightarrow L_1} \rightarrow L_{p1} \rightarrow U_{CM1}$ Loop 3 for CM2: $U_{CM2} \rightarrow \binom{C_2 \rightarrow L_2}{C_4 \rightarrow R_2} \rightarrow L_{p2} \rightarrow U_{CM2}$ Loop 4 for CM1: $U_{CM1} \rightarrow \binom{C_2 \rightarrow L_2}{C_4 \rightarrow R_2} \rightarrow C_{Q3} \rightarrow L_{p2} \rightarrow U_{CM1}$ Loop 4 for CM2: $U_{CM2} \rightarrow \binom{C_3 \rightarrow R_1}{C_1 \rightarrow L_1} \rightarrow L_{p1} \rightarrow C_{Q3} \rightarrow U_{CM2}$ •
- •
- •
- •

Table 2. The common mode (CM) and differential mode (DM) parameters' value of the equivalent circuit elements.

Circuit Element	Value	Circuit Element	Value	Parameter	Value
C _{Q2}	1000 pF	R_2	50 Ω	C_{p1}	26 pF
C_{Q3}	1000 pF	L_1	50 µH	C_{ps1}	60 pF
$\tilde{L_r}$	30 µH	L_2	50 µH	$\dot{C}_{\rm L}$	80 pF
L_{f}	50 µH	C_1	5 µF	L_{s}	0.2 µH
$R_{ m L}$	$0.48 \ \Omega$	C_2	5 µF	R_{s}	0.1Ω
$C_{\rm out}$	2000 µF	C_3	470 nF	L_{p1}	10 nH
R_1	50 Ω	C_4	470 nF	L_{p2}	10 nH

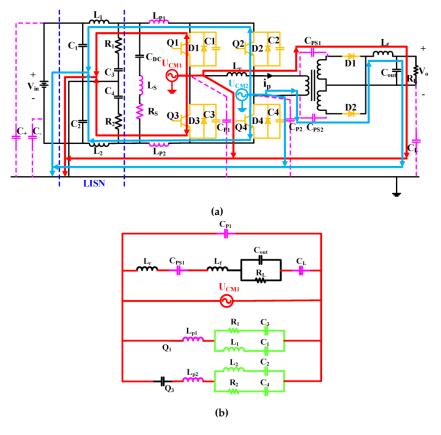


Figure 5. (a) The main common-mode paths and (b) its equivalent circuit.

The MOSFET in the closed state is equivalent to short circuit, and it can be represented by conductor; the MOSFET in the open state is replaced by the capacitor in parallel. In addition, no matter which MOSFET produces interference noise, it will always cause the rapid change of the voltage and the current at the midpoint of the bridge leg, so it is most appropriate to choose the middle point of the bridge as the interference source.

2.4.4. High Frequency Parasitic Parameters of Differential Mode EMI

Similarly, due to the existence of the main DM parasitic parameters, The DM interference can flow through these parasitic inductances and the DM parasitic parameter of the input capacitor to form the DM interference paths. These main parasitic parameters are L_p , R_s , L_{p1} , and L_{p2} . Similarly, it can be known that the structures of the DM interference paths of U_{DM1} and U_{DM2} are similar. The main DM paths and the equivalent circuits of U_{DM1} are shown in Figure 6a,b, respectively. The two loops for the DM EMI propagation paths can be listed, as follows:

- Loop 1 for DM1: $U_{DM1} \rightarrow L_{p1} \rightarrow \begin{pmatrix} L_1 \rightarrow C_1 \\ R_1 \rightarrow C_3 \end{pmatrix} \rightarrow \begin{pmatrix} C_2 \rightarrow L_2 \\ C_4 \rightarrow R_2 \end{pmatrix} \rightarrow L_{p2} \rightarrow C_{Q3} \rightarrow U_{DM1}$ Loop 1 for DM2: $U_{DM2} \rightarrow C_{Q1} \rightarrow L_{p1} \rightarrow \begin{pmatrix} L_1 \rightarrow C_1 \\ R_1 \rightarrow C_3 \end{pmatrix} \rightarrow \begin{pmatrix} C_2 \rightarrow L_2 \\ C_4 \rightarrow R_2 \end{pmatrix} \rightarrow L_{p2} \rightarrow U_{DM2}$
- Loop 2 for DM1: $U_{DM1} \rightarrow L_{p1} \rightarrow C_{DC} \rightarrow L_s \rightarrow R_s \rightarrow L_{p2} \rightarrow C_{Q3} \rightarrow U_{DM1}$
- Loop 2 for DM2: $U_{DM2} \rightarrow C_{Q2} \rightarrow L_{p1} \rightarrow C_{DC} \rightarrow L_s \rightarrow R_s \rightarrow L_{p2} \rightarrow U_{DM2}$

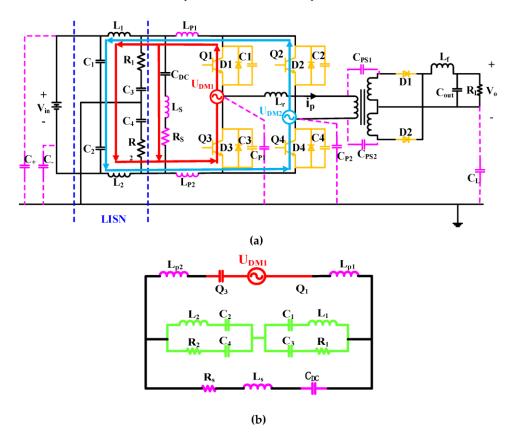


Figure 6. (a) The main differential-mode paths and (b) its equivalent circuit

3. Characteristics Analysis and Simulation Prediction for the Conduction Interference

3.1. The Establishment of Transfer Functions

Each noise source can be equivalent to a linear system with single input and single output. Therefore, the two CM transfer functions can be linearly equivalent to the Equation (3), and it is the same to the two DM EMI sources. According to the equivalent circuit of common mode interference

paths, the corresponding transfer function of U_{CM1} is established, as shown in Equation (1), and the Equation (2) can be obtained by substituting the values that are provided in Table 2.

$$G(s)_{\rm CM1} = \frac{U_{O_CM1}}{U_{\rm CM1}} = \frac{\frac{R_1\left(sL_1 + \frac{1}{sC_1}\right)}{\left(\frac{1}{sC_3} + R_1\right) + \left(sL_1 + \frac{1}{sC_1}\right)}}{\frac{\left(\frac{1}{sC_3} + R_1\right)\left(sL_1 + \frac{1}{sC_1}\right)}{\left(\frac{1}{sC_3} + R_1\right) + \left(sL_1 + \frac{1}{sC_1}\right)} + sL_{p1}}$$
(1)

$$G(s)_{\rm CM1} = \frac{2.35 \times 10^{11} s^3 + 9.4 \times 10^{20}}{47s^4 + 2.35 \times 10^{11} s^3 + 10^{16} s^2 + 9.4 \times 10^{20} s + 4 \times 10^{25}}$$
(2)

$$U_{\rm CM_{-}O} = G(s)_{\rm CM1} \times U_{\rm CM1} + G(s)_{\rm CM2} \times U_{\rm CM2}$$
(3)

The Bode diagram, as shown in Figure 7, can be obtained by the transfer function of Equation (2). From Figure 7, it can be seen that large CM conducted interference exists within 150 kHz–30 MHz. The interference is especially obvious in the lower frequency band before 300 kHz, and it begins to drop at 30 MHz. Hence, it can be seen that the CM conducted interference mainly exists in the frequency bands before 30 MHz.

Similarly, the transfer function of the DM1 interference paths can be obtained, as shown in Equation (5), and Equation (6) is its numerical expression. The DM bode diagram that is obtained by the transfer function (7) is shown in Figure 8. From Figure 8, it shows that the DM conducted interference is relatively smaller in low frequency band, and there exists a peak value at frequency from 30 MHz to 40 MHz due to the circuit resonance. Therefore, it can be known from Figures 7 and 8 that CM interference is the dominated interference in the frequency band from 150 kHz to 108 MHz.

$$Z_{\text{LISN}(\text{DM})} = \frac{\left(\frac{1}{sC_3} + R_1\right)\left(sL_1 + \frac{1}{sC_1}\right)}{\left(\frac{1}{sC_3} + R_1\right) + \left(sL_1 + \frac{1}{sC_1}\right)} + \frac{\left(\frac{1}{sC_4} + R_2\right)\left(sL_2 + \frac{1}{sC_2}\right)}{\left(\frac{1}{sC_4} + R_2\right) + \left(sL_2 + \frac{1}{sC_2}\right)}$$
(4)

$$G(s)_{\rm DM1} = \frac{U_{\rm O_DM1}}{U_{\rm DM1}} = \frac{Z_{\rm LISN(DM)} / / \left(\frac{1}{sC_{DC}} + sL_s + R_s\right)}{sL_{p1} + Z_{\rm LISN(DM)} / / \left(\frac{1}{sC_{DC}} + sL_s + R_s\right) + sL_{p2} + \frac{1}{sC_{Q3}}}$$
(5)

$$G(s)_{\rm DM1} = \frac{1.56s^6 + 7.81 \times 10^7 s^5 + 3.64 \times 10^{12} s^4 + 3.12 \times 10^{17} s^3 + 1.45 \times 10^{22} s^2}{252s^6 + 8.88 \times 10^7 s^5 + 1.25 \times 10^{19} s^4 + 5.32 \times 10^{23} s^3 + 2.50 \times 10^{30} s^2 + 1.06 \times 10^{35} s + 1.13 \times 10^{36}} \tag{6}$$

$$U_{\text{DM}_O} = G(s)_{\text{DM}1} \times U_{\text{DM}1} + G(s)_{\text{DM}2} \times U_{\text{DM}2}$$

$$\tag{7}$$

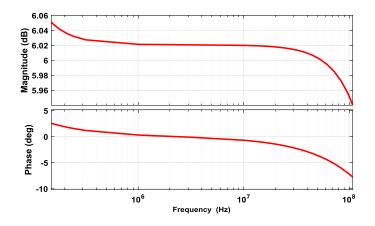


Figure 7. Bode diagram of the CM transfer function.

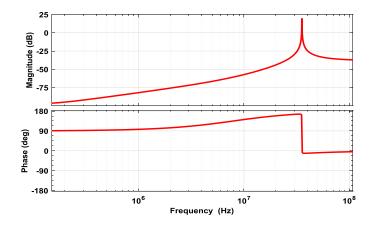


Figure 8. Bode diagram corresponding to the DM transfer function.

3.2. Extraction of the Noise Sources

According to Figure 9, a circuit model with high-frequency parameters of the DC-DC converter system is built in Matlab/Simulink, so that the noise source signals of CM interference and DM interference can be obtained. All of the main parasitic parameters are shown in red background. The two CM sources are the voltage between the midpoint of the bridges of the DC-DC converter and the chassis, as shown in green background. The two DM sources are the voltage between the midpoint of the bridges of the DC-DC converter and the negative or the positive terminal, as shown in yellow background. The CM and the DM noise source signals of the advanced bridge are shown in Figure 10a,b, respectively.

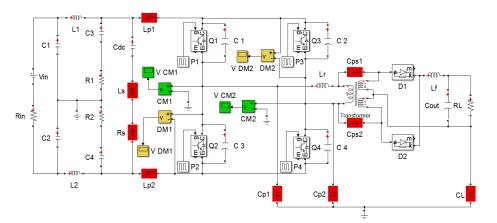


Figure 9. Equivalent circuit for EMI emission in Matlab/Simulink.

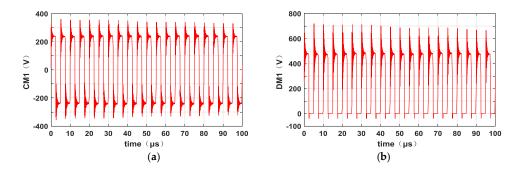


Figure 10. (a) Waveform of CM interference source and (b) Waveform of DM interference source.

3.3. Simulation for the Conducted Interference

The conducted interference both in the time domain and in the wide-range frequency domain can be obtained by Computer Simulation Technology (CST). The conducted interference voltage that is shown in Figure 11 can be obtained by establishing the high-frequency circuit model of the DC-DC converter in CST. The acquisition of the signals of the DM and CM interference sources U_{CM1} (U_{CM2}) and U_{DM1} (U_{DM2}) can achieved in Matlab/Simulink, as shown in Figure 10. As the important indicator for conducted-EMI, the conducted interference voltage can be obtained by modeling the LISNs consisting of R_1 , R_2 , L_1 , L_2 , C_1 – C_4 and adding probe "P1" and "P2", port 1 and port 2 in red circles are CM ports, port 3 and port 4 in blue circles are DM ports, which are all shown in Figure 11.

The positive conducted voltage of the single mode and CM+DM, which can be measured by the LISN, is compared in Figure 12. The conducted voltage of the CM+DM mode is represented by the black curve, the CM conducted voltage is represented by the red curve and the DM conducted voltage is represented by the blue curve. It can be seen that some resonances appear at the same frequency 200 kHz, 400 kHz, 600 kHz, 800 kHz etc. which have the same frequency interval. In addition, there are two resonance points at 7.8 MHz and 30 MHz in the CM mode and the hybrid mode. In terms of the conducted voltage in Figure 12, the CM+DM waveform, in fact, can be better represented by the CM waveform of the conducted voltage, and the CM conducted EMI is the dominated interference in a frequency range of 150 kHz–108 MHz.

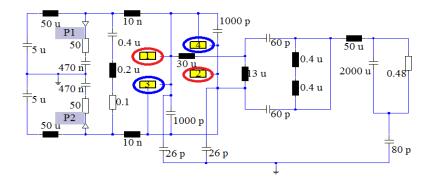


Figure 11. Simulation model of conducted interference for DC-DC converter.

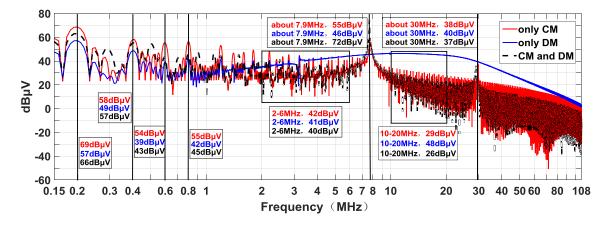


Figure 12. The conduction interference voltage measured on line impedance stabilization networks (LISN).

There is good consistency between the simulation result of the conducted voltage and the change of the Bode diagram by transfer function. Therefore, from Figures 7 and 12, it can be concluded that

the CM interference is mainly responsible for the conducted-EMI from the DC high voltage power cables of the DC-DC converter.

4. Design of High Frequency EMI Filter

From the discussion above, the conducted EMI of the high-low voltage DC-DC converter mainly comes from the CM interference. Therefore, the design for the CM filter is given priority to take into account in order to mitigate the conducted-EMI from the high-low voltage DC-DC converter in EVs.

4.1. Parameters Calculation of CM EMI Filter

The insertion loss method is adopted to calculate the values of the main passive components in the EMI filter. Firstly, the attenuations of the CM interference should be determined. The required attenuation amounts A_{CM} of the CM interference can be obtained through Equation (8):

$$A_{\rm CM}[dB\mu V] = A_{\rm nCM} - A_{\rm L} + m \tag{8}$$

The A_{nCM} is the amplitude of the nth harmonic (in the case of the fundamental frequency of 100 kHz); A_L is the limit of CISPR25/GB/T18655 level 3 in the frequency band from 150 kHz to 108 MHz; A_L is 50 dBµV in the frequency range of 0.53–1.8 MHz; and, m is 6 dBµV, the safety margin of filter suppression.

The influence of CM interference is dominant in the high frequency band, therefore, according to the test result and its limit line of Level 3 in Figure 4 and following the principle that, it can be known that the superscalar of CM interference reaches the maximum value of 43 dBµV at 1.4 MHz, and the A_{nCM} is 93 dBµV. Thus, the target attenuation frequency of the CM interference is 1.4 MHz. When considering the safety margin of 6 dBµV, the target attenuation of the CM is 49 dBµV. A_{req_att} [dBµV] is the target attenuation of CM.

Then, the corner frequency (cutoff frequency) f_0 of the CM filter needs to be obtained by calculating. In order to restrain the interference effectively, the corner frequency of the filter must be low enough, so that they can meet the suppression demand in the whole frequency band required. In generally, the corner frequency is calculated by using the frequency (i.e., 1.4 MHz) of the first highest interference amplitude point of CM interference (see in Equation (9)).

$$f_0 = \frac{f_{h_att}}{10^{\frac{A_{req_att}}{filter_att}}}$$
(9)

where $f_{h_{att}}$ is the frequency for attenuation; $A_{req_{att}}$ is the attenuation; *filter_att* is the slope of the attenuation slash, 40 dB/dec. The attenuation frequency of CM that was obtained by Equation (9) is 37.25 kHz.

The CM inductance L_C and the CM capacitance C_Y of the CM filter can be calculated by the Equation (10):

$$L_{\rm C} = \left(\frac{1}{2\pi f_0}\right)^2 \times \frac{1}{2C_{\rm Y}} \tag{10}$$

It is usually assumed that C_Y takes the normal value, 3300 pF, so the value of L_C can be calculated as 2.766 mH.

4.2. Topology Selection of CM Filter

In order to determine the best CM filter topology, the volume and weight of the filter are both considered, four different topologies are designed and inserted into the high-frequency model in CST, respectively. And these four kinds of topologies include the topology of capacitance + inductance (CL), the topology of inductance + capacitance (LC), the topology of capacitance + inductance + capacitance (CLC) and the topology of inductance + capacitance + inductance (LCL). The comparison in attenuation

between the four kinds of filters is shown Figure 13, the attenuation values at some important frequency points are listed, and the corresponding curves of CLC, LCL, CL, and LC are presented in pink, sky blue, blue, and brown, respectively. From Figure 13, it can be seen that the topologies of LCL and CLC have the better suppression effect than that of CL and LC in the low-frequency band (less than 500 kHz), and the CLC topology has an obviously better suppression effect than other topologies at the frequency from 150 kHz to 180 MHz. Besides, CLC has a smaller volume than LCL. By considering both the suppression effect in the whole frequency band and the size of the filter, the optimal topology of the CM filter for the high-low voltage DC-DC converter is CLC, as shown in Figure 14. R_d (25 k Ω) and R_c (10 Ω) are the equivalent impedance of the filter, L_P (0.2 µH) and R_s (0.1 Ω)are the high frequency parasitic parameters of C_Y , respectively.

In order to verify the suppression effect of the CM filter with CLC topology in Figure 14, a simulation model with the CLC topology for the high-low voltage DC-DC converter is established in CST, as shown in Figure 15. The conducted voltage of simulation results with and without the CM filter with CLC topology are shown in Figure 16.

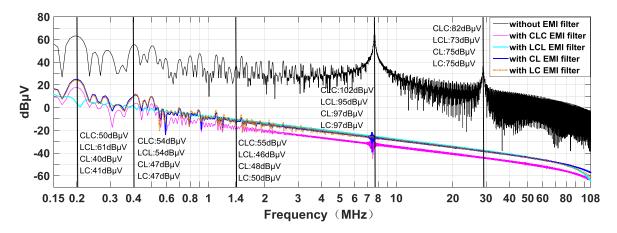


Figure 13. The comparison in attenuation between the four kinds of filters.

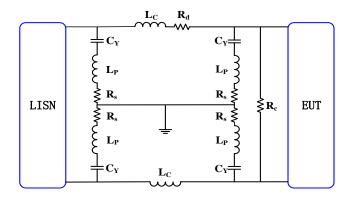


Figure 14. The final EMI filter with high frequency parameters.

From Figure 16, it can be known that the conducted voltage of simulation has a sharp reduction in the whole frequency band of 150 kHz–108 MHz. Most important of all, the conducted voltage is decreased by 55 dB μ V at the target frequency 1.4 MHz and it meets the designed attenuation 49 dB μ V very well. The detail values of the conducted voltage with and without the CM filter are listed in Table 3.

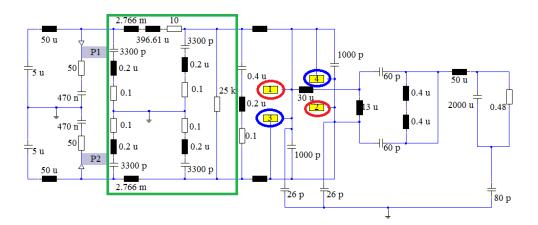


Figure 15. The simulation model of the DC-DC converter with the final EMI filter.

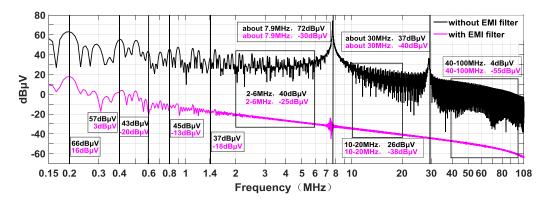


Figure 16. The interference contrast with and without the final filter.

Frequency	Simulation Results (dBµV)			
	without Filter	with Filter	Attenuation	
200 kHz	66	16	50	
400 kHz	57	3	54	
600 kHz	43	-20	63	
800 kHz	45	-13	58	
1.4 MHz	37	-18	55	
2–6 MHz	40	-25	65	
7.8 MHz	72	-30	102	
10-20 MHz	26	-38	64	
30 MHz	37	-40	77	
50 MHz	8	-50	58	

Table 3. The simulation results of conducted voltage.

4.3. Mitigation Effect and Stability Analysis of the High Frequency EMI Filter

The high frequency parameters of the filters have an important effect on its stability. The equivalent circuit with the CLC filter is shown in Figure 17. The corresponding transfer function is expressed by the numerical equation, as shown in Equation (12).

$$G_{\text{CM1 filter}}(s) = \frac{6.9e13s^{12} + 1.25e38s^{11} + 1.25e44s^{10} + 3.8e53s^9 + 1.9e59s^8 + 2.88e68s^7 + 7.58e68s^6}{4.01e9s^{13} + 7.25e33s^{12} + 6.32e28s^{11} + 2.24e49s^{10} + 2.78e40s^9 + 1.6e64s^8 + 1.63e70s^7} \\ + 1.15e78s^5 + 3.99e70s^4 + 2.76e76s^3 + 1.39e81s^2 + 1.06e86s + 4.91e90}{+7.98e74s^6 + 3.83e78s^5 + 4.38e72s^4 + 1.68e78s^3 + 1.44e83s^2 + 3.77e87s + 1.64e91}$$
(11)

$$U_{\rm CM_O} = G(s)_{\rm CM1 \ filter} \times U_{\rm CM1} + G(s)_{\rm CM2 \ filter} \times U_{\rm CM2}$$
(12)

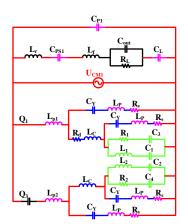


Figure 17. The equivalent circuit with the CM filter.

According to Equation (12), the corresponding Bode diagram can be obtained, as shown in Figure 18. It can be seen that the magnitude is decreased by the expectation attenuation. There is no new resonance appearance at the whole frequency band 150 kHz–108 MHz. From Figure 18, the DC-DC converter with the CM filter has better stable characteristics and can achieve a good mitigation effect for the conducted EMI.

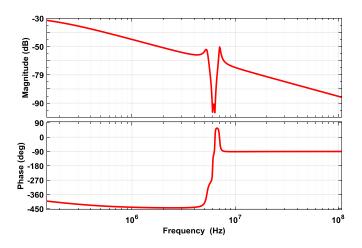


Figure 18. Bode diagram with the CM filter.

From Figure 18, it can be seen that the conducted voltage can be decreased by a continuous attenuation (from $-40 \text{ dB}\mu\text{V}$ to $-95 \text{ dB}\mu\text{V}$) in 150 kHz–108 MHz. When comparing with the Bode diagram without the CM filter in Figure 7, it can be seen that the amplitude has sharply reduced.

5. Experimental Verification

Comparison and Analysis for the EMI Experimental Result and EMI Simulation Result

A conducted voltage experiments is built by CISPR 25(GB/T18655), as shown in Figure 3, to validate the suppressive effect of the CM filter with CLC topology. The CM filter with CLC topology is added at DC input terminals inside the high-low voltage DC-DC converter, as shown in Figure 19. After inserting the CLC filter, the measurement result of the conducted voltage on the primary DC power cable can be seen in Figure 20.

From Figure 20, the conducted voltage is lower than the limit of CISPR 25(GB/T18655) in the whole frequency band and it meets the standard requirements. The attenuation comparison of the experiment results and simulation results is listed in Table 4. It can be seen that the attenuation

results of simulation and experiment are basically identical (roughly the same amount of interference suppression). In those important resonant points and frequency band, the attenuation errors between the experiment results and simulation results are very small, which validate the availability of the proposed high-frequency model and the designed EMI filter. Besides, it notes that the attenuation at 1.4 MHz is 53 dB μ V, which matches the simulation result 55 dB μ V and meets the target attenuation 49 dB μ V very well. In addition, the harmonics results of simulation that start from 200 kHz with the interval of 200 kHz match the harmonics results of the experiment very well. In addition, the harmonics results of the experiment very well. In addition, the harmonic amplitude of the experiment is significantly greater than that of the simulation due to real operating condition.

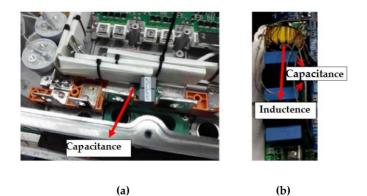


Figure 19. The components of filters in the DC-DC converter (a) capacitance (b) inductance and capacitance.

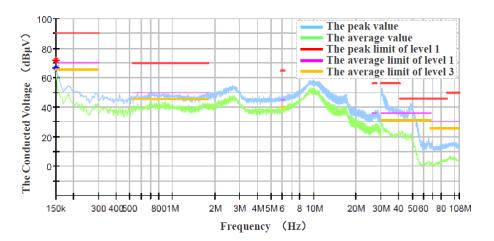


Figure 20. The experiment result with the CM filter.

 Table 4. The attenuation comparison of the experiment results and simulation results.

Frequency	Attenuation (dBµV)			
	Measurement	Simulation	Error (dBµV)	
200 kHz	58	50	8	
400 kHz	55	54	1	
600 kHz	65	63	2	
800 kHz	54	58	-4	
1.0 MHz	42	42	0	
1.4 MHz	53	55	-2	
2.0 MHz	42	49	-7	
50 MHz	54	58	-4	

6. Conclusions

A conducted EMI prediction and mitigation strategy that is based on transfer function for the high-low voltage DC-DC converter in EVs are proposed. The equivalent circuits of the CM and DM interference for the DC-DC converter are built based on the measurement results of high-frequency parasitic parameters. The characteristics of the conducted EMI from the DC power cables are obtained. The dominated conducted EMI is predicted by establishing the corresponding transfer functions of the DM interference and CM interference. By analyzing the transfer functions and the simulation results, the CM interference is known as the dominated interference that is responsible for the conducted EMI. By the simulation and the experiment, a strategy of giving priority to the dominated interference mode is proposed for designing the optimal CM interference filter with CLC topology. From the experiment results, the conducted voltage of the DC power cables is decreased, respectively, by 58 dBµV, 55 dBµV, 65 dBµV, 53 dBµV, and 54 dBµV at frequency 200 kHz, 400 kHz, 600 kHz, 1.4 MHz, and 50 MHz. The conduced voltage in frequency range from 150 kHz to 108 MHz can be mitigated to below the limit level-3 of CISPR25 standard (GB/T 18655-2010) by adding the CM interference filters. The DC-DC converter with the CM filter has better stable characteristics and can achieve a good mitigation conducted EMI effect. In the future, the equivalent circuit model for the high-low voltage DC-DC converter should be improved in the frequency 30 MHz-108 MHz to predict the radiated EMI from the DC power cables of the DC-DC converter.

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