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Novel Cathode Design to Improve the ESD Capability of 600 V Fast Recovery Epitaxial Diodes

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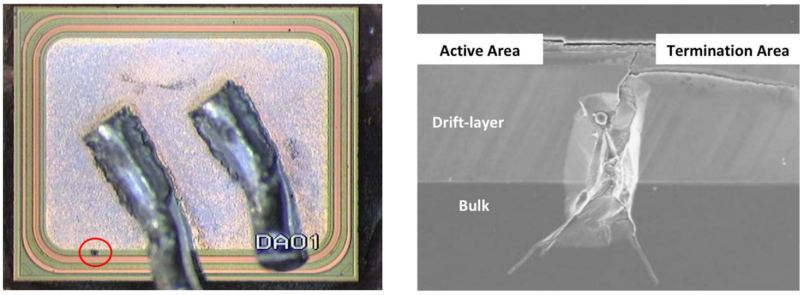
Abstract: Silicon power diodes are used to design different types of electrical energy systems. Their performance has been improved substantially, as a result of a concentrated research efforts that have taken place in the last two decades. They are considered immune to electrostatic discharge (ESD) failures, since usually they withstand an avalanche energy one order of magnitude higher than that of the ESD. Consequently, few works consider this aspect. However, it was observed that during the mounting of power diodes in automotive systems (e.g., with operators touching and handling the devices), ESD events occur and devices fail. In this paper the ESD capability of 600 V fast recovery epitaxial diode (FRED) is analyzed by means of Technology Computer-Aided Design (TCAD) simulations, theoretical analyses and experimental characterization. Two doping profiles are investigated in order to improve the ESD robustness of a standard device and an optimized doping profile is proposed. The proposed design exhibits a higher ESD robustness and this is due to its superior capability in keeping the current distribution uniform in the structure in a critical condition such as the impact ionization avalanche effect. Both experimental and numerical results validate the proposed design.

Keywords: electrostatic discharge (ESD); impact ionization; fast recovery epitaxial diode (FRED); sustainable energy systems

1. Introduction

Recent developments in power semiconductor device design are showing an increased demand for devices that can withstand strong electrical overstresses. A power diode is usually designed to display static, such as forward voltage (V_{ON}) and breakdown voltage (BV), and dynamic performance features like the reverse recovery behavior [1]. Recent requests coming from the power semiconductor industry also demand ESD capability for these devices. Although the behavior of power diodes in avalanche conditions is a well studied field, the ESD ruggedness of vertical devices is still not well addressed in terms of design guidelines. As no critical oxide layers are present in a power diode structure, once the VF and the BV are optimized, the ESD capability is not further evaluated during the validation of the design, since power diodes typically can withstand an avalanche energy one order of magnitude higher than that of an ESD event. However, a deeper characterization of the power diodes under test has shown that some ESD events can lead to unexpected failures. In this work we have optimized a fast recovery epitaxial diode (FRED), designed to sustain 600 V, for improved robustness under ESD conditions. Experimental characterization highlighted an overall reduced ESD

capability for some devices (Human Body Model ESD (HBM-ESD) [2]) and a large variability in terms of maximum applicable voltage. It is known that ESD current is sustained by carriers generated by impact ionization and in this condition electrical behavior related to the presence of a Negative Differential Resistance (NDR) can arise. As it has been demonstrated in [3–8] the presence of a NDR branch in the blocking I-V curve can lead to current filamentation and possible early failure of the device. Optical investigations have highlighted damages coherent with current filamentation (Figure 1). It has been proven that, at least for static avalanching (or Unclamped Inductive Switching UIS [9]), this mechanism can be mitigated by the insertion of a buffer layer [5] at the N++-N− transition. In this work we show a novel cathode design proposed to improve also the ESD capability for a FRED diode 600 V rated. Results are validated by means of TCAD simulations. The FRED design with such an improved design has been fabricated and the experimental results are also reported in the paper.



(**a**) (**b**)

Figure 1. (**a**) An optical microscope picture of a typical failure location (highlighted by the red circle) on the anode side of the device after the electrostatic discharge (ESD) test for the 600 V rated fast recovery epitaxial diode (FRED) diode. The two black wires connect by wire bonding to the anode and the failure occurs in the area between the active area and the termination area; and (**b**) a scanning electron microscopy (SEM) section of the failure area.

2. ESD Failures

The aim of this work is the investigation of the phenomena involved in the failure of 600 V-rated power diodes under the ESD test. The ESD condition is usually dangerous for electrical systems and devices [10]. In our case, the devices under investigation have shown a weakness in HBM-ESD in terms of reduced values of maximum voltage during the discharge. Experimental details of the observed failure in the devices under test are illustrated in Figure 1. The area of the failure is hardly visible by means of the optical microscope, therefore a laser beam is adopted to highlight the surrounding area of the failure to improve its visibility, as shown in Figure 1a. A scanning electron microscopy (SEM) analysis of the ESD failure is shown in Figure 1b. The location of the failure is the edge of the active area, between the main junction and the first ring of the termination region. The failure has a cylindrical shape with a radius of few micrometers and extends to the Drift layer region and part of the Bulk (cathode) region, with the typical morphology of a local melting of the silicon. Characterization results shows that the failure occurs in a very small area of the device and the failure position depends on the voltage of the ESD test. The tiny failure area is due to the difference in energy stored in the capacitance of the ESD test circuit. The equivalent schematic of the ESD test is reported in Figure 2. Basically, the ESD test circuit forces a current in the device from the discharge of a capacitance through a resistance. To achieve this, the circuit is divided in two parts, the left side, consisting in the charging circuit and the right side, consisting in the DUT in series with a resistance. The test is performed by switching the capacitance C first to the left side of the circuit and then to the right side of the circuit. R, C, Lpara, Cpara1 and Cpara2 model the human body equivalent circuit when the finger touches an electrical system. Lpara, Cpara1 and Cpara2 are not relevant from the point of view of the present analysis since they introduce only some delay at the waveform, but they do not change the amount of current flowing in the structure. Therefore, only R and C are kept into account for the

mixed-mode TCAD simulations and their values is 1.5 kΩ and 100 pF, respectively. In a standard ESD characterization of a semiconductor device, the ESD event is applied for any operative condition. For the specific power diode, the analysis should be performed in both forward and reverse conduction conditions. However, this approach can be simplified for the power diode under test. In conduction conditions, the current flowing in the device for the ESD event, referring to Figure 2, can be calculated as $I = (V_C - V_F)/R \approx V_C/R$, where V_C is the C capacitance voltage before the ESD event, V_F is the voltage drop of the diode under test in forward conduction and R is the resistance value. Keeping into account the R value and the voltage rate of the investigated devices, the current flowing into the device is in the order of some amperes. Under conduction conditions this current level does cause the device to fail, since the surge current of a power diode is higher than the ESD-induced current. On the other hand, the current flowing in blocking conditions in the DUT can be calculated as $I = (V_C - V_{BR})/R$, where V_{BR} is the breakdown voltage of the DUT. The device works at its breakdown voltage for the current level coming from the previous relation. The avalanche current is sustained by the impact ionization effect and both the high voltage and high current occurring during the ESD test exacerbate the spatial instability [11]. The high dynamic of the ESD event also concurs to the current crowding in the structure. In this work the ESD capability is evaluated for 600 V-rated FRED power diodes. First, the static, dynamic and avalanche characterization of the devices was carried out (the avalanche capability has been evaluated by means of the UIS test [9]). The ESD test has been performed by increasing the applied voltage until failure was observed. As reported in Figure 1, the device fails because of a hot spot on the surface of the device with a higher failure rate close to the termination area. The literature regarding the ESD capability for power diodes is not exhaustive since many works (e.g., [12,13]) are more concerned the ESD failure in semiconductor devices for signal processing applications. In these papers the high electric field in the oxide and the high temperature increase are addressed as the failure cause. However, in the field of power semiconductor devices, only few works deal with ESD capability [14,15] and only a recent work regards the ESD capability for 200 V FRED diodes [16].

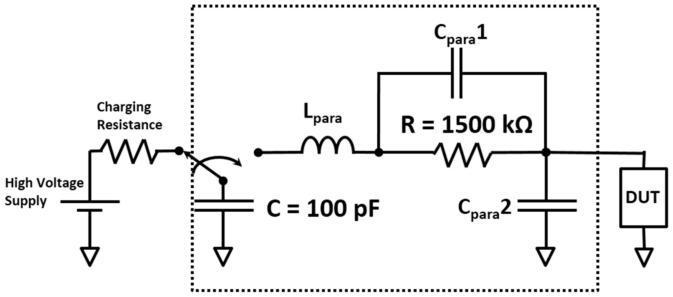


Figure 2. The schematic of the ESD test circuit in HBM configuration for the experimental characterization of the power diodes.

3. Theoretical Background

As reported in the previous section, the experimental characterization of FRED power diodes, with a voltage rate of 600 V and a current rate of 12 A, highlights a weakness of the devices under ESD conditions (namely, failure for an ESD energy on the order of 400 μJ), even if the structure shows a good avalanche capability under UIS conditions (up to a UIS failure energy of 40 mJ). Therefore, a theoretical and numerical analysis has been carried out to investigate the physical phenomena occurring during the ESD test in the structure and the solutions, validated by the TCAD simulations. In general, the electric field distribution and the charge density in the drift region is described by the Poisson law as in (1):

$$\frac{dE}{dx} = \frac{q}{\varepsilon}(N_D + p - n) \quad (1)$$

where N_D is the doping concentration of the Drift layer, x is the spatial coordinate, q is the electron charge, ε is the silicon permittivity, n and p are the free electron and hole density, respectively. When the free carriers concentration, p-n, is negligible compared to N_D under blocking conditions, the electric field slope is constant. This is also valid when the critical electric field is achieved at the p/n-junction at the breakdown voltage. When the free charge flowing in the depletion area is comparable to N_D, the right hand side term of (1) is not constant anymore and the electric field is warped. The latter effect leads to the current level dependence of the breakdown voltage. In (2) an estimation of the current flowing during the peak (the current exponentially decreases during the test) in the DUT is carried out for a ESD test where V_C = 12 kV:

$$I_{peak} = (1200 - 600)\ V / \ 1500\ \Omega \ = \ 7.6\ A \tag{2}$$

Especially for low current rate devices, the peak current calculated in (2) can lead to the failure of the device because current filamentation can arise. Recalling Equation (1), the current level calculated in (2) is high enough for a free carrier concentration comparable to the fixed charges, therefore electric field—charge interaction occurs. Many works have tried to find a closed analytical form to describe the interaction between the electric field and the free charges ([11,17]), however the analysis becomes too complex for structures slightly different from the very basic structure, therefore TCAD simulations are mandatory to investigate the exact behavior of the structure for the different operative condition of the structure. In this work both the active area and the termination area are kept into account to evaluate the behavior in ESD conditions.

4. Numerical Results

2D TCAD simulations have been carried out to highlight the physical phenomena occurring in the structure during the ESD test and to evaluate the best design to achieve, at the same time, suitable static, dynamic and ESD capability performances.

4.1. Doping Profiles

The structure under test is a PiN diode and a sketch is shown in Figure 3a illustrating the active area of the device. Basically, the N− region, called drift layer, is characteristic of the power devices since it sustains the high voltage under blocking conditions. The details of the electric field distribution are reported in Figure 3b. The electric field in the drift region is almost flat because of the very low doping concentration to sustain very high BV with reduced layer thickness. Starting from the standard doping profile, named DEV1 in Figure 4, a sketch of the new doping profile, named DEV2, is here proposed to improve the ESD capability of the device under test. In Figure 4 the anode region is labeled P+, the drift-layer region is labeled N− and the cathode region is labeled as N++.

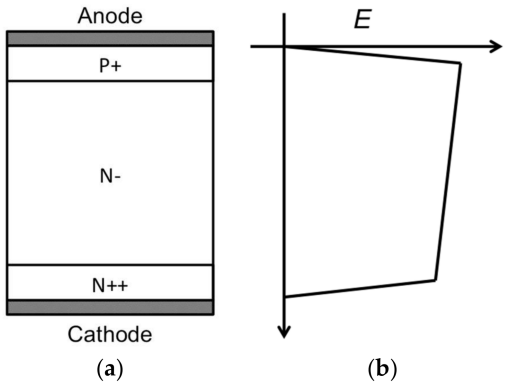


Figure 3. (**a**) A sketch of the power diode structure; and (**b**) the typical electric field distribution in the device in avalanche conditions along any vertical section of the active area of the device.

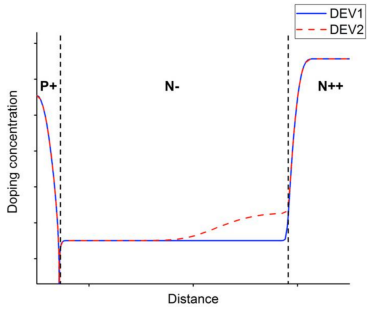


Figure 4. A sketch of the DEV1 and DEV2 doping profiles. The doping type is specified for the three main layers.

The DEV2 doping profile in Figure 4 has to be considered only a principle doping profile, since the introduction of a buffer layer acts on other features of the device (e.g., V_F, Trr, V_{BR}) and a careful engineering is mandatory. Basically, a buffer layer has been introduced [8] at the cathode side (N−/N++ transition) and a deep analysis of its effect on the performances is carried out. As a first step, the DEV1 doping profile is calibrated starting from a 600 V 12 A device. Standard models are adopted to simulate the transport phenomena and the Van Overstraten [18] model is adopted to take into account the avalanche generation in the structure. The latter model is the most relevant since takes into account the high non-linearity of the impact ionization generation occurring during the ESD test in the overall structure. Lifetime killing techniques are adopted to improve the dynamic performances of the device and a proper trap energy and lifetime levels are chosen to match the experimental static and dynamic curves. As it is visible in Figure 4, the DEV1 doping profile is a standard design with an abrupt transition from the N++ cathode region to the N− region. This structure has the advantage to achieve high performance in both static and dynamic conditions by acting on the drift layer thickness, doping concentration of the drift layer, injection efficiency of the anode and lifetime in the structure.

Different works shows that the introduction of a buffer layer on the cathode side of a power diode can improve both the avalanche capability and the ESD robustness [8,16]. However, the introduction of the buffer layer, because of the increase of the doping concentration, leads to the increase of the V_{ON} and a reduction of the breakdown voltage (BV). The latter aspect is especially relevant for 600 V power diodes, since the typical static performances requests lead to a reduced margin for the maximum drift layer thickness. Therefore an extensive analysis of the impact of the doping profile of the buffer layer has been carried out to define the best solution to improve the ESD capability and, at the same time, to keep both the V_{ON} and the V_{BR} within acceptable values. Basically, the introduction of the buffer layer in the design DEV2 leads to the reduction of the BV, if the distance between the P+/N− junction and the N/N++ junction in DEV2 is equal to the drift layer width in DEV1 design. This because of the increase of the doping concentration, by means of (1), increases the slope of the electric field with the consequent reduction of the voltage drop when the device operates in avalanche conditions. On the other hand, the increase of the drift layer width in DEV2 increases the BV, but increases V_{ON}, strongly dependent on the low doped region width. It has to be pointed out that the peak doping concentration of the buffer layer is equal to eight times the drift layer doping concentration, with a very smooth shape.

The optimized buffer layer presented in this work is a further optimization of the double-epi buffer layer presented in [16]. The design presented in [16] has good performances with 200 V-rated diodes, however it is not suitable in terms of ESD capability for 600 V-rated devices. TCAD simulations show as while for the 200 V-rated diodes a double-epi profile assures a uniform distribution of the current all over the device during the ESD event, for 600 V-rated devices filamentation occurs for excessively low current levels. The design features of the double-epi buffer layer where investigated in terms of current uniformity during the ESD event and the most relevant parameter is the transition between the buffer layer and the drift region slope.

4.2. Elementary Cell Analysis

As a first analysis step, the elementary cell of the active area of the device is investigated. The ESD event leads to the impact ionization effect in the device, therefore the elementary cell analysis is carried out with a specific focus on the IV curve under blocking condition. Since the doping profile of the active area is uniform, the elementary cell analysis reduces to the analysis of the 1D structure of the active area. Specific works demonstrate some parameters of the IV curve in blocking condition (See [4,5]) of the elementary cell give an estimation of the avalanche robustness of the structure. Typically, in power diodes the IV curve in blocking condition shows a Positive Differential Resistance (PDR) starting from low current levels, up to a transition point where the differential resistance switches and shows a NDR branch. More in detail, two parameters are relevant in terms of avalanche robustness: the PDR extension voltage and the current level where the IV curve passes from the PDR region to the NDR region, named turn-over point in the following paragraphs. The PDR extension voltage is defined as the voltage difference between the BV at low current levels and the BV at the turn-over point. In Figure 5 both the IV curves in avalanche conditions of the elementary cell of the active area for designs DEV1 and DEV2 are reported. The very smooth shape of the buffer layer has the role to shift the second injection point at higher current levels by compensating the slope increase due to the high electron concentration at the cathode side when the free carrier level is comparable to the drift layer doping concentration. A good balance was found from the static point of view by adopting the DEV2 design, since it has a reduction of 10% and 1.33%, respectively, of BV and VF. No relevant variations occurs for the dynamic performances since the anode doping profile and the lifetime in the structure are not affected by the changes at the cathode side. As is visible, the DEV2 structure has a lower BV, for low current levels, compared to the DEV1 structure, since V_{BR_DEV1} = 763 V while V_{BR_DEV2} = 678 V. From the point of view of the peak current level (defined as the current level where turn-over point occurs), the DEV1 structure exhibits I_{PEAK_DEV1} = 337 A/cm^2, while for the structure DEV2 I_{PEAK_DEV2} = 1285 A/cm^2. From the point of view of the PDR extension voltage, the DEV2 structure shows a great improvement with a PDR extension of 75 V. On the other hand, the PDR extension voltage for DEV1 is almost negligible. It can be concluded that the two designs have similar forward performances, but the DEV2 design shows a superior robustness in avalanche conditions, according to the blocking IV curve parameters identified by the specific literature.

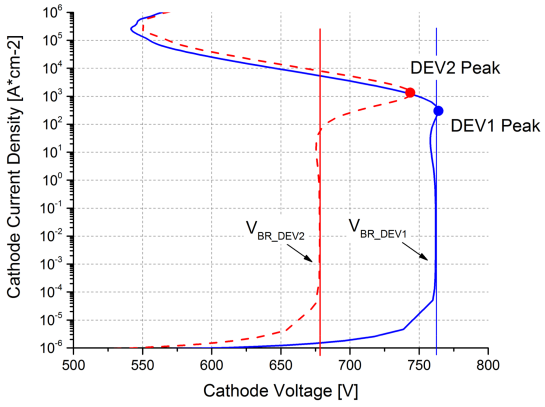


Figure 5. Active area numerical I-V curves under blocking conditions for elementary cells of both the DEV1 and DEV2 designs.

4.3. Wide Area Simulaitons

The ESD test failures arisen during the experimental characterization of the diodes have a typical fingerprint associated to the current filamentation effect, therefore large area 2D TCAD simulations are mandatory to correctly investigate the carrier distribution. A 1 mm wide PiN structure with a planar junction has been analysed under ESD conditions by means of mixed-mode TCAD simulations.

This structure has been simulated to investigate the intrinsic dynamics of the active area of the device under ESD test conditions. Both the DEV1 and DEV2 designs have been evaluated under the same conditions. In Figure 6 both the cathode voltage and the cathode current waveforms during the ESD test at V = 7.5 kV for the two designs are reported. As is visible, the DEV1 design shows a cathode voltage collapse at t = 0.06 µs while the DEV2 design does not show any relevant variation of the cathode voltage. Typically, the voltage drop of the cathode electrode highlights the current filamentation in the structure as described in [9]. To understand the carrier distribution within the structure during the ESD test, the times $t = t_1 = 0.04$ µs and $t = t_2 = 0.08$ µs are investigated referring to Figure 6 and the current distribution is reported Figure 7 for both designs.

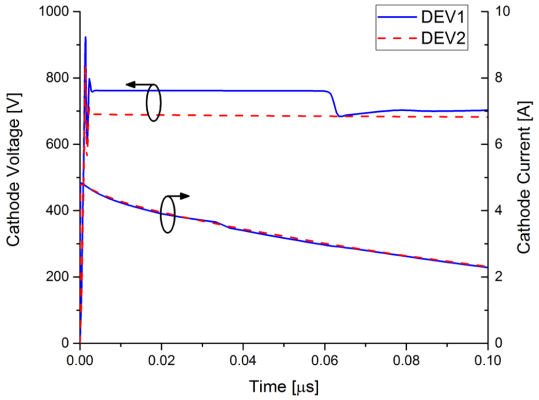


Figure 6. Numerical cathode voltage and current waveforms of DEV1 and DEV2 structures during the ESD test (only active area). $V_C = 725$ V.

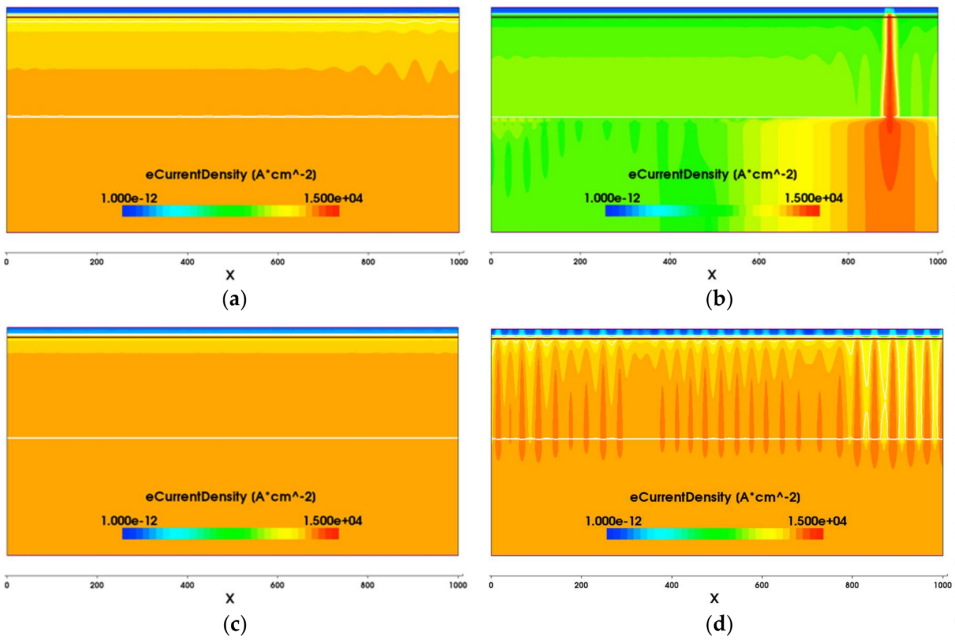


Figure 7. Electron current density distribution in the structure DEV1 at: (**a**) $t = t_1$; and (**b**) $t = t_2$. Electron current density in the structure DEV2 at (**c**) $t = t_1$; and (**d**) $t = t_2$.

The two structures exhibit the same current distribution for $t = t_1$, while they have a very different behaviour at $t = t_2$. More in detail, for DEV1 the current crowds in a very narrow area of the device. For DEV2 the current distribution is almost uniform all along the structure, with a weak periodic increase of the current level along vertical stripes. From the point of view of the power dissipation, DEV2 structure exhibits a constant dissipation.

It can be concluded that the DEV1 structure has a weakness during the ESD test due to the current filamentation that focuses the power dissipation in a very limited area of the device. It has to be pointed out that the junction is ideal since it is flat and there are no spatial variations along the longitudinal direction, proving that the current filamentation is intrinsic for the DEV1 structure.

4.4. Effect of Termination Region

In real devices, especially for high voltage rates power diodes such as the 600 V category, the termination area properties have a crucial role during avalanche events. Usually the termination area in power diodes is designed to have lower BV compared to the active area, to sustain the reverse current flow. This aspect cannot be neglected in any thorough analysis of the ESD capability.

A sketch of the termination region is depicted in Figure 8. The floating field ring (FFR) technique [19] is adopted together with a field plate on the last ring. The blocking IV curves of the termination for both DEV1 and DEV2 designs are reported in Figure 9. Differently from the trend in the active area, the BV of DEV2 is higher than that of DEV1. This is due to the complex design of the termination region, where the lateral interactions are relevant as well as the vertical ones. However, at high current densities the DEV2 structure preserves its higher turn-over point compared to the DEV1 one. This also demonstrates the higher robustness in avalanche conditions for the new design. The complete structures (active area plus the termination area) for both DEV1 and DEV2 deigns were analysed. As an example, the complete structure for the design DEV1 is reported in Figure 10. It is a single structure with a portion for the active area and another one for the termination region. The ratio between the extension of the two zones refers to that of a 12 A rated real device. The behaviour of the two designs has been evaluated in ESD test conditions, for V_C = 7.5 kV, in mixed mode to keep into account lumped elements of the circuit. In Figure 11 both the cathode voltage and current for the two structures is reported. Differently from what observed in Figure 6, no abrupt variations at for the cathode voltage occur during the ESD test. Comprehension of the dynamics of the phenomena occurring in the structure can be achieved by observing the electron current density for the two structures reported in Figure 12, where the electron current density is reported for t = 0.08 µs (referring to Figure 11) for both the structures. Numerical results concerning the temperature during the ESD event demonstrate that the current filaments do not show any movement driven by temperature gradients, in spite of results coming from, e.g., IGBTs during UIS (See [6]). This is due to the very short duration of the ESD event, that occurs in a tenth of a microsecond. In this work, numerical results show as the temperature variation follows the spatial current variation. Regarding the local temperature increase, the only way to predict the temperature increase is a 3D TCAD simulation, since the shape of the filament can be assumed cylindrical. Therefore, the aim of the 2D TCAD simulations is the identification of the critical locations where high current densities occur, considering that in the same location the temperature increases in a critical way. Without the insertion of the buffer layer (Figure 12a) the current only flows through the termination area. This is due to the lower BV of the termination area, as it observable from Figures 5 and 9. Termination area and active area can be schematized as connected in parallel, therefore, for any voltage level, the current flows in the region where the IV curve exhibits the higher current. When the overall device achieves the Breakdown condition, if the BV of the active area is different from that of the termination area, only the area with lower BV is working under breakdown conditions and the current flows there. In the other area the leakage current flows. However, this is true only if the BV of the two regions strongly differ. If they are close enough, TCAD simulations are mandatory to establish the current paths. The termination area has a NDR branch (See Figure 9) at high current densities and the same dynamics observed in the structures of Figure 7 can occur. Current filaments can appear along the longitudinal coordinate of the termination area. On the other hand, even if the filamentation effect does not occur in the termination area, the power dissipation is located in that region with a consequent reduction of the avalanche capability, compared to the ideal condition of uniform distribution of the current in the device. A strong improvement of the ESD capability is achieved for the structure with the buffer layer in Figure 12b. As is visible, a great

portion of the current flows in the termination area, but a comparable amount of current flows in the active area of the device. It has to be pointed out that the current density in the active area is arranged in areas with higher current density alternated with lower current density areas, but from the power dissipation point of view it can be assumed uniform along the structure. Two important improvements are achieved by the DEV2 design: the current is homogeneously distributed in the structure, with consequent increase of the avalanche capability, and current necessary to trigger current filamentation effects in both the active area and the termination region is shifted to higher current densities.

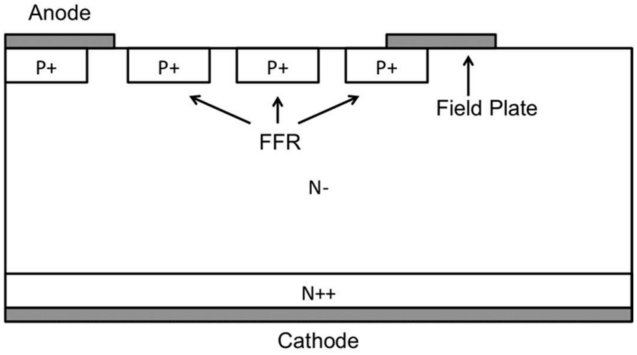


Figure 8. A sketch of the termination area.

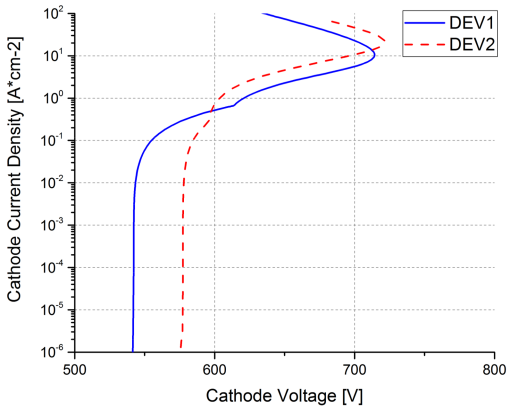


Figure 9. Termination area numerical I-V blocking curves for design DEV1 and DEV2.

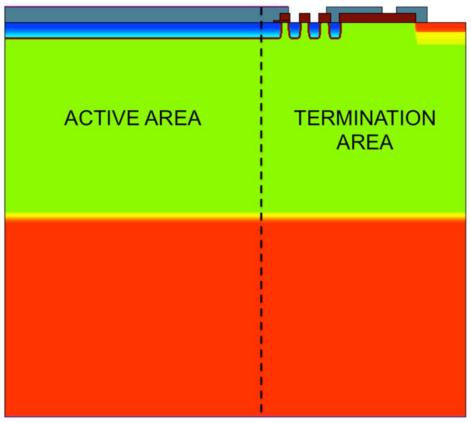


Figure 10. 2D TCAD structure of DEV1 device where active area and termination area are kept into account.

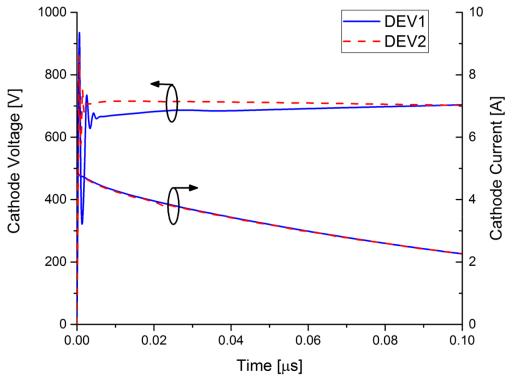


Figure 11. Cathode voltage and current waveforms of DEV1 and DEV2 structures during the ESD test simulation (termination area included).

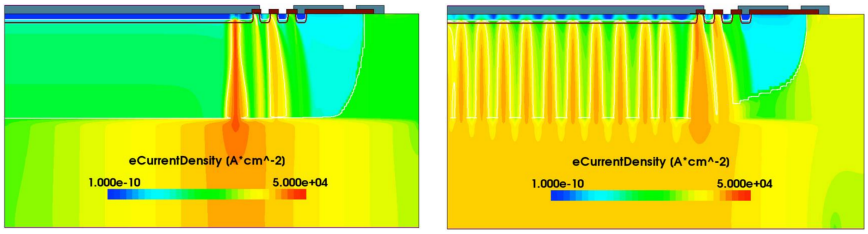


Figure 12. Electron current density distribution at t = t_1 in the: (**a**) DEV1 structure; and the (**b**) DEV2 structure.

5. Experimental Results

New samples have been fabricated to prove the ESD capability increase for the new cathode design. In Figure 13 the experimental doping profiles of the two designs are reported. As mentioned in a previous section, the introduction of the buffer layer in the structure implies the engineering of the rest of the drift layer area. Indeed, the drift layer doping concentration is lower in order to keep the breakdown voltage unchanged between the two designs. In addition to the optimized buffer, both the overall drift layer width and the drift layer doping concentration were optimized in order to achieve, at the same time, the higher ESD capability and a reduced variation of the V_{ON} and the breakdown voltage. A drift layer extension is needed to keep constant the breakdown voltage of the device. The new samples have been experimentally characterized from both the static and dynamic point of view. In Figure 14 the I-V curves in forward conduction are reported for the two designs, evaluated for two temperatures: T = 25 °C and T = 125 °C. As expected, the introduction of the buffer layer increases the On-state voltage drop with a percentage of +5.4% (see Table 1).

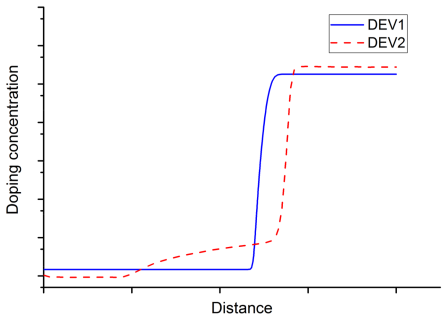


Figure 13. Comparison between the measured doping profiles of the old design (DEV1) and the new design (DEV2).

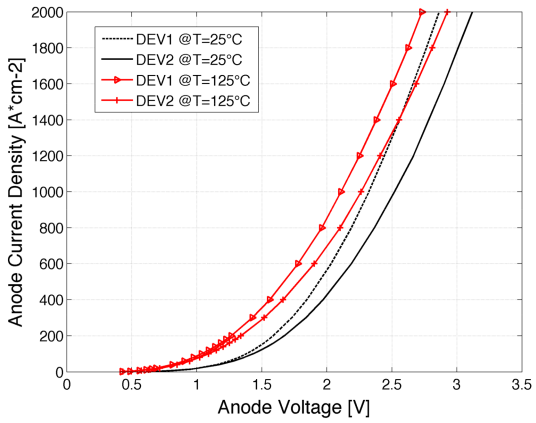


Figure 14. Comparison between the experimental I-V curves in forward conduction of the old design (DEV1) and the new design (DEV2) for T = 25 °C and T = 125 °C.

Table 1. Performance summary of the two designs.

Test	Test Conditions	DEV1	DEV2
UIS	Median (Avalanche current@Tc = 25 °C - L = 1 mH) (A)	8.8	13.6
UIS	Median (Avalanche current@Tc = 25 °C - L = 10 mH) (A)	4.2	5.3
UIS	Median (Avalanche current@Tc = 25 °C - L = 40 mH) (A)	2.7	3.6
Current Pulse	Median (Square pulse avalanche current@Tc = 25 °C, tp = 5 µs) (A)	5.8	8.4
ESD	Fail@2 kV	0/10	0/10
ESD	Fail@4 kV	0/10	0/10
ESD	Fail@6 kV	1/10	0/10
ESD	Fail@8 kV	-	0/10
$\mathbf{V_{ON}}$	Variation compared to DEV1	-	+5.4%
$\mathbf{V_{BR}}$	Variation compared to DEV1	-	−8%

The introduction of the buffer layer also leads to a remarkable improvement of the switching softness of the new design. Basically, the absence of the abrupt passage from the low doped region (drift layer) to the highly doped region (bulk connected to the cathode contact) allows to the electric field increase without any abrupt variation during the reverse recovery phase. In Figure 15 the reverse recovery waveforms relative to the two designs are reported and a superior softness of the new design is highlighted. While the DEV1 structure exhibit a pronounced voltage oscillation (due to the snappy behavior [20]) at the end of the reverse recovery phase (di/dt = 1000 µA/µs), the DEV2 structure does not show any oscillation and the current waveform has soft transitions at any time. The comparison between the two designs is reported in Table 1. The first relevant result is that the ESD capability is improved and no failures occur up to 8 kV for the DEV2 design, while the DEV1 design exhibits the first ESD failure at 6 kV. The improvement in terms of ESD capability leads to the UIS capability improvement as well. Depending on the load inductance (L), the improvement of the UIS capability (defined as the maximum current during the UIS test that does not lead to the failure of the device before the load inductance completely discharge) increase up to +54% for a load inductance of 1mH, while the increase is +26% for a 10 mH load inductance. This result is coherent with the fact that both the UIS test and the ESD event bring the device under breakdown conditions. The evaluation of the avalanche capability has been carried out by means of a constant current pulse with a duration of 5 µs. Again, the new design shows a superior avalanche capability compared to the DEV1 one.

The overall set of experimental data confirm the superior performances of the proposed design in terms of avalanche capability, however, as expected from the TCAD results, a weak degradation of both the V_{ON} and V_{BR} values occur.

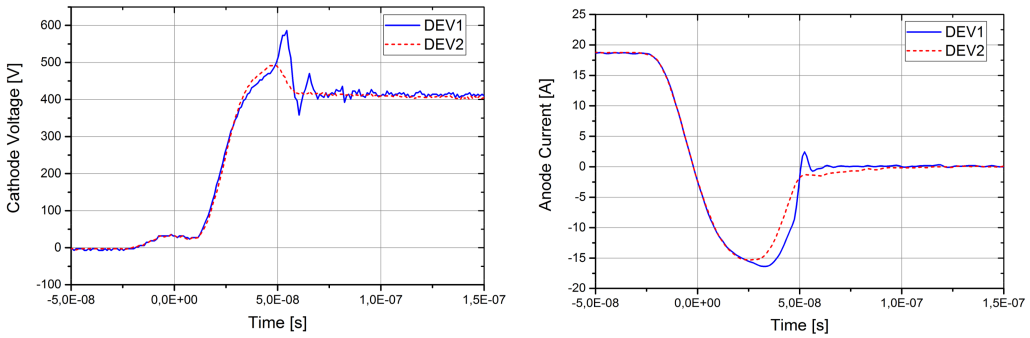


Figure 15. Comparison between the experimental DEV1 and DEV2 design reverse recovery waveforms. I_A = 20 A, di/dt = 1000 A/µs, V_K = 400 V and T = 25 °C. (**a**) Voltage drop; and (**b**) current.

6. Conclusions

An optimized doping profile, tailored to boost the ESD capability of a 600 V Si FRED diode has been presented. The presence of a buffer layer at the transition between the Epi-layer and the high doped cathode has proved as beneficial to both avalanche and ESD capability. An in depth analysis has been carried out to determine the best doping profile capable of improving the ESD robustness by means of 2D TCAD simulations for a complete diode structure (active area together with the termination area). The new design improves the ESD capability since it is able to ensure the current distribution uniform in the structure. The proposed modification does not substantially alter the forward and reverse capabilities of the device, in both static and dynamic conditions. Experimental characterization of the fabricated devices with the new design have proven the higher ESD capability. Moreover, the proposed design improves the softness of the diode during the reverse recovery.

Author Contributions: Simulations results were carried out by Luca Maresca, Giuseppe De Caro and Gianpaolo Romano. The simulations results were reviewed and interpreted by Luca Maresca, Andrea Irace and Giovanni Breglio. Laura Bellemo, Nabil El Baradai and Rossano Carta carried out the production of the samples and performed all the experimental results on investigated devices. The experimental results were reviewed and interpreted by Michele Riccio, Luca Maresca, Andrea Irace and Giovanni Breglio. Finally, Luca Maresca wrote the paper and all authors contributed to the reviewing and proofreading of the journal paper.

Conflicts of Interest: The authors declare no conflict of interest.

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