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Improved Modulated Carrier Controlled PFC Boost Converter Using Charge Current Sensing Method

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Abstract: An improved modulated carrier control (MCC) method is proposed to offer high power factor (PF) and low total harmonic distortion (THD) at a wide input voltage range and load variation. The conventional MCC method not only requires a multiplier and divider, but also is hard to be implemented with a micro controller unit without a high frequency oscillator. To overcome the problem and maintain the advantages of the conventional MCC method, the proposed MCC method adopts a current integrator, an output voltage amplifier, a zero-current duration (ZCD) demodulator of the boost inductor, and a carrier generator. Thus, it can remove a multiplier and well, as it allows for being operable with a general micro control unit. This paper presents an operation principle of the proposed control method. To verify the proposed control method, experimental results with 400 W PFC boost converter is demonstrated.

Keywords: modulated carrier control; ac-dc power converters; power factor correction (PFC); power conversion

1. Introduction

Nowadays, power factor correction (PFC) converters have been indispensable in various applications such as lightings, TVs, computers, and so on. Since drastic electricity demands in those electric devices leads to increase harmonic currents on the power grids, lots of installation of the electric power systems is required, for example, power plants and transmission lines. For the reason, harmonic regulation gets more stringent such as IEC61000-3-2 and various PFC converters and control methods have been proposed and employed widely in various applications, so far [1,2]. Among various types of PFC control method, modulated carrier controlled (MCC) method was proposed and has been utilized for middle to high power range [3–9].

However, the conventional MCC method has a drawback. When a converter using the method operates in discontinuous conduction mode (DCM), PFC performance can be deteriorated [10]. Accordingly, various control methods have been proposed to overcome the current distortion caused by DCM operation [11–14].

Figure 1 shows a control block diagram of MCC method proposed in [15], which could improve the current distortion at DCM operation. It has offered many advantages; a simple control loop that is not requiring the line input voltage detection, fast dynamic response due to no current error amplifier, low total harmonics distortion (THD) with relatively small inductance thanks to a compensation signal of zero current duration demodulator, when compared to the conventional MCC PFC converters. However, the MCC method requires a multiplier and a divider to calculate a current control signal using the sensed inductor current. Thus, if the calculation is carried out using a digital circuit e.g., MCU (Micro Control Unit), an MCU with high frequency oscillator should be employed to do a calculation of fast-varying inductor current. For example, operating frequency of an oscillator for an

MCU must be used at least 5 up to 10 times faster than a switching frequency of the PFC converter considering mathematics instructions processing time. This could be a barrier to utilize digital circuit at the conventional MCC method in practice.

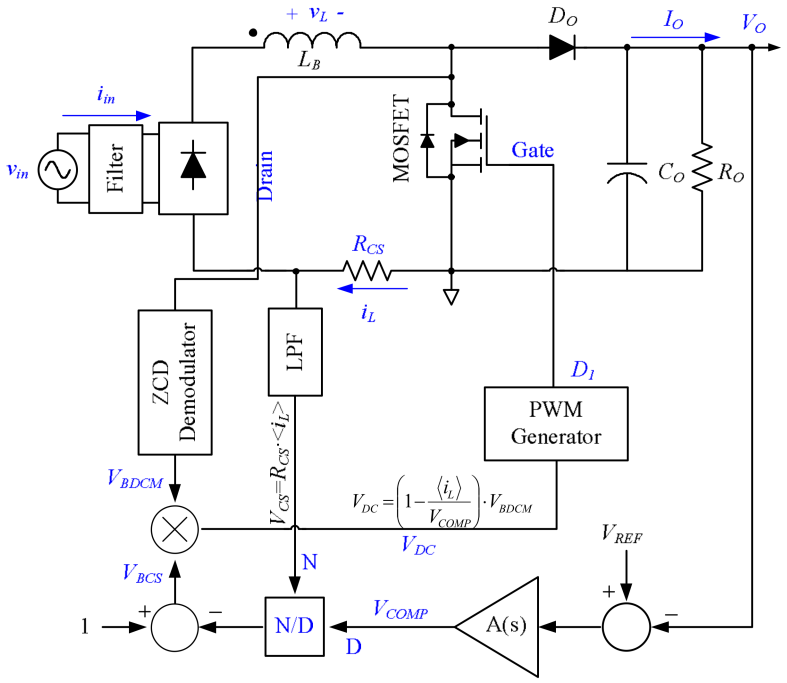

Figure 1. Control block diagram of the conventional modulated carrier controlled (MCC) boost power factor correction (PFC) converter.

This paper proposes an improved MCC method by analyzing and organizing the control equation that is introduced in [15]. The improved MCC method can overcome the problems of conventional one and maintain the advantages of the conventional MCC method. Even, it does not require a multiplier. Thus, it can be easily realized based on analog-digital mixed consisting of a zero-current duration (ZCD) demodulator detecting the continuous conduction time of the inductor current, a modified carrier generator, a current integrator, an MCU operating roles of an output voltage error amplifier and dividing operation.

In this paper, a basic operating principle of the proposed MCC method is explained with introducing detail diagrams of each circuit block. To validate the proposed MCC concept, PFC boost converter with 400 W is tested.

2. Description of Proposed Method

Figure 2 shows a block diagram of the proposed MCC PFC boost converter. The control part is composed of an output voltage error amplifier, ZCD demodulator, a divider, a V/I converter, a carrier generator, and a current integrator.

The ZCD demodulator detects current conduction time of a boost inductor current and translates the time to a voltage. The divider generates a compensation signal by dividing the output voltage error amplifier signal with a voltage corresponding to the current conduction time of a boost inductor current. The value come from the divider is converted from voltage to current, which is transmitted to the carrier generator.

The modified carrier generator consists of a saw-tooth waveform generators and a voltage controlled current source, which generates a compensated carrier signal. In other words, the voltage controlled current source generates I_{saw}. This I_{saw} adjusts amplitude of carrier signal formed of a saw-tooth waveform, which will be used as the compensated carrier signal. Finally, by comparing the

compensated carrier with an integral current, the proposed MCC method can obtain appropriate gate signals that are able to control shape and phase of an input line current same as the input line voltage, regardless of input voltage and load range.

From this section, the control equation well introduced in [15] is re-analyzed and a new control equation is proposed how to overcome the problem. The principle introduced in [15] can also be applied to this proposed MCC control method. The PFC controller controls an input line current i_{in} to be proportional to following an ac input line voltage v_{in} in practice, while keeping an output voltage V_o as a specified reference V_{ref}.

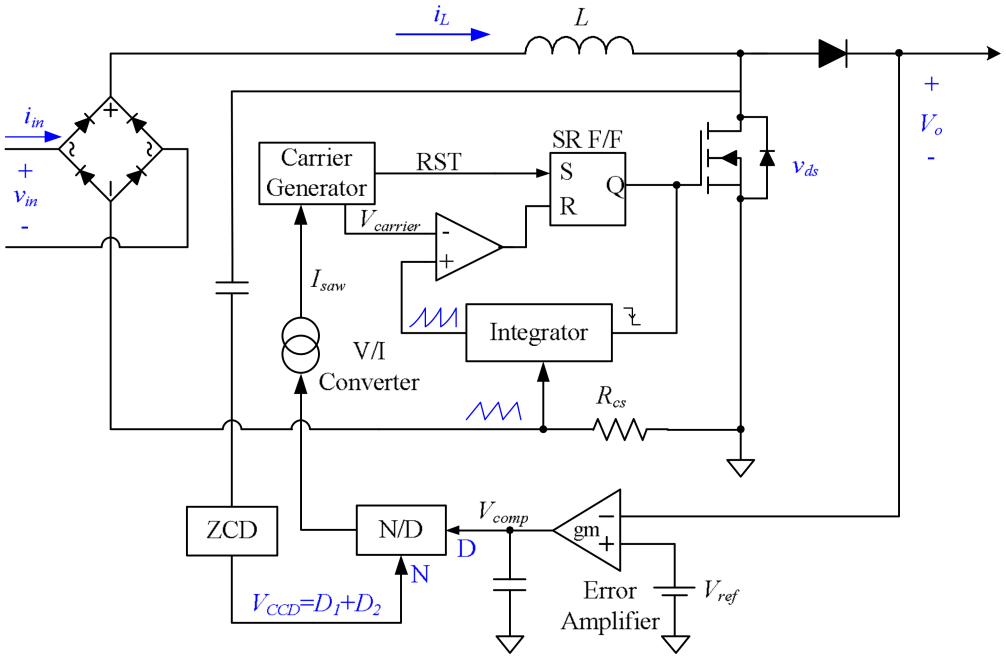

Figure 2. Block diagram of the proposed MCC method.

With this assumption, an input impedance of the PFC converter can be expressed as

$$R_e = \frac{v_{in}}{i_{in}} \tag{1}$$

where R_e is an emulated resistance.

The input current i_{in} can be expressed with a function of the average current of the boost inductor $\langle i_L \rangle$ as

$$i_{in} = \langle i_L \rangle = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt \tag{2}$$

where T_s is a switching period of the MOSFET and i_L is an instantaneous inductor current.

Figure 3 shows inductor voltage and current waveforms, while a boost converter operates in CCM and DCM. Assuming the negligible power losses between the input and output, and slowly-varying v_{in}, voltage conversion ratio of the PFC boost converter can be defined as (3).

$$\begin{aligned} v_{in} \cdot D_1 &= (V_o - v_{in}) \cdot D_2 \\ v_{in} &= \frac{D_2}{D_1+D_2} V_o \end{aligned} \tag{3}$$

where D_1 and D_2 are each ratio of current charging and discharging time of the boost inductor to the switching period, respectively.

Substituting (1) and (2) into (3), a relationship between the output voltage V_o and the average inductor current $\langle i_L \rangle$ can be expressed as

$$R_e \cdot \frac{1}{T_s}\int_0^{T_s} i_L(t)dt = \frac{D_2}{D_1+D_2}\cdot V_o$$
$$\int_0^{T_s} i_L(t)dt = \frac{D_2}{D_1+D_2}\cdot\frac{V_o}{R_e}\cdot T_s \quad (4)$$

Therefore, a final control equation of the conventional MCC method can be expressed as follows

$$\int_0^{T_s} i_L(t)dt = \left(1-\frac{D_1}{D_1+D_2}\right)\cdot V_{comp} \quad (5)$$

where V_{comp} is equal to $\frac{V_o}{R_e}T_s$, that stands for a control signal from the output voltage error amplifier.

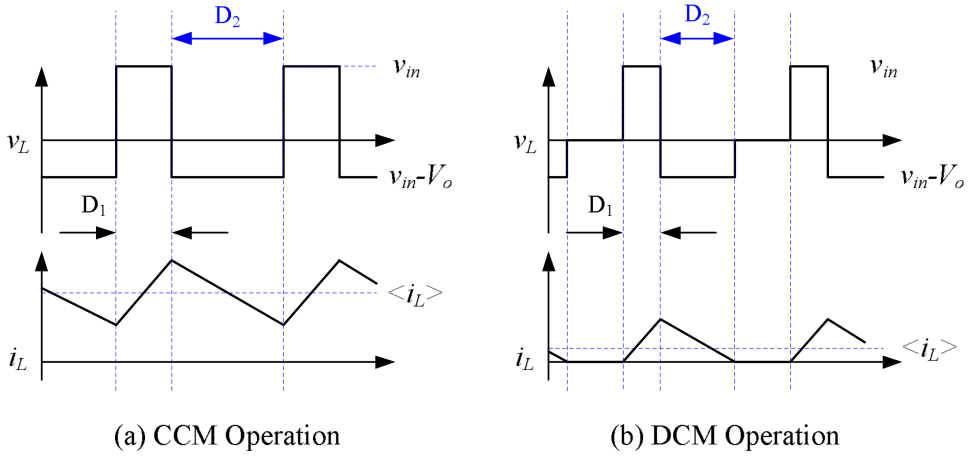

Figure 3. Operating waveforms of the boost converter.

In the mean time, a ratio of the MOSFET turn-on time to the switching period D_1 is the objective to obtain in (5). But, it is hard to obtain D_1 at the same time during dividing V_{comp} with the amount of D_1 and D_2. Therefore, in practice, D_1 and D_2 in previous cycle should be utilized and the dividing calculation should be completed. By simplifying the dividing calculation, the final control equation of the proposed MCC method can be simplified as

$$\int_0^{T_s} i_L(t)dt = V_{comp} - k\frac{t_{on}}{T_s} \quad (6)$$

where k is $\frac{V_{comp}}{D_1+D_2}$ and achieved in previous cycle, and t_{on} is turn-on time of the MOSFET in present cycle.

If proper k can be obtained by calculating V_{comp} with amount interval of D_1 and D_2, required turn-on time t_{on} at the present can be generated by comparing the integrated inductor current.

Moreover, the average inductor current $\langle i_L \rangle$ varies in proportion to the input voltage so that appropriate t_{on} can be obtained to make an input current proportional to the input voltage, regardless of CCM and DCM operation. Therefore, this concept can offer high PFC performance not to use big boost inductance, too.

In addition, a bandwidth of the output voltage error amplifier is typically designed to be less than the input line frequency in PFC converters so that V_{comp} can be considered as a constant value at the scope of the switching frequency. It implies that k and V_{comp} in the left part of (6) does not need to be calculated with high speed, which allows for an MCU without high speed oscillation clock to be implemented, in this control scheme.

3. Configuration of Proposed Method

3.1. Zero-Current Duration (ZCD) Demodulator

Figure 4 shows a simplified ZCD demodulator and the output voltage error amplifier implemented by an MCU. The ZCD demodulator measures a ratio of amount of D_1 and D_2 and converts the measured ratio to a voltage using a zero current detector and a time-to-voltage converter, respectively.

As discussed in previous section, a basic operation of the zero current detector is based on a differentiator based on the ac-coupling capacitor C_D. The ac-coupling capacitor connects to the drain of MOSFET.

In the mean time, when the RST of D-FF (flip-flop) is high during turn-on interval of the MOSFET, the D-FF is in a reset state, so the Q-bar of D-FF does not change regardless of input signal to the CLK Once a gate signal is low and v_{DS} starts to decrease, a current flows with $-I_{CD}$. If the $-I_{CD}$ is higher than reference current I_B, V_D declines to zero and the Q-bar of D-FF becomes low. Next, due to the resonance by the boost inductor and equivalent output capacitance of the MOSFET, V_D switches from low to high. However, a constant high signal is applied to D port of D-FF so that Q-bar output does not change until next gate turn-on signal.

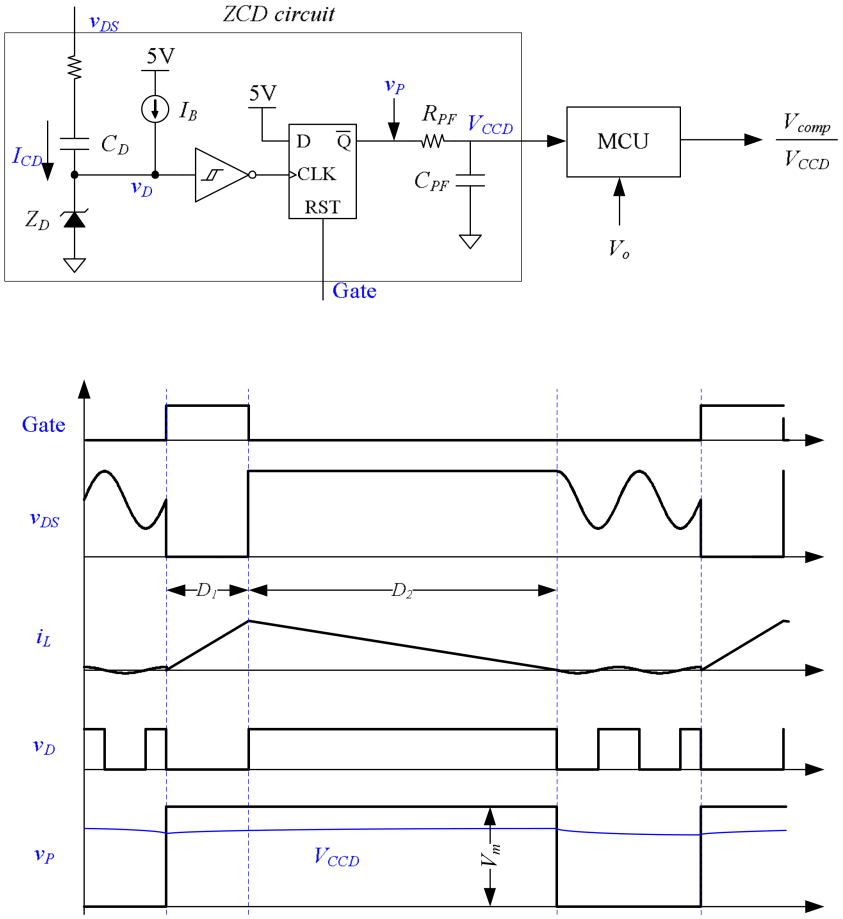

Figure 4. Zero-current duration (ZCD) Demodulator circuits and the operating waveforms.

Therefore, high interval of the Q-bar is the same as the interval of continuous current conduction time, i.e., amount of D_1 and D_2 in a switching period. This pulse can be simply converted to dc voltage by the resistor-capacitor filter R_{PF} and C_{PF}, which can be expressed as follows,

$$V_{CCD} = \frac{1}{T_s}\int_0^{(D_1+D_2)T_s} V_m dt = V_m(D_1 + D_2) \tag{7}$$

where V_m means a peak voltage of the Q-bar pulse.

As for utilizing an MCU, the same is true of V_{CCD}. The value is varied along as low line frequency so that this calculation can be carried out by an MCU using low frequency oscillation clock, as can be seen in Figure 4.

3.2. Current Integrator

In this proposed MCC method, a charge current current control method is employed using charge current integral circuit. This method allows for easily obtaining an average inductor current at a case of constant detecting period. This block consists of an integral capacitor with a switch and a voltage-to-current converter, as shown in Figure 5.

A reset switch M_C is turned on for short instance only whenever a gate signal is low. An inductor current is sensed by the sensing resistor R_{cs} shown in Figure 2. The sensed voltage on R_{cs} is converted to a current and next, it is charged into the integral capacitor C_i. In addition, next gete-turn-off signal reset *G.RST* fully discharges total charges stored in C_i.

A total charge stored in C_i in every switching cycle can be expressed as

$$v_{ics} = \frac{1}{C_i}\left(\int_{D_{2(n-1)}T_s}^{T_s} i_{cs}(t)dt + \int_0^{D_{1(n)}T_s} i_{cs}(t)dt\right) i_{cs} = (i_L \cdot R_{cs}) \cdot A_i \tag{8}$$

where A_i is a gain of the voltage-to-current converter.

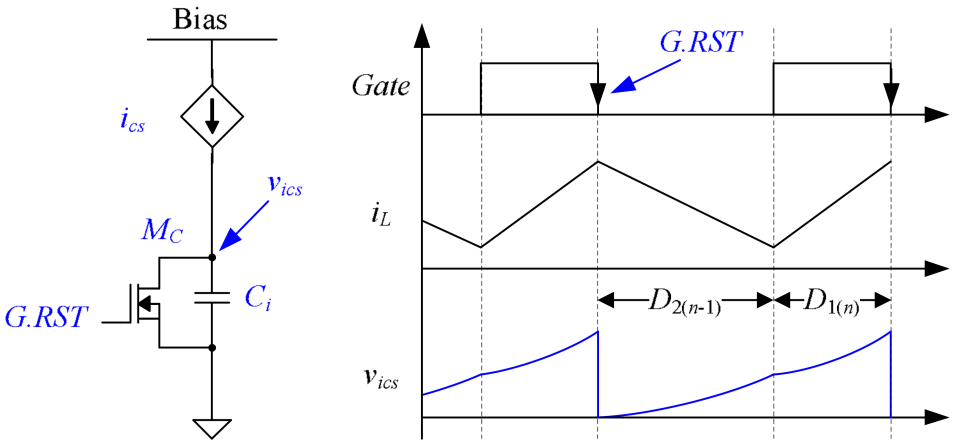

Figure 5. Current integrator and operating waveforms.

Because of low-frequency varying of the inductor current, $D_{2(n-1)}$ can be considered to be almost same as $D_{2(n)}$ so that (8) can be simplified as follows

$$v_{ics} = \frac{1}{C_i}\int_0^{T_s} i_{cs}(t)dt \tag{9}$$

3.3. Carrier Generator

Figure 6 shows a carrier generator comprised of a reset switch, a capacitor and a voltage-controlled current-source. A saw-tooth reset signal *SAW.RST* is synchronized with the gate signal for the main

MOSFET. Whenever the gate signal switches from low to high, a saw-tooth reset signal *SAW.RST* occurs. Once *SAW.RST* is high for short time, C_{cr} is charged up to V_{comp} immediately. Next, a charge stored into C_{cr} starts to be discharged by a carrier current $i_{carrier}$.

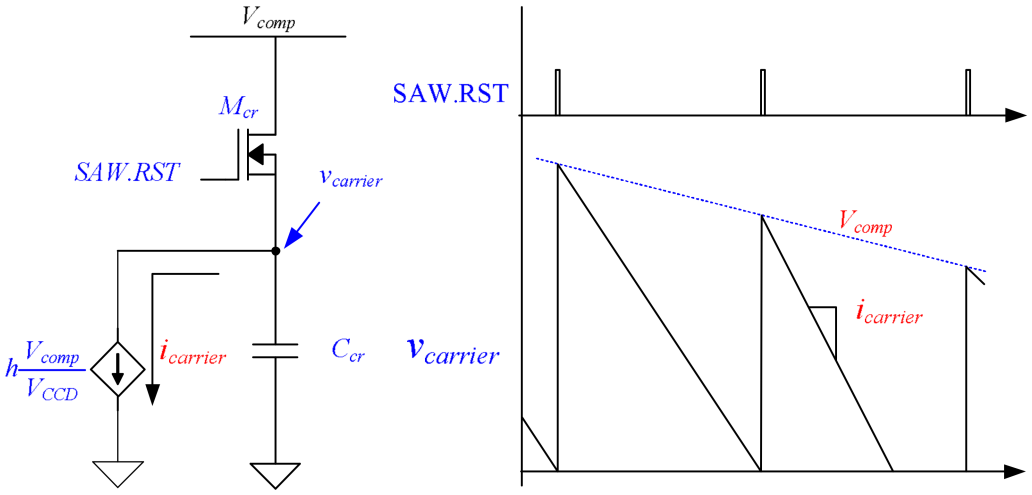

Figure 6. Carrier generator and operating waveforms.

In the mean time, the ZCD demodulator divides V_{comp} into V_{CCD}. The value from the ZCD demodulator is converted to $i_{carrier}$ by the voltage-controlled current-source.

These operation can make a saw-tooth waveforms with different slopes and amplitude depending on V_{comp} and V_{CCD}.

An equation of the saw-tooth waveform can be expressed as

$$v_{carrier} = V_{comp} - \frac{1}{C_{cr}} i_{carrier} \cdot t \tag{10}$$

The equation of the voltage-controlled current-source can be expressed as

$$i_{carrier} = h\frac{V_{comp}}{V_{CCD}} \tag{11}$$

where V_{CCD} is the converted voltage of the amount time of D_1 and D_2, and h is a conversion ratio of voltage-controlled current-source.

Substituting (11) with (10), the carrier function can be expressed as

$$v_{carrier}(t) = V_{comp} - \frac{h}{C_{cr}} \cdot \frac{V_{comp}}{V_{CCD}} \cdot t \tag{12}$$

3.4. Pulse Width Modulation (PWM) Circuit

Figure 7 shows a PWM circuit where it can be seen that an integrated current v_{ics} obtained from (9) is compared with with a carrier signal $v_{carrier}$ generated from (12). This comparison can generate a gate turn-on signal for the main MOSFET.

By comparing the integrated current and carrier signal, proper turn-on time t_{on} of the MOSFET can be obtained and expressed as

$$\frac{1}{C_i}\int_0^{T_s} i_{cs}(t)dt = V_{comp} - \frac{h}{C_{cr}} \cdot \frac{V_{comp}}{V_{CCD}} \cdot t_{on} \tag{13}$$

In addition, T_s is constant due to fixed switching frequency and V_m is set to unity so that t_{on} can be considered as D_1, shown in (6).

Finally, proper duty ratio D_1 can be obtained to control the input current same as the shape of the input voltage regardless of variation of line input voltage or load condition.

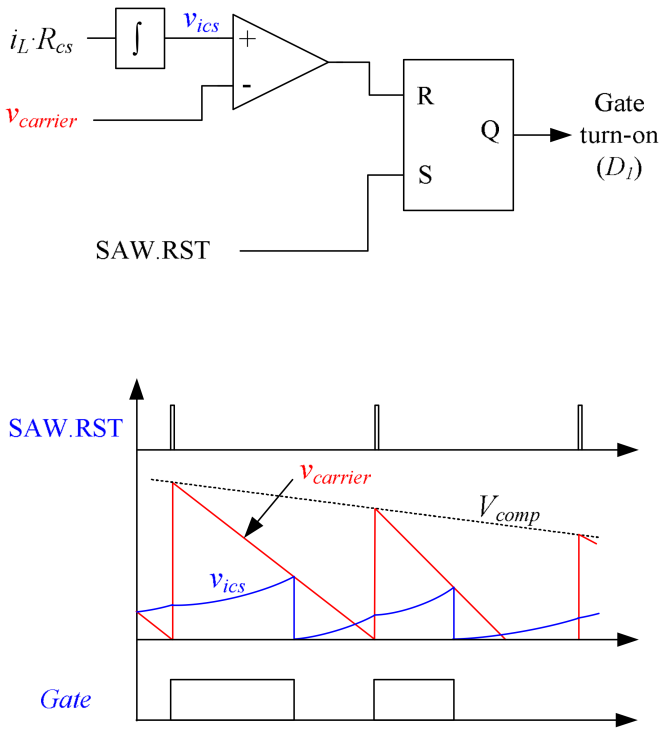

Figure 7. Plus width modulation circuit and operating waveforms.

4. Experimental Results

4.1. Implementation Control Circuit

The proposed control method can be implemented with fully analog circuits or analog-digital mixed. As discussed previously, the divider's bandwidth is no longer required for high speed because of a calculating low-frequency varying values of the output voltage error amplifier and the ZCD demodulator. It allows that the proposed MCC method is realized with the analog-digital mixed, as shown in Figure 8.

The division calculation was carried out using an MCU, which conducts operations of an output voltage error amplifier and division operation. Each operation generates the output voltage error amplifier's output V_{comp} and the ZCD demodulator's output V_{CCD}. In the schematic, a 'V/I' block stands for V/I converter composed of some p- and n-type bi-polar junction transistors and amplifiers, as shown in Figure 9.

Table 1 shows key parameters used in experiments for the proposed MCC PFC boost converter, respectively. In the table, 'Vrms' stands for the root mean square value of voltage.

Table 1. Electrical specifications and key parameters of the boost converter.

Parameter	Values
Input Voltage	85 Vrms~265 Vrms
Line Frequency	60 Hz
Output Voltage	380 Vdc
Output Power	400 W
Switching Frequency	100 kHz
Boost Inductance	750 μH
CCD filter	R_{PF}: 1 kΩ, C_{PF}: 22 nF

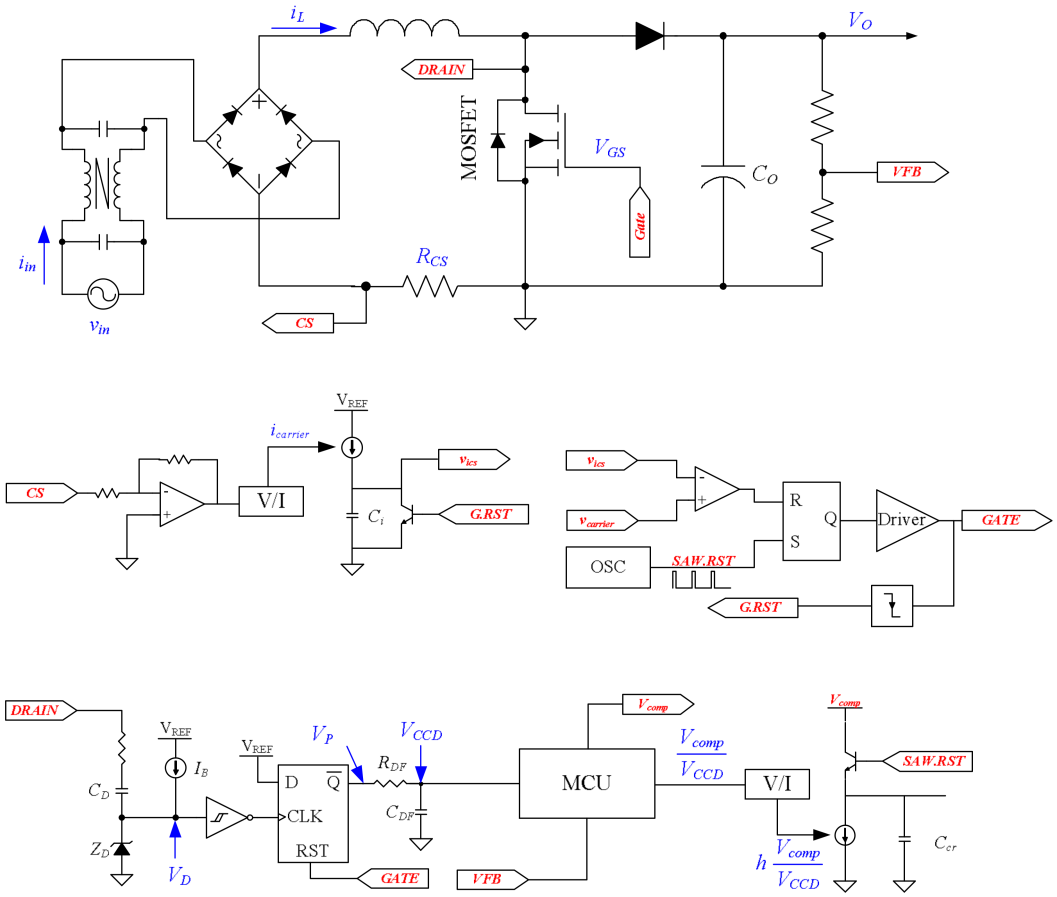

Figure 8. Schematic of the proposed MCC method implemented in the PFC boost converter.

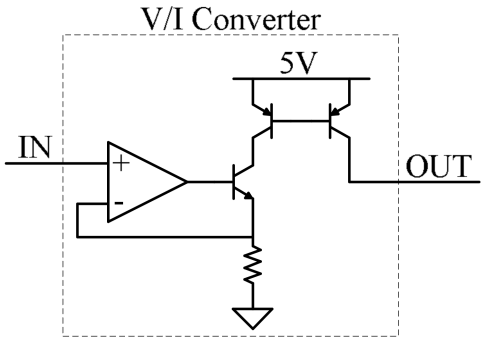

Figure 9. V/I converter circuit.

4.2. Experimental Results

Figure 10 illustrates experimental waveforms of the ZCD demodulator. At the waveforms, each notation is identical to the presented ones shown in Figure 4. It can be seen that when the drain-to-source voltage v_{DS} decrease, ZCD pulse signal V_P becomes low and it lasts until the next gate-turn-on instance and the interval of V_P equals to the interval of inductor current conduction.

Figure 11 illustrates experimental waveforms of PWM circuit part. By comparing the carrier signal $v_{carrier}$ with the integral value of sensed inductor current v_{ics}, a gate signal is low and then, v_{ics} is reset for short time and is increased by the integrator.

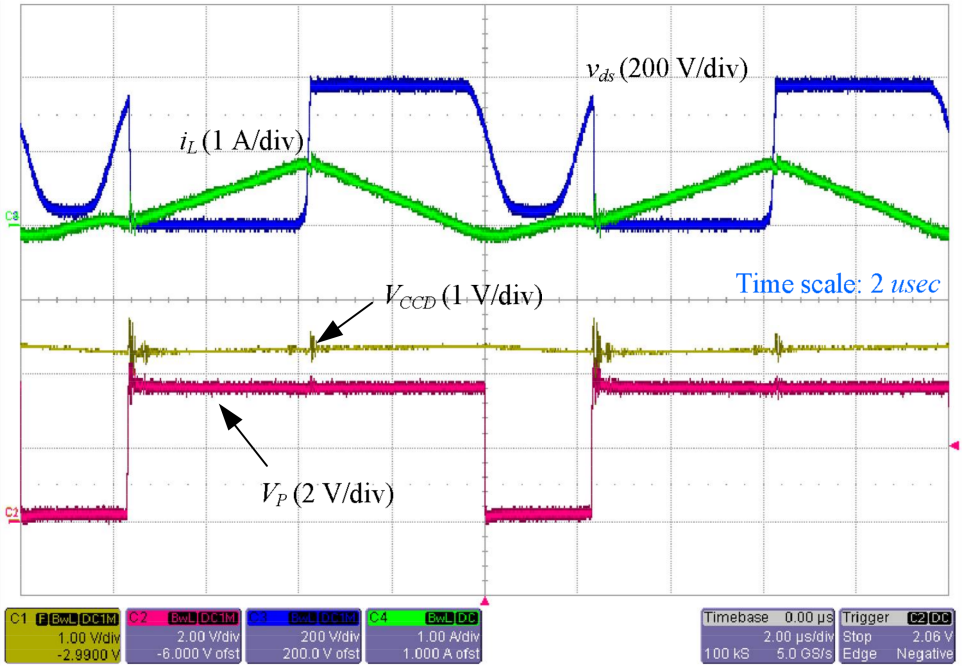

Figure 10. Experimental waveforms of ZCD demodulator.

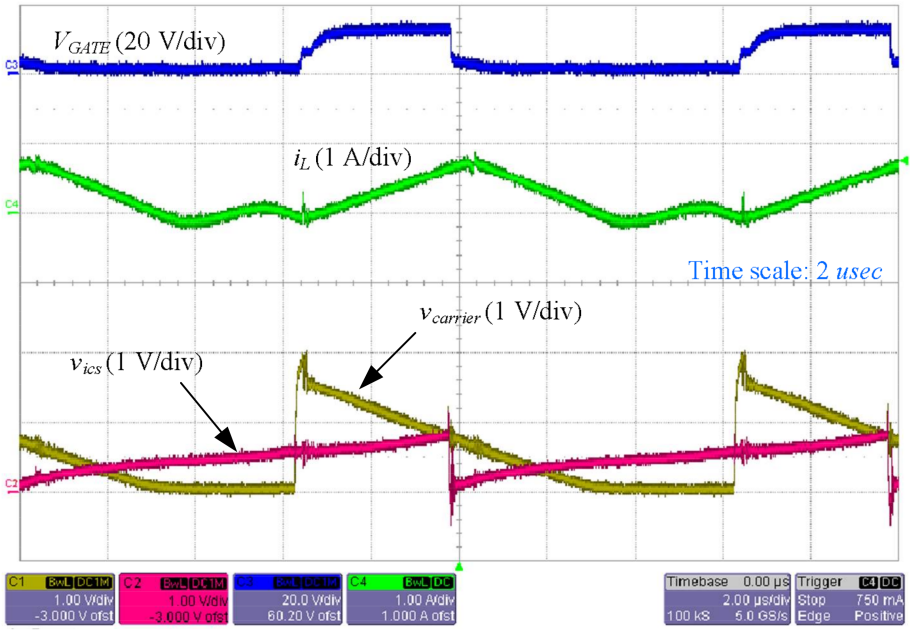

Figure 11. Experimental waveforms of PWM circuit.

These results are in good agreement with the explanation discussed in previous sections.

Figures 12 and 13 show operating waveforms of the proposed MCC PFC boost converter at an input line voltage of 220 Vrms with different load condition of 400 W and 160 W.

The ZCD demodulator output voltage V_{CCD} of 3 V implies CCM operation of the PFC boost converter. Once the PFC boost converter enters into DCM, V_{CCD} starts decreases less than 3 V. In Figure 12, V_{CCD} is maintained as 3 V that means that the PFC boost converter is operating in CCM in the whole ac line cycle. On the contrary, Figure 13 shows that V_{CCD} fluctuates near the side band of ac line zero-crossing point. It infers DCM operation of the PFC boost converter at the region due load decrease.

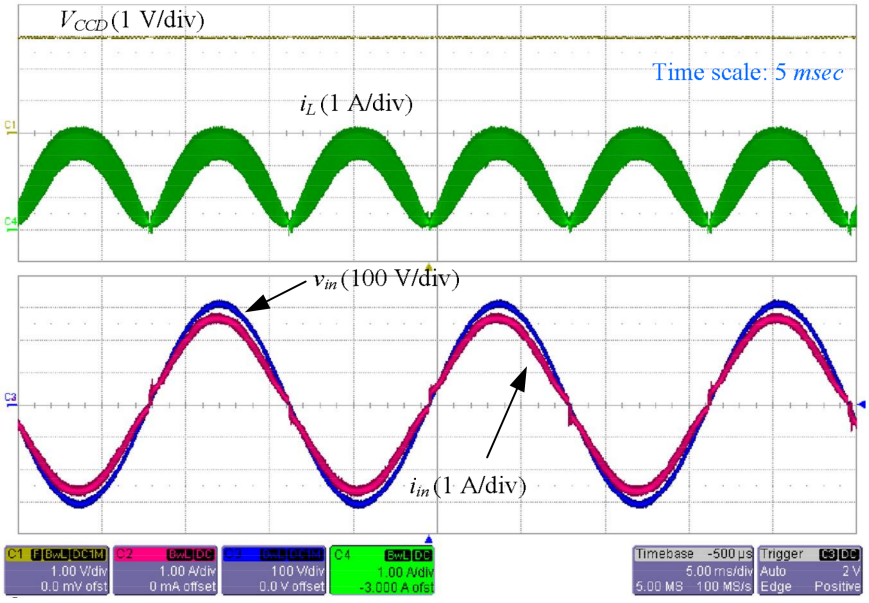

Figure 12. Experimental waveforms at 220 Vrms and 400 W load.

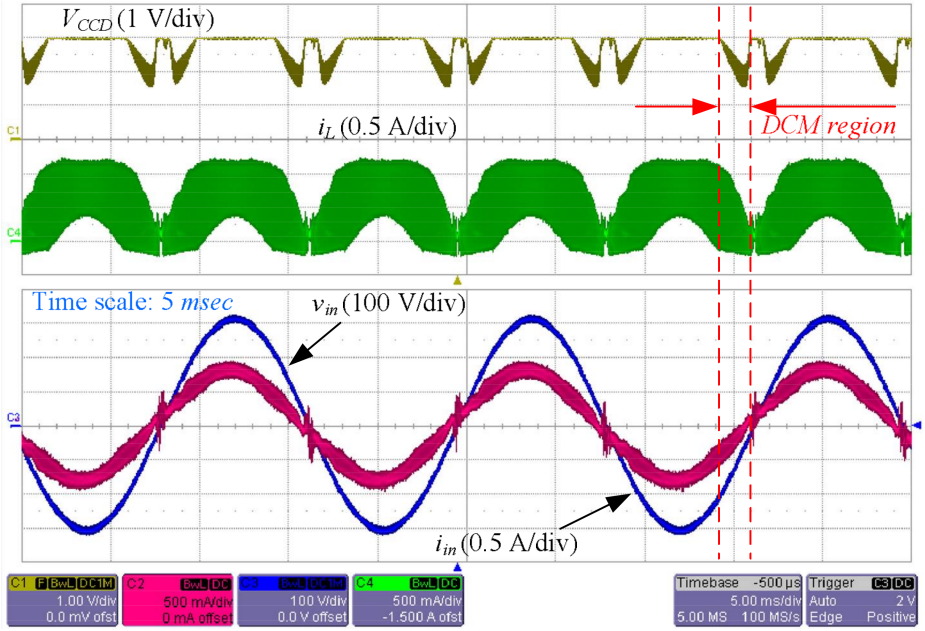

Figure 13. Experimental waveforms at 220 Vrms and 160 W load.

It can be seen in Figure 12 that inductor current is well controlled by the proposed MCC method, at 400 W load condition so that the shape and phase of input line voltage i_{in} is almost the same as the input line voltage v_{in}. Since load decreases from 400 to 200 W, partial DCM operation of the PFC boost converter can be seen in Figure 13. The inductor current is also well controlled like the case of 400 W, that results in the input line current same as the input line voltage. In addition, little current distortion can be seen at the transition between CCM and DCM.

Figure 14 shows a measured THD (left Y-axis) and power factor (PF) (right-Y-axis) at an input line voltage of 220 Vrms, depending on load variations. In full load condition of 400 W, THD of 3.03% is measured.

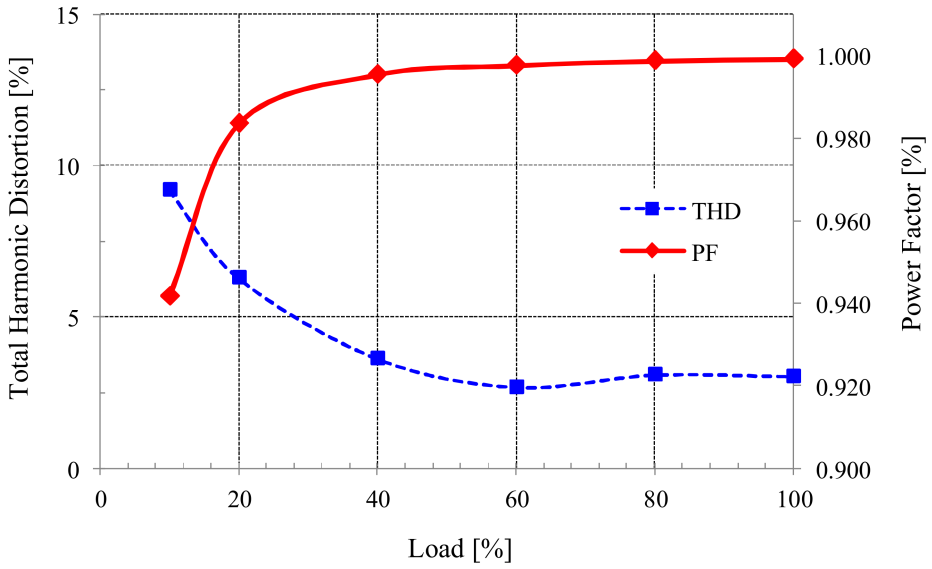

Figure 14. Total harmonics distortion (THD) & power factor (PF) results of the proposed MCC converter.

As can be inferred in Figure 13, the PFC converter starts entering into DCM from around 200 W. So, THD starts to be distorted and THD at 160 W is measured up to 3.62%. Besides it, even if the load condition decreases to 10%, THD is not big increased that is less than 10%. In the mean time, PF is higher than 0.94 at 10% load condition as well.

5. Conclusions

In this paper, an improved MCC method is proposed for a PFC boost converter and implemented based on analog-digital mixed circuits, consisting of a current integrator, a carrier generator and a ZCD demodulator circuit, and a digital MCU, while maintaining advantages of the simple control structure and fast dynamic response of the conventional MCC method. In addition, it can offer a high PF and low THD at wide load range even if using relative small inductance unlike the conventional MCC method using a big enough inductor to guarantee CCM under as much load range as possible so that harmonic regulations are satisfied. It means that better power density can be expected.

The proposed control method and feasibility was verified using 400 W PFC boost converter. The measured THD are 3.03% and 3.62% at 400 W and 160 W load condition in 220 Vrms, respectively. Even the measured PF is higher than 0.94 at 10% load condition. It showed an outstanding performance the same as the conventional MCC method with a multiplier.

Given the results, the proposed control method could be a good candidate as a controller for high density and high performance PFC boost converter.

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Author Contributions: Jintae Kim conceived, designed the circuit, performed the experiments, and wrote the manuscript. Chung-Yuen Won participated in research plan development and revised the manuscript. All authors have contributed to the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. International Electrotechnical Commission. *Electromagnetic Compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16 A per Phase), IEC 61000-3-2*; International Electrotechnical Commission: Geneva, Switzerland, 2014.

2. Institute of Electrical and Electronics. *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*; IEEE Std 519-2014 (Revision of IEEE Std 519-1992); Institute of Electrical and Electronics: Piscataway, NJ, USA, 2014; pp. 1–29.
3. Maksimovic, D.; Jang, Y.; Erickson, R. Nonlinear-carrier control for high-power-factor boost rectifiers. *IEEE Trans. Power Electron.* **1996**, *11*, 578–584. [CrossRef]
4. Hwang, J.; Chee, A.; Ki, W.-H. New universal control methods for power factor correction and DC to DC converter applications. In Proceedings of the IEEE 1997 Applied Power Electronics Conference, Atlanta, GA, USA, 27 February 1997; pp. 59–65.
5. Wang, Y.; Li, J. A Novel High-performance Single-phase PFC Approach Based on One-cycle Control. In Proceedings of the IEEE Conference on IEEE Industrial Electronics, Paris, France, 6–10 November 2006; pp. 1763–1768.
6. Luo, J.; Jeoh, M.K.; Huang, H.C. A new continuous conduction mode PFC IC with average current mode control. In Proceedings of the IEEE International Conference on Power Electronics and Drive Systems, Singapore, 17–20 November 2003; pp. 1110–1114.
7. Jiang, T.; Mao, P.; Xie, S. Analysis and improvement on input current of one-cycle controlled PFC converter. In Proceedings of the IEEE 2010 Conference on Industrial Electronics and Applications, Taichung, Taiwan, 15–17 June 2010; pp. 2094–2098.
8. Orabi, M.; Haron, R.; El-Aroudi, A. Comparison between Nonlinear-Carrier Control and Average-Current-Mode Control for PFC Converters. In Proceedings of the IEEE Power Electronics Specialist Conference, Orlando, FL, USA, 17–21 June 2007; pp. 1349–1355.
9. Chiang, J.-H.; Liu, B.D.; Chen, S.-M. A Simple Implementation of Nonlinear-Carrier Control for Power Factor Correction Rectifier with Variable Slope Ramp on Field-Programmable Gate Array. *IEEE Trans. Ind. Inform.* **2013**, *9*, 1322–1329. [CrossRef]
10. De Gusseme, K.; Van de Sype, D.M.; Van den Bossche, A.P.M.; Melkebeek, J.A. Input-Current Distortion of CCM Boost PFC Converters Operated in DCM. *IEEE Trans. Ind. Inform.* **2007**, *54*, 858–865. [CrossRef]
11. Lim, S.F.; Khambadkone, A. A simple digital DCM control scheme for boost PFC operating in both CCM and DCM. *IEEE Energy Convers. Congr. Expos.* **2010**, *47*, 1218–1225.
12. Ku, C.-P.; Chen, D.; Lin, S.-H. A new control scheme for boost PFC converters for both CCM and DCM operations. *IEEE Energy Convers. Congr. Expos.* **2011**, 1334–1338. [CrossRef]
13. Chen, Y.-L.; Chen, Y.-M. Line Current Distortion Compensation for DCM/CRM Boost PFC Converters. *IEEE Trans. Power Electron.* **2016**, *32*, 2026–2038. [CrossRef]
14. Chen, F.-Z.; Maksimović, D. Digital Control for Improved Efficiency and Reduced Harmonic Distortion over Wide Load Range in Boost PFC Rectifiers. *IEEE Trans. Power Electron.* **2010**, *25*, 2683–2692. [CrossRef]
15. Kim, J.; Choi, H.; Won, C.-Y. New Modulated Carrier Controlled PFC Boost Converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4772–4782. [CrossRef]