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Coordination Control Method Suitable for Practical Engineering Applications for Distributed Power Flow Controller (DPFC)

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Abstract: To control multiple series units of distributed power flow controller (DPFC), a hierarchical control method is proposed. This coordination control system consists of a coordination controller and multiple series unit controllers. According to the demand of power flow ordered by a dispatch center, the corresponding series-compensated voltage is calculated by a high-level controller and transferred to each series unit controller. Comparing the targeted compensated voltage with actual injected voltage, the modulation signal of the converter will be modified to change the power flow accurately. The DPFC system model is built in Power Systems Computer Aided Design/Electromagnetic Transients including DC (PSCAD/EMTDC). The simulation result indicates that the proposed hierarchical control method is effective and can be considered as an option for practical engineering applications in the future.

Keywords: AC transmission; distributed power flow controller; hierarchical coordination control; series compensated voltage

1. Introduction

The mechanically controlled AC power transmission systems, including the use of high-power electronics, advanced control centers, and communication links, were proposed in 1986 by N.G. Hingorani from American Electric Power Research Institute (EPRI) [1–3]. For a simple flexible AC transmission system (FACTS) parallel device or a simple FACTS series device, only the reactive power can be exchanged if the energy storage unit is not disposed on the DC capacitor side within the FACTS device. That is, its effect is equivalent to a tunable inductor or an adjustable capacitor. As a consequence, it is limited and not flexible enough for regulating the power flow of the transmission line.

The conception of a unified power-flow controller (UPFC) was proposed in 1991 by Dr. L. Gyugyi [4,5] and has been extensively studied to date [6–11]. The UPFC can be regarded as the combination of shunt and series FACTS linked by a common DC. Generally, the shunt device is a static synchronous compensator (STATCOM), while the series device is an example of a static synchronous series compensator (SSSC). Bidirectional active power can flow between the parallel and series units via the DC-bus capacitor to realize 'four quadric' power-flow regulation. Additionally, the active power flow and reactive power flow of the transmission line can be controlled independently, which matches its "universal" mind for control. However, the parallel and series units of UPFC are installed centrally; as a consequence, many land resources are required for the installation. The series side is integrated into one unit, which causes a large fold line change in the voltage distribution of the transmission line. Besides this, the requirement for the insulation is high due to the direct electrical connection of the parallel and series units. The aforementioned factors have led research workers to rethink UPFC from the aspects of project cost, ease of operation and maintenance.

Prof. Deepak Divan proposes the concept of distributed FACTS (D-FACTS) [12–14]. As a member of the DFACTS family, the distributed static series compensator (DSSC) has been studied widely [15–19]. Multiple DSSCs are sparsely hung onto the transmission line through a single-turn transformer (STT). As a single-phase inverter with small capacity, the DSSC can be designed into a simple structured device with low insulation cost and easy installation. The control principle of DSSC is similar to that of SSSC, both of which control the power flow effectively by changing the line reactance flexibly.

The idea of a distributed power flow controller (DPFC) was proposed in 2007, as a new component within the FACTS family by Zhihui Yuan from Delft University of Technology [20–22]. DPFC is derived from UPFC. DPFC can be considered as a UPFC without a common DC link between the shunt and series converters. A parallel unit of the DPFC is installed in a central area while the series units of DPFC employ multiple distributed series units similar to DSSC. In UPFC, the active power support of the series unit is transported by a common DC link. In DPFC, however, the DC power channel is removed and replaced by the transmission power line. Due to the lower impedance characteristic of the third harmonic compared with higher-frequency harmonics, the third harmonic active power is chosen as an energy conversion medium. The parallel unit absorbs the base-frequency active power from the bus line and converts it into third harmonic active power. The third harmonic active power then is injected to the transmission line and flows along the line. The distributed series units control the exchange between the 3rd harmonic active power and base-frequency active power. Simultaneously, the responding voltages will be generated and injected into the transmission line. In our research, we only care about the base frequency voltage for base frequency power flow control. Thus, later in this paper, the series-compensated voltage indicates the base-frequency series-compensated voltage.

There are different research results about DPFC from different aspects of application. In [23–25], DPFC was used to improve power quality problems during voltage sag and swell conditions. In [26], taking the constraints of DPFC, an optimal scheduling model is established to realize wind power spillage minimization. However, the generation of the reference base-frequency voltage is not clear. In [27], by introducing an MMC (modular multilevel converter) at the shunt side of the DPFC, a new topology of DPFC is proposed. References [28,29] proposed a specific power flow control method: taking the terminal voltage of the transmission line as a reference, this technique requires high-speed communication links to transfer the real-time waveform of the terminal voltage to multiple series unit controllers. From the point view of engineering applications, this power flow control method is not practical and needs to be improved.

To address the above issue, this paper proposes a hierarchical coordination control method for DPFC series units. Taking advantage of the fact that the DPFC series unit is able to collect the real-time phase of the transmission line current, the phase difference between the fundamental frequency line current and the terminal voltage of the transmission line can be reflected by a sine wave generator within the DPFC series unit. Therefore, the waveform of the real-time phase of the terminal voltage can be reproduced correctly during a control period. In this way, a high-speed communication link is not required. In addition, a wide area measurement system (WAMS) is introduced to transfer the receiving-end voltage of the transmission line back to the upper-level controller.

The rest of paper is structured as follows. The basic principle of DPFC is presented in Section 2. In Section 3, the coordination control system is discussed. The computation of the reference series-compensated voltage is introduced in detail, and the lower-level series-unit control scheme is depicted. In Section 4, simulation results in PSCAD/EMTDC are used to demonstrate the effectiveness of the proposed coordination control method, and these are compared with the state-of-the-art methods for DPFC power flow control. In Section 5, conclusions and future work are presented.

2. Basic Principle of the DPFC

A parallel FACTS device and many distributed series FACTS devices constitute a DPFC. The structure of a DPFC is shown in Figure 1. In the following, the parallel FACTS device is called a parallel

unit while the series FACTS devices are called series units. The parallel unit is located at the sending end of the transmission line, and series units are distributed along the transmission line.

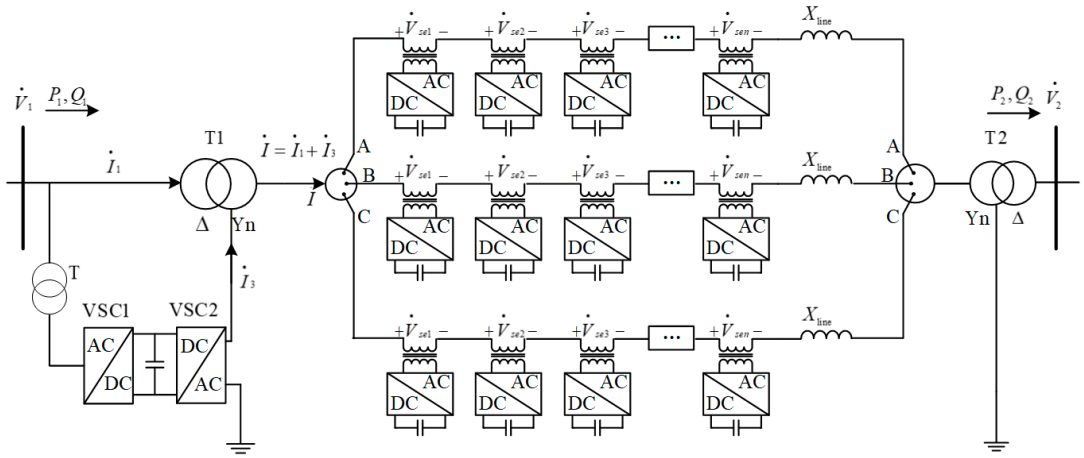

Figure 1. Structure of a distributed power flow controller (DPFC).

As shown in Figure 1, T1 and T2 are delta-wye grounded transformers The delta side of the transformer is blocked for the third harmonic current while the wye grounded side is allowed for flowing 3rd harmonic current; thus, the energy channel of third harmonic active power is formed, which makes the active power exchange between the parallel unit and series units of the DPFC possible.

The parallel unit of the DPFC is composed of two back-to-back voltage source converters (VSCs). VSC1 is a three-phase converter which is responsible for maintaining the bus voltage and keeping the DC capacitor voltage stable. VSC2 is a single-phase converter, which is used to generate a constant third harmonic current. Thus, the parallel unit of the DPFC plays the role of absorbing the active power from the bus, and then converting it to the third harmonic active power. The third harmonic active power is injected into the transmission line and taken in by the DPFC series units as active power support. After that, the base-frequency active power is generated by the power exchange control in the series units.

In Figure 1, $\dot{V}_1$ and $\dot{V}_2$ represent the voltage at the sending-end and receiving-end of the transmission line, respectively. $\dot{I}_3$ is the equivalent third harmonic current. P_1, Q_1, P_2, and Q_2 indicate the power flow at the sending-end and receiving-end of the transmission line, respectively. Each DPFC series unit generates a compensated voltage $\dot{V}_{\mathrm{sei}}$ (i = 1, 2, 3, . . . , n), and all the $\dot{V}_{\mathrm{sei}}$ values form a final compensated voltage $\dot{V}_{\mathrm{se}}$. X_{line} is the equivalent impedance of the transmission line.

By injecting the compensated voltage $\dot{V}_{\mathrm{se}}$, the active and reactive power of the transmission line can be controlled. The equivalent phasor diagram of the DPFC is expressed in Figure 2.

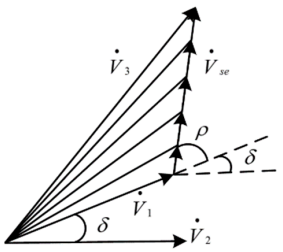

Figure 2. The working principle of the DPFC.

In Figure 2, $\dot{V}_{\mathrm{se}}$ represents the integrated compensated voltage, δ represents the phase angle where $\dot{V}_1$ surpasses $\dot{V}_2$, ρ stands for the phase angle where $\dot{V}_{\mathrm{se}}$ surpasses $\dot{V}_1$, and $(\delta + \rho)$ indicates the

phase angle where $\dot{V}_{se}$ surpasses $\dot{V}_2$. $X_\Sigma = X_{T1} + X_{line} + X_{T2}$ denotes the total impedance of the AC transmission power system, where X_{T1} and X_{T2} represent the impedance of the transformer T1 and T2, respectively. Thus, the natural power flow of the transmission line is expressed as

$$P_{20} = \frac{V_1 V_2 \sin\delta}{X_\Sigma} \tag{1}$$

$$Q_{20} = \frac{V_1 V_2 \cos\delta - {V_2}^2}{X_\Sigma} \tag{2}$$

With DPFC series units, the power flow becomes

$$P_2 = \mathrm{Re}\left[\dot{V}_2 \overset{*}{I_1}\right] = \frac{V_1 V_2 \sin\delta + V_{se} \times V_2 \sin(\delta+\rho)}{X_\Sigma} \tag{3}$$

$$Q_2 = \mathrm{Im}\left[\dot{V}_2 \overset{*}{I_1}\right] = \frac{V_1 V_2 \cos\delta + V_{se} \times V_2 \sin(\delta+\rho) - {V_2}^2}{X_\Sigma} \tag{4}$$

$\dot{V}_1$ and $\dot{V}_2$ can be regarded as constant during a certain period of time in the actual power system operation, and so the increment of active and reactive power flow at the receiving-end can be written as follows:

$$\Delta P_2 = \frac{V_{se} \times V_2 \sin(\delta+\rho)}{X_\Sigma} \tag{5}$$

$$\Delta Q_2 = \frac{V_{se} \times V_2 \cos(\delta+\rho)}{X_\Sigma} \tag{6}$$

Based on the above equations, it is obvious that the power flow of the transmission line can be controlled efficiently by changing the magnitude value and phase angle of the series-compensated voltage slightly and flexibly.

3. Coordination Control System of a DPFC

The proposed coordination control system of a DPFC consists of an upper-level controller, a parallel unit controller and multiple series unit controllers. The schematic diagram of this control system is depicted in Figure 3.

In Figure 3, E_{dcsh_ref} is the reference value of the DC capacitor voltage in the parallel unit while I_{3_ref} indicates the referenced third harmonic frequency. The control method for the parallel unit can be found in [20–22]; thus, the control scheme of the coordination control method for the series unit is mainly discussed in this research work.

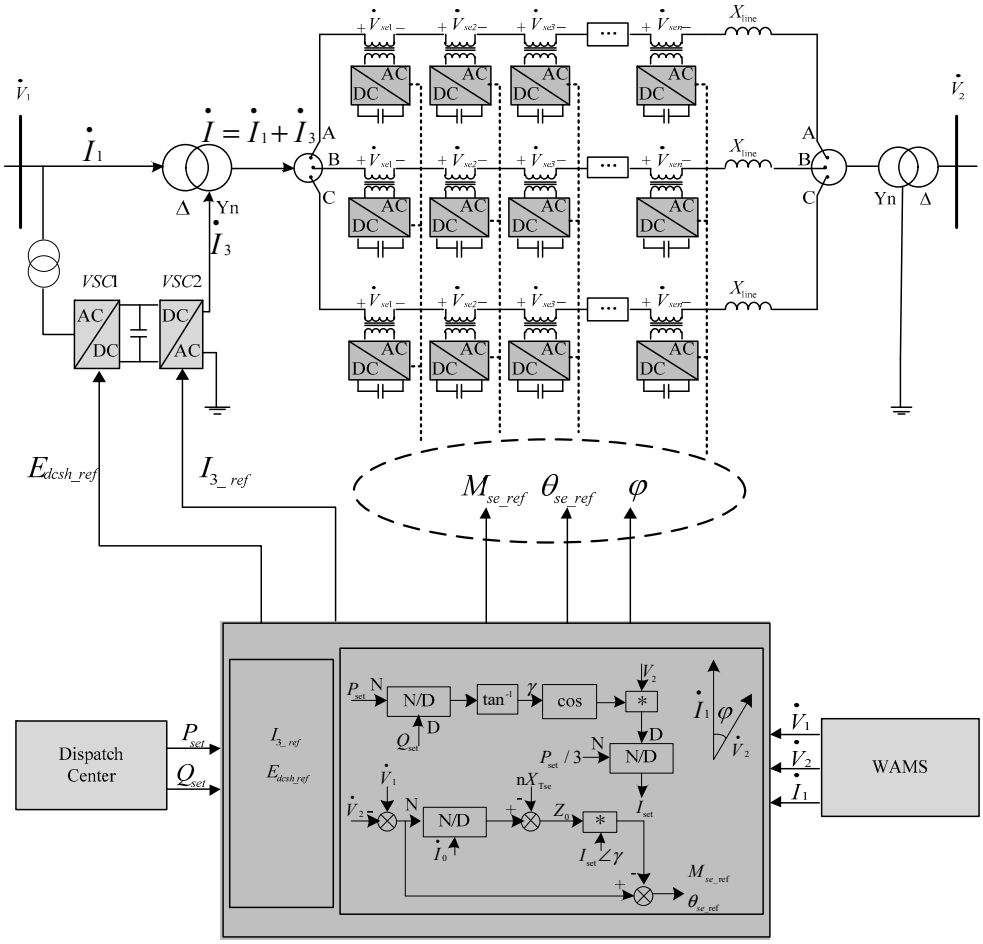

Figure 3. The structure of the coordination control system of a DPFC.

3.1. The Computation of Reference Compensated Voltage

According to the demand of power flow P_{set} and Q_{set} ordered by the dispatch center, and the states of transmission line $\dot{V}_1$, $\dot{V}_2$ and $\dot{I}_1$ attained by WAMS, the corresponding series-compensated voltage $\dot{V}_{\text{se\_ref}}$ is calculated by an upper-level controller. The calculation process is as follows:

- Setting the number of DPFC series units to be n, the total base-frequency impedance between the sending-end and receiving-end of the power transmission system is Z_0, the short circuit reactance of each series unit is X_{Tse}, and the initial current phasor of transmission line is

$$\dot{I}_0 = \frac{\dot{V}_1 - \dot{V}_2}{Z_0 + nX_{\text{Tse}}} \tag{7}$$

- Corresponding to the target power flow, I_{set} and α represent the RMS value of $\dot{I}_1$ and phase angle that $\dot{I}_1$ leads $\dot{V}_2$, respectively.

$$P_{\text{set}} = \text{Re}\left[\dot{V}_2 \dot{I}_{\text{set}}^{\,*}\right] = V_2 I_{\text{set}} \cos\alpha \tag{8}$$

$$Q_{set} = \text{Im}\left[\dot{V}_2 \dot{I}_{\text{set}}^{\,*}\right] = V_2 I_{\text{set}} \sin\alpha \tag{9}$$

where $\dot{I}_{set}^{*}$ denotes the conjugate complex of the targeted current line $\dot{I}_{set}$.
Supposing that the voltage phasors at the sending-end and receiving-end of the transmission system are unchanged during one control cycle, then we have

$$I_{set} = \frac{P_{set}}{V_2 \cos \alpha} \tag{10}$$

$$\alpha = \arctan(Q_{set}/P_{set}) \tag{11}$$

- The corresponding series-compensated voltage generated by each DPFC series unit is $\dot{V}_{se\_ref} = M_{se\_ref}\angle\theta_{se\_ref}$, where M_{se_ref} is the RMS value of the $\dot{V}_{se\_ref}$ and θ_{se_ref} is the phase angle that $\dot{V}_{se\_ref}$ surpasses the voltage phasor $\dot{V}_2$. From the view of the total system, the effect of $\dot{V}_{se\_ref}$ can be regarded as an equivalent series impedance Z_{set} injected by each series unit. Then, another expression of the transmission line is

$$\dot{I}_{set} = \frac{\dot{V}_1 - \dot{V}_2}{Z_0 + nZ_{set}} \tag{12}$$

According to the obvious assumption and analysis, the series-compensated voltage is

$$\dot{V}_{se\_ref} = Z_{set}\dot{I}_{set} = \frac{\dot{V}_1 - \dot{V}_2 - Z_0\dot{I}_{set}}{n} = M_{se\_ref}\angle\theta_{se\_ref} \tag{13}$$

- At the initial stable state $t = t_0$, the phase angle that $\dot{I}_1$ surpasses $\dot{V}_2$ is φ, and all these measurements are saved in the upper-level controller.
- The RMS value and phase angle of the corresponding series-compensated voltage M_{se_ref}, θ_{se_ref} and the phase angle φ are transferred to each series unit via a power line carrier communication link.

3.2. The Control Scheme of DPFC Series Units

The structure of the DPFC series unit is shown in Figure 4.

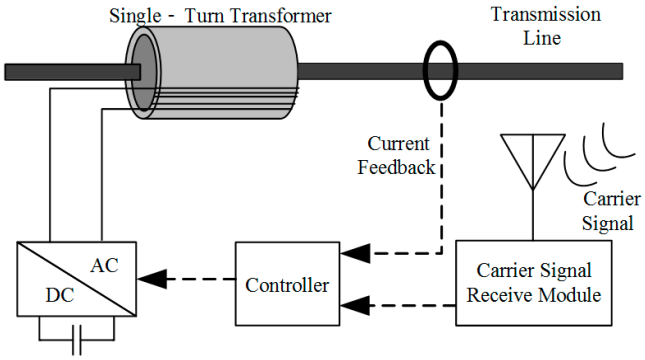

Figure 4. The structure of the DPFC series unit.

The series unit of the DPFC consists of a single-turn transformer (STT), a single-phase inverter, an associated controller, and a built-in communication model. The SST uses the transmission line as the secondary winding, inserting compensated voltage into the power line. Each unit of DPFC is controlled by power line carrier communication.

The DPFC series unit has the task of maintaining the DC capacitor voltage and responding to the reference signal effectively. The control scheme for the DPFC series unit including the single-phase locked loop (SPLL), DC capacitor voltage control and power flow control loop is depicted in Figure 5.

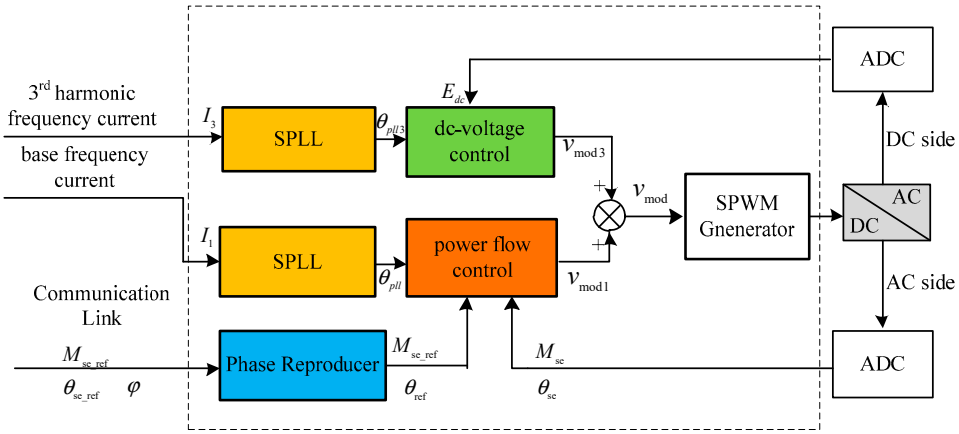

Figure 5. The working principle of the DPFC series unit controller. Single-phase locked loop (SPLL): single-phase locked loop. ADC: analog-to-digital converter. SPWM: sinusoidal pulse-width modulation (PWM).

The reference value of the compensated voltage $M_{\text{se\_ref}}$ and $\theta_{\text{se\_ref}}$ are transferred to the DPFC series unit via power line carrier (PLC) communication link. In a phase reproducer, the real-time phase of the reference voltage θ_{ref} will be generated, leveraging the advantage that the real-time phase of the transmission line base-frequency current can be captured by series units. The actual value of the compensated voltages M_{se} and θ_{se} are acquired and converted to a digital signal by the analog-to-digital converter (ADC) unit. By comparing the real-time reference values $M_{\text{se\_ref}}$ and θ_{ref} with actual values M_{se} and θ_{se}, the proportional-integral (PI) controller within the power flow control loop will generate a compensated phase and a magnitude correction factor to modify the modulation signal v_{mod1} of the base-frequency compensated voltage.

Based on the comparison of the actual value with the reference value of the DC capacitor voltage in the DPFC series unit, the DC-voltage control loop will generate the modulation signal v_{mod3} to maintain the DC capacitor voltage. Consequently, the output of the AC/DC converter equals the mutual control effects of v_{mod1} and v_{mod3}.

3.2.1. The Single-Phase Locked Loop (SPLL)

The adopted phase locked loop method is based on the literature [30]. However, the literature [30] directly integrates the angular frequency to obtain the phase-locked output, which easily leads to the saturation of the integral link. Therefore, the above method is improved in this paper, which can effectively prevent the integral saturation phenomenon.

The single-phase locked loop here is designed to track the frequency and phase of the base-frequency current $\dot{I}_1$ and third harmonic current $\dot{I}_3$. The measured value of the line current phase is obtained by current transformer (CT). As shown in Figure 6, the third harmonic current $\dot{I}_3$ and base-frequency current $\dot{I}_1$ are separated by the filter, and then their phases are locked by the single-phase locked loop (SPLL) in the DPFC series unit. The outputs of SPLL for the base-frequency current and SPLL for third harmonic current are expressed as follows:

$$\theta_{\text{pll}} = \omega t + \theta_{\text{pll0}} \tag{14}$$

$$\theta_{\text{pll3}} = \omega_3 t + \theta_{\text{pll30}} \tag{15}$$

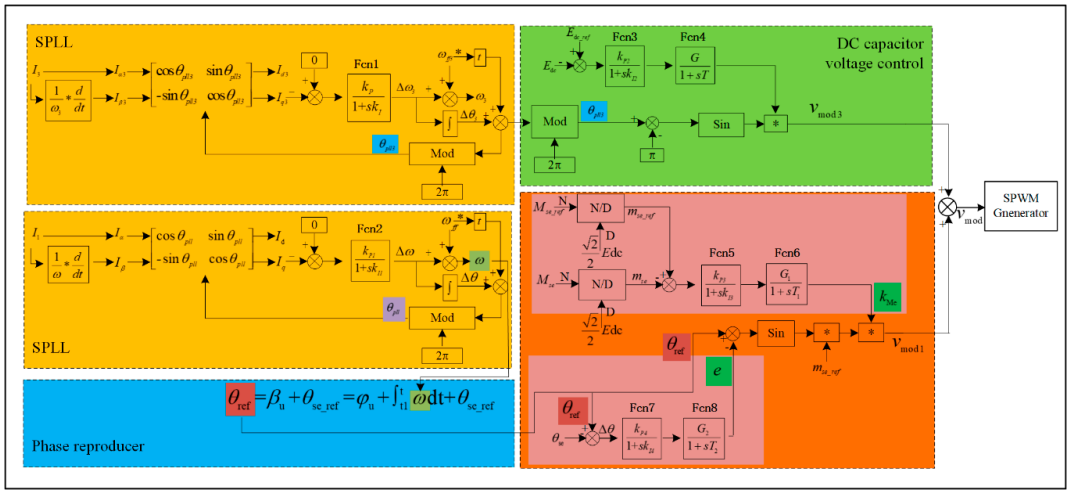

Figure 6. The scheme of the DPFC series unit controller.

3.2.2. The Reproduced Real-Time Phase for Reference Series-Compensated Voltage

The time when the program of the phase locked loop of the line current is started is marked as $t = 0$. Recording a certain zero-crossing point of the fundamental frequency current phasor of the transmission line as t_1, at this time, the phase of the line current is measured as φ_i, and then the phase of $\dot{V}_2$ at time $t = t_1$ is

$$\varphi_u = \varphi_i - \varphi \tag{16}$$

The real-time phase of $\dot{V}_2$ can be attained by

$$\beta_u = \varphi_u + \int_{t_1}^{t} \omega dt \tag{17}$$

Then, the real-time phase of the reference series-compensated voltage $\dot{V}_{\text{se\_ref}}$ can be denoted as

$$\theta_{\text{ref}} = \beta_u + \theta_{\text{se\_ref}} = \varphi_u + \int_{t_1}^{t} \omega \text{dt} + \theta_{\text{se\_ref}} \tag{18}$$

Considering that DPFC series units have the advantage of capturing the real-time phase of the transmission line current, the waveform of the real-time phase of the terminal voltage can be reproduced during a control period, which is very practical for engineering applications.

3.2.3. The DC Capacitor Voltage Control

The DC capacitor voltage control loop is shown in Figure 6. By comparing the actual DC capacitor voltage E_{dc} with the reference DC capacitor voltage $E_{\text{dcsh\_ref}}$, the PI controller will generate the magnitude value of the modulation signal v_{mod3}. To simulate the dynamic characteristics of the converter, a first-order inertial loop is introduced for DC capacitor voltage control. To avoid causing extra voltage changes or power loss, the series unit is required to exchange only the active power of the third harmonic with the transmission line. Hence, the modulation signal v_{mod3} should be the same or inverse to the phase of the third harmonic current of the transmission line.

Thus, the DC-voltage control loop generates the modulation signal v_{mod3} for the third harmonic frequency voltage. The third harmonic active power generated by the parallel unit can change according to the demand for active power of the DC side to maintain the voltage of the DC capacitor in series units.

3.2.4. The Power Flow Control

SPWM (sinusoidal PWM) control is adopted by the series unit. The relationship between the RMS value (root-mean-square) of the inverter output voltage and the DC capacitor voltage is

$$V_{\mathrm{se}} = \frac{\sqrt{2}}{2} k_{\mathrm{se}} m_{\mathrm{se}} E_{\mathrm{dc}} \tag{19}$$

where k_{se} represents the ratio of STT, m_{se} is the fundamental frequency voltage modulation ratio, and E_{dc} is the DC capacitor voltage.

In fact, the phase of the control reference voltage signal of the series unit port will be shifted after passing through the inductor-capacitor (LC) filter. In addition, due to the active power loss, the amplitude of the series fundamental frequency voltage actually injected into the transmission line is smaller than the reference value. This will lead to deviations in the flow control. Therefore, it is necessary to correct the fundamental frequency compensation voltage modulation signal by taking the measurement of the mean value correction and the phase compensation.

The target and actual value of the compensated voltage are sent to the comparison module after being conversed and processed in the ADC unit. Then, the PI controller generates the compensated phase and magnitude correction factor to modify the modulation signal v_{mod1}. The modulating signal for compensated base-frequency voltage is modified as follows:

$$v_{\mathrm{mod1}} = k_{Me} m_{\mathrm{se\_ref}} \sin(\theta_{\mathrm{ref}} - e) \tag{20}$$

where k_{Me} is the magnitude modified factor and e represents the correction for the phase. $m_{\mathrm{se\_ref}}$ denotes the modulation ratio of the fundamental frequency voltage.

According to the above analysis, integrating the four control modules together, the detailed scheme for the DPFC series unit can be depicted in Figure 6, where ω_{ff} represents the rated angular frequency for fundamental-frequency components, and ω_{ff3} represents the rated angular frequency for third harmonic components. Fcn1, Fcn2, Fcn3, Fcn5and Fcn7 are PI controllers. Fcn4, Fcn6 and Fcn8 are first-order inertia blocks. G, G_1 and G_2 represent the gain of the first-order inertia blocks.

4. The Simulation and Analysis of the DPFC Coordination Control System

4.1. Simulation of the DPFC Control System

The model of the transmission system including DPFCs is shown in Figure 7. It is built by the software tool PSCAD/EMTDC 4.2.1. The parallel unit is equivalent to the third harmonic current source and the series units of DPFC are built as detailed models.

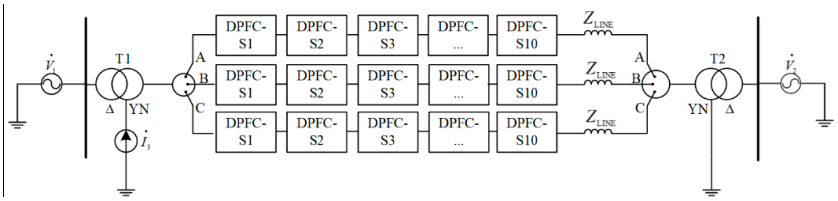

Figure 7. The simulation model of the DPFC.

4.1.1. Test Case 1

The device parameters of the DPFC are listed in Table 1.

Table 1. DPFC device parameters.

Items		Parameter
System fundamental frequency		50 Hz
Magnitude of third harmonic current $\dot{I}_3$		6 A
Number of series units		10
Magnitude of $\dot{V}_1$ and $\dot{V}_2$		380 V
Phase angle of voltage at sending-end δ		8.92°
Phase angle of voltage at receiving-end		0°
Transformer T1		380 V/380 V, 1 kVA, 0.1 p.u, Δ-YN
Transformer T2		380 V/380 V, 1 kVA, 0.1 p.u, YN-Δ
Single-turn transformer of series unit		20 V/100 V, 0.5 kVA, 0.1 p.u
Reference value of DC capacitor voltage		20 V
Value of DC capacitor of VSC in series unit		2200 μF
LC filter of VSC in series unit		1.33 mH, 100 μF
Switch frequency of Insulated-gate bipolar transistor (IGBT)		2100 Hz
Z_{line}		R_{line} = 0.279 Ω, L_{line} = 0.0127 H
Initial phase angle φ		5.03°
Starting time for the breaker of series unit		0.5 s
Starting time for the power flow control		2.5 s
Targeted power flow	t = 2.5–5.0 s	P_{set1} = 800 W, Q_{set1} = −100 Var
	t = 5.0–10.0 s	P_{set2} = 1000 W, Q_{set2} = −100 Var

The corresponding parameters for the control loops of DPFC series unit are shown in Table 2.

Table 2. Tuning parameters for the control loops.

Fcn1	Fcn2	Fcn3	Fcn4
k_p = 5 k_I = 5 × 10^−5 s	k_{p1} = 5 k_{I1} = 5 × 10^−5 s	k_{p2} = 10 k_{I2} = 0.2 s	G = 0.1 T = 0.02 s
Fcn5	**Fcn6**	**Fcn7**	**Fcn8**
k_{p3} = 10 k_{I3} = 0.005 s	G_1 = 0.2 T_1 = 0.02 s	k_{p4} = 0.95 k_{I4} = 0.5 s	G_2 = 1 T_2 = 0.02 s

The simulation results of the DPFC coordination control system are depicted in Figure 8.

Figure 8a shows the power flow at the receiving-end of the transmission system by employing the proposed control method. At time t = 3.5 s, P_{r} and Q_{r} are stable at 799.83 W and −100.66 Var, respectively. At time t = 6.0 s, P_{r} and Q_{r} are at a new stable state at 999.978 W and −98.25 Var, respectively. Considering the setting value given in Table 2, the power flow control is effective.

Figure 8a also shows the power flow at the receiving end of the transmission system by using the state of art (SOA). At time t = 3.5 s, SOAP_{r} and SOAQ_{r} are stable at 800.14 W and −98.11 Var, respectively. At time t = 6.0 s, SOAP_{r} and SOAQ_{r} are at a new stable state 1000.42 W and −99.998 Var, respectively. Considering the setting value given in Table 2, the power flow control is effective.

Comparing the proposed method with the SOA according to the simulation results of the independent active power flow control, it is indicated that both are effective and the control effects are similar.

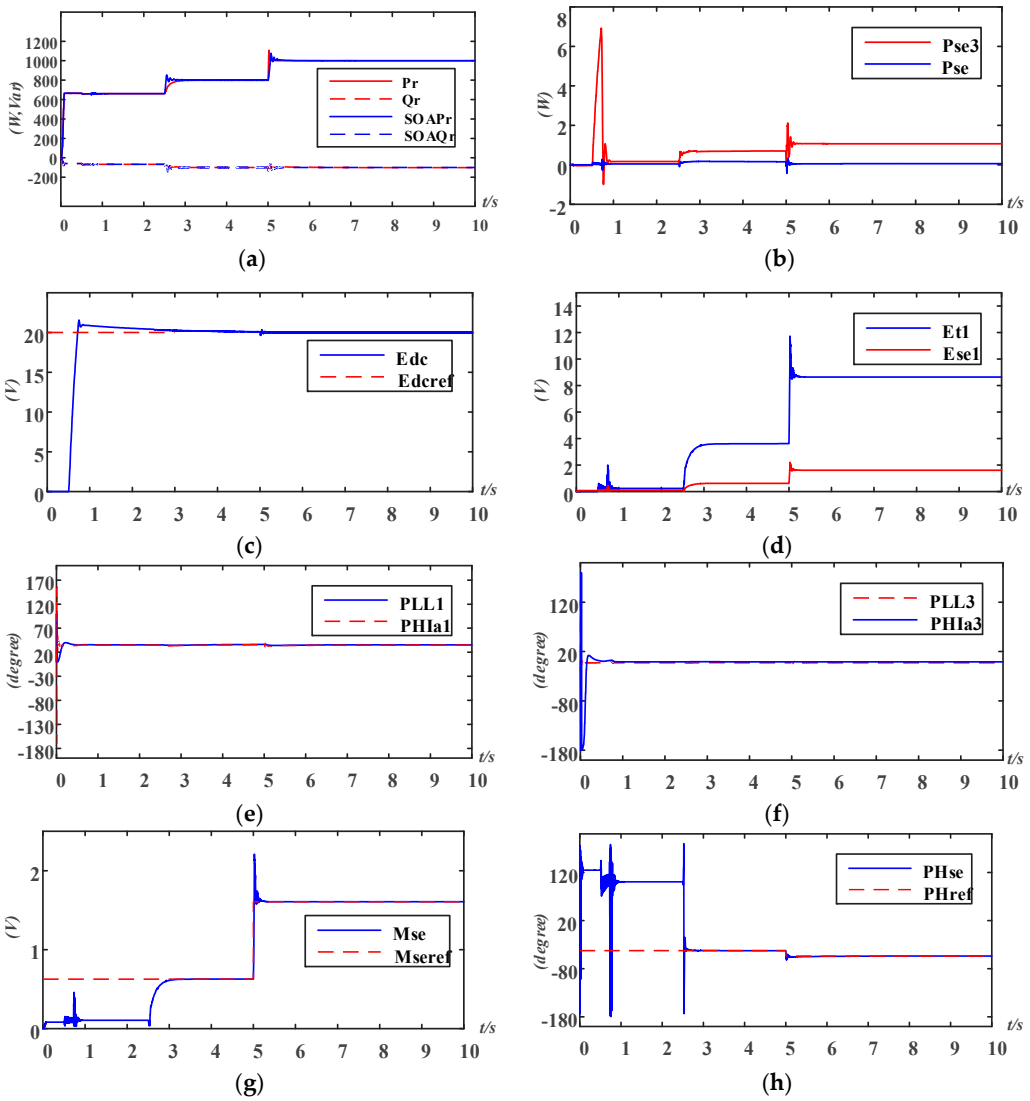

Figure 8. The simulation results of the DPFC control system. (**a**) Three-phase power flow at the receiving-end; (**b**) exchange of active power flow in the series unit; (**c**) DC capacitor voltage of each series unit; (**d**) magnitude of voltage of the single-turn transformer (STT); (**e**) SPLL result of the base-frequency line current by fast Fourier transform (FFT) component extraction; (**f**) SPLL result of the third harmonic current by FFT component extraction; (**g**) the magnitude of compensated voltage for each series unit; (**h**) the phase angle of compensated voltage for each series unit.

Figure 8b displays the exchange of the third harmonic active power flow P_{se3} and base-frequency active power flow P_{se1} for each series unit. It is worth noting that $P_{se3} \neq P_{se1}$ for the reason that active power loss of VSC at the third harmonic and base frequency are not equal. Combining this power exchange process with the DC capacitor voltage in Figure 8c, it is verified that the third harmonic frequency active power is used for building and maintaining the voltage of the DC capacitor.

Figure 8c indicates the DC capacitor voltage E_{dc} of VSC. E_{dc} grows dramatically and then remains stable at the reference value 20 V, which verifies the validity of DC-voltage control.

Figure 8d represents the magnitudes of the base-frequency voltage at the primary side and secondary side of STT. E_{t1} is the primary-side voltage while E_{se1} is the secondary-side voltage. At t = 3.5 s, E_{t1} = 3.606 V and E_{se1} = 0.626 V. At t = 6.0 s, E_{t1} = 8.643 V and E_{se1} = 1.607 V. The ratio of STT is 20:100 (secondary side to primary side); however, the ratio between the actual voltage E_{se1} and E_{t1} is not strictly equal to 1:5. Therefore, a modification for the modulation signal v_{mod1} is needed.

Figure 8e,f display the SPLL results of the line current by FFT (fast Fourier transform) component extraction. Both the phases of base-frequency and the third harmonic line current can be locked quickly and accurately.

Figure 8g,h indicate the magnitude and phase angle of the base-frequency series-compensated voltage for each DPFC series unit. At t = 3.5 s, the actual values are M_{se} = 0.626 V and θ_{se} = −42.365° while the setting values are M_{se_ref} = 0.627 V and θ_{se_ref} = −42.502°. At t = 6.5 s, the actual values are M_{se} = 1.607 V and θ_{se} = −54.068° while the setting values are M_{se_ref} = 1.607 V and θ_{se_ref} = −53.665°. Thus, the control of the base-frequency series-compensated voltage is effective.

4.1.2. Test Case 2

The target power flows are changed to P_{set3} = 800 W and Q_{set3} = −100 Var from t = 2.5 to 7.0 s while these are P_{set4} = 800 W and Q_{set4} = −50 Var from t = 7.0 to 10.0 s. The simulation results are shown in Figure 9.

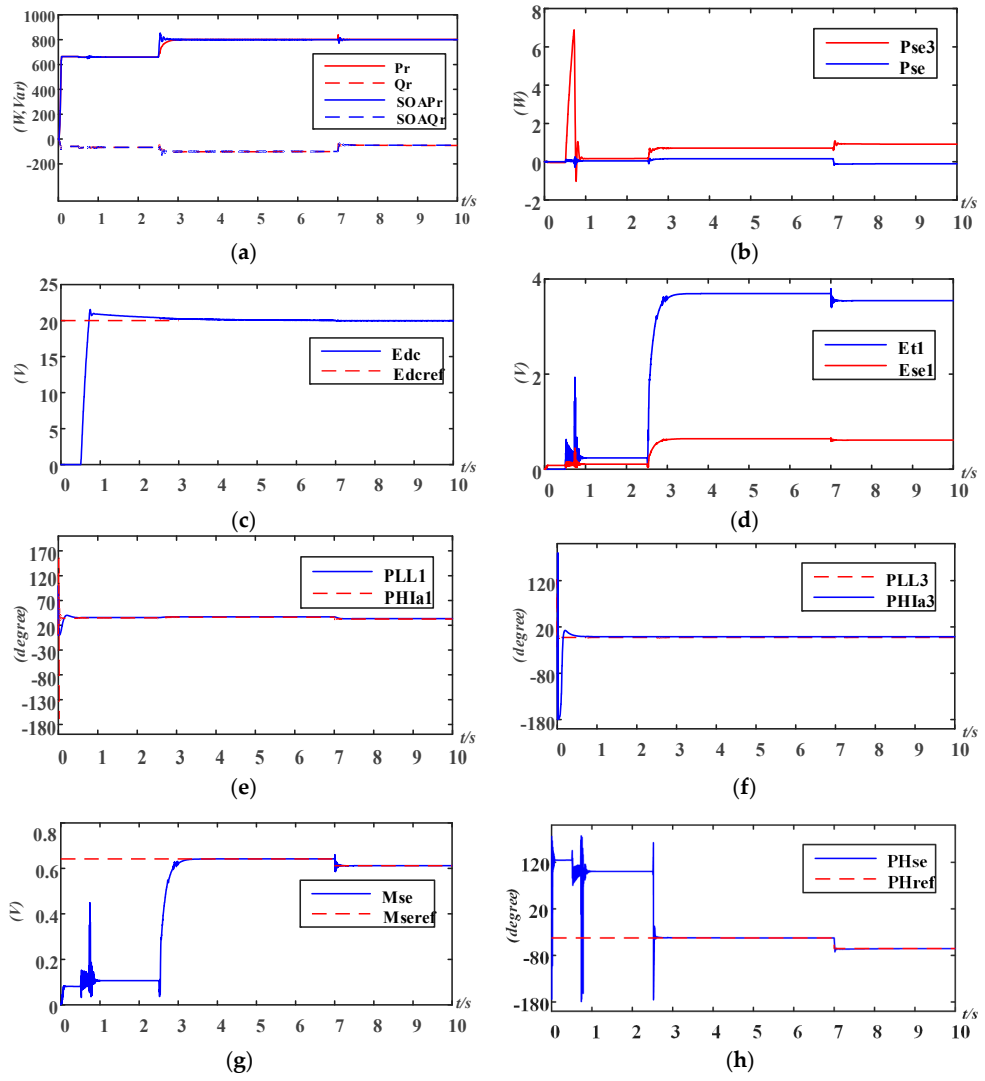

Figure 9. The simulation results of the DPFC control system. (**a**) Three-phase power flow at the receiving-end; (**b**) exchange of active power flow in the series unit; (**c**) DC capacitor voltage of each series unit; (**d**) magnitude of voltage of STT; (**e**) SPLL result of base-frequency line current; (**f**) SPLL result of third harmonic current; (**g**) the magnitude of compensated voltage; (**h**) the phase angle of compensated voltage.

Figure 9a shows the power flow at the receiving end of the transmission system by employing the proposed control method. At time t = 3.5 s, P_r and Q_r are stable at 802.59 W and −101.81 Var, respectively. At time t = 8.0 s, P_r and Q_r are at a new stable state of 802.86 W and −50.43 Var, respectively. Considering the given setting value, the power flow control is effective.

Figure 9a also indicates the power flow at the receiving-end of the transmission system by using the state of art (SOA). At time t = 3.5 s, SOAP_r and SOAQ_r are stable at 800.14 W and −98.11 Var, respectively. At time t = 8.0 s, SOAP_r and SOAQ_r are at a new stable state of 800.01 W and −49.997 Var, respectively. Considering the given setting value, the power flow control is effective.

Therefore, it is verified that both the proposed method and SOA method are effective for the independent reactive power flow control. Additionally, the effects of these two methods are similar.

Figure 9b displays the exchange of the third harmonic active power flow P_{se3} with base-frequency active power flow P_{se1} for each series unit. It is worth to noting that the power exchange process is consistent with the tendency of the DC capacitor voltage in Figure 9c; hence, it is indicated that the third harmonic frequency active power is used for building and maintaining the voltage of the DC capacitor.

Figure 9c indicates the DC capacitor voltage E_{dc} of VSC. E_{dc} can still stay stable at 20 V when the target power flow changes, which verifies the validity of the DC capacitor voltage control.

Figure 9d represents the magnitudes of the base-frequency voltage at the primary side and secondary side of STT. E_{t1} is the primary-side voltage while E_{se1} is the secondary-side voltage. At t = 3.5 s, E_{t1} = 3.691 V and E_{se1} = 0.641 V. At t = 8.0 s, E_{t1} = 3.545 V and E_{se1} = 0.612 V. The ratio of STT is 20:100 (secondary side: primary side); however, the ratio between the actual voltage E_{se1} and E_{t1} is not strictly equal to 1:5. Therefore, a correction for the modulation signal v_{mod1} is necessary.

Figure 9e,f display the SPLL results of the line current extracted by FFT. It is verified that both the phases of the base-frequency and third harmonic line current can be locked quickly with high precision.

Figure 9g,h indicate the magnitude and phase angle of the base-frequency series-compensated voltage generated by each DPFC series unit. At t = 3.5 s, the actual values are M_{se} = 0.641 V and θ_{se} = −42.271° while the setting values are M_{se_ref} = 0.642 V and θ_{se_ref} = −42.401°. At t = 8.0 s, the actual values are M_{se} = 0.612 V and θ_{se} = −65.776° while the setting values are M_{se_ref} = 0.612 V and θ_{se_ref} = −65.281°. The control of the base-frequency series-compensated voltage is verified to be effective.

4.2. Comparison of the Proposed Method with the State-of-the-Art

Comparing the proposed method with the SOA in [28] based on the simulation results of power flow control in Figures 8a and 9a in Section 4.1, it is indicated that the control effect of the proposed and existing method are similar in independent active and reactive power flow control.

It should be mentioned that the starting time of the simulation in PSCAD/EMTDC for the phasors of terminal voltage and line current are the same; thus, both the initial phases of the terminal voltage and line current are measurable. In the actual operation system, however, there is no way to acquire the initial phase angle of the terminal voltage except for the phase difference between two phasors.

The SOA takes the real-time phase of the terminal voltage as the input angle of the inverse Park's transformation and generates corresponding reference values of the series-compensated voltage. Thus, the real-time phase of the terminal voltage must be provided for power flow control in multiple series units by high-speed communication link, which is not practical for the actual transmission system.

Using the proposed real-time phase reproducer of the terminal voltage, only the initial difference between the terminal voltage and line current is needed by leveraging the real-time phase of line current locally at the lower control scheme. Hence, the proposed method is much more suitable for practical engineering applications due to the limitations of communication speed, which is not considered in the existing method.

5. Conclusions

A coordination control method for DPFC series units has been proposed and verified in this paper. The waveform of the real-time phase of the terminal voltage can be reproduced correctly during a control period within the DPFC series units, and so a high-speed communication link is not required for the real-time power flow control. Hence, it is much more practical for engineering applications. To control the series-compensated voltage exactly, measures to modify the magnitude and angle of the modulation signal through PI control loops have been taken. The control parameters of each series unit are the same to avoid the interaction's inverse impact on multiple series unit. Simulation results from PSCAD/EMTDC have indicated that the proposed power flow control method is effective. By comparing the proposed method with the SOA in simulation and considering the speed limitations of the communication link in an actual transmission system, it can be concluded that the proposed method is more suitable for practical engineering applications with an equivalent control effect to the SOA. In future research work, experimental testing will be carried out to verify the proposed method further.

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