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Control of the Bidirectional Buck-Boost Converter Operating in Boundary Conduction Mode to Provide Hold-Up Time Extension

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Abstract: A hold-up time extension circuit (HTEC) is used to charge and discharge an auxiliary capacitor. This capacitor stores the energy required to extend the operation time of critical loads experiencing short duration failures (SDF) at the DC bus to which they are connected. This paper presents complete modeling and a control-wise approach to a parallel HTEC based on the bidirectional buck-boost converter, which operates in Boundary Conduction Mode (BCM) with a variable switching frequency. The circuit permanently regulates the voltage of the auxiliary capacitor as well as the voltage of the DC bus during SDF, which is uncommon in industrial versions of HTEC. Enforcing the operation in BCM allows a reduction in the size of the inductor in the converter without requiring additional control circuitry. The entire behavior of the proposed HTEC, in all its operation modes, was analyzed theoretically and validated using simulation and experimental results, showing the potential of the circuit to be used in real applications.

Keywords: hold-up time extension; bidirectional buck-boost converter; boundary conduction mode; hysteresis current control

1. Introduction

The occurrence of temporary interruptions and other short duration failures (SDF) in the input source of critical DC loads affects the reliability of many electrical systems considerably. This is the case for regulated DC sources fed by non-regulated buses, which are installed onboard commercial and civil aircraft to feed measurement instruments. Hence, current regulations require that this equipment support the SFD [1,2] to some extent. Since DC power systems are increasingly implemented in terrestrial vehicles and in commercial and residential buildings, solutions that provide robustness to SDF have become relevant [3,4]. Although the majority of DC-sourced devices have included an input capacitance of considerable value, providing a short hold-up time after failure [5], manufacturers now focus on reducing the size and weight of devices, even at expense of hold-up features. Special techniques and methods have been developed to overcome this issue [6]. However, when the continuous operation of a load is critical, the hold-up time has been extended by means of external additional devices—so-called hold-up time extension circuits (HTEC) [7–9].

Most of the existing HTEC use an auxiliary capacitor for energy storage. This element is charged during normal operation of the DC bus and discharged during SFD. Depending on the topology connecting the bus, the HTEC, and the load, solutions can be classified as either series-architecture or parallel-architecture. The limitation of series-architectures is the size of the capacitor due to the

limited voltage level of the DC bus. In addition, there is an obvious loss of efficiency because all the power consumed by the load passes through the HTEC. However, because of the direct connection of the circuit with the input of the critical load, reliability is higher when compared with other architectures [10]. Parallel off-line architectures charge the capacitor using the HTEC, keeping it in standby until an SDF occurs. Then, the load is connected to the capacitor through a switch, which produces an undesired transitory behavior. This is the most common architecture of commercial HTEC [11,12]. The parallel on-line architectures of HTEC have a converter to charge and discharge the auxiliary capacitor to a higher voltage level, allowing more energy to be stored with the same capacitance [13]. Then, the required converter in these architectures must have boost capabilities and bidirectional power flow. Among the existing possibilities, some special topologies, such as the converter presented in Reference [14], may provide a high-gain at the expense of additional complexity. Due to the main property of the non-inverting synchronous buck-boost converter, which ensures the same electrical reference for the source and the load, this can be one of the preferred topologies [15]. However, because of the intended intermittent operation, criteria such as simplicity and a reduced number of components become more relevant, as in Reference [16], where the authors employed a conventional synchronous boost converter. In this case, as in some applications for microgrids, the symmetry of the circuit configuration for the charging and discharging mode of the conventional bidirectional buck-boost converter (BBBC) is a relevant criterion since it leads to simpler control [17].

A first version of the proposed control operating on a BBBC in boundary conduction mode (BCM) was presented in Reference [18]. Only three operational modes, with some transitions defined between them, were identified, namely a charging mode, a standby mode, and a discharging mode. However, the power converter and the auxiliary capacitor were considered as ideal elements, making it difficult to understand the need for the additional operational modes. After a deeper analysis, including experimental testing, an improved version of the control was developed considering the power conduction losses in the inductor and the auto-discharge parasitic resistance of the capacitor. As a result, a new operational mode has been included in the decision-event approach and a linear voltage regulator has been replaced by a hysteresis controller, considerably improving the overall performance of the HTEC. The rest of the paper is organized as follows: Section 2 presents a description of the operational modes of the HTEC; modeling and control of the HTEC are described in detail in Section 3. Section 4 focuses on simulation and experimental results, validating the theoretical analysis. Finally, conclusions and future work are presented in Section 5.

2. General Description of the Control System

Figure 1 shows a block diagram of an Extra Low Voltage DC (ELVDC) bus in which both critical and noncritical loads are connected. HTEC devices are connected in parallel to critical loads and have a dedicated auxiliary capacitor external to the circuit. In this context, when the ELVDC bus operates normally, its voltage is the same voltage as the load. However, when an undesired voltage level is detected, the switch S_1 has the function of differentiating the voltage of the critical load and the voltage of the bus. Then, due to the bidirectional power flow of HTEC devices, the input voltage of each load can be regulated during failure.

Figure 2 shows a detailed block diagram of an HTEC interconnection with the ELVDC bus and one critical load. The HTEC consists of a power stage and a control stage. The power stage consists of a DC-DC converter and the switch S_1, which is bidirectional in terms of current and unidirectional in terms of voltage. The control module is composed of a block of power-flow control, which selects the controller to charge or discharge the capacitor. The control module provides the gate with signals for the power module; it also provides the gate signal for the switch.

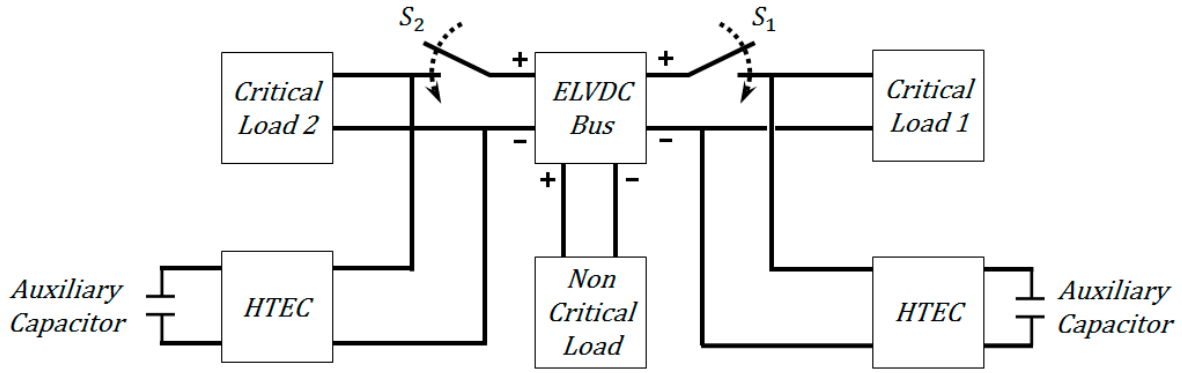

Figure 1. Block diagram representing application context of proposed hold-up time extension circuit (HTEC) in an Extra Low Voltage DC (ELVDC) bus.

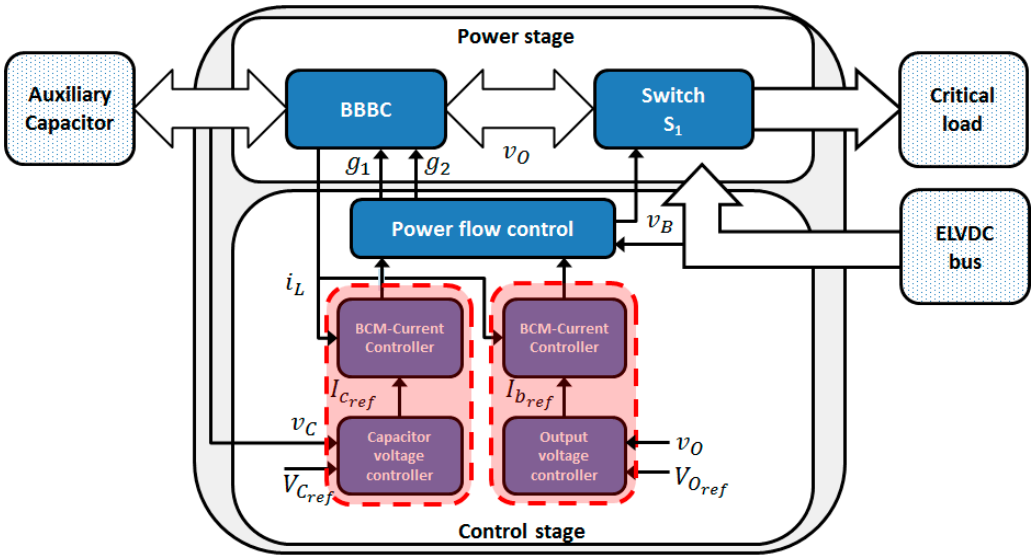

Figure 2. Block diagram representing proposed HTEC, ELVDC bus and critical load.

The circuit model of the BBBC connected to an ELVDC bus is depicted in Figure 3. Notice that the diode of the conventional buck-boost has been replaced by the MOSFET (Metal Oxide Semiconductor Field Effect Transistor), M_2, to allow a bidirectional power-flow capability. The capacitor, C_{aux}, is the storage element of the circuit, which has an auto-discharge resistance (R_{cp}). The capacitance, C_{bus}, represents the bus capacitance, which is the combination of the input capacitance of the critical load and the input-output capacitance of the HTEC. The load connected to the ELVDC bus (critical load for the HTEC) has been represented as R_{bus}. The control circuit of the HTEC generates the signals for the gates of the two MOSFETs denoted as g_1 and g_2. The signals come from measurements of the current of the inductor i_L, the DC bus voltage v_B, the auxiliary capacitor voltage v_c and the load voltage v_o. To distinguish v_B from v_o, it is important to mention that the voltage of the DC bus, regulated by another element, is considered as the source v_B, which is disconnected by means of switch S_1 when an undesirable voltage level is detected. During this event, the load has voltage v_o, a voltage value regulated by the HTEC.

Operation of the proposed HTEC can be summarized using the event-based diagram depicted in Figure 4. At the start-up of the HTEC, it enters in the off-line mode, in which controllers are deactivated. Once the voltage of the bus exceeds $V_{B_{nom}}$, the charge mode is activated. In this mode, the capacitor, C_{aux}, is charged at a constant rate (driven by current I_{ref}) using a hysteresis comparator, which ensures ripples between zero and the positive value of I_{max}, resulting in enforcement of the BCM operation of the BBBC. Once the voltage of the capacitor reaches the maximum programmed

voltage, $V_{c_{max}}$, the current charge controller is deactivated and the system passes to a stand-by mode. In this mode, due to the self-discharge of the capacitor, a hysteresis voltage controller is activated, allowing the recharge of the capacitor when its voltage falls below the minimum programmed voltage, $V_{C_{nom}}$. Then, the steady-state operation of the system consists of large intervals of the stand-by mode and short intervals of the charge mode, preserving the desired energy level in the auxiliary capacitor. Being in either stand-by mode or charge mode, the discharge mode is activated if the voltage of the bus falls below $V_{B_{min}}$. The capacitor, C_{aux}, is discharged simultaneously, regulating the voltage in the load $v_o = V_{O_{ref}}$. In this mode, a proportional-integral (PI) regulator enforces the amplitude of the discharge current; that is, the regulator dictates the upper bound of the discharge hysteresis band (a negative value of I_{max}, enforcing also BCM). If the auxiliary capacitor discharges below the permissible limit, $V_{C_{min}}$, the system returns to the off-line mode.

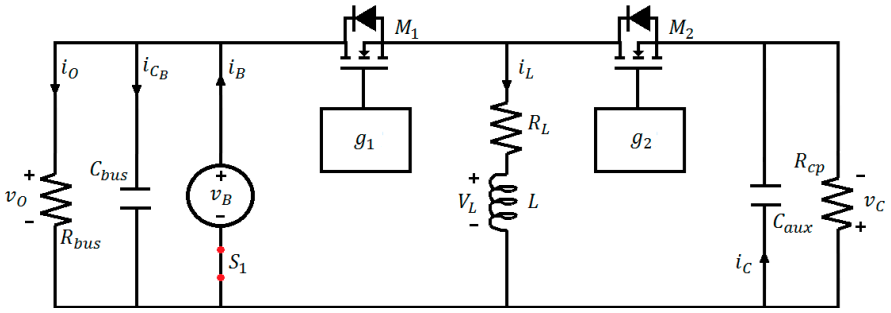

Figure 3. Schematic circuit model of the bidirectional buck-boost converter.

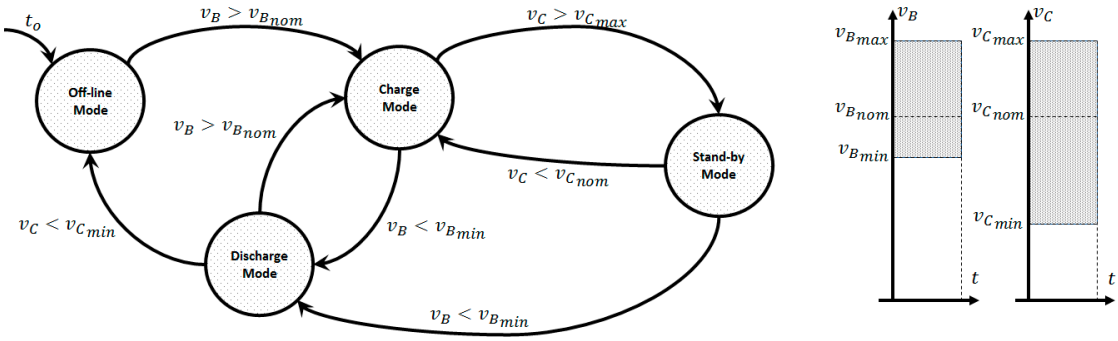

Figure 4. Event based diagram defining control modes and transition events.

3. Modeling and Control of the BBBC Converter

3.1. Capacitor Charging Mode

The two circuit structures of the BBC converter, operating in Continuous Conduction Mode CCM (or BCM), associated with the charging mode, are depicted in Figure 5. In this case, the converter can charge the capacitor, C_{aux}, by taking energy from the DC bus. This charging process is enforced at a constant-current rate by changing the state of the control switch, M_1, maintaining switch M_2 off. The variable u_1 is defined in such a way that $u_1 = 1$ when M_1 is on, and $u_1 = 0$ when M_1 is off. The intrinsic diode of M_2 is on when M_1 is off.

The nonlinear dynamic behavior of the BBBC converter in this mode can be represented as the bilinear equation system (1).

$$\begin{aligned} L\frac{di_L}{dt} &= v_B u_1 - v_C(1-u_1) - i_L R_L \\ C_{aux}\frac{dv_C}{dt} &= i_L(1-u_1) - \frac{v_C}{R_{cp}} \end{aligned} \tag{1}$$

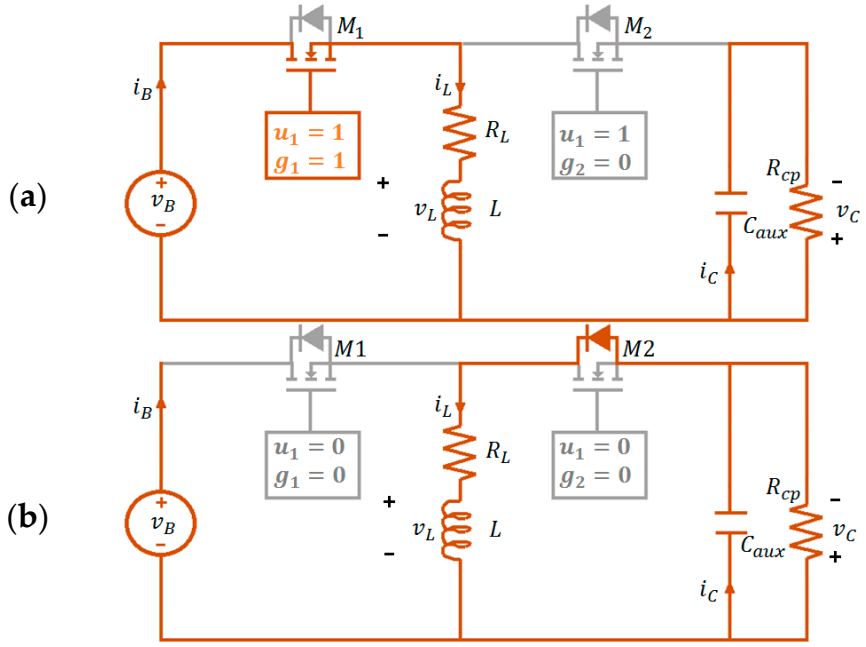

Figure 5. Circuit structures of the Bidirectional Buck-Boost Converter (BBBC) during the charging mode operation. (**a**) Control switch on; (**b**) control switch off.

Then, operation in BCM can be enforced on the inductor current, setting a hysteresis band with limits at $I_{max} > 0$ and zero, as defined in the following switching law:

$$u_1 = \begin{cases} 1 & i_L \leq \delta \\ 0 & i_L \geq I_{max} \end{cases} \tag{2}$$

where δ is a small positive value. Then, the capacitor charges depending on the average value of the current; this means that the charging process is related to the average value of the control signal, u_1. From conventional sliding-mode analysis [19], the value u_{1avg} denotes the equivalent control signal when the switches at the converter change states are at an infinite frequency, in other words, u_{1avg} represents the average value of the duty cycle (i.e., the control signal as a continuous variable). In the case of the converter operating in BCM [20], due to the triangular shape of the current, it is possible to ensure that the cycle-by-cycle average of the current is half the maximum limit of the current. Then, by defining $I_{ref} = \frac{I_{max}}{2}$, $S(x) = i_L - I_{ref}$, $\dot{S}(x) = \frac{di_L}{dt}$ and $S(x) = \dot{S}(x) = 0$, from Equation (1), equivalent control Equation (3) can be obtained.

$$u_{1avg} = \frac{2v_C + I_{max}R_L}{2(v_B + v_C)} \qquad 0 \leq u_{1avg} < 1. \tag{3}$$

Using Equations (1) and (3), and considering that $R_{cp} \gg v_C$, the ideal dynamic behavior of the average voltage at the capacitor is:

$$\frac{dv_C}{dt} = \frac{I_{max}}{4C_{aux}}\left(\frac{2v_B - I_{max}R_L}{v_B + v_C}\right). \tag{4}$$

By solving Equation (4), considering $v_C(0) = 0$, the instantaneous output voltage is:

$$v_C(t) = -v_B + \sqrt{v_B^2 + \frac{I_{max}(2v_B - I_{max}R_L)}{2C_{aux}}t}. \tag{5}$$

The charge time can be computed by substituting the final value of v_C as $V_{C_{max}}$, obtaining:

$$t_a = \frac{2C_{aux}}{I_{max}}\left(\frac{{V_{C_{max}}}^2 + 2V_B V_{C_{max}}}{2v_B - I_{max}R_L}\right). \tag{6}$$

3.2. Stand-By Mode

In this mode, both switches M_1 and M_2 are off. The circuit defining $v_C(t)$ becomes solely the parallel between C_{aux} and R_{cp}. Therefore, the dynamic behavior is defined by:

$$\frac{dv_C}{dt} + \frac{v_C}{R_{cp}C_{aux}} = 0. \tag{7}$$

By solving Equation (7), considering $v_C(t_a) = V_{C_{max}}$, the output voltage is obtained as:

$$v_C(t) = V_{C_{max}} e^{-\left(\frac{t}{R_{cp}C_{aux}}\right)}. \tag{8}$$

The stand-by interval can be computed by substituting the final value of v_C as $V_{C_{nom}}$, obtaining:

$$t_b = -R_{cp}C_{aux}\ln\left(\frac{V_{C_{nom}}}{V_{C_{max}}}\right). \tag{9}$$

3.3. Recharging Mode of the Capacitor

During this interval, the circuit operates in charging mode until the capacitor voltage reaches $V_{C_{max}}$ again. The behavior of v_C can be modelled by analyzing the cycle-by-cycle waveform of the current at capacitor (see Figure 6). It is possible to observe that the contribution of each current pulse on the capacitor's charge is given by:

$$\Delta_{Q_c} = \frac{2L{I_{max}}^2}{2v_C + I_{max}R_L}. \tag{10}$$

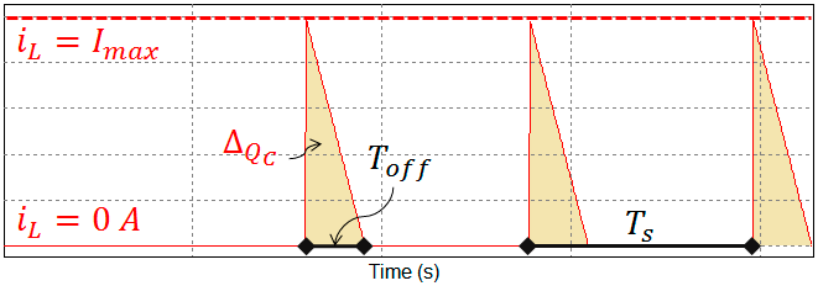

Figure 6. Current on the capacitor C_{max} during recharge mode.

By taking into account Equation (10), it can be deduced that the drop voltage, $\Delta_{V_c} = V_{C_{max}} - V_{C_{nom}}$, is recovered with N current pulses during a time interval t_c defined by:

$$t_c \approx \frac{2C_{aux}\Delta_{V_c}(V_B + V_{C_{max}} + V_{C_{nom}} + I_{max}R_L)}{V_B I_{max}}. \tag{11}$$

3.4. Discharging Mode of the Capacitor

Figure 7 shows the on and off structures of the BBBC circuit in the discharging mode. In this mode, the energy transfer from the capacitor, C_{aux}, to the critical load (connected in parallel to capacitor C_B) is accomplished using the converter. For this analysis, R_{cp} is not included because its effect on the

dynamic behavior is negligible compared with the load R, which is now connected to the input side of the converter.

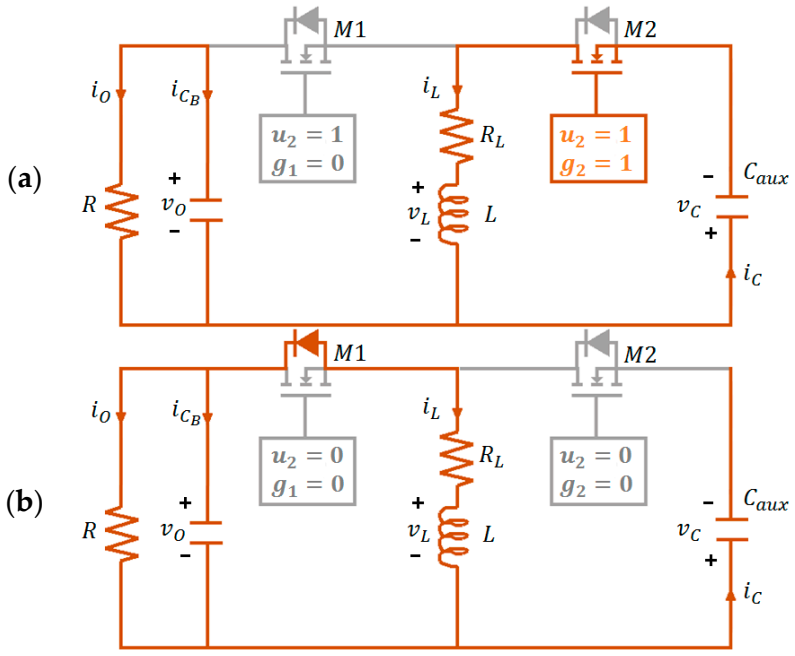

Figure 7. Circuit structures of the BBBC in the discharging mode. (**a**) Control switch on; (**b**) control switch off.

By deriving and combining equations for each circuit structure, the following bilinear system of equations is obtained:

$$\begin{aligned} L\frac{di_L}{dt} &= -v_C u_2 + v_O(1-u_2) - i_L R_L \\ C_{aux}\frac{dv_C}{dt} &= i_L u_2 \\ C_B\frac{dv_O}{dt} &= -\frac{v_O}{R} - i_L(1-u_2). \end{aligned} \tag{12}$$

Similar to the derivation of Equation (3), we have $S(x) = i_L - i_{ref}$, $\dot{S}(x) = \frac{di_L}{dt} - \frac{di_{ref}}{dt}$ and $S(x) = \dot{S}(x) = 0$, then, from Equation (12), the following average control is obtained:

$$u_{2avg} = \frac{v_O - L\frac{di_{ref}}{dt} - i_{ref}R_L}{v_O + v_C} \qquad 0 \le u_{2avg} < 1, \tag{13}$$

obtaining switching law Equation (14).

$$u_2 = \begin{cases} 1 & i_L \ge -\gamma \\ 0 & i_L \le i_{\max dch} \end{cases} \tag{14}$$

where γ is a small positive value. From Equations (12) and (13), the ideal dynamic behavior of the average voltage at the capacitors is:

$$\begin{aligned} C_{aux}\frac{dv_c}{dt} &= i_{ref}\left(\frac{v_O - L\frac{di_{ref}}{dt} - i_{ref}R_L}{v_O + v_C}\right) \\ C_B\frac{dv_O}{dt} &= -\frac{v_O}{R} - i_{ref}\left(\frac{v_C + L\frac{di_{ref}}{dt} - i_{ref}R_L}{v_C + v_O}\right). \end{aligned} \tag{15}$$

By combining the two expressions in Equation (15), the following linear Equation (16) is derived.

$$C_B \frac{dv_O}{dt} = -\frac{v_O}{R} - i_{ref} + C_{aux} \frac{dv_c}{dt}. \tag{16}$$

In the discharge mode, an outer voltage controller will enforce $v_O = V_O$ by means of the reference current, i_{ref}. The cycle-by-cycle average current can be derived by imposing zero dynamics in Equation (12) obtaining $i_{ref} = -\frac{V_O}{R} - \frac{{V_O}^2}{Rv_c}$. Then, substituting this expression in Equation (16), the dynamic behavior of v_c is:

$$\frac{dv_C}{dt} + \frac{{V_O}^2}{RC_{aux}v_C} = 0. \tag{17}$$

By solving Equation (17), considering $v_C(0) \approx V_{C_{max}}$, the instantaneous output voltage is:

$$v_C(t) = \sqrt{{V_{C_{max}}}^2 - \frac{2{V_O}^2}{RC_{aux}}t}. \tag{18}$$

The discharge interval can be computed by substituting the final value of v_C as $V_{C_{min}}$, obtaining:

$$t_d = \frac{RC_{aux}}{2}\left(\frac{{V_{C_{max}}}^2 - {V_{C_{min}}}^2}{{V_O}^2}\right). \tag{19}$$

Regulation of the voltage at the bus can be accomplished by using a simple proportional-integral (PI) controller. The transfer function of the current-controlled converter can be obtained from the Laplace transform of Equation (16). The reference current, i_{ref}, has been replaced by $i_{max}/2$ since this value defines the average value of the current on the inductor i_L.

$$V_O(s) = I_{max}(s)\underbrace{\frac{-\frac{1}{2C_b}}{s + \frac{1}{RC_b}}}_{G_{iv}(s)} + V_C(s)\underbrace{\frac{\frac{C}{C_b}}{s + \frac{1}{RC_b}}}_{G_{vv}(s)}. \tag{20}$$

In Equation (20) the voltage $V_C(s)$ must be considered as a disturbance; then, assuming its value as zero, the DC bus voltage is obtained for a maximum-current transfer function. Then, the output voltage can be indirectly regulated by configuring a nested loop architecture in which the outer controller regulating the output voltage gives the reference of the inner current loop [21,22]. By defining the PI controller transfer function in the classical way, we have:

$$C(s) = \frac{K_p s + K_i}{s}. \tag{21}$$

The parameters of Equation (21) can be computed by applying any classical design method, such as frequency-response, root-locus or advanced-control methods, especially methods that allow a robust response to the changes in operation point (i.e., the use of the instantaneous voltage from the auxiliary capacitor) with uncertainty about the parameters (e.g., power consumption of the critical load) [22]. Regardless of the method, the closed-loop transfer function is:

$$\frac{V_O(s)}{V_{ref}(s)} = \frac{\frac{K_p s + K_i}{2C_b}}{s^2 + \frac{1}{C_b}\left(\frac{1}{2R} + K_p\right)s + \frac{K_i}{2C_b}}. \tag{22}$$

3.5. Complete Control Diagram

To clarify the implementation of the proposed control module, the block diagram in Figure 8 is presented. In this figure, we have separated the control of the charge from the discharge control since the two control sub-modules have slight differences. Both the charge and discharge control modules have a hysteresis comparator to force the inductor current to operate in BCM, which corresponds to the

switching laws in Equations (2) and (14), respectively. The control signals u_1 and u_2, which are given by the inner current controllers, are also conditioned to the existence of enabling signals, provided by the mode-selection logic described in Figure 3. In the case of the charge control, the nonlinear outer loop of voltage regulation constitutes a nested loop or cascade control architecture (together with the hysteresis comparator). This controller corresponds to definitions given in Sections 3.2 and 3.3. The output of the outer loop defines whether the maximum value of the current is the I_{max} value configured by the user or zero, deactivating the inner loop. In the case of the discharge control, also a nested loop is used, in which the PI controller defined in Equation (21) gives the reference for the current controller in order to regulate the input voltage of the critical load. Details of the circuit implementation are given in the results section.

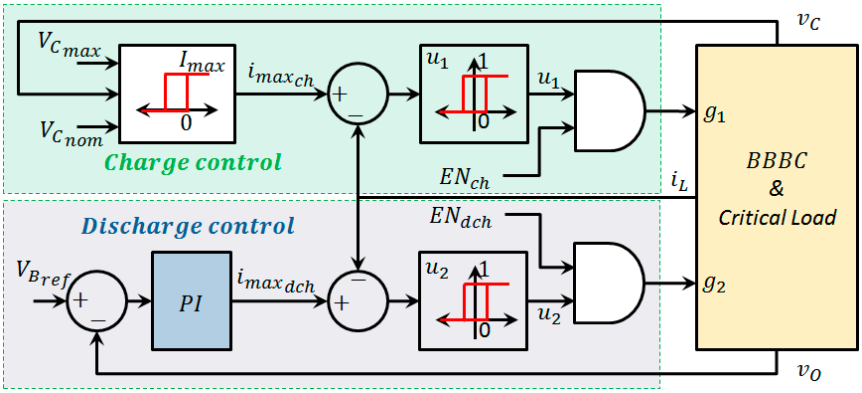

Figure 8. Block diagram of the proposed control for the HTEC based on the BBBC.

3.6. Converter Design Parameters

Operation of the converter in BCM implies a variable switching frequency. Then, the inductor of the converter must be designed considering the extreme cases. In order to determine the range of switching frequencies during the charge mode, the on and off time intervals are determined as:

$$\begin{aligned} T_{on} &= L\left|\tfrac{I_{max}}{V_B}\right| \qquad V_B > 0 \\ T_{off} &= L\left|\tfrac{I_{max}}{V_C}\right| \qquad V_C > 0. \end{aligned} \tag{23}$$

The switching period can be obtained as $T_s = T_{on} + T_{off}$, and hence, the switching frequency can be derived. The singularity of $V_C = 0$ appears only at the start of the charge interval. In that case, T_{off} is equal to zero because there is no change for the inductor current.

$$f_s = \frac{1}{T_s} = \frac{v_C v_B}{L I_{max}(v_B + v_O)}. \tag{24}$$

Notice that the per-cycle value of the frequency depends on the capacitor's voltage, which varies during the charging process. Therefore, the range of the switching frequency is defined by the value of the inductance. The auxiliary capacitor is designed depending on the extension required in the hold-up time. Capacitance is determined to ensure a defined amount of stored energy to be delivered in order to support the momentary power failures. Considering a load connected to the DC bus with a power consumption of P and a desired autonomy time of t_d, the value of the required capacitance can be computed as:

$$C_{aux} = \frac{2\,P\,t_d}{\eta\left({V_{C_{max}}}^2 - {V_{C_{min}}}^2\right)}, \tag{25}$$

where η represents the efficiency of the HTEC. This value can be related to the losses in the power converter, which in fact depend on the operation point and the critical load consumption. A good

choice for this value can be the minimum converter efficiency that always satisfies t_d. Converter efficiency as a function of the operation point of the converter can be experimentally determined by applying a test bench of controlled variation in the voltage of the capacitor and the load power.

4. Simulation and Experimental Results

First, to validate the correct operation of the proposed circuitry and control module, several simulation runs were conducted using the PSIM software package. The parameters of the simulation are listed in Table 1.

4.1. Simulation Results

In Figure 9, the system starts in off-line mode until it enters in the charge mode at 0.75 s when the capacitor begins charging at 75 V using pulse-wise current limited between zero and the defined maximum value (5 A). In the second interval (stand-by mode), the capacitor's voltage decreased due to the self-discharge resistance (since the real self-discharge resistance was very high, a resistance of 1 kΩ was used to reduce the duration of this interval). Once the capacitor voltage fell out of the hysteresis band (its value decreased below 73 V), the charge mode was reactivated again to recover the voltage level. After that, a bus failure was introduced at 0.35 s; the bus capacitor discharged first down to the voltage level programmed to activate the operation in the discharge mode. After that, the circuit entered a discharging mode regulating the bus voltage to a reference value of 24 V.

Table 1. Specifications and parameters of the studied HTEC.

General Operation Specifications				Converter Parameters			
Parameter	**Symbol**	**Value**	**Units**	**Parameter**	**Symbol**	**Value**	**Units**
Nominal bus voltage	$V_{B_{nom}}$	28	V	Bus capacitor	C_B	1.880	μF
Maximum bus voltage	$V_{B_{max}}$	36	V	Auxiliary capacitor	C_{aux}	600	μF
Minimum bus voltage	$V_{B_{min}}$	22	V	Self-discharge capacitor resistance	R_{cp}	1	kΩ
Regulated bus voltage	$V_{B_{ref}}$	20	V	Inductor	L	25	μH
Auxiliary capacitor max. voltage	$V_{C_{max}}$	78	V	Bus load resistance	R	12	Ω
Auxiliary capacitor nom. voltage	$V_{C_{nom}}$	73	V	**Discharge PI Regulator Parameters**			
				Parameter	**Symbol**	**Value**	
Auxiliary capacitor min. voltage	$V_{C_{min}}$	12	V	Proportional gain (Discharge)	K_p	15	
Maximum charge current	I_{max}	10	A	Integral gain (Discharge)	K_i	5.000	

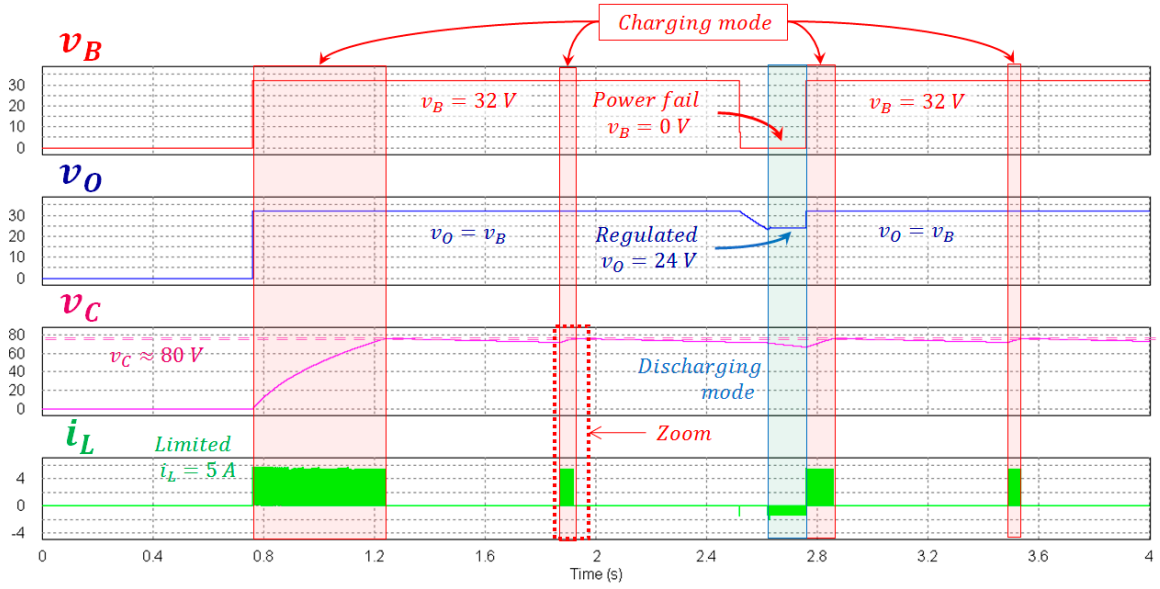

Figure 9. Simulation results showing waveforms for all operational modes of the proposed HTEC.

A detail of the first charging mode interval in Figure 9 is depicted in Figure 10a for a test with a reduced interval in off-line mode. As shown in the figure, the entire interval had an approximate duration of 500 ms, during which switching frequency increased from 2.6 to 200 kHz, staying at around 150 kHz for most of the charging interval. Figure 10b shows the period of the current signal at around 0.4 s when the charging voltage was close to its final value; this corresponded to a switching frequency of 166 kHz. For these results it is worth considering that an additional resistor of 1 kΩ must be also be fed during the charging mode, increasing the complete charging time interval. Approximately at 0.55 s, the system entered stand-by mode and the inner commutation was switched off.

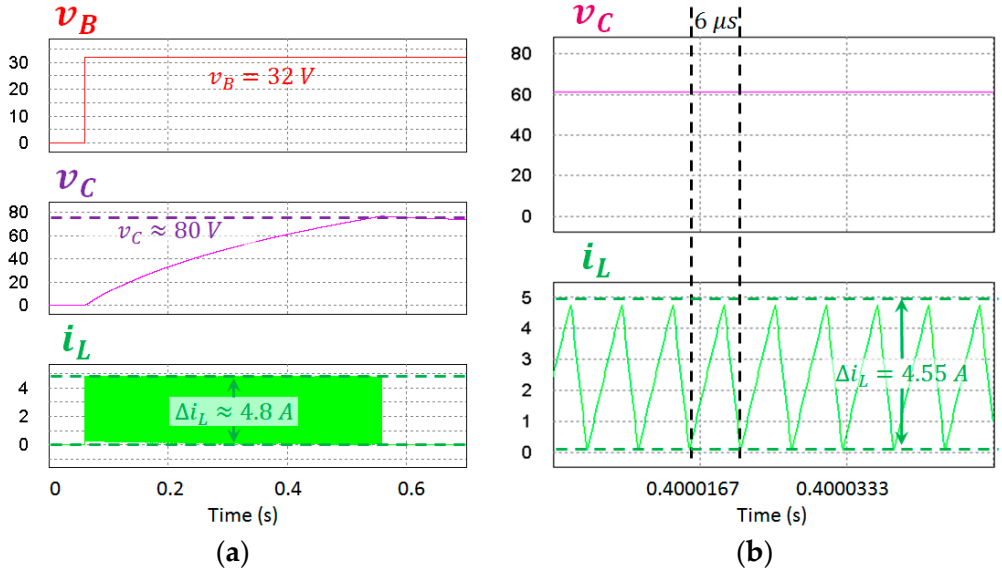

Figure 10. Simulation results detailing charging mode. (**a**) Details of the auxiliary capacitor voltage; (**b**) details of the inductor current.

Figure 11a details the charging mode in which the system entered after a stand-by interval. In this case, some current pulses were required to recover the voltage level in the capacitor, avoiding prolonged self-discharge. For this test, it is important to mention that a mean value of 74.5 V was established in the auxiliary capacitor through a hysteresis band defined between 72 and 77 V. In Figure 11b, the detail of a bus failure can be observed. The voltage of the bus fell to zero at 0.52 s, then, after disconnecting the load from the bus, the voltage decreased until reaching the limit of 24 V defined to activate the discharging mode. A short and almost imperceptible transient state was observed between 0.61 and 0.65 s when the voltage was regulated, maintaining the conditions until the bus recovered an acceptable voltage level to operate at 0.72 s.

4.2. Experimental Results

A prototype of the proposed system was built to provide the experimental results. The power module was built using the converter parameters in Table 1, two AOTF15S60 MOSFET (Alpha & Omega Semiconductor, CA, USA), and one opto-isolated driver TLP350 (Toshiba Corporation, Tokyo, Japan). The bus capacitance and auxiliary capacitance were built by paralleling four 470 μF/100 V capacitors and six 100 μF/160 V capacitors, respectively. An additional resistor of 1 kΩ in parallel with the auxiliary capacitor was added to emphasize the effect of the self-discharging resistance and facilitate signal capture, evaluating the entire behavior of the circuit. As sensors, two isolated closed-loop hall-effect transducers LV-20P (LEM International SA, Ginebra, Switzerland) were used to measure the bus voltage and the auxiliary capacitor voltage; one isolated closed-loop hall-effect transducer CAS 15-NP (LEM International SA, Ginebra, Switzerland) was used to measure the inductor current. These sensors were selected to provide a reliable and accurate validation of the control proposal. However, for implementation of the

systems in a commercial product, these elements can be replaced by low cost circuits. The control circuit depicted in Figure 12 was built using LM319 comparators, LM347 operational amplifiers (Freescale Semiconductors, TX, USA), and CD4027 flip-flops (Texas Instruments, TX, USA).

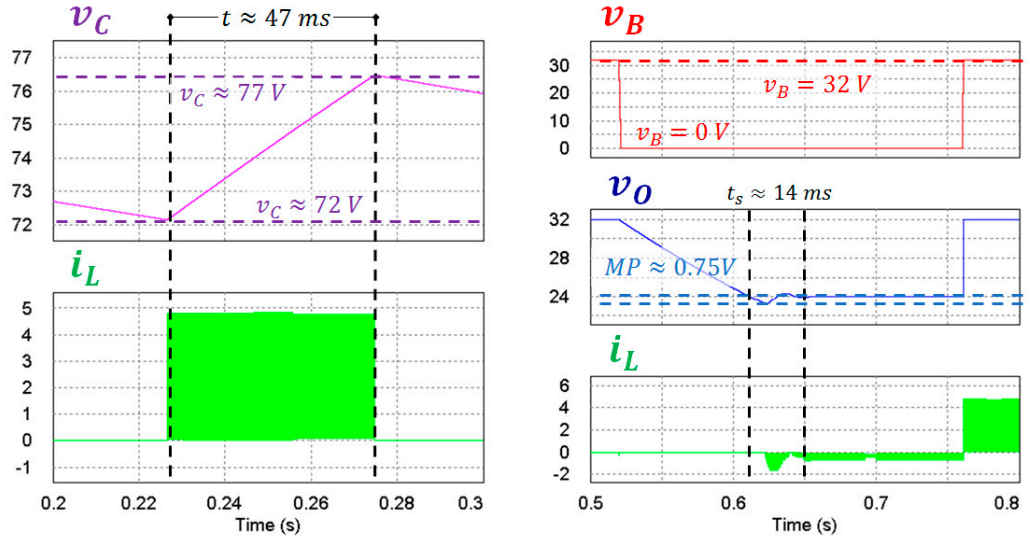

Figure 11. Detailed simulation results. (**a**) Auxiliary capacitor voltage during the recharging mode; (**b**) ELVDC bus voltage during discharging mode.

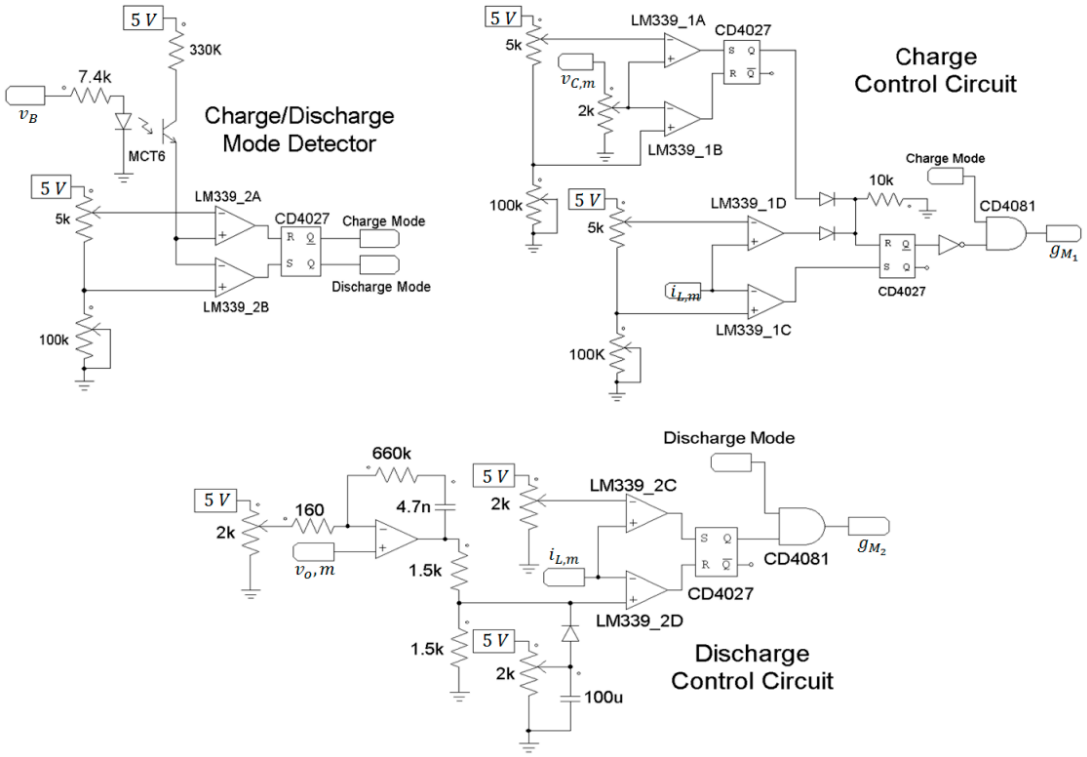

Figure 12. Schematic circuit diagram of the proposed control for the HTEC.

The experimental set-up was composed of a Mixed Signal Digital Oscilloscope MSO2014B equipped with an isolated current probe TCP0020 (Tektronix, OR, USA) and three isolated voltage probes. Figure 13 shows an oscilloscope capture of the circuit variables during a test, evaluating its entire functionality. Overall, the circuit operated as expected, in line with the simulation results. To detail

the results for each operation mode, Figure 14a shows the charging mode coming from the off-line mode, while Figure 14c details the charging mode coming from the stand-by mode. In Figure 14b, the charging mode is detailed at the switching frequency level to show the current waveform associated with the converter operating in BCM. Finally, Figure 14d details the discharging mode, illustrating the performance of the bus regulation control module while the auxiliary capacitor is discharging.

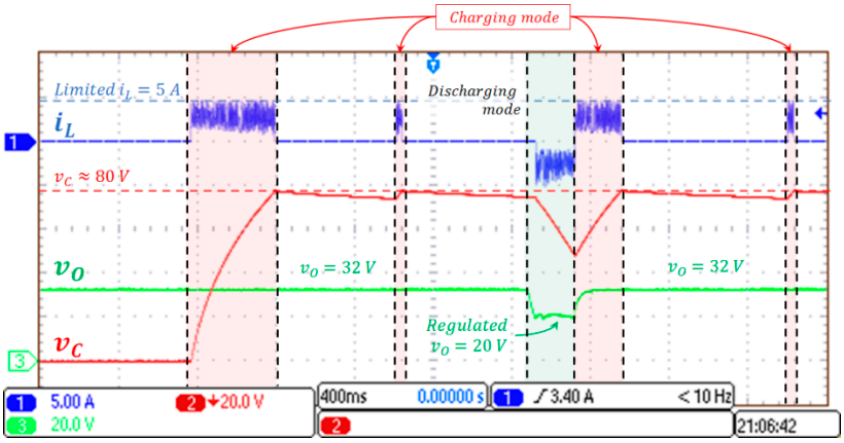

Figure 13. Oscilloscope capture showing all operation modes of the HTEC.

As shown in all captures in Figure 14, the behavior of the real HTEC agrees with the simulation results and the theoretical analysis. Current regulation in the two modes was accomplished and external voltage control was equally effective, obtaining the hysteretic behavior for the auxiliary capacitor, which prevents the undesired switching of the converter and limits the recharging process of the capacitor to short intervals. Although the recharging interval was close to 4 ms (in measurements), it is worth pointing out that this value was related to the additional resistor used to reduce the stand-by time, which was included to obtain the comprehensive graphic capture of the circuit operation depicted in Figure 13. Regulation of the bus was really effective because no overshoot was present and the steady-state error was limited to ± 1 V around the reference value.

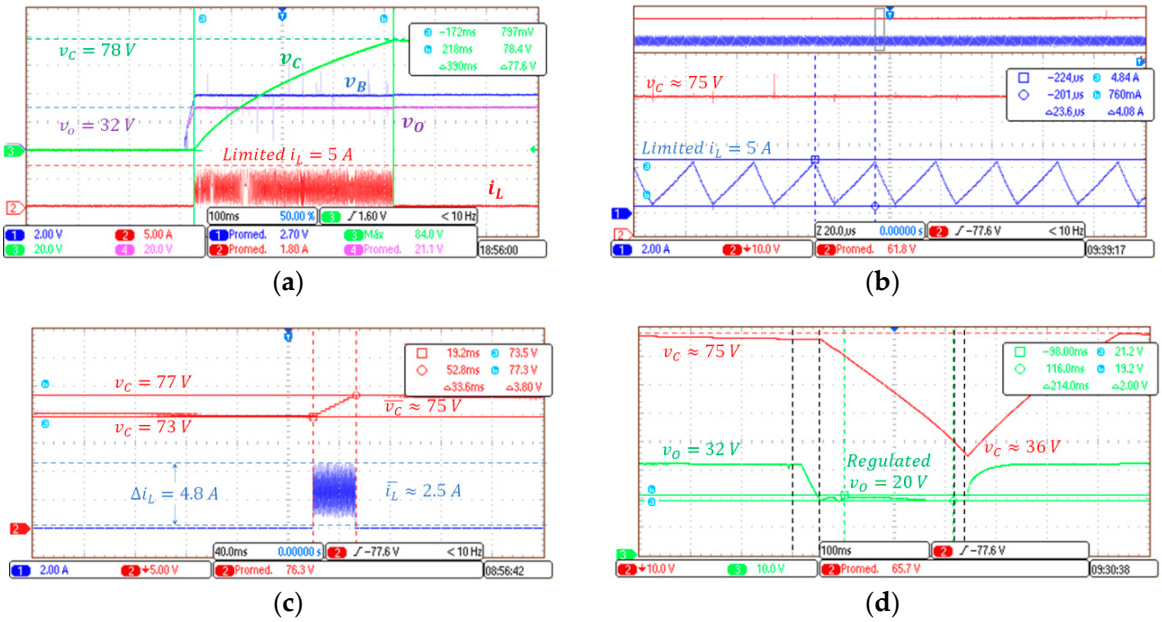

Figure 14. Detailed experimental results. (**a**) Charging mode and standby mode; (**b**) details of the inductor current during charging mode; (**c**) standby mode and recharging mode; (**d**) discharging mode.

5. Conclusions

An improved-control approach for the parallel HTEC, based on the BBBC operating in BCM, has been proposed and described in detail. The developed control module stands out for its simplicity, robustness and reliability. Every operational mode of the converter has been modelled, obtaining a comprehensive set of expressions to analyze the behavior of the circuit and facilitate its design. Both simulation and experimental results confirmed the validity of the approach and its potential use in real applications. Current efforts towards improving the HTEC are focused on the digital implementation of the control module in a microcontroller with an analog comparator module, which promises to enhance the performance of the system without losing precision or simplicity due to discretization. The experimental validation of this new approach will include optimization of the components and the Printed Circuit Board area.

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