Studies on a Hybrid Full-Bridge/Half-Bridge Bidirectional CLTC Multi-Resonant DC-DC Converter with a Digital Synchronous Rectification Strategy

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Abstract: This study presents a new bidirectional multi-resonant DC-DC converter, which is named CLTC. The converter adds an auxiliary transformer and an extra resonant capacitor based on a LLC resonant DC-DC converter, achieving zero-voltage switching (ZVS) for the input inverting switches and zero-current switching (ZCS) for the output rectifiers in all load range. The converter also has a wide gain range in two directions. When the load is light, a half-bridge configuration is adopted instead of a full-bridge configuration to solve the problem of voltage regulation. By this method, the voltage gain becomes monotonous and controllable. Besides, the digital synchronous rectification strategy is proposed in forward mode without adding any auxiliary circuit. The conduction time of synchronous rectifiers equals the estimation value of body diodes' conduction time with the lightest load. Power loss analysis is also conducted in different situations. Finally, the theoretical analysis is validated by a 5 kW prototype.

Keywords: bidirectional CLTC resonant DC-DC converter; light load; synchronous rectification strategy; power loss analysis

1. Introduction

With advantage of ZVS + ZCS, the bidirectional resonant DC-DC converter (BRDC) is gaining more attention in DC distribution system or DC microgrid applications [1–8]. All the power switching devices, including metal oxide semiconductor field effect transistor (MOSFET) switches and diodes have the desirable soft-switching features, and the switching loss is greatly decreased. In addition, the electromagnetic interference (EMI) is also restricted. As a result, BRDCs are characterized by high efficiency, high power density and low EMI, and are applicable to high frequency applications [9,10]. Among all the BRDCs, the bidirectional series resonant converter (BSRC) is a candidate topology [11–16]. All the switches of a BSRC work in either ZVS or ZCS for a wide variation of voltage gains with phase-shift control [13]. A novel control scheme was developed for BSRC in discontinuous mode [14]. With the accumulation of energy packets to raise output voltage, it is possible to have a gain greater than one. A novel method for analyzing the frequency response is also presented based on a mixture of the Fourier and the average state-space methods [15]. The analysis method provides enough information to properly control the BSRC. A BSRC using a continuous current mode was proposed in [16]. Experimental results from a 6 kW prototype validated the theoretical analysis, and higher efficiency is obtained compared to the phase-shift DAB in a wide power range. However, the efficiency

is not ideal for the whole frequency range. A bidirectional LLC resonant DC-DC converter is also a good option. A bidirectional three-level LLC resonant converter has a very wide voltage gain range with PWAM control [17]. It overcomes the limitation of voltage gain in LLC resonant converters. A bidirectional LLC resonant converter with automatic forward and backward mode transition is proposed in [18]. An auxiliary inductor is added to raise the voltage gain in backward operation. Based on LLC, a symmetrical bidirectional CLLC resonant converter was recently proposed [19–21]. The voltage gain in backward operation is the same as that in forward operation. However, with the growth of output power and voltage conversion ratio, the resonant inductance is small and the resonant capacitance is big. These parameters are hard to design.

Besides, the regulation capability of a resonant DC-DC converter is weak under light load conditions. Due to parasitic parameters in the resonant tank, the output voltage goes up as the switching frequency increases, and an upturn drifting occurs in the voltage gain curve [22]. This phenomenon causes trouble for voltage regulation under light load conditions. To solve this problem, many researchers have changed the control method for light load conditions [23–28]. Burst mode is used in [23,24], but the ripple of the output voltage is large and the dynamic response is slow. The phase-shift and PWM control methods are effective in [25–28], but the control scheme is complex due to the additional control elements. The changes are also conducted with the topology of resonant DC-DC converter. Adding an additional output capacitor to switches can reduce current ripple and decrease powering transmitted between two sides of transformer [29], but the ZVS range this time is narrow. An additional capacitor is paralleled with the resonant inductor to improve the gain characteristics in [30]. ZVS is acquired under entire load condition, and efficiency is improved with less turn-off loss, but the design of the transformer and additional capacitor is complex due to resonance between leakage inductor and the additional capacitor.

The synchronous rectification (SR) strategy for resonant converters is also important toward achieving working efficiency [31–34]. A novel driving scheme with a compensation network for synchronous rectifiers is used in LLC resonant converters. The conduction loss and switching loss are also reduced considerably [35]. A hybrid driving scheme for full-bridge SR is proposed in [36]. It uses one transformer auxiliary winding to drive two high-side SR switches and a simple current transformer (CT) to drive two low-side SR switches. The proposed method operates well under DCM and CCM conditions. A novel SR control strategy is developed, through accurately tracking the target switching moments in [37]. However, the strategies above are complex in application and they are not verified in BRDCs. A new synchronous rectification strategy, which is simpler and compatible to bidirectional power flow, needs to be developed.

In this study, a new bidirectional CLTC multi-resonant DC-DC converter is proposed. As Figure 1 shows, the converter is composed of a high-voltage side (HVS) full-bridge, low-voltage side (LVS) full-bridge and a multi-resonant tank. An auxiliary transformer T_2 and an extra resonant capacitor C_{r2} are added on bidirectional LLC resonant DC-DC converter, so the converter is named by CLTC. The gain range in two directions is broadened with the added devices. ZVS for the input inverting switches and ZCS for the output rectifiers are realized in all load range. U_H represents HVS DC voltage, while U_L represents LVS DC voltage. Power flows in both forward and backward mode are modulated with pulse frequency modulation (PFM). In forward mode, S_1 & S_4 and S_2 & S_3 run with 50% duty cycle, the rectifier switches S_6 & S_7 and S_5 & S_8 are driven by the SR signals. In backward mode, S_6 & S_7 and S_5 & S_8 run at 50% duty cycle, S_1 & S_4 and S_2 & S_3 don't work, diodes on HVS realize SR.

This paper is organized as follows: the operation principles and characteristic descriptions of the proposed converter are discussed in Section 2. Hybrid full-bridge/half-bridge configuration is used to improve the light load regulation capability in Section 3. Stresses of power devices, load and working frequency range in half-bridge CLTC are also given to prove the feasibility of the half-bridge configuration. SR strategy based on estimation of the diodes' conduction time is proposed in Section 4. Power loss distribution and comparison tests are conducted with different loads and LVS DC voltages in Section 5. A 5 kW prototype is built with HVS voltage of 400 V and LVS DC voltage of 42–58 V.

Experimental results are shown to validate the theoretical analysis above in Section 6. Conclusions are drawn in Section 7.
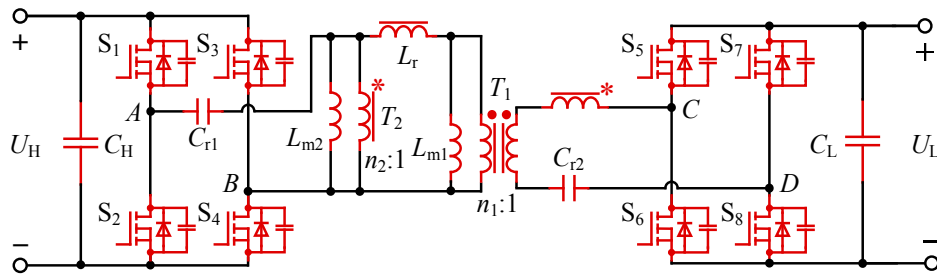

Figure 1. The proposed bidirectional CLTC multi-resonant DC-DC converter.

2. Operation Principles and Characteristic Description

In this section, the main operation principles of CLTC multi-resonant converter are given. It is similar to a LLC resonant converter as two stages of resonance exist. The resonant frequency, voltage gain and ZVS characteristic are analyzed, forming research foundations for the following sections.

2.1. Operation Principles

Figure 2 shows different states of the CLTC multi-resonant converter. In Figure 2, i_{Lm1} is excitation current of transformer T_1 on HVS, i'_{Lm1} is excitation current of transformer T_1 on LVS, i_{Lr} is current of resonant inductor, i_{Cr1} and i_{Cr2} are currents of resonant capacitors on HVS and LVS, u_{GS14} is the driving signal of S_1 and S_4, u_{GS23} is the driving signal of S_2 and S_3, u_{GS58} is the driving signal of S_5 and S_8, u_{GS67} is the driving signal of S_6 and S_7, u_{DS14} is the drain-source voltage of S_1 and S_4, u_{DS23} is the drain-source voltage of S_2 and S_3, u_{DS58} is the drain-source voltage of S_5 and S_8, u_{DS67} is the drain-source voltage of S_6 and S_7, i_{DS14} is the drain-source current of S_1 and S_4, i_{DS23} is the drain-source current of S_2 and S_3, i_{DS58} is the drain-source current of S_5 and S_8, i_{DS67} is the drain-source current of S_6 and S_7.
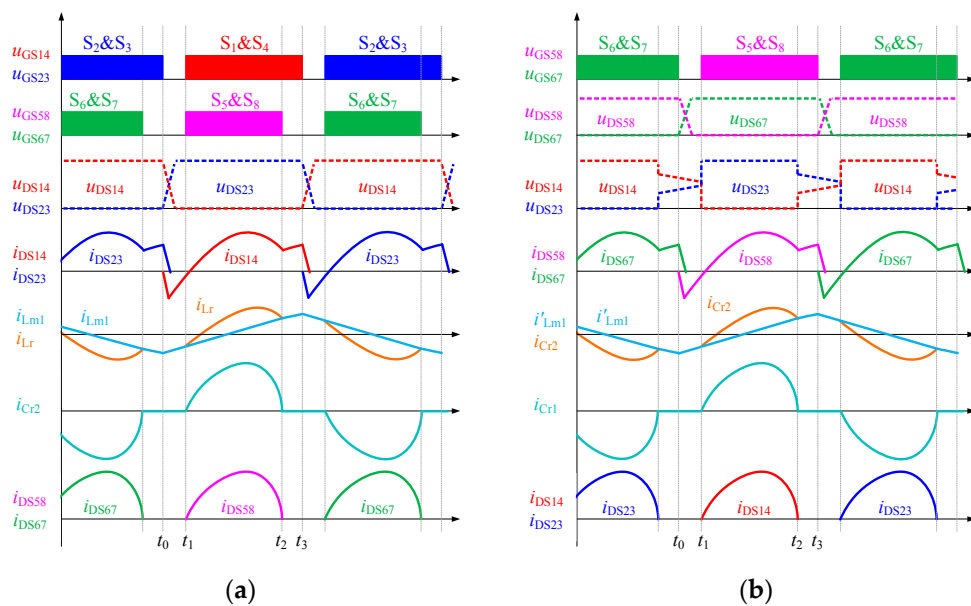

Figure 2. The current and voltage waveforms of CLTC multi-resonant converter: (**a**) forward mode; (**b**) backward mode.

2.1.1. Forward Mode

The equivalent circuits in forward mode are listed in Figure 3. Detailed descriptions and explanations of the operational modes in half period are as follows:

Mode A [t_0–t_1]: S_2 and S_3 have just turned off at t_0. The HVS current charges the output capacitor of S_2 and S_3, and discharges the output capacitor of S_1 and S_4. After that, the HVS current passes through the antiparallel diode of S_1 and S_4, which makes the switches turn on under the ZVS condition.

(a)

(b)

(c)
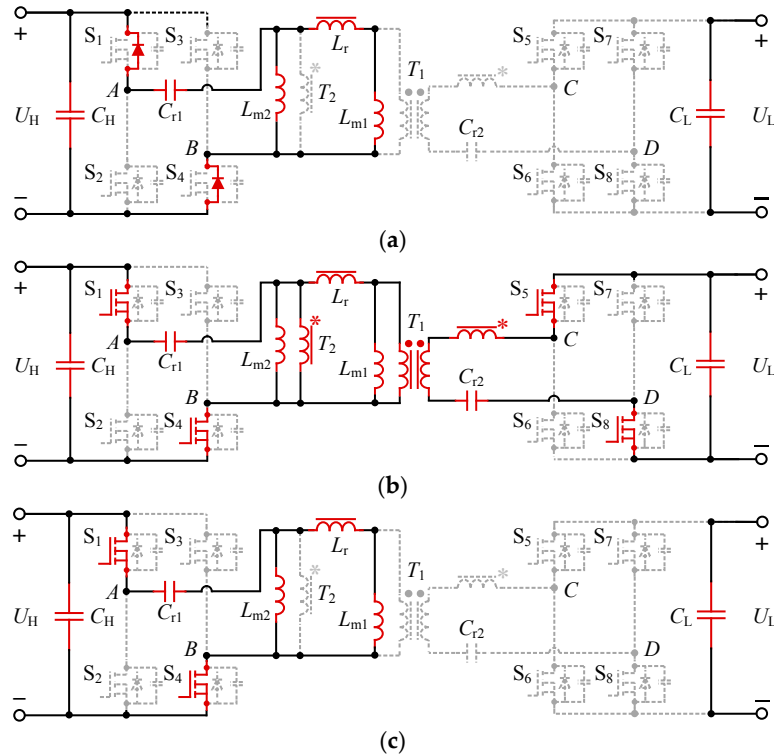
Figure 3. Equivalent circuits for each stage in forward mode: (**a**) Mode A; (**b**) Mode B; (**c**) Mode C.

Mode B [t_1–t_2]: At t_1, S_1, S_4, S_5 and S_8 turn on and power is transferred from HVS to LVS. The resonant current changes in a sine-wave with main resonant frequency, f_r. At t_2, i_{Lr} is equal to i_{Lm1}, i_{Cr2} and i_{ds58} become zero.

Mode C [t_2–t_3]: S_1 and S_4 are still on in this mode, S_5 and S_8 are off in this mode. As i_{Cr2} and i_{ds58} are zero in t_2, S_5 and S_8 turn off under ZCS condition. The HVS goes into secondary resonance with the frequency of f_{r2f}. At t_3, S_1 and S_4 are off and ready to go into dead-time duration.

When working frequency is bigger than main resonant frequency, Mode C and ZCS of LVS power switches disappear like LLC. The turn-off currents increase largely in this situation.
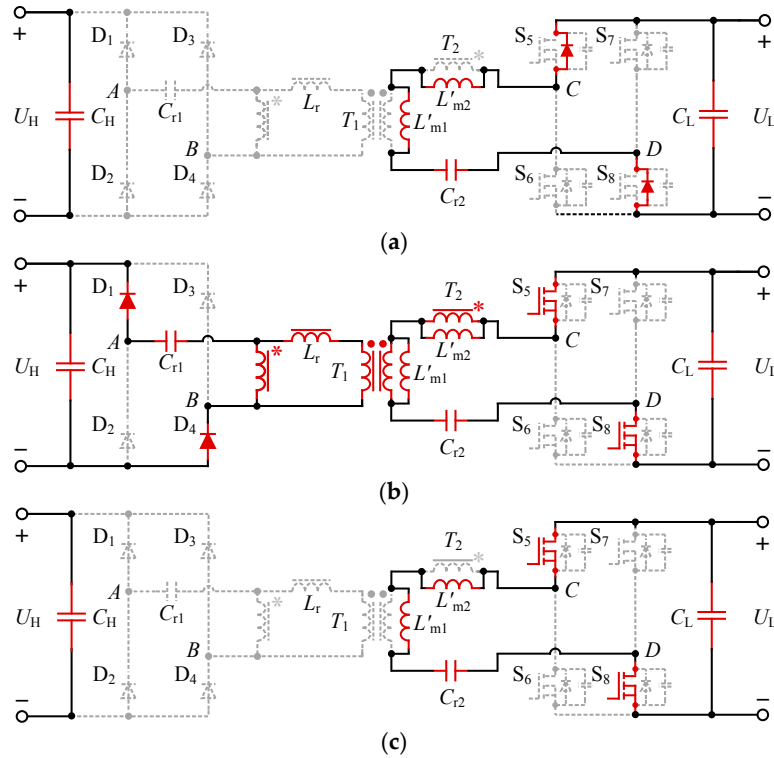
2.1.2. Backward Mode

The equivalent circuits in backward mode are listed in Figure 4. L'_{m1} and L'_{m2} are the magnetizing inductors on LVS. The modes are similar to those in forward mode. Detail descriptions and explanations of the operational modes in half period are shown as follows:

Mode A [t_0–t_1]: S_6 and S_7 turn off at t_0. The resonant current on LVS charges the output capacitor of S_6 and S_7, and discharges the output capacitor of S_5 and S_8. After that, the LVS current passes through the antiparallel diode of S_5 and S_8, which makes the switches turn on under the ZVS condition.

Mode B [t_1–t_2]: At t_1, S_5, S_8, D_1 and D_4 turn on and power is transferred from LVS to HVS. The resonant current on LVS changes in a sine-wave with main resonant frequency. At t_2, i_{Cr2} is equal to i'_{Lm1}, i_{Cr1} and i_{ds14} become zero.

Mode C [t_2–t_3]: S_5 and S_8 are still on in this mode, D_1 and D_4 are off in this mode. ZCS of D_1 and D_4 is realized as i_{Cr1} and i_{ds14} become zero at t_2. The LVS goes into secondary resonance with the frequency of f_{r2b}. At t_3, S_1 and S_4 are off and ready to go into dead-time duration.

When working frequency is bigger than main resonant frequency, Mode C and ZCS of HVS diodes disappear like LLC. The turn-off currents increase largely in this situation.

Figure 4. Equivalent circuits for each stage in backward mode: (**a**) Mode A; (**b**) Mode B; (**c**) Mode C.

2.2. Characteristic Description

Main resonant frequency of CLTC converter in two power flows, f_r, is:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{A}{B}} \tag{1}$$

where:

$$A = A_1 + A_1{}^2 - A_2 \tag{2}$$

$$A_1 = C_{r1}L_{m2}(L_{m1}+L_r)n_1{}^2n_2{}^2 + (L_{m1}+L_r)C_{r2}L_{m2}n_1{}^2 + (L_{m2}+L_r)C_{r2}L_{m1}n_2{}^2 + 2C_{r2}L_{m1}L_{m2}n_1n_2 \tag{3}$$

$$A_2 = 4C_{r1}C_{r2}L_{m1}L_{m2}L_r(L_{m1}+L_{m2}+L_r)n_1{}^2n_2{}^4 \tag{4}$$

$$B = 2C_{r1}C_{r2}L_{m1}L_{m2}L_rn_2{}^2 \tag{5}$$

f_r is obtained when no load is added and imaginary part of AC input impedance of CLTC is zero.

The secondary resonant frequency in forward mode, f_{r2f}, and the secondary resonant frequency in backward mode, f_{r2b}, are:

$$f_{r2f} = \frac{1}{2\pi}\sqrt{\frac{L_r+L_{m1}+L_{m2}}{C_{r1}L_{m2}(L_r+L_{m1})}} \tag{6}$$

$$f_{r2b} = \frac{1}{2\pi\sqrt{(L'_{m1}+L'_{m2})C_{r2}}} \tag{7}$$

f_{r2f} and f_{r2b} are obtained with the resonant capacitance and inductance in secondary resonance. The resonant capacitance and inductance are shown in Figures 3c and 4c.

By use of the fundamental harmonic analysis (FHA) method, Figures 5a and 6a show 3D voltage gain curves according to load P_o and normalized working frequency f_s/f_r. G_F is gain in forward mode and G_B is gain in backward mode. As is shown in Figures 5b and 6b, when the working frequency is below the main resonant frequency, G_F and G_B increase at first and decrease subsequently with the growth of working frequency. The peak gains are more than 1 over all the load range and obtained around secondary resonant frequency, f_{r2f} and f_{r2b}. At main resonant frequency f_r, the gain of the converter is 1. As is shown in Figures 5c and 6c, when working frequency is above main resonant frequency, G_F and G_B decrease with the growth of working frequency. When load is lighter, the voltage gain is higher and the slope of gain curve is sharper. Voltage gain range of CTLC converter is wide enough to adapt applications like battery charger and DC microgrid.
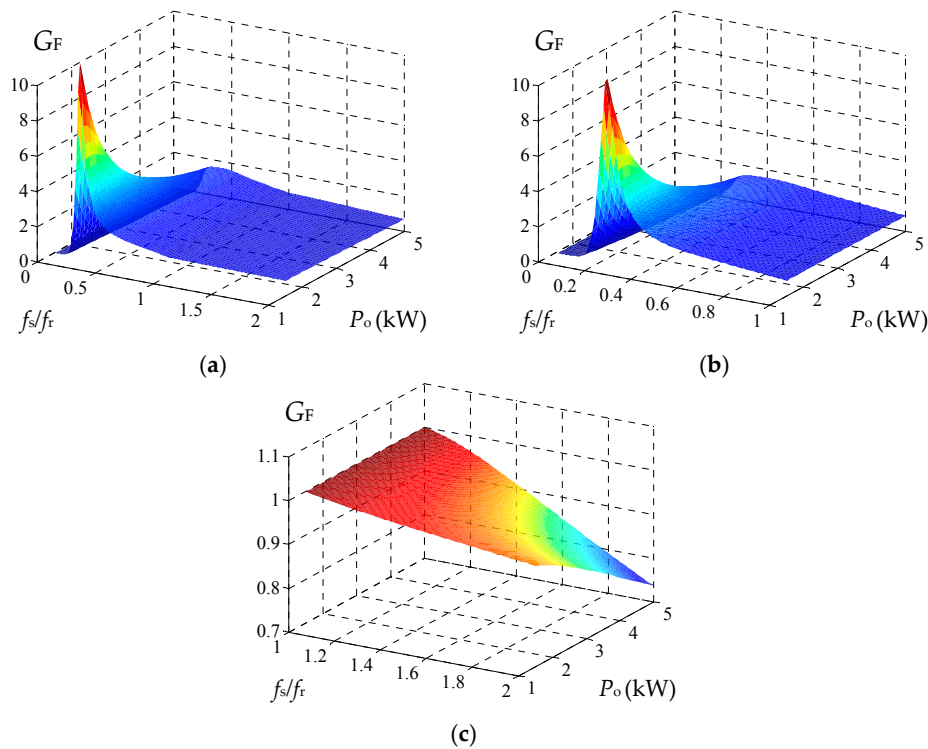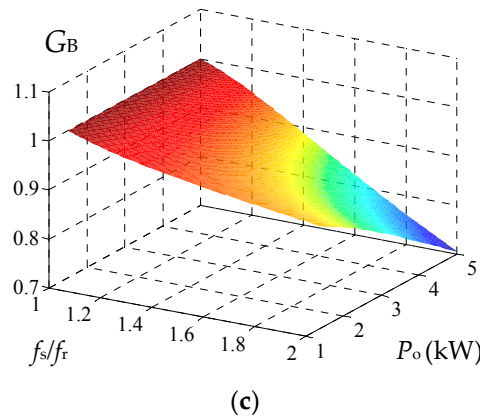

Figure 5. Voltage gain obtained by FHA model in forward mode: (**a**) whole frequency range; (**b**) $f_s < f_r$; (**c**) $f_s \geq f_r$.

Figure 6. *Cont.*

(c)
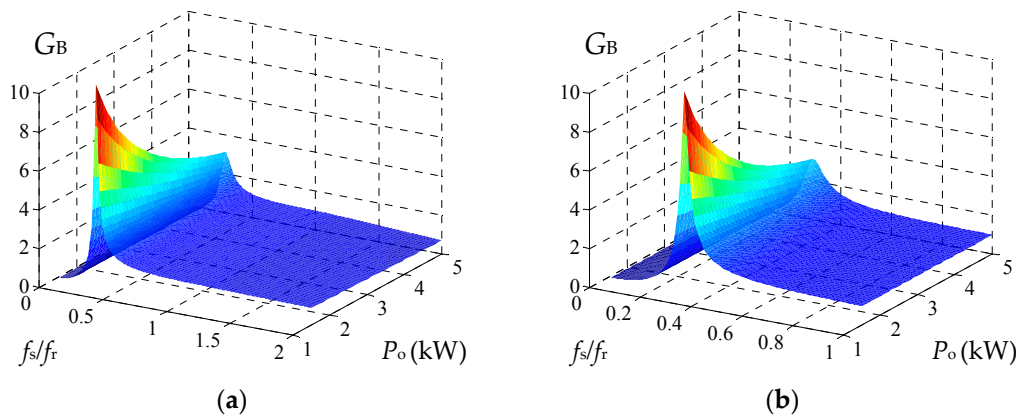
Figure 6. Voltage gain obtained by FHA model in backward mode: (**a**) whole frequency range; (**b**) $f_s < f_r$; (c) $f_s \geq f_r$.

In order to realize ZVS for HVS switches, in forward mode, the dead-time duration t_{dt_F} should satisfy (6) using the ZVS mechanism analyzed by [19]. C_{oss_H} is the output capacitance of HVS switch:

$$t_{dt\_F} \geq \frac{16C_{oss\_H}L_{m2}(L_r + L_{m1})f_s}{L_r + L_{m1} + L_{m2}} \tag{8}$$

Similarly, in backward mode, the dead-time duration t_{dt_B} of LVS switches should satisfy:

$$t_{dt\_B} \geq 16C_{oss\_L}(L'_{m1} + L'_{m2})f_s \tag{9}$$

C_{oss_L} is the output capacitance of LVS switch in (7).

The inequations can be easily satisfied with different loads and working frequencies, which is good for efficiency. The t_{dt_F} and t_{dt_B} are set to 200 ns in experiments.

## 3. Hybrid Full-Bridge/Half-Bridge Configuration

In this section, the reason for the upturn phenomenon is analyzed. A full-bridge configuration is used with a normal load. Half-bridge configurations are used for light load conditions with the advantage of monotonous gain curve and lower frequency. Because the situations in forward and backward mode are similar, the discussion in this section is conducted only in forward mode, and details are not provided for the backward mode.

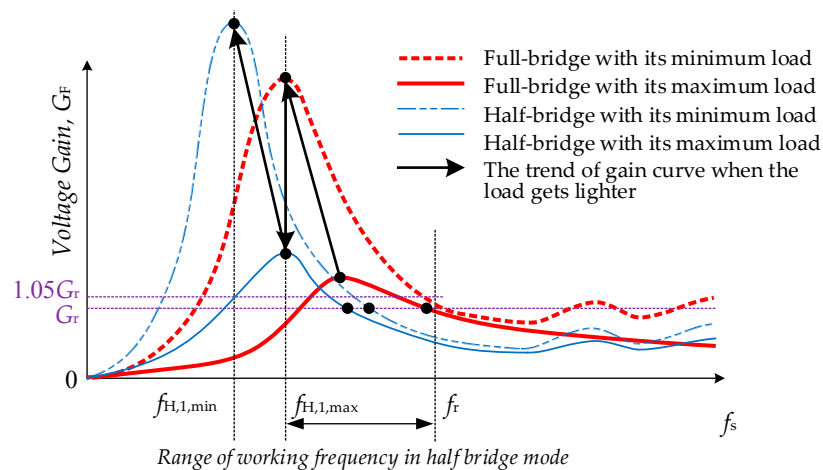### 3.1. Half-Bridge Configuration at Light Load Condition

Using the analysis method proposed in [22], it is found that transformer wiring capacitance is the main factor leading to the upturn problem. As is shown in Figure 7a, the ideal gain curve without considering parasitic parameters in forward mode is monotonous with working frequency under light load conditions. However, the voltage gain curve considering transformer wiring capacitance and experimental gain curve has upturns. As the experiment gain curve is not monotonous, the gain cannot be regulated well with PFM. For example, the voltage gain of 1.02 in Figure 7a is obtained with four different working frequencies. When PFM is adopted to control LVS voltage, the working frequency may be around $1.4f_r$ instead of $0.8f_r$, and fluctuates quickly as the gain curve is not monotonous.

To overcome the above problem, a half-bridge configuration is introduced in this paper to regulate the required output voltage. In forward mode, the full-bridge in HVS is transformed into a half-bridge by turning off Q_3 and turning on Q_4 incessantly. The voltage gain is reduced by half, with the same load and resonant parameters. Thus, when the voltage gain needed is below 1 under light load conditions, a half-bridge configuration is adopted and the required gain is obtained with lower working frequency.

In Figure 7b, when the working frequency is around $0.35f_r$, twice the required gain is acquired in full-bridge configuration. Thus, a gain of 1.02 is acquired in half-bridge configuration with the same working frequency and load. Also, the gain of 1.02 is controllable in half-bridge mode, because the working frequency decreases largely, away from the region where the gain is not monotonous.

(a)

(b)
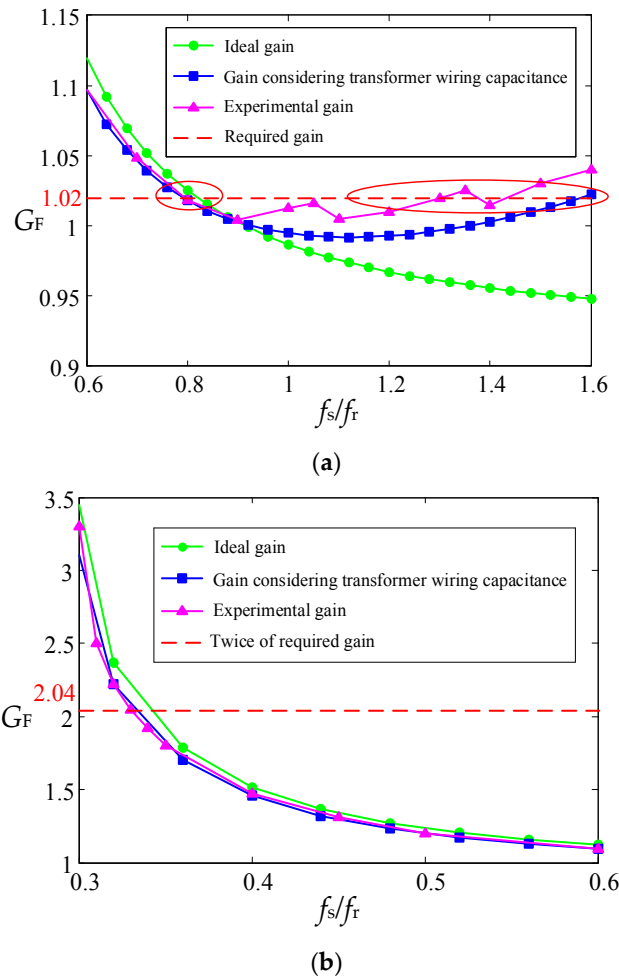
Figure 7. Voltage gain curve of full-bridge CLTC converter at light load condition. (**a**) Around gain of 1.02; (**b**) around again of 2.04.

Figure 8. Voltage gain curve of CLTC converter at light load condition.

The mechanism of transformation between full-bridge and half-bridge configuration is displayed in Figure 8. With the decrease of load in full-bridge configuration, the gain curve rises. Then, the full-bridge configuration is transformed into a half-bridge configuration, working frequency gets lower and the gain curve is monotonous around G_r. At last, half-bridge configuration is used to adapt lighter load instead of full-bridge configuration. The mechanism of transforming full-bridge into half-bridge is simple and effective, still, several considerations of the method are discussed here.

3.2. Voltage and Current Stresses

The stresses in both full-bridge and half-bridge configurations need to be checked. Voltage stresses of all the switches do not change. When the same power is transmitted, current stresses of LVS switches stay the same. Current stresses of HVS switches in half-bridge are twice of those in full-bridge as the AC input voltage is cut by half. Thus, the load must be light if half-bridge is adopted, to ensure the current amplitude is acceptable.

3.3. Load and Working Frquency Range

The peak gain should be larger than the required gain, G_r. It is because if the peak gain is smaller than G_r, G_r cannot be tracked. Taking a margin of $0.05G_r$ into consideration, the DC output resistance in half-bridge configuration, $R_{o,H}$, should satisfy the following equation:

$$G_{F,H}(f_{H,1}, R_{o,H}) \geq 1.05G_r \tag{10}$$

In (8), $G_{F,H}$ is the voltage gain of half-bridge CLTC, $f_{H,1}$ is the maximum point.

Also, $R_{o,H}$ should be bigger than twice of the rated resistance, $R_{o,H,rated}$, in full-bridge. As Section 3.2 tells, the selection of $R_{o,H}$ should guarantee that the current stresses in half-bridge are no bigger than those in full-bridge. Thus:

$$R_{o,H} \geq 2R_{o,F,rated} \tag{11}$$

The working frequency of CLTC in half-bridge configuration, should be in the range of $[f_{H,1,max}, f_r]$. The working frequency should be lower than f_r to avoid upturn phenomenon of gain curve. Also, when load is heavier in half-bridge, $f_{H,1}$ gets larger as Figure 8 shows, so the lower limit of the working frequency is the largest value of $f_{H,1}$, $f_{H,1,max}$. In the range of $[f_{H,1,max}, f_r]$, the gain curve monotonously declines with working frequency, and the slope is sharper in half-bridge configuration. It is ideal for voltage regulation of CLTC.

4. Synchronous Rectification Strategy Based on Estimation of Body Diodes' Conduction Time

In consideration of improving the efficiency, a digital synchronous rectification strategy is proposed in forward mode. No auxiliary circuit is added. The proposed strategy adjusts conduction time of switches in LVS by calculating rectifier diodes' conduction time in half period, t_{SR}. A whole process of calculating t_{SR} is proposed and verified in this section. It can be used in both full-bridge configuration and half-bridge configuration.

4.1. Synchornous Rectification Strategy

With the proposed digital synchronous rectification strategy, all the driving signals of HVS switches S_1–S_4 and LVS SR switches S_5–S_8 are given by STM32F series chip. The turn-on time of SR switches is set to the same with HVS main switches. But the conduction time (the interval between turn-on and turn-off time) is set with the estimation value of body diodes' conduction time in half period, t_{SR}, so t_{SR} should be calculated for synchronous rectification.

4.2. Estimation of the Body Diodes' Conduction Time

When working frequency of CLTC is larger than main resonant frequency, t_{SR} is half working period because the secondary resonance doesn't exist. However, when working frequency is smaller than main resonant frequency, t_{SR} is a variable with respect to R_o and f_s. So discussion is focused on t_{SR} when working frequency is smaller than main resonant frequency.
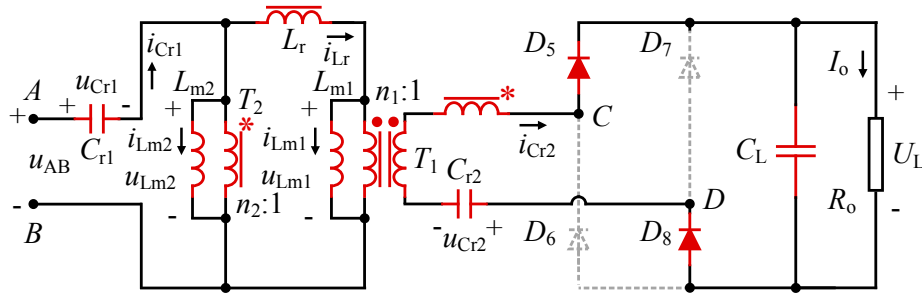

Figure 9. Topology decomposition in forward mode without synchronous rectification strategy.

In Figure 9, assuming resonant current on LVS, i_{Cr2}, is approximated to a sinusoidal pulse:

$$i_{Cr2} = \begin{cases} I_{Cr2} \sin(\frac{\pi \times t}{t_{SR}}), & 0 \leq t \leq t_{SR} \\ 0, & t_{SR} \leq t \leq T \end{cases} \tag{12}$$

I_{Cr2} is the peak value of i_{Cr2}, t is the real time, T_2 is half period, $1/(2f_s)$. The value of u_{AB} is U_H in this period.

By using the law of conservation of electric charge, it can be obtained that:

$$\int_0^{t_{SR}} I_{Cr2} \sin(\frac{\pi \times t}{t_{SR}}) \, dt = I_o \times T_2 \tag{13}$$

According to (13), I_{Cr2} can be expressed by:

$$I_{Cr2} = I_o \frac{\pi T_2}{2 t_{SR}} \tag{14}$$

The voltage of C_{r2} can be expressed by:

$$u_{Cr2}(t) = \frac{1}{C_{r2}} \int_0^t I_{Cr2} \sin(\frac{\pi \times t}{t_{SR}}) \, dt + U_{Cr2,0} \tag{15}$$

As i_{Cr2} is 0 and the voltage of C_{r2} stays the same during t_{SR}–T_2, the following equation is found:

$$U_{Cr2,0} = -u_{Cr2}(T_2) = -u_{Cr2}(t_{SR}) \tag{16}$$

Applying (15) into (16), the $U_{Cr2,0}$ can be expressed by:

$$U_{Cr2,0} = -\frac{t_{SR}^2 U_L}{2 C_{r2} T_2 R_o} \tag{17}$$

The voltage of magnetizing inductance L_{m1} and L_{m2}, u_{Lm1} and u_{Lm2}, can form following equations:

$$\begin{cases} \frac{u_{Lm1}(t)}{n_1} + \frac{u_{Lm2}(t)}{n_2} = U_L + U_{Cr2}(t) \\ (1 + \frac{L_r}{L_{m1}}) u_{Lm1}(t) + \frac{1}{n_1} L_r \frac{di_{Cr2}(t)}{dt} = u_{Lm2}(t) \end{cases} \tag{18}$$

so u_{Lm2} can be expressed by:

$$u_{Lm2}(t) = \frac{\frac{n_2}{n_1}L_r\frac{di_{Cr2}(t)}{dt} + (1 + \frac{L_r}{L_{m1}})n_1n_2[U_L + U_{Cr2}(t)]}{n_2 + n_1(1 + \frac{L_r}{L_{m1}})} \tag{19}$$

The instantaneous voltage between HVS full-bridge legs, u_{AB}, can be expressed as:

$$u_{AB}(t) = U_{Cr1,0} + \frac{1}{C_{r1}}\int_0^t i_{Cr1}(t)\,dt + u_{Lm2}(t) \tag{20}$$

where, $U_{Cr1,0}$ is the initial voltage of resonant capacitor C_{r1} at t_0, and the instantaneous current of C_{r1}, i_{Cr1}, can be expressed as:

$$i_{Cr1}(t) = i_{Lm1}(t) + i_{Lm2}(t) + (\frac{1}{n_1} + \frac{1}{n_2})i_{Cr2}(t) \tag{21}$$

In order to simplify calculation process, L_{m2} is supposed to be subject to u_{AB} during 0–t_{SR}. So i_{Lm2} and i_{Lm1} can be expressed as linearly increasing currents:

$$i_{Lm1}(t) = \frac{U_H}{2(L_{m1} + L_r)}t + I_{Lm1,0} \tag{22}$$

$$i_{Lm2}(t) = \frac{U_H}{2L_{m2}}t + I_{Lm2,0} \tag{23}$$

$I_{Lm1,0}$ and $I_{Lm2,0}$ is the initial value of I_{Lm1} and I_{Lm2}:

$$I_{Lm1,0} = -\frac{U_H \times t_{SR}}{4(L_{m1} + L_r)} \tag{24}$$

$$I_{Lm2,0} = -\frac{U_H \times t_{SR}}{4L_{m2}} \tag{25}$$

Realizing that $u_{AB}(t) = U_H$ and substituting (19) and (21) into (20), gives:

$$U_H = U_{Cr1,0} + \frac{1}{C_{r1}}\int_0^t \left[i_{Lm1}(t) + i_{Lm2}(t) + (\frac{1}{n_1} + \frac{1}{n_2})i_{Cr2}(t)\right]dt + \frac{\frac{n_2}{n_1}L_r\frac{di_{Cr2}(t)}{dt} + (1 + \frac{L_r}{L_{m1}})n_1n_2[U_L + U_{Cr2}(t)]}{n_2 + n_1(1 + \frac{L_r}{L_{m1}})} \tag{26}$$

Getting the derivative of the above equation:

$$0 = -D\frac{\pi^2}{t_{SR}^2}\sin(\frac{\pi \times t}{t_{SR}}) + E \times \sin(\frac{\pi \times t}{t_{SR}}) + F \times t_{SR} \times t + \frac{I_{Lm1,0} + I_{Lm2,0}}{I_{Cr2}} \tag{27}$$

In (27), D, E, F are:

$$D = \frac{C_{r1}n_2L_r}{n_1\left[n_2 + n_1(1 + \frac{L_r}{L_{m1}})\right]} \tag{28}$$

$$E = \frac{C_{r1}(1 + \frac{L_r}{L_{m1}})n_1n_2}{C_{r2}\left[n_2 + n_1(1 + \frac{L_r}{L_{m1}})\right]} + \frac{1}{n_1} + \frac{1}{n_2} \tag{29}$$

$$F = \left[\frac{1}{2(L_{m1} + L_r)} + \frac{1}{2L_{m2}}\right]\frac{U_H}{I_{Cr2}t_{SR}} \tag{30}$$

U_H can be expressed as U_L/M_{SD}, so F can be simplified by:

$$F = \left[\frac{1}{2(L_{m1} + L_r)} + \frac{1}{2L_{m2}}\right]\frac{2R_o}{\pi T_2 M_{SD}} \tag{31}$$

$\frac{I_{\text{Lm1,0}}+I_{\text{Lm2,0}}}{I_{\text{Cr2}}}$ is close to 0 as I_{Cr2} is much larger than $I_{\text{Lm1,0}} + I_{\text{Lm2,0}}$. When t is close to 0, $\frac{\pi \times t}{t_{\text{SR}}} \approx \sin\left(\frac{\pi \times t}{t_{\text{SR}}}\right)$, t_{SR} is the solution of (27):

$$t_{\text{SR}} = \sqrt{\frac{-\pi E + \pi\sqrt{E^2 + 4DF\pi}}{2F}} \tag{32}$$

In Figure 10, the normalized estimated conduction time t_{SR}/T_2 versus normalized operating frequency $f_{\text{s}}/f_{\text{r}}$ and different load (dots—simulation, solid lines—theoretical prediction). Figure 10 reveals good agreement between theoretical values and simulation results. The curve of t_{SR}/T_2 is basically proportional to $f_{\text{s}}/f_{\text{r}}$, and grows with the increase of load.

Based on the above analysis, the conduction time of LVS switches is set to estimated conduction time t_{SR} obtained when load is the lightest, so the conduction time of LVS switches in the proposed synchronous rectification strategy is not relevant to the load. It is a parameter changing with operating frequency. LVS switches turn on firstly to reduce conduction loss. Then, as estimated conduction time t_{SR} is a little smaller than the real conduction time of LVS body diodes, the body diodes of LVS switches conduct until the LVS resonant current becomes zero. Efficiency is not affected because the duration when body diodes conduct is short. The proposed digital synchronous rectification strategy is simple and effective, the effects are discussed in sections below.
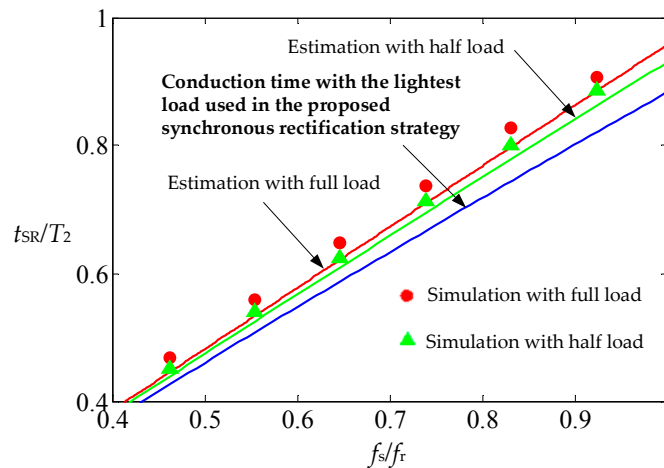
Figure 10. Normalized estimated conduction time t_{SR}/T_2 in calculation and simulation.

5. Power Loss Analysis

The power loss of converters is the key factor for component selection and design. In this section, the power loss distribution is calculated with mathematical models and compared with different LVS DC voltages. The HVS DC voltage of the converter stays the same. The power loss with half-bridge configuration and synchronous rectification strategy are discussed in this section, too.

Before further analysis, several parameters are defined as follows, $P_{\text{HSW,off}}$ is the turn-off loss of HVS power switches, $P_{\text{HSW,con}}$ is the conduction loss of HVS power switches, $P_{\text{LSW,off}}$ is the turn-off loss of LVS power switches, $P_{\text{LSW,con}}$ is the conduction loss of LVS power switches, P_{L} is the power loss of resonant inductor, $P_{\text{T,}\Sigma}$ is the total power loss of transformers, $P_{\text{WIRE,con}}$ is the conduction loss in printed circuit board and copper bar, P_{HD} is the power loss of HVS diodes, P_{LD} is the power loss of LVS body diodes in power switches.

5.1. Loss Distribution with Different LVS DC Voltages

Power loss distribution with 5 kW load in forward and backward mode is shown in Figure 11. The power loss distribution is conducted with three LVS DC voltages of 42, 50 and 58 V and the HVS

voltage of 400 V. In forward mode, the column of "50 V" is obtained around main resonant frequency, while the column of "42 V" is obtained with higher frequency and column of "58 V" is obtained with lower frequency. In backward mode, the column of "50 V" is obtained around main resonant frequency, while the column of "42 V" is obtained with lower frequency and column of "58 V" is obtained with higher frequency.
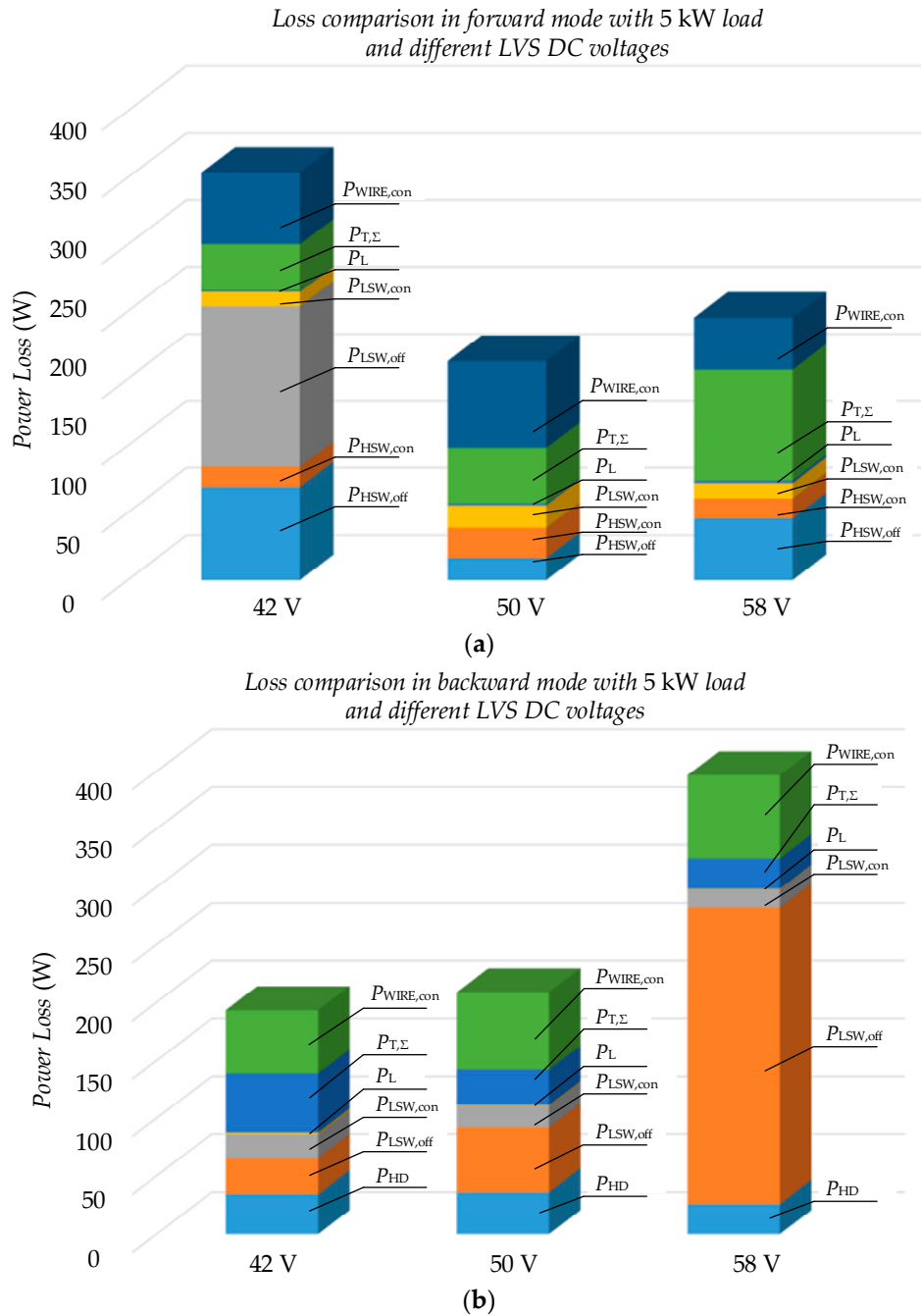
Figure 11. The power loss distribution with 5 kW and different LVS DC voltages: (**a**) forward mode; (**b**) backward mode.

$P_{HSW,off}$ and $P_{LSW,off}$ are the dominant power losses. P_L and $P_{T,\Sigma}$ change little with the change of LVS DC voltage. $P_{WIRE,con}$ is large due to proximity effect and skin effect. The column of "42 V" in forward mode and the column of "58 V" in backward mode have greater power loss compared to the

other columns. This is mainly because $P_{\text{HSW,off}}$ and $P_{\text{LSW,off}}$ are larger due to larger turn-off currents and higher working frequencies. The HVS switches are SiC power devices, and the LVS switches are Si power devices. Compared to LVS switches, the HVS switches have less turn-off delay time and fall time. So the switching loss of LVS switches is larger than that of HVS switches. Thus, the efficiency in forward mode is higher than that in backward mode in general.

5.2. Power Loss Distribution and Comparison between Full-Bridge and Half-Bridge Configuration

The power loss distribution and comparison between full-bridge and half-bridge configuration is made to demonstrate the advantage of half-bridge configuration in efficiency. Taking forward mode for example, changing from full-bridge configuration to half-bridge configuration has impacts as follows:

(1) $P_{\text{HSW,off}}$ and $P_{\text{LSW,off}}$ decrease largely. In forward mode, switches staying on on-off mode in HVS decrease from 4 to 2, and their working frequency decreases from 160 kHz to around 40 kHz. So $P_{\text{HSW,off}}$ decreases largely with half-bridge configuration. Also, $P_{\text{LSW,off}}$ decreases with less turn-off current and lower working frequency.

(2) The conduction loss of all devices increases. Resonant current on HVS increases to about twice, so $P_{\text{HSW,con}}$, conduction loss of resonant inductor and primary windings of transformers are amplified. However, as resonant current on LVS changes little, $P_{\text{LSW,con}}$ and the conduction loss of secondary windings in transformers stay the same.

(3) Core loss of resonant inductor and transformers stays the same. In half-bridge LLC, working frequency f_s decreases. However, B_{max}, the peak flux density, increases because peak value of current increases. With Steinmetz's equation $P_{\text{core}} = Kf_s^{\alpha}B_{\text{max}}^{\beta}V_e$, the core losses of resonant inductor and transformers in half-bridge configuration change little.

Figure 12a shows power loss distribution and comparison with load of 200 W in forward mode. Efficiencies of half-bridge and full-bridge configuration are 87.7% and 86.7%. The power loss distribution is in accordance with the above analysis. Compared to full-bridge configuration, efficiency is a little higher in half-bridge configuration.

Figure 12b shows power loss distribution and comparison with load of 200 W in backward mode. $P_{\text{LSW,off}}$ gets much smaller in half-bridge configuration. The power loss is cut down by 26.7% and the efficiency is 81.5% in half-bridge configuration.
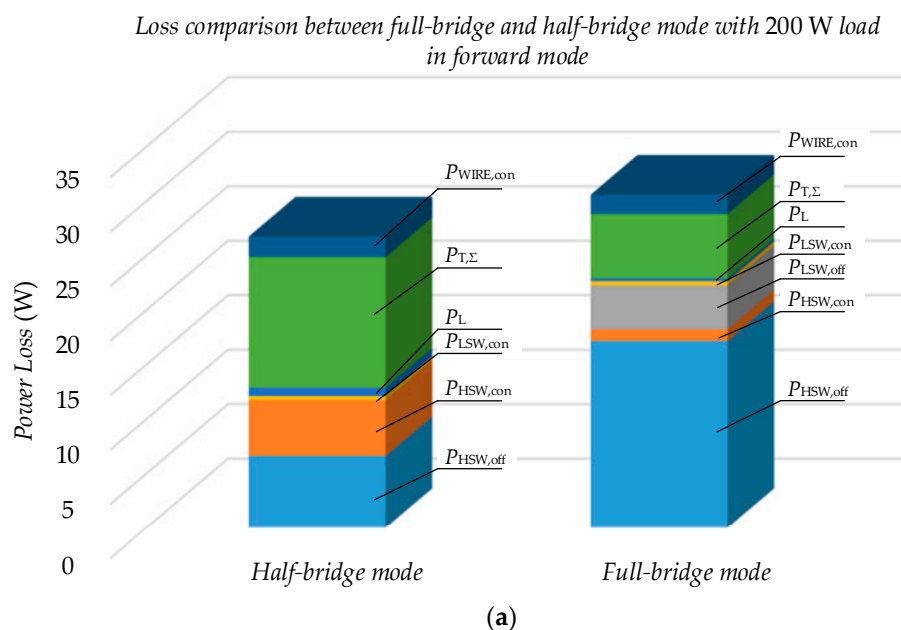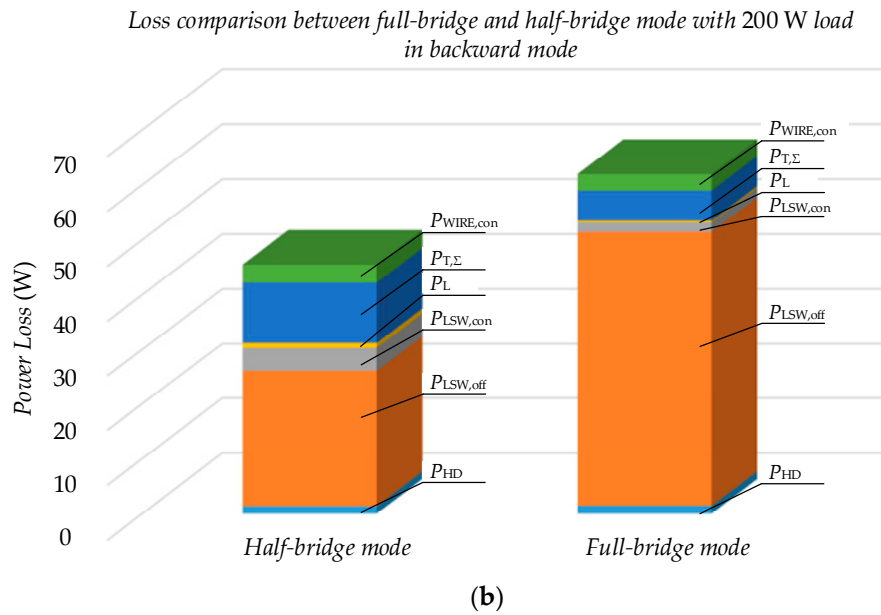

Figure 12. *Cont.*

Loss comparison between full-bridge and half-bridge mode with 200 W load
in backward mode

(b)

Figure 12. The power loss distribution and comparison between full-bridge and half-bridge configuration with 200 W load: (**a**) forward mode; (**b**) backward mode.

5.3. Power Loss Distribution and Comparison with and without Synchronous Strategy

Figure 13 shows the power loss distribution and comparison with and without synchronous strategy. When body diodes of LVS switches are used to realize rectification, P_{LD} is quite large with diode forward voltage of 0.9 V. However, the drain-source on-state resistance of LVS switches is only 0.7 mΩ. Thus, with the use of the proposed synchronous strategy, $P_{LSW,con}$ is quite small. The total loss is cut by 49% with the use of synchronous strategy, showing the advantage in power loss reduction and efficiency enhancement.

Loss comparison with and without synchronous strategy
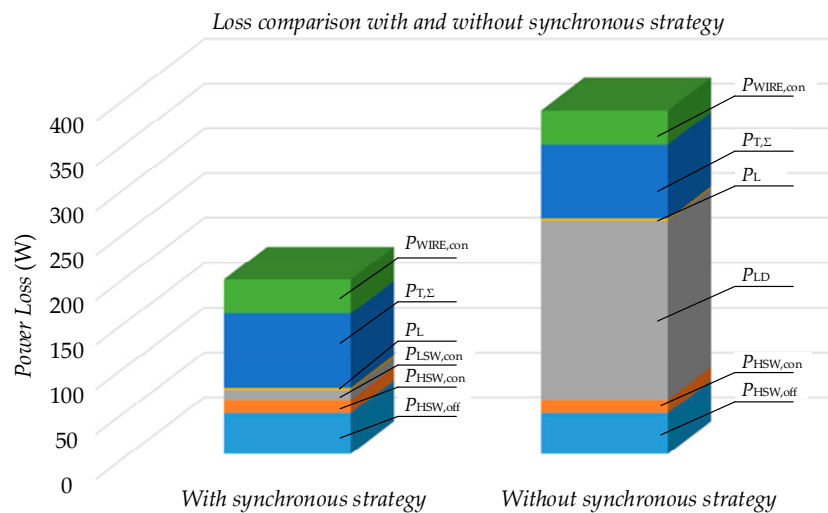
Figure 13. The power loss distribution and comparison with and without synchronous strategy.

6. Experimental Results

A 5 kW prototype is built in the laboratory to verify the above analysis. The parameters of the components are listed in Table 1.

Table 1. Parameters of the converter.

Component	Model/Value
Rated power	5 kW
HVS DC voltage	380–420 V
LVS DC voltage	42–58 V
S_1, S_2, S_3, S_4	C3M0065090D
S_5, S_6, S_7, S_8	4 IPB036N12N3G in parallel
D_1, D_2, D_3, D_4	C3D30065D
L_{m1}	140 μH
n_1	11:1
L_{m2}	875 μH
n_2	20:1
L_r	57 μH
C_{r1}	251 nF
C_{r2}	10 μF
t_{dt_F}	200 ns
t_{dt_B}	200 ns

Figure 14 shows that ZVS of power switches can be realized in both forward and backward modes. In forward mode, the D-S voltage of S_1 decreases to 0, before the driving signal of S_1 comes. In backward mode, the D-S voltage of S_5 decreases to 0, before the driving signal of S_5 comes. The dead time of 200 ns is wide enough for both HVS and LVS power switches, while the efficiency is not greatly reduced.
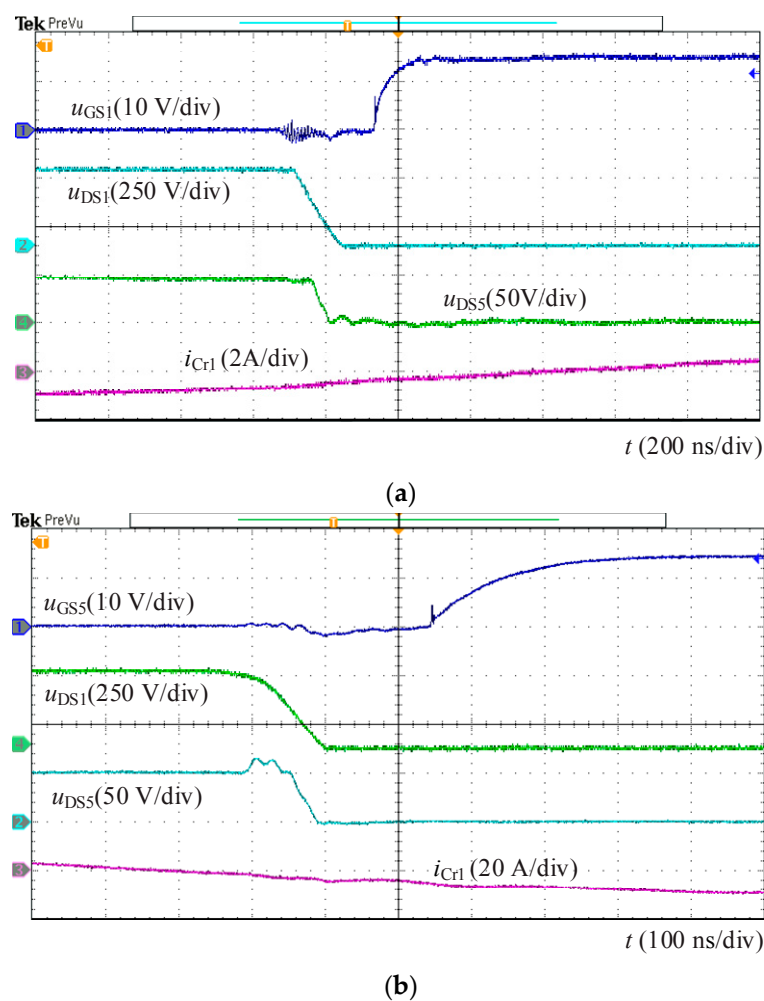

(a)

(b)

Figure 14. Experimental results of ZVS: (**a**) forward mode, 500 W; (**b**) backward mode, 5 kW.

Figure 15 shows experiment results in forward mode. The t_{SR} is 4.6 µs in Figure 15a with working frequency of 60 kHz and load of 3.5 kW. The t_{SR} is 4.5 µs with Equation (25) and 4.3 µs in the proposed synchronous rectification strategy, which is basically consistent with the experiment results. The accuracy of calculation and the effectiveness of proposed synchronous rectification strategy are verified through experiments. Figure 15b shows the waveforms around main resonant frequency. The resonant current is quite close to sinusoidal wave. The power loss is lower because of smaller turn-off loss in this situation.
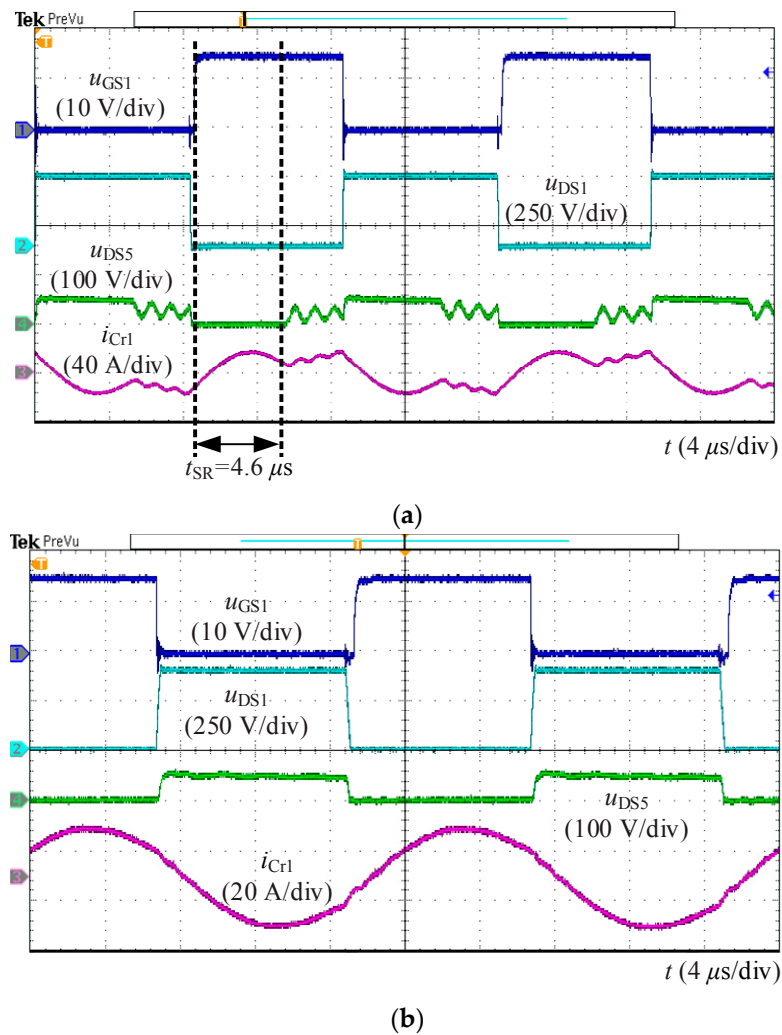
Figure 15. Experimental results in forward mode: (**a**) 60 kHz, 3.5 kW; (**b**) 100 kHz, 5 kW.

Figure 16 shows experiment results in backward mode. In Figure 16a, secondary resonance does not happen, so ZCS of HVS diodes cannot be realized. In Figure 16b, the resonant current is quite close to sinusoidal wave around main resonant frequency. The power loss in Figure 16b is lower because of smaller turn-off loss.
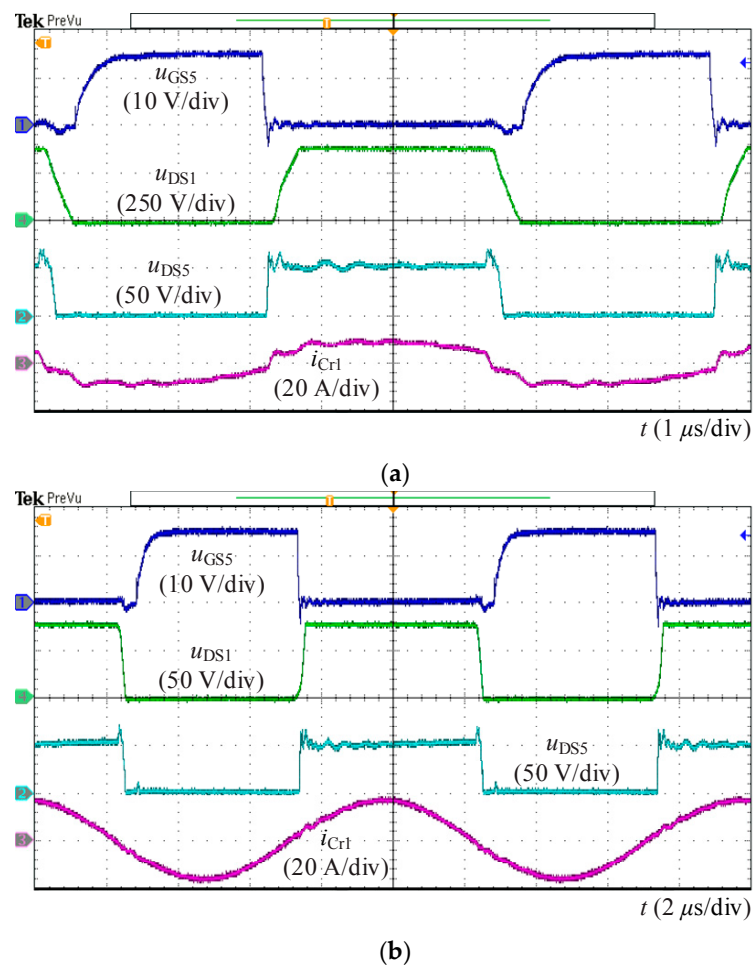
(**a**)

(**b**)

Figure 16. Experimental results in backward mode: (**a**) 160 kHz, 2.5 kW; (**b**) 100 kHz, 5 kW.

Experiments are conducted to verify the effectiveness of half-bridge configuration at light load condition in Figure 17. In both forward and backward mode, the adoption of half-bridge configuration can track a gain of 1.02. Compared to full-bridge, the fall of working frequency in half-bridge configuration reduces turn-off loss, which is very good for efficiency.
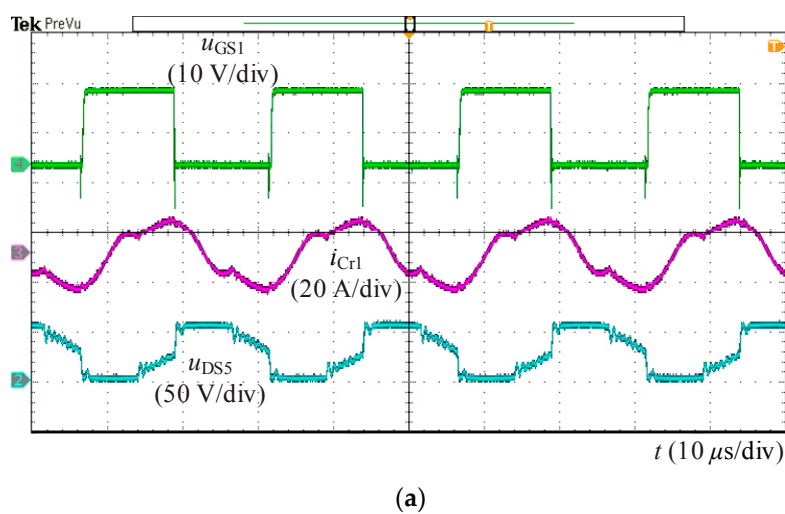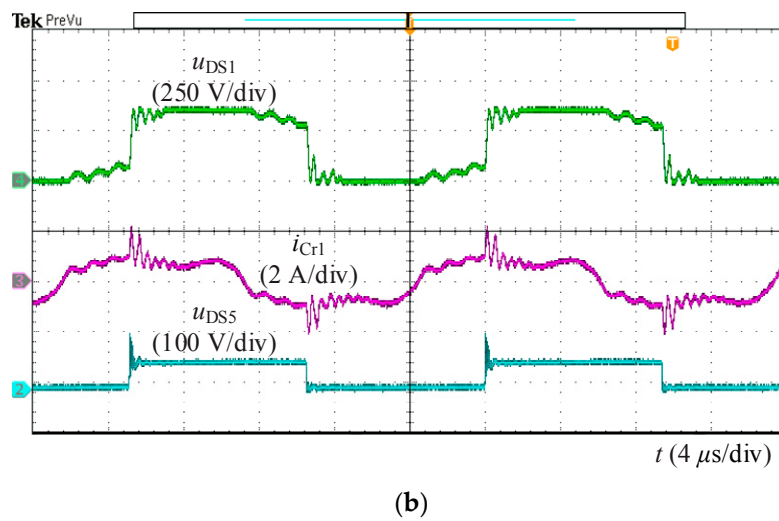

(**a**)

Figure 17. *Cont.*

(b)

Figure 17. Experimental results with half-bridge configuration at light load condition: (**a**) forward mode, 200 W; (**b**) backward mode, 200 W.

Efficiency comparison is conducted with experiments at light load condition. In Table 2, the efficiency in half-bridge configuration is higher than that in full-bridge, which is in accord with analysis in Section 5.2. The advantage of half-bridge configuration is verified through experiments.

Table 2. Efficiency comparison with load of 200 W.

Type	Half-Bridge	Full-Bridge
Forward	87.3%	83.0%
Backward	82.1%	70.9%

Efficiencies of the proposed converter with different loads and LVS DC voltages are measured and plotted in Figure 18. The efficiency with 5 kW load and 50 V LVS DC voltage is 95.9% and 94.9% in forward and backward mode. The maximum efficiency of the converter is 97.0%, with load of 2 kW and LVS DC voltage of 50 V in forward mode. Due to less turn-off currents and lower working frequencies, the efficiency of "58 V" or "50 V" is higher than that of "42 V" in forward mode and the efficiency of "42 V" or "50 V" is higher than that of "58 V" in backward mode. It is in accord with theoretical analysis in Section 5. High efficiency can be achieved in a wide load range. Even with 1 kW load, the efficiency is still over 92% due to the wide ZVS soft switching operation range and little turn-off currents.

The comparative experiments are conducted with and without synchronous rectification strategy when LVS DC voltage is 50 V, displayed as "50 V" and "Diode 50 V". From the converter power loss distribution, the LVS diode conduction loss is the dominant part in "Diode 50 V", which occupies nearly 50% of the total power loss. Experiment results show that the efficiency is improved largely with the help of the proposed synchronous rectification strategy.
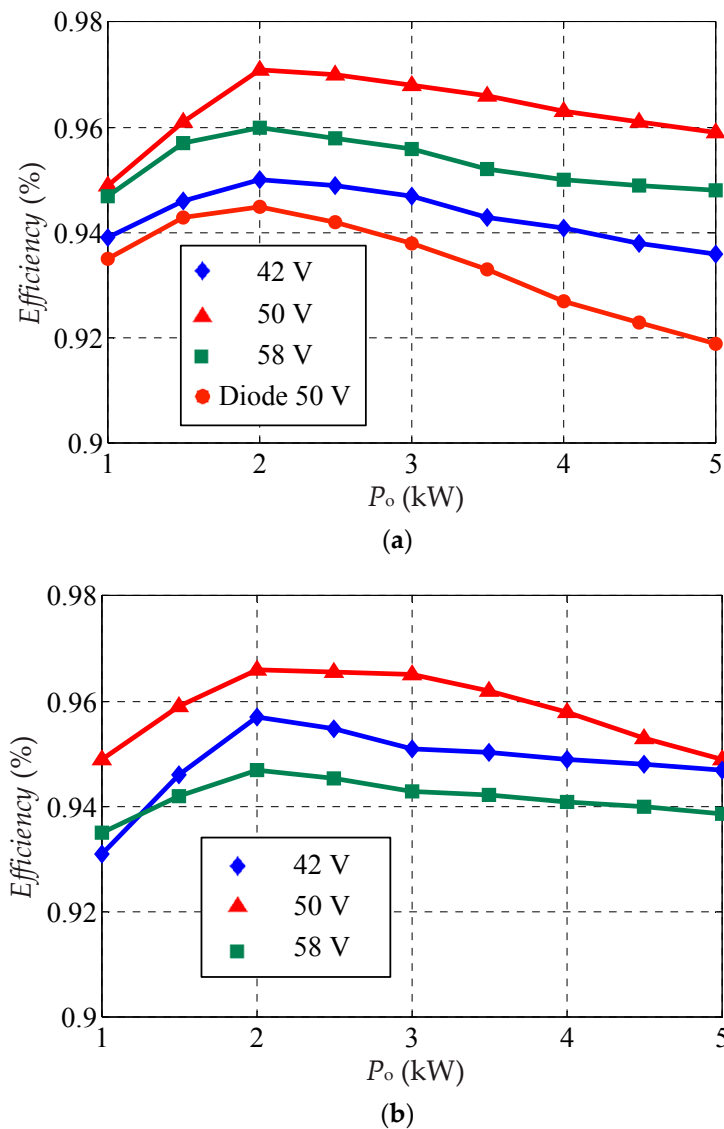
(**a**)

(**b**)

Figure 18. Measured efficiency: (**a**) forward mode; (**b**) backward mode.

7. Conclusions

In this work, a new CLTC multi-resonant DC-DC converter is proposed. Possessing the optimal ZVS + ZCS soft switching feature in all load range, CLTC benefits from little turn-off loss and high efficiency. The gain range is so wide that the demands of applications like battery chargers and DC microgrids can be satisfied easily. The problem of voltage regulation under light load conditions is so serious that voltage is not controllable. The hybrid full-bridge/half-bridge configuration is proposed to make gain curve monotonous under light load conditions. Discussion about voltage and current stresses, load and working frequency range in half-bridge configuration are put forth as well. Besides, a digital synchronous rectification strategy is proposed in forward mode to improve the working efficiency. The turn-on time of LVS switches is set to the same as the HVS switches. The conduction time of LVS switches equals the estimation value of body diodes' conduction time with the lightest load. Simulations verify the accuracy of this estimation. Furthermore, power loss analysis is conducted with different LVS DC voltages in two directions. Power loss is much more when the working frequency is beyond main resonant frequency, because of high conduction losses and turn-off losses. Efficiency with a half-bridge configuration is a little higher than that with full-bridge configuration in both directions, due to less turn-off losses. The loss is cut by 49% with the use of a synchronous strategy, showing

the advantage in improving efficiency. At last, experiments are conducted to validate the theoretical analysis above. ZVS feature, the effectiveness of hybrid full-bridge/half-bridge configuration, and the validity of proposed digital synchronous rectification strategy are all verified through experiments. With the help of ZVS + ZCS feature, high efficiency can be harvested in a wide load range. The full load efficiency is 95.9% in forward mode and 94.9% in backward mode with LVS DC voltage of 50 V. The maximum efficiency is 97.0% with a LVS DC voltage of 50 V and load of 2 kW.

Author Contributions: Shu-huai Zhang, Yi-feng Wang, Bo Chen designed the main parts of the study, including hybrid full-bridge/half-bridge configuration, synchronous rectification strategy loss model, power loss analysis and experiments. Yi-feng Wang is also responsible for writing and revising the paper. Fu-qiang Han and Qing-cui Wang helped in the hardware development.

Conflicts of Interest: The authors declare no conflict of interest.

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