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High Gain Boost Interleaved Converters with Coupled Inductors and with Demagnetizing Circuits

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Abstract: This paper proposes double interleaved boost converters with high voltage gain and with magnetically coupled inductors, while a third coupled winding is used for magnetic flux reset of the core during converter operation. The topology of the proposal is simple, it does not require many additional components compared to standard interleaved topologies, and it improves the transfer characteristics, as well as system efficiency even for high power levels. The investigation of steady-state operation was undertaken. It was discovered that the proposed converter can be designed for a target application where very high voltage gain is required, while adjustment of voltage gain value can be done through duty-cycle variation or by the turns-ratio modification between individual coils. The 1 kW prototype was designed to test the theoretical analysis. The results demonstrate that the proposed converter achieves very high voltage gain (1:8), while for the designed prototype the peak efficiency reaches >96% even when two additional diodes and one winding were implemented within the converter's main circuit. The dependency of the output voltage stiffness on load change is minimal. Thus, the presented converter might be a proper solution for applications where tight constant DC-bus voltage is required (a DC-DC converter for inverters).

Keywords: interleaved boost converter; magnetically coupled inductors; demagnetizing circuit

1. Introduction

Current trends in automotive applications are characterized by a common rule—green energy, or blue energy. More and more non-conventional energy systems and powered electronic systems are used within the internal infrastructure of vehicles, whose energy storage and conversion systems are still transforming and being optimized as electric vehicles are being considered. The main reasons are efficiency, reliability and power density. Worth mentioning are energy storage systems, drive systems, fuel cells, solar panels, electronic devices for energy conversion etc. Most of the green energy systems are of low output voltage. If practical use of such devices is required or requested, then a proper conversion system must be used, i.e., low voltage energy source must be boosted to the values that are necessary for other electronic devices (power inverter and electric machine for example). For application within a power train of electric vehicles it is required to boost 80 V_{DC}/120 V_{DC} to the values that are required for electric driving, i.e., 400 V_{DC}. Therefore, a boost converter must be used.

Conventional boost converters have limits that are related to voltage gain, power capability and efficiency. In other words, when high voltage gain is required, the converter may operate at an unacceptable duty cycle, which results in a very high voltage stress of devices, and conversion loss of the circuit will ensue. For that reason, perspective topological modification has been made. Most of the proposals are focused on the optimization of the voltage gain ratio in the pursuit of duty cycle improvement [1–5]. Many single-stage high voltage gain converters have been developed [6–10] with

switched capacitors [11–16]. Interleaved topologies with coupled inductors [17–22] or with voltage lift techniques have been proposed [23–25]. However, there still exist several disadvantages that might be further optimized in order to improve the electrical behavior at the power stage, which deal with power limit when interleaved topology is considered, while voltage gain is limited at high powers because of the conduction losses of the circuit, which increase by an extreme amount at high power levels together with losses of magnetic material, which are also a limiting factor when saturation or DC biasing comes into account [26–30]. Almost magnetic components are very important parameters, and attention must be paid for perspective proposals when interleaved boost topology is considered. The inductors of interleaved boost converters, which are magnetically coupled, are continuously saturated by DC current components. The variable that is the most negatively affected in this case is efficiency.

This paper proposes a double interleaved boost converter with high voltage gain and with magnetically coupled inductors, while a third coupled winding is used for magnetic flux reset of the core during the converter operation as well as for the voltage gain adjustment. The topology of the proposal is simple, it does not require many additional components compared to standard interleaved topologies [31–35] and it improves the transfer characteristics, as well as system efficiency even for high power levels [36]. With its superior behavior related to the output voltage stiffness in dependency on load change, it might be a proper solution for applications where constant DC-bus voltage is required (DC-DC converter for inverters). The main focus within this paper is given to the steady state analysis, voltage transfer characteristic derivation, magnetic component stress reduction and system efficiency identification.

2. Dual Interleaved Boost Converter with Magnetically Coupled Inductors and with Demagnetizing Circuit

Figure 1 shows the dual interleaved DC-DC boost converter with magnetically coupled inductors. Analysis of the DC-DC converter (Figure 1) is primarily done under operation in the CCM mode, so that the currents i_1 and i_2 are always positive. The advantages of CCM operation against DCM operation include the minimization of circuit ringing, inductor and input ripple current reduction, and voltage ripple effects elimination as well as elimination of their associated mitigation. Waveforms from steady state operation of dual interleaved boost converters for CCM operation with a duty ratio greater than 0.5 (while duty cycle of T_1 and T_2 is equal), are shown in Figure 2. It shows input current (i_{IN}), inductor voltages (V_1, V_2), inductor currents (i_1, i_2), and T_1 and T_2 gate drives. For CCM operation, the voltage gain is the same as that given for a simple boost converter described by (1).

$$V_{OUT} = V_{IN} \times \frac{1}{(1-D)} \tag{1}$$

where V_{OUT} is output voltage of the converter, V_{IN} is input supply voltage and D is the duty cycle.

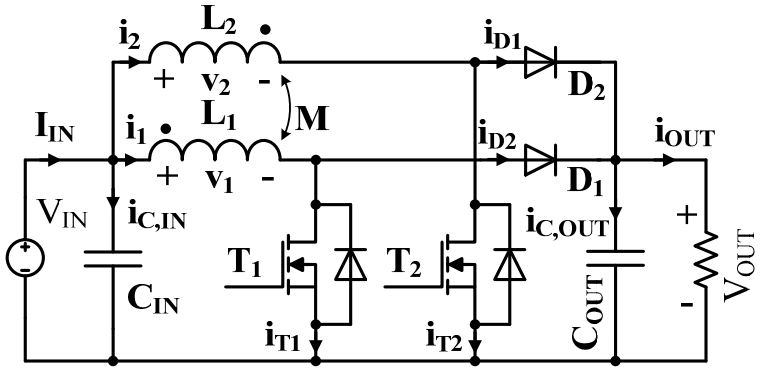

Figure 1. Standard dual interleaved boost converter with coupled inductors.

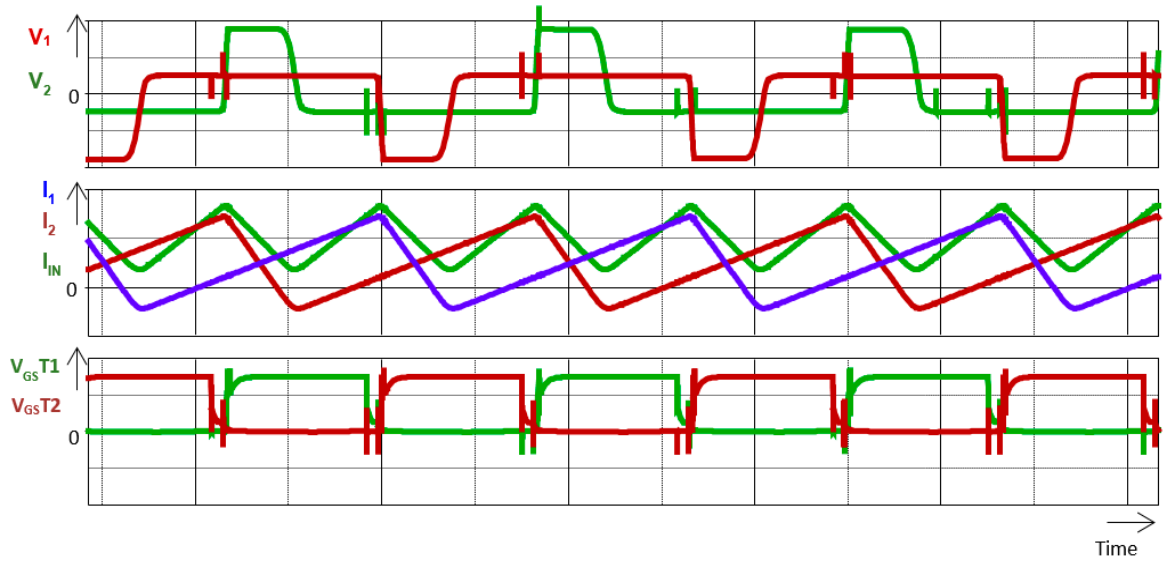

Figure 2. Operational waveforms of a dual interleaved boost converter with coupled inductors during CCM operation.

It is observed that the voltage gain is primarily dependent on the duty cycle of the converter operation.

The standard solution to dual interleaved boost converters with magnetically coupled inductors has its advantages compared to the classic boost converter. They apply even when higher power demands are given on the power stage. Instead of that, reduction of voltage and current ripple enable a reduction in passive components, even when a high switching operation is considered. However, on the other side, some disadvantages arise and are related to the voltage gain and magnetic design and operation of coupled inductors. During each operating cycle, the DC component of the current of each winding (L_1 and L_2) exists. This limits the magnetic component to be used for higher power, and bulky magnetic core or special geometry modifications must be used in order to prevent saturation of the magnetic core. In the same way, the efficiency is affected and can be decreased when wrong magnetic design is performed.

The proposed interleaved boost converter with magnetically coupled inductors and with demagnetizing circuit is shown in Figure 3. It is composed of a standard double interleaved boost converter (Figure 1), where a demagnetizing circuit, which consists of L_3-D_4-D_2 is added to the output part of the proposed converter. This demagnetizing circuit also creates an additional pseudo transformer within the proposed converter circuit, and as will be seen later, the ratio between boost inductances (L_1, L_2) and demagnetizing inductance (L_3) influences the voltage gain. The proposed converter is voltage gain independent on the duty cycle operation in wide operational range, and thus constant output voltage within wide range of output load can be achieved.

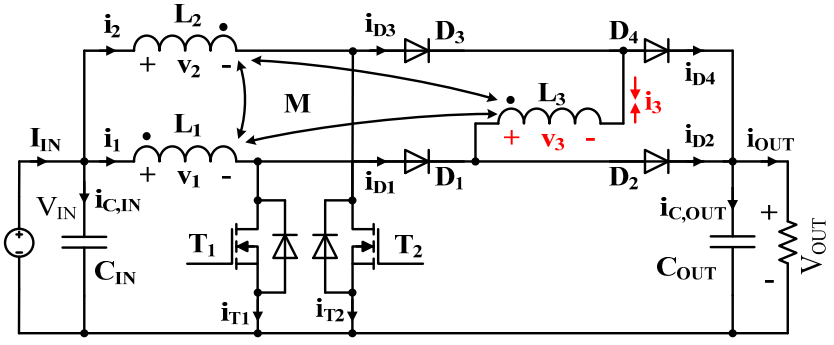

Figure 3. Proposed dual interleaved boost converter with coupled inductors and demagnetizing circuit.

The switching operation is similar to the standard interleaved converter, i.e., transistors T_1 and T_2 are switching in an interleaved manner with given dead time. Inductor L_3 is magnetically coupled altogether with L_1 and L_2 and serves as a demagnetizing snubber whose effect applies during each switching action of each transistor. In this configuration, it servers as an AC magnetic flux reset inductor. The current flow I_3 during each operation cycle is opposed to the current of inductors L_1 and L_2. This enables a reduction in the magnetic core saturation, thus the DC component of the inductor currents can be eliminated.

3. Operational Analysis of Proposed Converter

The operation of the dual interleaved boost converter with magnetically coupled inductors and with demagnetizing circuits can be divided into four operational intervals. One switching cycle can be then understood as in an ON and OFF state after consequent switching of transistors T_1 and T_2. Thus, 2 active and 2 passive intervals exist. For initial investigation of converter operation it can be assumed that the duration of active interval will be equal to the duration of the passive interval. The switching driving signals for this situation are shown in Figure 4. It is also considered that the turns ratio between individual coils is equal to 1:1:1, so all inductors have the same value. The operational waveforms for analyzed steady state are shown on Figure 5.

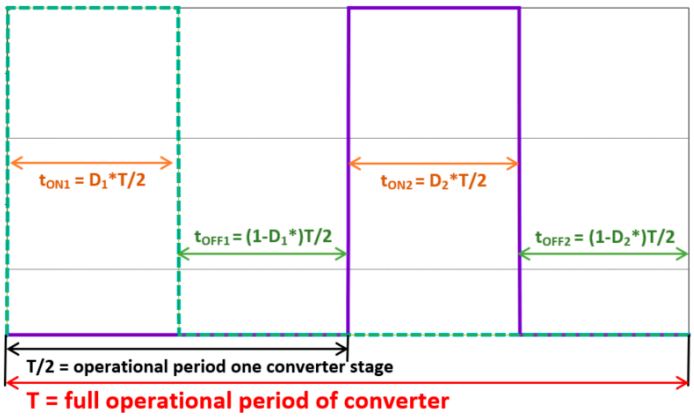

Figure 4. Driving impulses of transistors T_1 and T_2.

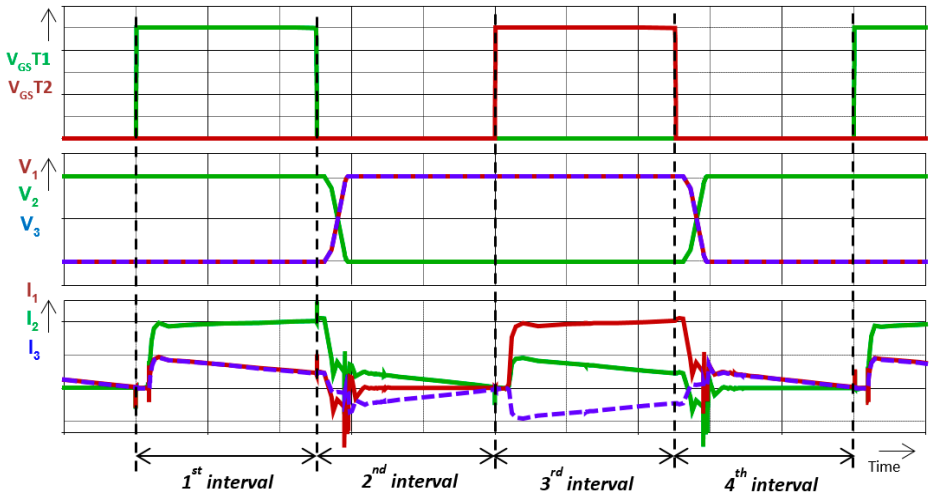

Figure 5. Operational waveforms for analyzed steady state of proposed converter—nominal load (**top**: driving signals, **middle**: voltages on inductors, **bottom**: inductor currents).

3.1. Working Intervals of Proposed Converter

The operation of the converter can be divided into four consecutive intervals, which periodically repeat. The initial analysis of the operation is done for the conditions where $L_1 = L_2 = L_3 = L$, and $M_1 = M_2 = M_3 = M$. The operation of the converter shall be considered within steady-state operation.

3.1.1. Interval (Active—T_1—ON, T_2—OFF)

Initial conditions:

- T_1—ON,
- T_2—OFF (the transistor T_2 was before this interval in conduction state, thus L_2 is accumulated with the energy),
- D_2, D_3—conducting,
- L_1 is accumulating the energy,
- L_2 and L_3 are transferring energy into output capacitor C_{OUT} and to the load R_L.

This interval (Figure 6) starts after turn-on of T_1, while its ON-period is equal to the half of the half period cycle, i.e., $t_{ON1} = D_1 \times T/2$, whereby $D_1 = 0.25$. The current in the inductor L_1 linearly rises, while the current in the inductors L_2 and L_3 is linearly decreasing and is half the value of current i_1. The voltage on the coil L_1 is the opposite polarity to the voltages on inductors L_2 and L_3. Using Kirchhoff's second law, it is possible to derive dependency of the output voltage on the inductor voltages. For the first-time interval of the converter's operation, the following equations are valid:

$$V_{IN} = V_1 = L\frac{di_1}{dt} - 2M\frac{di_2}{dt} \tag{2}$$

$$\frac{di_1}{dt} = \frac{V_{IN}}{L} + \frac{2M}{L}\frac{di_2}{dt} \tag{3}$$

$$\frac{di_2}{dt} = \frac{L}{2M}\frac{di_1}{dt} - \frac{V_{IN}}{2M} \tag{4}$$

$$V_{IN} + V_2 + V_3 = V_{OUT} \tag{5}$$

$$V_{IN} + L\frac{di_2}{dt} + M\frac{di_2}{dt} - M\frac{di_1}{dt} + L\frac{di_2}{dt} + M\frac{di_2}{dt} - M\frac{di_1}{dt} = V_{OUT} \tag{6}$$

$$V_{IN} + (2L + 2M)\frac{di_2}{dt} - 2M\frac{di_1}{dt} = V_{OUT} \tag{7}$$

$$\frac{di_1}{dt} = \frac{1}{2M}\left[V_{IN} - V_{OUT} + (2L + 2M)\frac{di_2}{dt}\right] \tag{8}$$

$$\frac{di_2}{dt} = \frac{1}{(2L + 2M)}\left(V_{OUT} - V_{IN} + 2M\frac{di_1}{dt}\right) \tag{9}$$

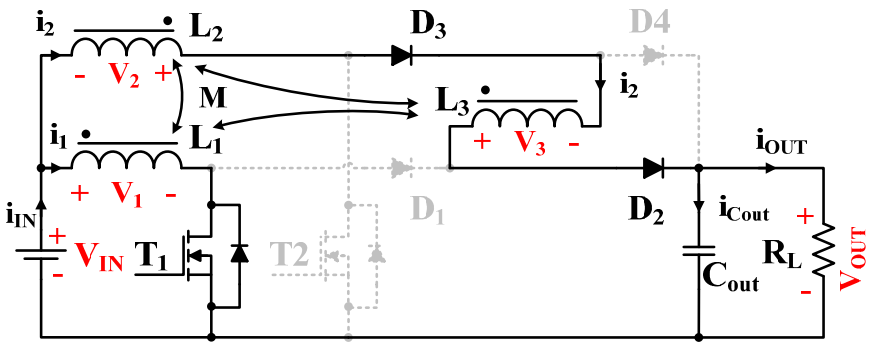

Figure 6. Equivalent circuit of proposed converter operation during 1st interval.

3.1.2. Interval (Passive—T_1—OFF, T_2—OFF)

Initial conditions:

- T_1—OFF,
- T_2—OFF,
- D_1, D_4—conducting,
- L_1 and L_3 are transferring energy into output capacitor C_{OUT} and to the load R_L.

This interval (Figure 7) begins after the transistor T_1 turns off. Duration of this interval is $t_{OFF1} = (1 - D_1) \times T/2$. This causes the polarity of the voltages on each inductor to change its polarity to the opposite value compared to the first interval. During this time interval, the current of inductor L_2 is equal to zero, because it is not connected to the main circuit. The current of the inductor L_1 flows also through the inductor L_3, while inductor L_1 acts as the source, thus its i_1 is linearly decreasing, whereby i_3 is linearly increasing. This interval can be characterized by the demagnetizing action of the common magnetic core, because inductor L_3 is acting in the opposite direction to the inductor L_1. It might be seen that within 1st and 2nd interval of the operation, the AC current is flowing through the L_3. The equation of the loop voltages within the main circuit during this time interval is given by (10), while the output voltage is defined by (11).

$$V_{IN} + V_1 + V_3 = V_{OUT} \tag{10}$$

$$V_{IN} + L\frac{di_1}{dt} + M\frac{di_1}{dt} + L\frac{di_1}{dt} + M\frac{di_1}{dt} = V_{OUT} \tag{11}$$

$$V_{IN} + (2L + 2M)\frac{di_1}{dt} = V_{OUT} \tag{12}$$

$$\frac{di_1}{dt} = \frac{1}{(2L + 2M)}(V_{OUT} - V_{IN}) \tag{13}$$

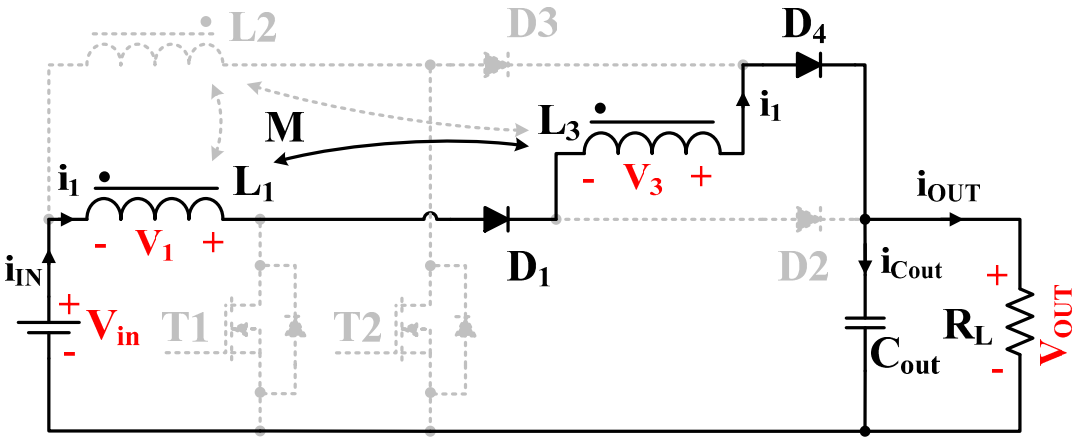

Figure 7. Equivalent circuit of proposed converter operation during 2nd interval.

3.1.3. Interval (Active—T_1—OFF, T_2—ON)

Initial conditions:

- T_2—ON,
- T_1—OFF,
- D_1, D_4—conducting,
- L_2 is accumulating the energy,
- L_1 and L_3 are transferring energy into output capacitor C_{OUT} and to the load R_L.

The third (Figure 8) interval is again the active interval, and its initialization is characterized by the turn on of the transistor T_2, while transistor T_1 is still turned off. This interval has the same ON period as the first one, i.e., $t_{ON2} = D_2 \times T/2$, where $D_2 = 0.25$. The polarity of the inductor voltages is unchanged compared to 2nd interval. Because direction of the current flow in L_3 is unchanged, and its current is linearly increasing from negative values, inductor L_1 is continuously acting as the voltage source, thus its current is linearly decreasing with the same slope as current i_3 rises. Inductor L_2 is being charged as in the case of standard boost converter. It is seen that the 3rd operational interval is similar to the 1st interval, while the only difference is the polarity and behavior of current i_3. Therefore based on the loop voltages, the equation for this time interval is given by (14), and consequently dependency of the output voltage is given by (18).

$$V_{IN} = V_2 = L\frac{di_2}{dt} - 2M\frac{di_1}{dt} \tag{14}$$

$$\frac{di_1}{dt} = \frac{L}{2M}\frac{di_2}{dt} - \frac{V_{IN}}{2M} \tag{15}$$

$$\frac{di_2}{dt} = \frac{V_{IN}}{L} + \frac{2M}{L}\frac{di_1}{dt} \tag{16}$$

$$V_{IN} + V_1 + V_3 = V_{OUT} \tag{17}$$

$$V_{IN} + L\frac{di_1}{dt} + M\frac{di_1}{dt} - M\frac{di_2}{dt} + L\frac{di_1}{dt} + M\frac{di_1}{dt} - M\frac{di_2}{dt} = V_{OUT} \tag{18}$$

$$V_{IN} + (2L + 2M)\frac{di_1}{dt} - 2M\frac{di_2}{dt} = V_{OUT} \tag{19}$$

$$\frac{di_1}{dt} = \frac{1}{(2L + 2M)} \tag{20}$$

$$\frac{di_2}{dt} = \frac{1}{2M}\left[V_{IN} - V_{OUT} + (2L + 2M)\frac{di_1}{dt}\right] \tag{21}$$

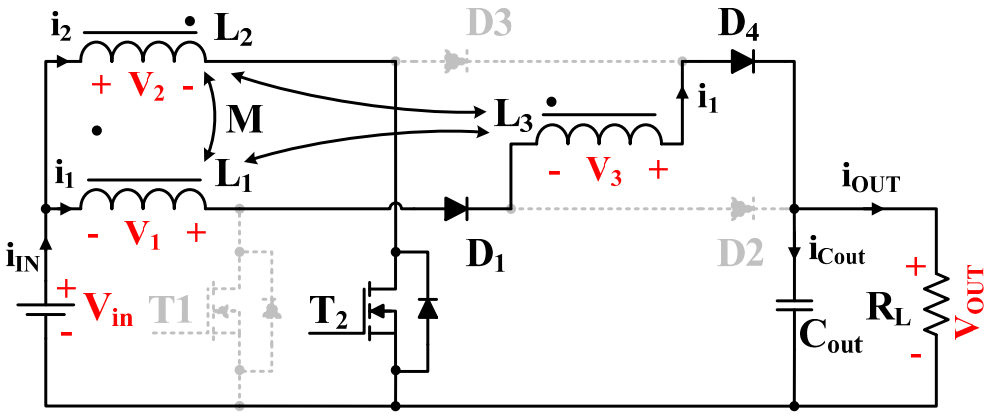

Figure 8. Equivalent circuit of proposed converter operation during 3rd interval.

3.1.4. Interval (Passive—T_1—OFF, T_2—OFF)

Initial conditions:

- T_1—OFF,
- T_2—OFF,
- D_2, D_3—conducting,
- L_2 and L_3 are transferring energy into output capacitor C_{OUT} and to the load R_L.

The 4th interval (Figure 9) is a passive interval and from the operational point of view it is again comparable to the 2nd interval of the converter's operation, thus duration is $t_{OFF2} = (1 - D_2) \times T/2$. Start of the interval is characterized by the turn-off action of transistor T_2; transistor T_1 is still in non-conductive state. The voltages on each inductor change their polarity compared to previous operational interval, thus inductors L_2 and L_3 are now acting as sources so their currents are linearly decreasing with the same ratio. Inductor L_2 is disconnected from the main circuit during this time interval, thus its current is equal to zero. The equation for final operational interval with steady state operation is given by (22). Dependency of the output voltage is given by (23).

$$V_{IN} + V_2 + V_3 = V_{OUT} \tag{22}$$

$$V_{IN} + L\frac{di_2}{dt} + M\frac{di_2}{dt} + L\frac{di_2}{dt} + M\frac{di_2}{dt} = V_{OUT} \tag{23}$$

$$V_{IN} + (2L + 2M)\frac{di_2}{dt} = V_{OUT} \tag{24}$$

$$\frac{di_2}{dt} = \frac{1}{(2L + 2M)}(V_{OUT} - V_{IN}) \tag{25}$$

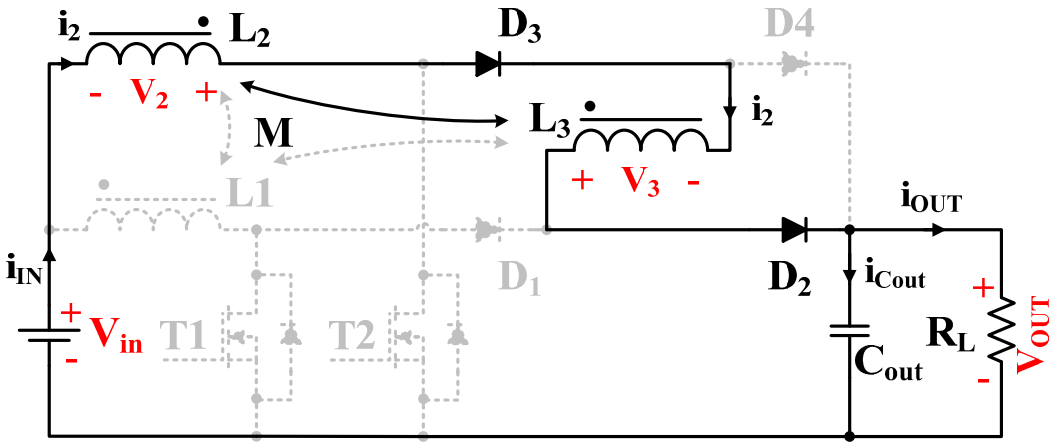

Figure 9. Equivalent circuit of proposed converter operation during 4th interval.

Based on the previous analysis, it is seen that the proposed converter has advantages related to the voltage gain, which is dependent on the duty cycle of the converter. Instead of that, the converter is able to operate in a wide range of load, while output voltage is not affected and the only voltage decrease of V_{OUT} is caused by the voltage drop on the individual parasitic components. Voltage ratio between V_{IN} and V_{OUT} can also be adjusted by the ratio between number of turns of the boost inductances ($N_1 = N_2$), and number of turns of AC demagnetizing inductance. The process of the determination of the turns ratio between individual inductances (L_1–L_3) is determined by the requirements of the converter operation, i.e., CCM, DCM, BCM mode. Therefore the inductances L_1 and L_2 are selected based on the standard procedure for interleaved converter [19,20,22]. The value of the L_3 inductance is then determined by the requirements on the voltage gain of the converter. Table 1 shows voltage gain of the proposed converter for pre-defined multiples of the turns of inductances. It is the voltage gain related to the change of inductance ratio, while duty cycle is considered to be within the previous analysis, i.e., $D_1 = D_2 = 0.5$.

Table 1. Dependency of voltage gain on the inductance ratio.

Turn's Ratio (TR) $N_1 = N_2 = N_{BOOST}$: AC Inductor N_3	V_{OUT}/V_{IN} (Voltage Gain)
4:1	2.2
3:1	2.3
2:1	2.5
1:1	3
1:2	4
1:3	5
1:4	6

3.2. Loss Distribution Analysis

Energy losses in elements of the boost converter can be divided into inductor losses, power switch losses and diode losses [37–40]. Total energy losses P_{TOT} is expressed as:

$$P_{TOT} = P_L + P_T + P_D \tag{26}$$

3.2.1. Inductor Losses

The estimation of the inductor losses is basically the same as that of the transformers. The conduction losses P_{LCON} are:

$$P_{LCON} = R_L I_L^2 \tag{27}$$

where R_L is serial resistance and I_L is current of L.

The core losses (Steinmetz equation) P_{LMAG} are:

$$P_{LMAG} = V_{CORE} k f_{SW}^{\alpha_{CORE}} \Delta B_L^{\beta_{CORE}} \tag{28}$$

where V_{CORE} is the volume of the magnetic core, ΔB_L is the flux swing, f_{SW} is switching frequency, k, α_{CORE}, β_{CORE} are the Steinmetz coefficients, which are provided by the manufacturer.

Then the losses of inductor are attained as:

$$P_L = \sum P_{LCON} + \sum P_{LMAG} \tag{29}$$

3.2.2. Power Switch Losses

The losses of power switches mainly comprise the switching loss, conduction loss free-wheeling diode loss and the drive loss. The switching losses P_{TSW} are:

$$P_{TSW} = (E_{TON} + E_{ToFF}) f_{SW} \tag{30}$$

where E_{TON}, E_{TOFF} are MOSFET turn-on and switch-off energy.

The conduction losses P_{TCON} are:

$$P_{TCON} = R_{DSON} I_T^2 \tag{31}$$

where R_{DSON} is on-state resistance and I_T is current of power switch.

The free-wheeling diode losses P_{TFWD} are:

$$P_{TFWD} = v_{D0} I_{FAV} + R_D I_{FRMS}^2 + E_{DON} f_{SW} \tag{32}$$

where v_{D0} is diode on-state zero-current voltage, I_{FAV} is average diode current, R_D is diode on-state resistance, I_{FRMS} is RMS value of the diode current, E_{DON} is diode energy during MOSFET switch-on transient.

The drive losses P_{TDRI} are:

$$P_{TDRI} = Q_{GD} V_G f_{SW} \tag{33}$$

where Q_{GD} is storage charge between the gate and drain, V_G is gate voltage.

Then the losses of power switch are attained as:

$$P_T = \sum P_{TSW} + \sum P_{TCON} + \sum P_{TDRI} + \sum P_{TFWD} \tag{34}$$

3.2.3. Diode Losses

The diode losses only contain the switching loss and conduction loss. The switching losses PDSW are:

$$P_{DSW} = V_R I_R \frac{t_{OFF}}{T} + E_{RR} f_{SW} \tag{35}$$

where V_R is diode applied voltage, I_R is diode reverse current, T is switching period, t_{OFF} is diode off-time, E_{RR} is switching energy loss due to reverse recovery.

The conduction losses P_{DCON} are:

$$P_{DCON} = V_F I_F \frac{t_{ON}}{T} \tag{36}$$

where V_F is diode forward voltage, I_F is diode forward current, t_{ON} is diode on-time.

Then the diode losses are attained as:

$$P_D = \sum P_{DSW} + \sum P_{DCON} \tag{37}$$

Based on the circuit parameters and circuit components, the determination of individual losses can be realized (Table 2). These losses are valid for 1 kW output power of the proposed converter, supplied from 100 V_{DC}, voltage gain equal to 3.6, with operating frequency 100 kHz.

Table 2. Values of power losses on the individual components (Computation).

Component	Power Loss (W)
Inductor L_1–L_3	3.71
Transistors	25.71
Diodes	9.1
Other—parasitic leads etc.	2

4. Simulation and Experimental Analysis of the Steady-State Operation

Initial investigation the analysis of the steady state operation is provided, in order to validate operational characteristics of the converter. In this study, these are related to the output characteristic (dependency of output voltage on the output power at constant duty cycle), efficiency characteristic (dependency of system efficiency on the output power at constant duty cycle), and voltage gain characteristic, i.e., dependency of the output voltage on the duty cycle at various output powers. Finally, the analysis of the voltage gain characteristic on the inductance ratio was performed, while the duty cycle is constant. The input-output condition of the simulation as well as of the experimental measurement are defined as follows, whereby OrCAD–Pspice was used for simulation analysis:

- *V_{IN} = 100 V*
- *Switching frequency (f_{SW}) = 100 kHz*
- *V_{OUT} = expected based on voltage gain = 400 V*
- *P_{OUT} = 1 kW (2.5 A)*
- *Duty cycle = D_1 = D_2 = range 0.1–0.45*
- *Voltage gain = 3.6 (N_1 = N_2 = 6, N_3 =10 $\geq$ TR = 1:1.7)*

- *Inductor core = feroxcube EI43/3F3 planar*
- *Power transistors = Cree C3M0065100K*
- *Power diodes = STPSC1206D*
- *Input capacitors = 3 × 390 µF/160 V SAMWHA*
- *Output capacitors = 4 × 22 µF/450 V Wurth Electronic*

The experimental prototype of the proposed converter is shown on Figure 10. The four-layer PCB was used for power stage. Control stage is realized with the universal board equipped by MCU, in order to provide various experiments related to the investigation of the steady-state performance. The integrated interleaved magnetics is equipped within planar technology, whereby EI E43 3F3 planar core was used.

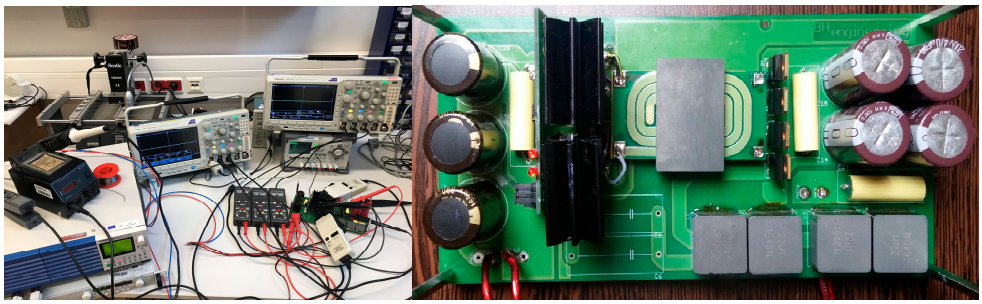

Figure 10. Measurement set-up (**left**) and experimental sample (**right**) of the proposed converter designed for 1 kW peak of output power.

4.1. Steady State Operation—Principal Waveforms

Initial experiments were performed in order to investigate the operational waveforms on the individual main components of the proposed converter within steady-state operation. Comparisons between simulation and measurements are given. Figures 11 and 12 show current waveforms of individual inductors. It is seen that the current of the boost inductors L_1 and L_2 has DC offset and is of DC character. This fact may saturate the core of the inductor because of the existence of the DC component, but as can be seen, current through the reset inductor L_3 is a product of the current i_2 and i_1 and has AC character. Therefore the core of the proposed converter will not be saturated by the DC component, which is beneficial because a lower volume of the inductive component can be used, or higher power at the same size can be delivered considering an alternate interleaved converter.

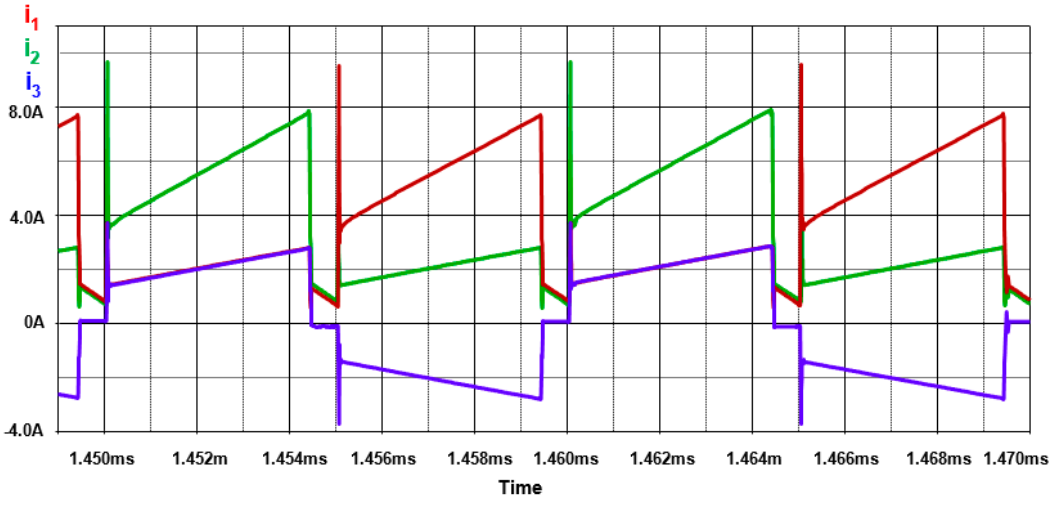

Figure 11. Current waveforms of the inductors L_1–L_3 (100% of output power)—Simulation.

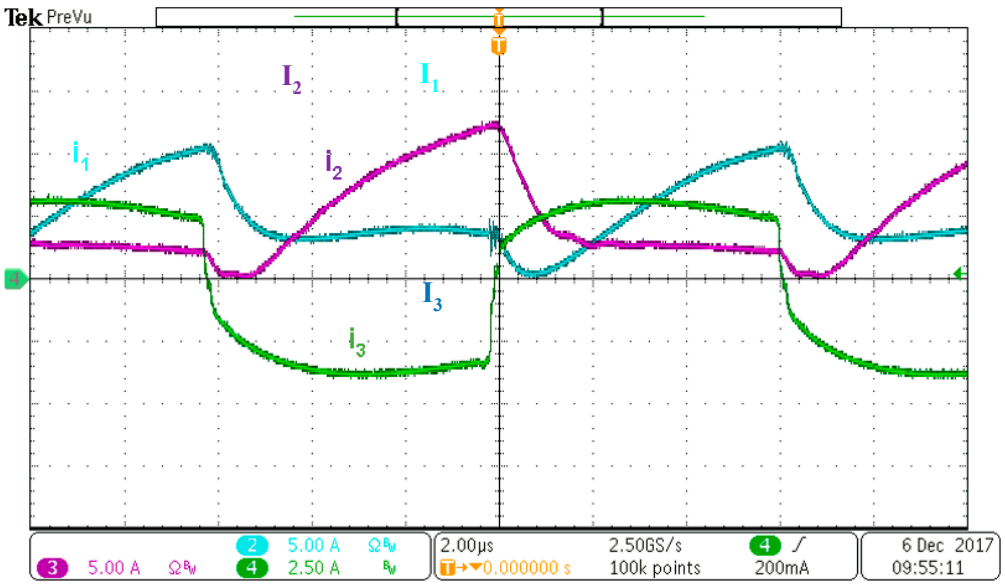

Figure 12. Current waveforms of the inductors L_1–L_3 (100% of output power)—Measurement.

Figures 13 and 14 show the voltage waveforms on the individual inductances. It is seen again that the voltage on the L_3 is of different amplitude compared to the both voltage waveforms on the L_1 and L_2. This is relevant to the voltage gain modification through the turn ratio. In this case, it was set to 10:6, thus the voltage on the inductance L_3 shall be 1.6 times higher the voltages on the inductances L_1 and L_2, whose amplitude is equal to the amplitude of the supply voltage. This is confirmed both by the simulation and by the measurement.

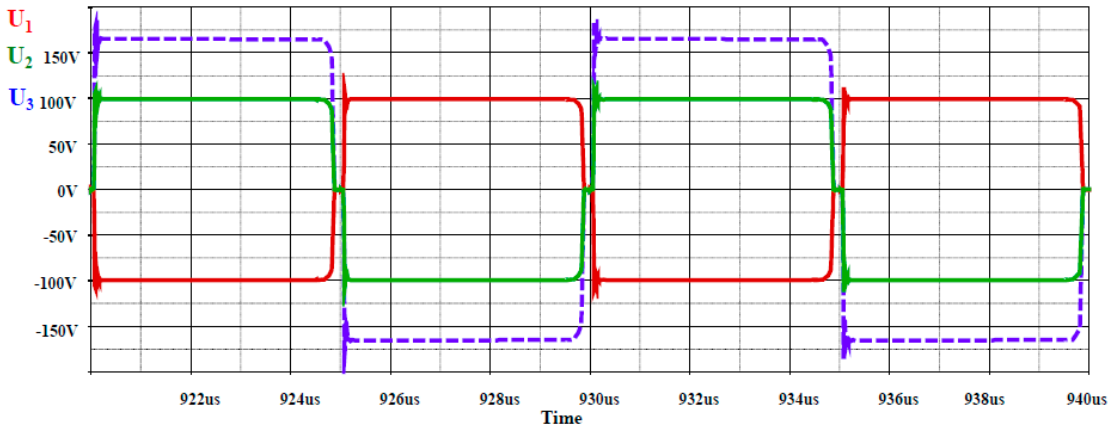

Figure 13. Voltage waveforms on the inductors L_1–L_3 (100% of output power)—Simulation.

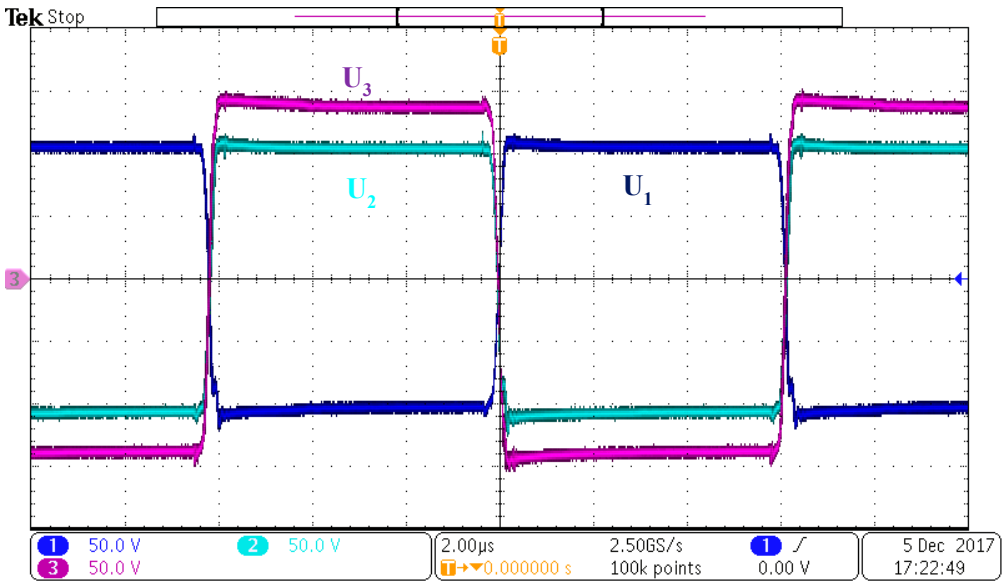

Figure 14. Voltage waveforms on the inductors L_1–L_3 (100% of output power)—Measurement.

Figures 15–18 show current and voltage waveforms of the semiconductor devices. The converter is operating in the hard-switching mode, while waveforms are relevant to the basic operational characteristics of the boost converter. Thus, switching losses will be the most important part of the losses affecting the system efficiency. For that purpose, the proper selection of semiconductor devices will be important, or implementation of the soft switching technique shall also be considered.

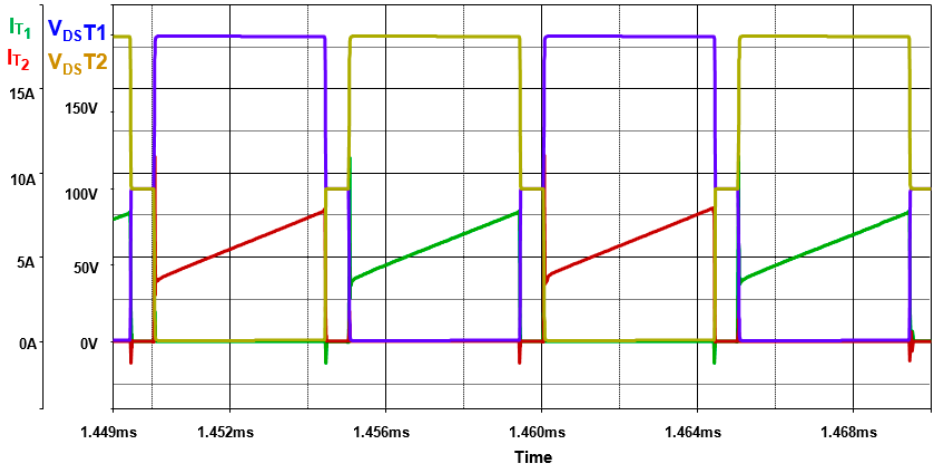

Figure 15. Voltage and current waveforms of the power transistors T_1, T_2 (100% of output power)—simulation.

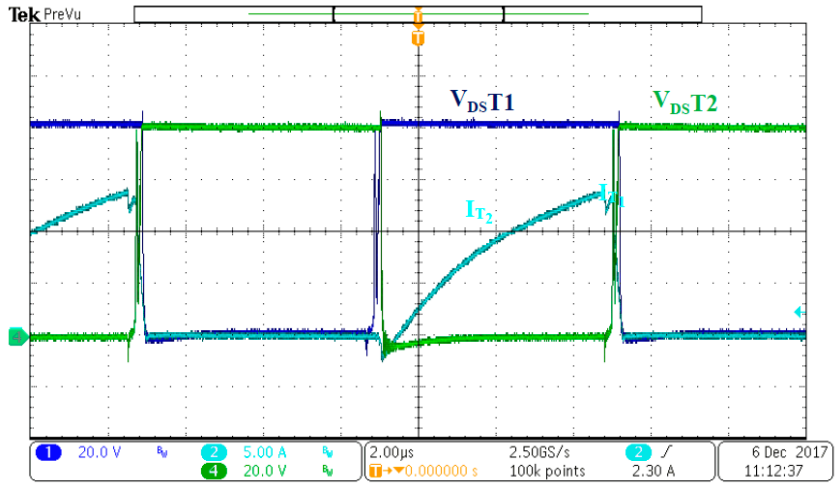

Figure 16. Voltage and current waveforms of the power transistors T_1, T_2 (100% of output power)—measurement.

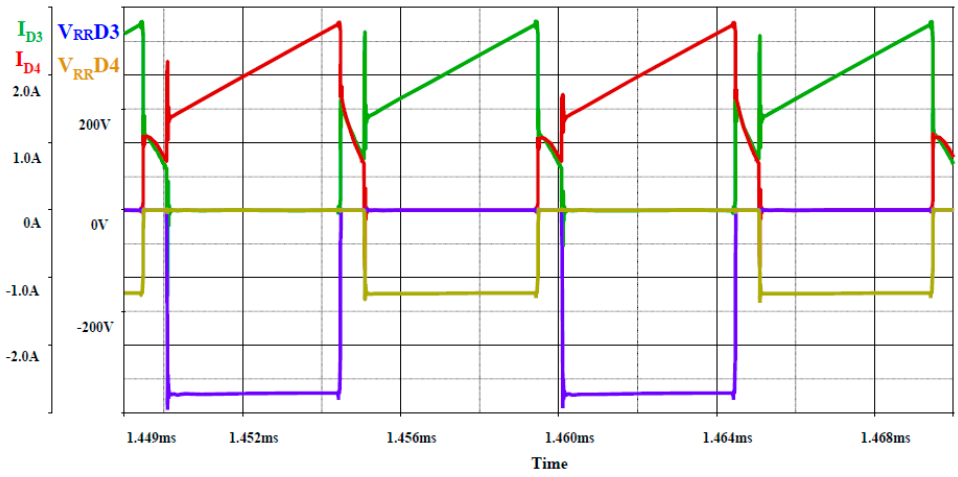

Figure 17. Voltage and current waveforms of the power diodes D_3, D_4 (100% of output power)—simulation.

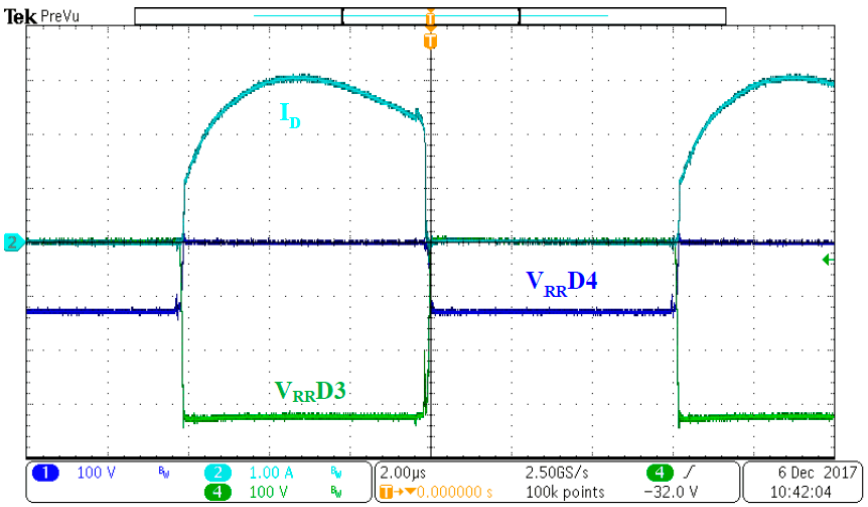

Figure 18. Voltage and current waveforms of the power diodes D_3, D_4 (100% of output power)—measurement.

Further investigation of the proposed converter is focused on the efficiency behavior within whole operational range, i.e., at various power levels and consequently the identification of the voltage transfer characteristic is done in dependency on the duty cycle, as well as on the value of turn's ratio.

4.2. Operational Characteristics

4.2.1. Efficiency, Output Voltage = f (Output Power), Duty Cycle = Constant

Within this part of investigation several measurements were taken in relation to the efficiency performance, and output characteristic of the proposed converter was investigated. The measurements were taken for the variable power at constant duty cycle, i.e., at $D_1 = D_2 = 0.45$. Change of load was in the range of 10–100%. Table 3 shows individual values of the efficiency and the value of the output power in dependency on the output power. This is graphically interpreted in Figure 19.

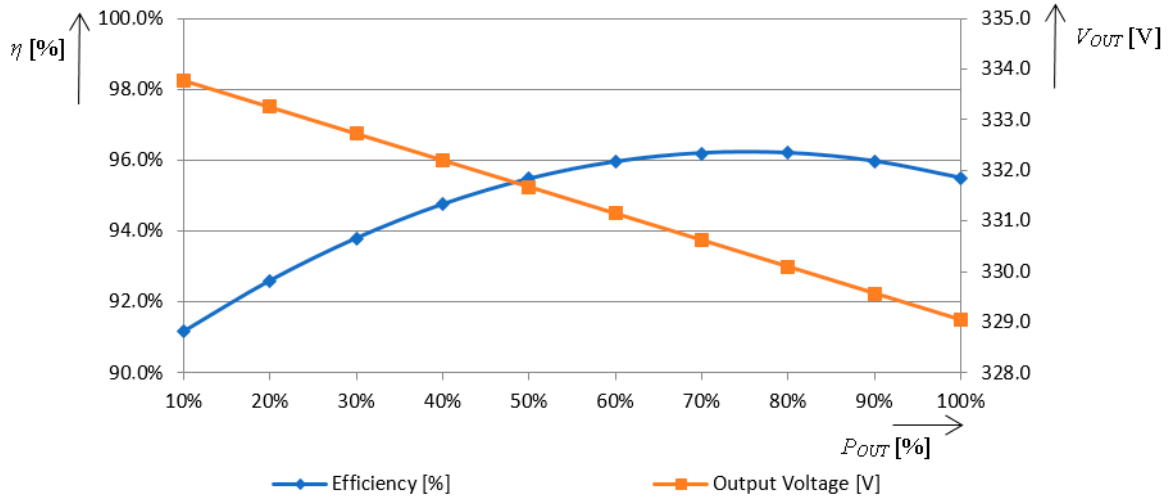

Figure 19. Dependency of the converter's efficiency and output voltage on the output power (measurement).

Table 3. Values of the efficiency and output voltage in dependency on the output power (Measurement).

Item	Values									
Output Power (%)	10	20	30	40	50	60	70	80	90	100
Efficiency (%)	91.2	92.6	93.8	94.8	95.5	96.0	96.2	96.2	96.0	95.5
Output Voltage (V)	333.8	333.3	332.7	332.2	331.7	331.1	330.6	330.1	329.6	329.0

It is seen (Figure 19) that the efficiency curve is flat when considering whole operating range, and system efficiency is not below 90%. This is a beneficial behavior for low-load conditions, whereby maximum efficiency is achieved at around the point of the maximal power, i.e., at 900 W, where efficiency is above 96%. It can be seen that the value of output voltage is not affected when considering the change of the output power. The converter has stiff behavior when the voltage drop from low load to the full load is 4 V. This behavior is highly valuable in applications where stiff DC voltage is required, i.e., for a DC bus for inverter stage.

Figure 20 shows power loss analysis based on Equations (26)–(37). The total calculated power loss is 40.53 W (Table 3) within the peak efficiency of the converter (96.2%). At nominal output power, the efficiency of the converter is 95.5%, which is related to the power losses at the value of 47.15 W. Because the proposed converter operates at hard-switching commutation mode, the highest portion of the losses belongs to semiconductor devices (more than 85% of total losses belong to switching losses). Therefore, proper selection of transistors and diodes are critical for efficiency performance of the proposed converter.

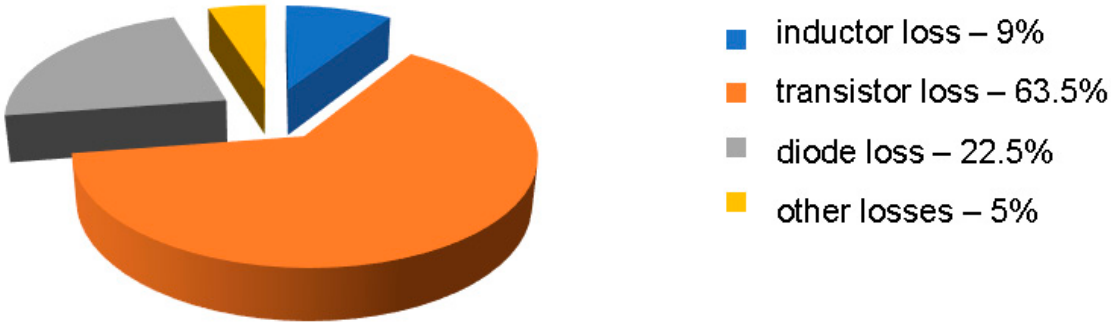

Figure 20. Power loss distribution of the proposed converter at highest efficiency 96.2%.

4.2.2. Voltage Gain = f (Duty Cycle), Output Power = 100%, 20%

Consequently, the investigation of the voltage gain in dependency on the duty cycle was performed. The results are listed in Table 4, wherein two situations have been considered. The power load of 20% and 100% was defined within measurements. From the table it can be seen that the change of the load has very low effect on the change of the value of voltage gain. The voltage gain characteristic in dependency on duty cycle is shown on Figure 21. At a given turns ratio, the voltage gain can be adjusted through the duty cycle modification in the range of 1.5–3.8.

Table 4. Values of the converter's voltage gain in dependency on the duty cycle.

Duty	0.05	0.1	0.15	0.2	0.25	0.3	0.35	0.4	0.45
V_{OUT}/V_{IN} (100% P_{OUT})	1.54	1.86	2.14	2.4	2.66	2.93	3.22	3.5	3.8
V_{OUT}/V_{IN} (20% P_{OUT})	1.63	1.99	2.29	2.56	2.81	3.07	3.32	3.58	3.86

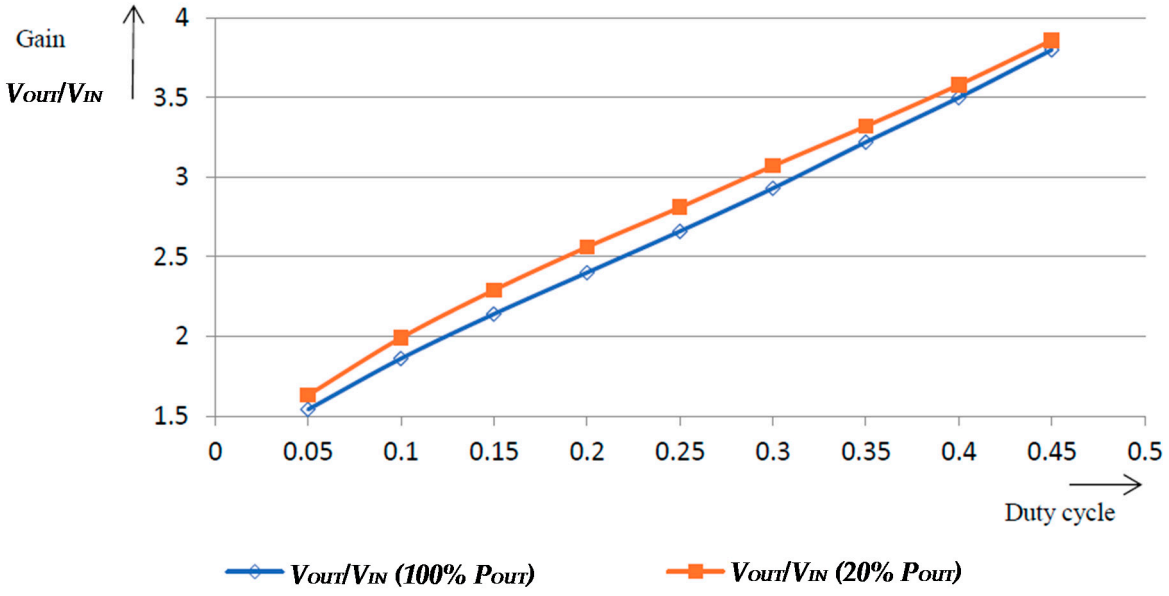

Figure 21. Dependency of converter's voltage gain on the duty cycle at P_{OUT} = 100% and P_{OUT} = 20%.

4.2.3. Voltage Gain = f (Inductance Ratio), Duty Cycle = Constant

The last investigation within the steady-state performance of the converter related to the voltage gain characteristic was realized by way of the turn's ratio modification. Within this experiment the number of turns on the boost inductors L_1 and L_2 was left constant, while the change of the turns on the reset inductance L_3 was provided. The duty cycle within this experiment was constant and equal to $D_1 = D_2 = 0.45$. The range of the turn's ratio was done within 1–8. The following Tables 5 and 6 show

the dependency of the voltage gain on the turn's ratio. It can be seen (Figure 22) that this dependency is in linear relationship, thus with the increase of the turns on the reset inductance, the higher voltage gain can be achieved. It is a beneficial property of this proposed converter's topology, because the range of the output voltage can be considerably increased.

Table 5. Values of the converter's voltage gain in dependency on the turns ration between boost and reset inductors ($N_1 = N_2$ = constant, N_3 = <*1–11*>).

Turns ratio N_3/N_1	0.17	0.33	0.50	0.67	0.83	1.00	1.17	1.33	1.50	1.67	1.83
Number of turns $N_1 = N_2$	6	6	6	6	6	6	6	6	6	6	6
Number of turns N_3	1	2	3	4	5	6	7	8	9	10	11
Voltage gain V_{OUT}/V_{IN}	2.06	2.16	2.26	2.36	2.45	2.94	3.1	3.25	3.41	3.56	3.71

Table 6. Values of the converter's voltage gain in dependency on the turns ration between boost and reset inductors ($N_1 = N_2$ = constant, N_3 = <*12–48*>).

Turns ratio N_3/N_1	2.00	2.17	2.33	2.50	3.00	4.00	5.00	6.00	7.00	8.00
Number of turns $N_1 = N_2$	6	6	6	6	6	6	6	6	6	6
Number of turns N_3	12	13	14	15	18	24	30	36	42	48
Voltage gain V_{OUT}/V_{IN}	3.86	4.01	4.16	4.3	4.72	5.51	6.21	6.82	7.35	7.76

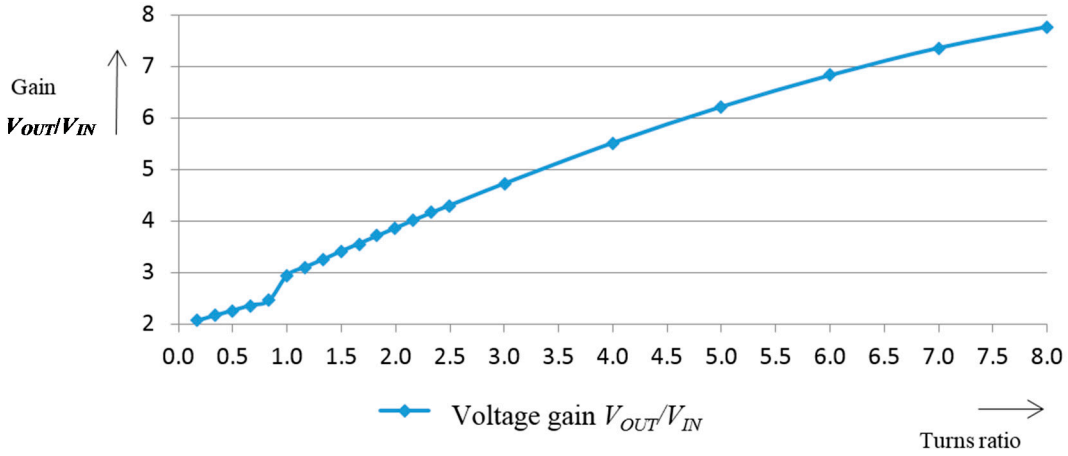

Figure 22. Dependency of converter's voltage gain on the turns ration between $L_1 = L_2$ and L_3.

4.3. Comparisons of Proposed Converter Performance to Other Circuit Alternatives

The given properties of the proposed converter are compared to the standard dual-interleaved boost type converter and to the classic boost converter. The input–output parameters are considered to be similar to those specified at the beginning of chapter 4, thus 1 kW output power supplied from input voltage source 100 V_{DC}, switching frequency is 100 kHz. The voltage gain of all converters was set to $V_{OUT}/V_{IN} = 3.6$. The results from the analysis related to the operational parameters/characteristics are listed in Table 7.

Table 7. Comparisons of proposed converter to other circuit alternatives.

Characteristic/Parameter	**Proposed Converter**	**Dual Interleaved Boost Converter**	**Boost Converter**
Output power	1 kW	1 kW	1 kW
Output voltage ripple	19 mV	180 mV	364 mV
Input ripple current	8.8 A	34 A	28 A
Output capacitor	33 µF	470 µF	470 µF
Inductor Volumes	EI PLT 43/10	E50/27/15	ETD59
Efficiency (full power)	95.5%	91%	90%
Voltage gain (V_{IN}/V_{OUT})	1:8	1:19	1:10

From Table 7 it is seen that the proposed converter has advantages related to the overall efficiency rated at full output power; even the number of components is higher. This is related to the fact that much a lower magnetic core can be used, while its performance is improved also by the fact that the AC component is continuously flowing through its circuit. In this way, core losses and hysteresis losses are much lower, because DC magnetization is eliminated. The value of bulky output electrolytic capacitor can be more than 10 times lower compared to the standard solution, and through this it is possible to eliminate losses related to parasitic ESR of electrolytic capacitor. Even when the value of capacitor of the proposed converter is very low, the output voltage ripple is more than 10 times lower compared to the interleaved boost converter and more than 25 times lower compared to the standard boost converter. The advantages are also related to the input current ripple, while due to the existence of an AC component in the circuit, the current ripple can be minimized compared to standard topologies. On the other hand, it is seen that the voltage gain of the proposed converter has limitations compared to other topologies, which is related to optimal selection of turns ratio between inductances L_1, L_2 and L_3.

5. Conclusions

Within this paper a new perspective topology was introduced. It is an interleaved boost converter with the core reset additional inductance. The existence of this inductance enables within each operational period of the converter a reset of the magnetic core, where all inductors are implemented. The AC waveform of the current flows through this inductance, thus the saturation of the core by the DC component is not critical, as opposed to the other standard interleaved boost topologies.

The steady state operation is described in more detail, while the main focus was placed on the efficiency, and voltage gain performance. It is seen that efficiency is competitive in the whole operational range, with the best-in-class topologies of power converters. Further improvements can be done with the implementation of a soft-switching technique, which will be the task for the future work. Voltage gain can be modified two ways, i.e., with the change of the duty cycle, or with the selection of the turns ratio between boost inductances and reset inductance. This feature will be valuable in applications where very high voltage gain is required. On the other hand, special focus must be given to the integrated magnetics design; this will also be a topic of the future research. Meanwhile, the highly advantageous characteristic of the proposed converter is its very tight output voltage character in the whole power range. This feature is highly appreciated in applications, such as the DC bus circuit, where requirements for stable voltage are given.

As mentioned, future work should focus further on efficiency improvements, and also on the dynamic and control analysis.

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Author Contributions: Michal Frivaldsky prepared the paper structure and has organized individual works within the paper preparations, made simulation analysis and finally he wrote the paper. Branislav Hanko has designed experimental prototype of proposed converter and has organized initial measurements. Michal Prazenica is responsible for the mathematical analysis and power loss analysis of the proposed converter. Jan Morgos was realizing the experimental verification and analysis of the data from simulations as well as from experimental measurements.

Conflicts of Interest: The authors declare no conflict of interest.

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