A New Backward Euler Stabilized Optimum Controller for NPC Back-to-Back Five Level Converters

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Abstract: This paper presents a backward Euler stabilized-based control strategy applied to a neutral point clamped (NPC) back-to-back connected five level converters. A generalized method is used to obtain the back-to-back NPC converter system model. The backward Euler stabilized-based control strategy uses one set of calculations to compute the optimum voltage vector needed to reach the references and to balance the voltage of the DC-bus capacitors. The output voltage vector is selected using a modified cost functional that includes variable tracking errors in the functional weights, whereas in classic approaches, the weights are considered constant. The proposed modified cost functional enables AC current tracking and DC-bus voltage balancing in a wide range of operating conditions. The paper main contributions are: (i) a backward Euler stabilized-based control strategy applied to a double, back-to-back connected, five level NPC converter; (ii) the use of cost functional weight varying as a function of the controlled variable tracking errors to enforce the controlled variables and to balance the DC capacitor voltages; and (iii) the demonstration of system feasibility for this type of converter topology and control strategy, ensuring a high enough computational efficiency and extending the modulation index from 0.6 to 0.93. Experimental results are presented using a prototype of a five level NPC back-to-back converter.

Keywords: multilevel converters; back-to-back converters; backward Euler based control; capacitors voltage balancing

1. Introduction

Multilevel power converters are the converters of choice for high power medium voltage applications such as electrical machine drives or the grid interface connection of renewable energy sources [1–4]. Considering today's power semiconductor limitations on voltage blocking and dv/dt, the attention and development of multilevel voltage source converters is increasing due to known attractive features, when compared with two level voltage source converters [5–8].

Among multilevel converters, the neutral point clamped (NPC) converter introduced in [5] is well accepted and used in several industrial applications [7]. The main drawback of the NPC topology is

the voltage imbalance of the DC-bus capacitors, which has been an active research topic using external circuits [8,9], modifying pulse width modulation (PWM) techniques [10–13], space vector modulation (SVM) [3,4,14], sliding mode control exploiting converter vector redundancies [15], and predictive control [16–18]. Some of these techniques require a significant computing power, or have limitations when redundant vector-based strategies are used to balance the capacitor voltages. The theoretical maximum output modulation index is around 0.6 for a back-to-back connected NPC converter with an active load and zero active power exchange, when using the SVM-based control strategy [3,4].

Known NPC modulation strategies such as PWM and SVM [10,12] while operating at a constant switching frequency, do not guarantee that controlled outputs are free from DC-bus voltage disturbances, semiconductor "ON" voltages, dead times, or switching delays.

Hysteretic control methods are robust to semiconductor non-idealities, load changes, and disturbances, and present fast dynamic responses. Their major drawback is the variable switching frequency, which depends on the operating conditions and load parameters. For some quality indexes, hysteretic control methods may need higher switching frequencies when compared to PWM or SVM modulation techniques [17,18].

Optimum predictive control techniques drive the output errors towards zero by minimizing the cost functional in each sampling period [19–22]. Given the controlled output references, the first step of the NPC predictive controller is to sample the state variables. The second step uses a non-linear model of the system to predict values of the state variables in the next sampling intervals for every possible NPC switching configuration (termed the vector). This requires a powerful numerical processor to compute all the possible future values of the state variables in a sampling step well below 100 μs, to allow switching frequencies around 5 kHz. The last step computes the cost functional for all NPC vectors and chooses the vector that gives the minimum cost functional value in that sampling interval. These three steps are repeated in the next sampling time.

Predictive controllers for power electronic converters seem to be a potential alternative since they are well suited to control variables (e.g., currents, voltages, power) presenting coupled dynamics, and can offer closed loop dynamics with decoupled behavior [19]. However, in each sampling time, predictive algorithms must compute the state variable values in the next sampling interval for all of the possible NPC vectors, together with the corresponding cost functional, requiring a powerful processing unity for converters with available vectors in excess of 27 (three level converters).

Predictive algorithms used to reduce time consumption have been reported by [23,24]. These algorithms use the system inverse dynamics to directly compute the necessary output voltage vector required to track references, while predictive controllers estimate the output errors for all the available vectors. The output voltage vector is then selected among those which are available by minimizing a cost functional that computes the distance between the optimal voltage vector and the existing voltage vectors. However, in [23], the voltage balancing problem was not addressed but only pointed out briefly in cases where the converter presented redundancies. In [24], the voltage balancing problem was solved for three level inverters, but the dependence on non-modeled dynamics is not addressed. This paper uses a stable method to compute the necessary output voltage vector and extends the voltage balancing to five level NPC converters, where balancing is more challenging, by using an approach that is valid even if there are no redundant vectors. In [24], only constant weights are used in the quadratic cost function, while the proposed paper uses variable weights as a function of variable tracking errors, for the cost functional equations of functions. The approach proposed here, while not needed in three level NPCs, is nearly mandatory in five level inverters, as balancing the four DC capacitor voltages using 250 vectors is, at least, more complex and difficult. The approach of this paper enables the enlargement of NPC voltage balancing range for different active and reactive power flow conditions. In view of these problems, this paper presents a backward Euler stabilized control strategy applied to a back-to-back five level NPC converter to control the line inject AC currents and to balance the four capacitor voltages. The paper starts with the back-to-back converter modeling, using a systematic switching variable generalized for *m* level converters (Section 2).

This modeling is an essential tool for the analysis and control strategy of the NPC back-to-back converter. The control strategy proposed (Section 3) uses a backward Euler stabilized approach to directly compute the optimum output voltage vector required to track the references in the next time step. The output voltage vector is then selected from the available voltage vectors by minimizing a variable weight cost functional that includes variable tracking errors in the weighting of the error between the optimal voltage vector and the possible voltage vectors. The new proposed cost function enables active and reactive power flow control and DC-bus voltage balancing, in a wide range of operating conditions. Simulation and experimental results for two five level NPC back-to-back connected converters validate the proposed control strategy and show the feasibility of the proposed system (Section 4). Experimental results are obtained using a 230 V ac/600 V dc/230 V ac five level NPC back-to-back converter prototype. Both converters are controlled using one Power PC-based board (DS1103) with a 32 μs sampling time, for acquiring all the data, completing the calculations of the two 125 vectors converters, and computing the gate signals to drive all the 48 IGBTs.

2. System Modeling

Figure 1 shows the *m* level back-to-back converter arrangement. The generalized system is composed by two three phase back-to-back *m* level diode-clamped converters, where each NPC converter is connected to an AC system using a transformer. The modeling assumes ideal electrical components and semiconductor devices (zero ON voltages, zero OFF currents, zero switching times).
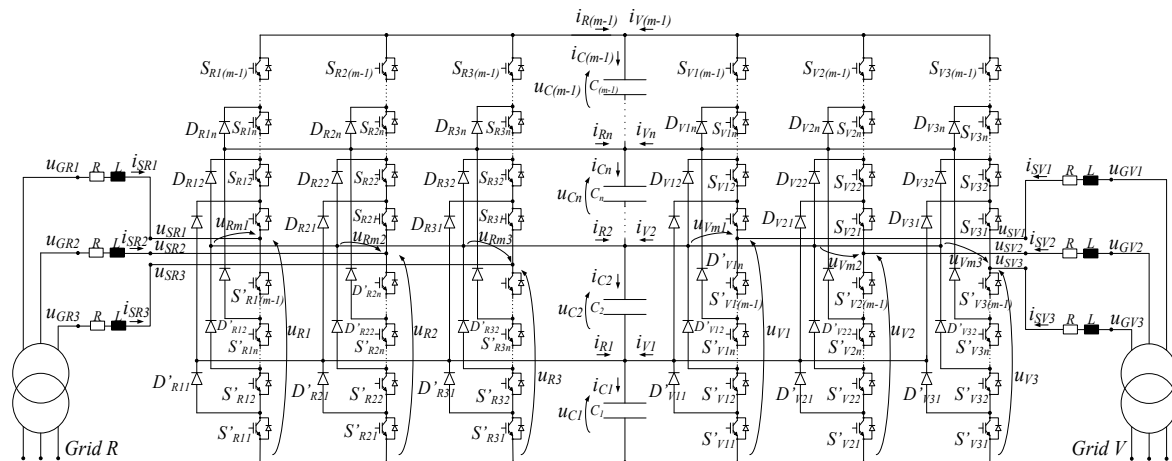

Figure 1. Multilevel NPC back-to-back connected converter.

To obtain a model valid for NPC multilevel converters having an arbitrary number of levels *m*, it is advantageous to start numbering the upper IGBT switches $S_{k1}, S_{k2}, \ldots S_{kn}, \ldots S_{k(m-1)}$ in each *k* leg ($k \in \{1, 2, 3\}$) from the leg midpoint, and $S'_{k1}, S'_{k2}, \ldots S'_{kn}, \ldots S'_{k(m-1)}$ up from the zero voltage node. The DC-bus capacitors are also numbered up from the zero voltage point. Each semiconductor and DC-bus capacitor index is associated with the respective voltage level.

The switching strategy for an *m* level NPC converter ensures that the upper leg switches $[S_{k1}\ S_{k2} \ldots S_{kn} \ldots S_{k(m-1)}]$ and the corresponding ones on the lower side $[S'_{k1}\ S'_{k2} \ldots S'_{kn} \ldots S'_{k(m-1)}]$ are always in complementary states. Consequently, if $S_{kn} = 1$, then S'_{kn} must be equal to 0, where $S_{kn} = 1$ means that the specified switch is ON, and $S_{kn} = 0$ shows that the switch is OFF.

2.1. Converter Generalized State Space Model

For each NPC leg, the output voltage variables u_k (u_{Rk} or u_{Vk} for the R-side converter and V-side converter, respectively) are defined from the *k* leg midpoint to zero voltage. The output voltage can be

written in terms of the logical state of the leg switches S_{kn} and DC-bus capacitor voltages, as in (1), where, u_{C_n} is the voltage of the nth dc-link capacitor.

$$u_k = \sum_{n=1}^{m-1} S_{kn} u_{C_n} \tag{1}$$

Considering a three phase balanced network, the k phase voltage u_{Sk} can be related to all leg output voltages u_k and, using (1), expressed as a function of the DC-bus capacitor voltages as (2), where the elements S_{Ukn} are determined by (3).

$$u_{Sk} = \sum_{n=1}^{m-1} S_{Ukn} u_{C_n} \tag{2}$$

$$S_{Ukn} = \frac{1}{3} \left(2S_{kn} - \sum_{\substack{i=1 \\ i \neq n}}^{3} S_{in} \right) \tag{3}$$

The DC-bus n level current i_n can be related to the phase currents i_{Sk} by (4):

$$i_n = \sum_{k=1}^{3} \gamma_{nk} i_{Sk} \tag{4}$$

where γ_{nk} is a time dependent switching variable, written in terms of the k leg switching logical states (5), as follows:

$$\gamma_{nk} = S_{k1} S_{k2} ... S_{kn} \left(1 - S_{k(n+1)}\right) \left(1 - S_{k(n+2)}\right) ... \left(1 - S_{k(m-1)}\right) \tag{5}$$

At each time, the load phase current i_{Sk} is connected to an n DC-bus level when $\gamma_{nk} = 1$, or to the zero voltage bus when $\gamma_{nk} = 0$.

Each DC-bus n level current capacitor i_{C_n} can be related to the corresponding voltage u_{C_n} by (6):

$$i_{C_n} = C_n \frac{du_{C_n}}{dt} \tag{6}$$

The above current i_{C_n} can be expressed in terms of the upper capacitor current $i_{C_{(n+1)}}$ and the corresponding DC-bus n level currents from the grid side i_{Rn} or i_{Vn}, by (7):

$$i_{C_n} = \sum_{j=n}^{m-1} \left(i_{Rj} + i_{Vj}\right) \tag{7}$$

Using Equations (4), (6), and (7) for both grid sides, the voltage capacitor time derivative is expressed in terms of the phase currents, i_{SRk} and i_{SVk}, as it is shown in (8):

$$\frac{d}{dt} \begin{bmatrix} u_{C_1} \\ u_{C_2} \\ \vdots \\ u_{C_n} \\ \vdots \\ u_{C_{(m-1)}} \end{bmatrix} = \begin{bmatrix} \frac{\Gamma_{R11}}{C_1} & \frac{\Gamma_{R12}}{C_1} & \frac{\Gamma_{R13}}{C_1} \\ \frac{\Gamma_{R21}}{C_2} & \frac{\Gamma_{R22}}{C_2} & \frac{\Gamma_{R23}}{C_2} \\ ... & ... & ... \\ \frac{\Gamma_{Rn1}}{C_n} & \frac{\Gamma_{Rn2}}{C_n} & \frac{\Gamma_{Rn3}}{C_n} \\ ... & ... & ... \\ \frac{\Gamma_{R(m-1)1}}{C_{(m-1)}} & \frac{\Gamma_{R(m-1)2}}{C_{(m-1)}} & \frac{\Gamma_{R(m-1)3}}{C_{(m-1)}} \end{bmatrix} \begin{bmatrix} i_{SR1} \\ i_{SR2} \\ i_{SR3} \end{bmatrix} + \begin{bmatrix} \frac{\Gamma_{V11}}{C_1} & \frac{\Gamma_{V12}}{C_1} & \frac{\Gamma_{V13}}{C_1} \\ \frac{\Gamma_{V21}}{C_2} & \frac{\Gamma_{V22}}{C_2} & \frac{\Gamma_{V23}}{C_2} \\ ... & ... & ... \\ \frac{\Gamma_{Vn1}}{C_n} & \frac{\Gamma_{Vn2}}{C_n} & \frac{\Gamma_{Vn3}}{C_n} \\ ... & ... & ... \\ \frac{\Gamma_{V(m-1)1}}{C_{(m-1)}} & \frac{\Gamma_{V(m-1)2}}{C_{(m-1)}} & \frac{\Gamma_{V(m-1)3}}{C_{(m-1)}} \end{bmatrix} \begin{bmatrix} i_{SV1} \\ i_{SV2} \\ i_{SV3} \end{bmatrix} \tag{8}$$

where the k column matrix element, Γ_{Rnk} or Γ_{Vnk} (k leg), is determined using the value of the time dependent switching variable, γ_{Rnk} or γ_{Vnk}, in the case of the R or V side, respectively, as (9) and (10):

$$\Gamma_{Rnk} = \sum_{i=n}^{m-1} \gamma_{Rik} \tag{9}$$

$$\Gamma_{Vnk} = \sum_{i=n}^{m-1} \gamma_{Vik} \tag{10}$$

Applying the Concordia transformation [25] to Equations (2) and (8) and considering that zero sequence components are null, the multilevel converter matrix equations in the $\alpha\beta$ coordinates are given by (11) and (12), as follows:

$$\begin{bmatrix} u_{S\alpha} \\ u_{S\beta} \end{bmatrix} = \begin{bmatrix} S_{U1\alpha} & S_{U2\alpha} & ... & S_{Un\alpha} & ... & S_{U(m-1)\alpha} \\ S_{U1\beta} & S_{U2\beta} & ... & S_{Un\beta} & ... & S_{U(m-1)\beta} \end{bmatrix} \begin{bmatrix} u_{C_1} \\ u_{C_2} \\ \vdots \\ u_{C_n} \\ \vdots \\ u_{C_{(m-1)}} \end{bmatrix} \tag{11}$$

$$\frac{d}{dt} \begin{bmatrix} u_{C_1} \\ u_{C_2} \\ \vdots \\ u_{C_n} \\ \vdots \\ u_{C_{(m-1)}} \end{bmatrix} = \begin{bmatrix} \frac{\Gamma_{R1\alpha}}{C_1} & \frac{\Gamma_{R1\beta}}{C_1} & \frac{\Gamma_{V1\alpha}}{C_1} & \frac{\Gamma_{V1\beta}}{C_1} \\ \frac{\Gamma_{R2\alpha}}{C_2} & \frac{\Gamma_{R2\beta}}{C_2} & \frac{\Gamma_{V2\alpha}}{C_2} & \frac{\Gamma_{V2\beta}}{C_2} \\ ... & ... & ... & ... \\ \frac{\Gamma_{Rn\alpha}}{C_n} & \frac{\Gamma_{Rn\beta}}{C_n} & \frac{\Gamma_{Vn\alpha}}{C_n} & \frac{\Gamma_{Vn\beta}}{C_n} \\ ... & ... & ... & ... \\ \frac{\Gamma_{R(m-1)\alpha}}{C_{(m-1)}} & \frac{\Gamma_{R(m-1)\beta}}{C_{(m-1)}} & \frac{\Gamma_{V(m-1)\alpha}}{C_{(m-1)}} & \frac{\Gamma_{V(m-1)\beta}}{C_{(m-1)}} \end{bmatrix} \begin{bmatrix} i_{SR\alpha} \\ i_{SR\beta} \\ i_{SV\alpha} \\ i_{SV\beta} \end{bmatrix} \tag{12}$$

where, $\Gamma_{v\alpha}$, $\Gamma_{v\beta}$, $S_{Un\alpha}$, and $S_{Un\beta}$ are obtained by applying the $\alpha\beta0$ transformation to the Γ_{n1}, Γ_{n2}, Γ_{n3}, and S_{Un1}, S_{Un2}, S_{Un3} variables.

2.2. Grid Side Interface Modeling

The time derivative of the k phase current of the R-side or V-side converter in $\alpha\beta$ coordinates, $i_{S\alpha\beta}$, is obtained using (13), where $u_{G\alpha\beta}$ is the grid voltage, R and L represent the grid connection per phase of resistance and inductance, and $u_{SR\alpha\beta}$ is the converter AC output voltage.

$$\frac{d}{dt} \begin{bmatrix} i_{S\alpha} \\ i_{S\beta} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{S\alpha} \\ i_{S\beta} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{G\alpha} \\ u_{G\beta} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{S\alpha} \\ u_{S\beta} \end{bmatrix} \tag{13}$$

3. Backward Euler Stabilized Optimum Control

3.1. Global System Control

The control structure of the NPC back-to-back converter system, shown in Figure 2, uses two controllers, one for each converter side. The R-side NPC controls the R-side AC currents, enforcing the DC-bus voltage u_{dc} (therefore ensuring energy balancing), and establishing the reactive power injected in the R-side grid. Additionally, it balances the capacitor voltages. The V-side NPC controls the V-side AC currents (establishing the active and reactive power to be delivered to the V-side), and balances the capacitor voltages. The power flow control enforces, via the u_{dc} bus voltage or directly, both R and V sides sinusoidal AC current references. Each NPC will be provided with one independent vector selection controller.
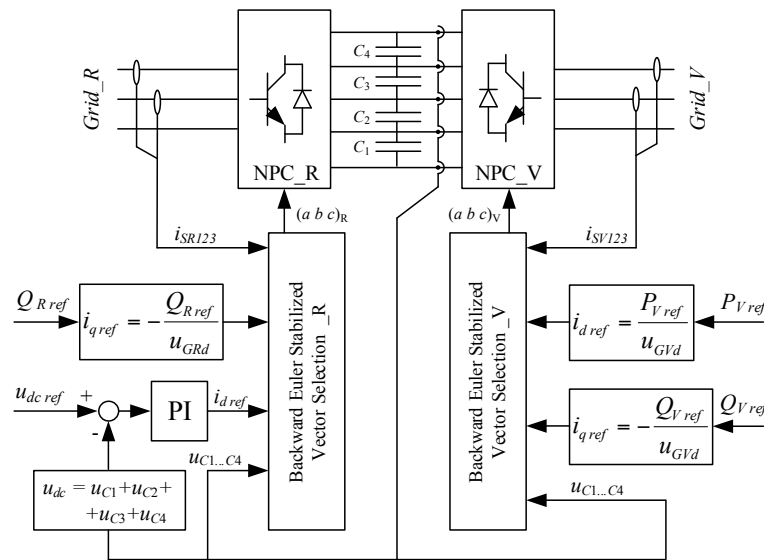
Figure 2. System control structure diagram.

The R-side converter maintains the DC-bus voltage u_{dc} at a given reference using a Proportional-Integral (PI) controller. From the u_{dc} controller output, a reference value for the grid current d component i_{SRdref} is obtained, enforcing the active power demanded from the R grid. The reactive power reference Q_{Rref} is used to obtain the grid current q component reference i_{SRqref}. These current reference values, as well as the grid currents i_{SR123} and the capacitor voltages $u_{C1} \ldots u_{C4}$, are the inputs of the backward Euler Stabilized optimum controller, whose output is the three phase vector to be applied by the converter ($a\ b\ c$).

The V-side controller controls the active power P_V and reactive power Q_V on the V-side grid. The reference value of the grid current d component i_{SVdref} is established from the reference of the active power flow. The reference value of the grid current q component i_{SVqref} is established from the reactive power reference. The reference currents $i_{SVdqref}$, together with the grid currents i_{SV123} and capacitor voltages, are the inputs of the backward Euler Stabilized optimum controller vector selection block. This controller also balances the capacitor voltages around their reference values.

3.2. Backward Euler Stabilized Optimum Current Control and Capacitor Voltage Balancing

3.2.1. AC Current Control

Using the stable Euler backward approach [26], the current values in the next time step, $i_{S\alpha\beta_{(t_s+T_s)}}$ can be obtained from (14):

$$i_{S\alpha\beta_{(t_s+T_s)}} = i_{S\alpha\beta_{t_s}} + T_s \left. \frac{di_{S\alpha\beta}}{dt} \right|_{t_s+T_s} \tag{14}$$

This is an implicit method used to solve stiff differential equations. Under the Lipschitz continuity assumption on the current derivative, it can be shown that if T_s is small enough, the Equation (14) has a unique solution. In addition, the Euler backward method is absolutely stable [26]. The backward Euler method is therefore very useful because its stability region contains the whole left half of the complex plane.

Using (14) and (13), the optimum vector that assures the references tracking in the next time step, $u_{S\alpha_{(t_s+T_s)}}$ and $u_{S\beta_{(t_s+T_s)}}$ components, denoted $u_{S\alpha\beta_{(t_s+T_s)}}$, is computed as (15):

$$\begin{bmatrix} u_{S\alpha} \\ u_{S\beta} \end{bmatrix}_{t_s+T_s} = -\frac{L+RT_s}{T_s} \begin{bmatrix} i_{S\alpha_{(t_s+T_s)}} - i_{S\alpha_{t_s}} \\ i_{S\beta_{(t_s+T_s)}} - i_{S\beta_{t_s}} \end{bmatrix} + \begin{bmatrix} -R & 0 \\ 0 & -R \end{bmatrix} \begin{bmatrix} i_{S\alpha} \\ i_{S\beta} \end{bmatrix}_{t_s} + \begin{bmatrix} u_{G\alpha} \\ u_{G\beta} \end{bmatrix}_{t_s+T_s} \tag{15}$$

From (15), it is possible to compute the optimum converter voltage vector components $\mathbf{V_I} = u_{S\alpha\beta_{(t_s+T_s)}}$ needed, so that the $i_{S\alpha\beta}$ current vector is equal to its reference at the next sampling time $i_{S\alpha\beta_{(t_s+T_s)}} = i_{S\alpha\beta ref}$. The optimum vector $\mathbf{V_I} = [u_{S\alpha_{(t_s+T_s)}}, u_{S\beta_{(t_s+T_s)}}]^T$ is only computed once in each sampling step and is used in the cost functional equations in order to select the best vector to be applied in the converter. Figure 3 shows a diagram of the backward Euler stabilized optimum control principle, where the selected vector is the one that minimizes a weighted distance to the optimum vector.
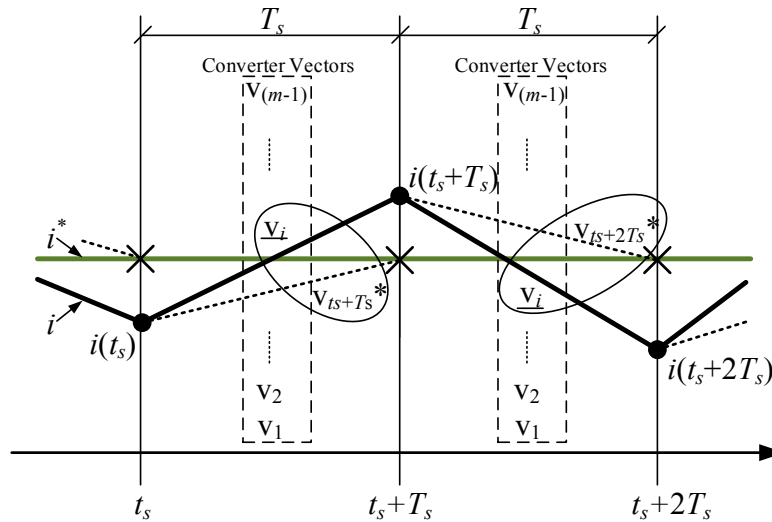
Figure 3. Illustration of the backward Euler stabilized control strategy.

3.2.2. Voltage Balancing Control

Similar to current control and using the Euler backward approach, each capacitor optimal current $i_{C_n(t_s+T_s)}$ that leads the nth capacitor voltage $u_{C_n t_s}$ towards the reference u_{Cref} in the next sampling time, $u_{C_n(t_s+T_s)} = u_{C_n ref}$, can be estimated using (16) as a discrete time approximation of (6). All the DC-bus capacitors have the same value for their voltage reference u_{Cref}. For each level, the total DC-bus level currents, $i_{Rn(t_s+T_s)}$ or $i_{Vn(t_s+T_s)}$, are obtained using (17).

$$u_{C_n(t_s+T_s)} = u_{C_n t_s} + T_s \frac{du_{C_n}}{dt}\Big|_{t_s+T_s} \Rightarrow u_{C_n(t_s+T_s)} = u_{C_n t_s} + T_s \frac{i_{C_n(t_s+T_s)} - i_{C_n t_s}}{C} \Rightarrow i_{C_n(t_s+T_s)} = \frac{C_n}{T_s}\left(u_{C_n(t_s+T_s)} - u_{C_n t_s}\right) \quad (16)$$

$$i_{RVn(t_s+T_s)} = \frac{i_{C_n(t_s+T_s)} - i_{C_{(n+1)}(t_s+T_s)}}{2} \quad (17)$$

Therefore, the needed DC-bus currents to be applied in the following time step in order to assure the desired capacitor voltages, can be written as a vector form $\mathbf{I_U}$ in (18):

$$\mathbf{I_U} = \left[\begin{array}{ccccc} i_{(m-1)(t_s+T_s)} & \cdots & i_{n(t_s+T_s)} & \cdots & i_{1(t_s+T_s)} \quad i_{0(t_s+T_s)} \end{array} \right]^T \quad (18)$$

The NPC converter available capacitor current vectors $\mathbf{I_{V_i}}$ can be computed using Equation (19). $\mathbf{I_{V_i}}$ is computed for each converter voltage vector $\mathbf{V_i}$ ($u_{S\alpha i}$, $u_{S\beta i}$), considering that the phase currents will approximately follow their references in the next sampling time. Equation (19) is applied separately to both converter sides.

$$\mathbf{I_{V_i}} = [\gamma_{nk}]_{V_i} \left[\begin{array}{ccc} i_{S1ref} & i_{S2ref} & i_{S3ref} \end{array} \right]^T \quad (19)$$

3.2.3. Cost Functional and Vector Selection

The vector selection strategy, applied to both converters independently, minimizes a cost functional (20), relating the weighted distances to the optimum vectors, where $W_I(i_{Sk})$, and $W_U(u_{C_n})$ are the weights of errors $e_{U_{V_i}}$ and $e_{I_{V_i}}$ between the references and the values obtained from the application of each NPC vector V_i, respectively.

$$f_C(V_i) = \sqrt{W_I(i_{Sk})e_{U_{V_i}}^2 + W_U(u_{C_n})e_{I_{V_i}}^2} \tag{20}$$

In (20), the vector error $e_{U_{Vi}}$ is given by (21) and evaluates the distance between the current control optimal-vector $\mathbf{V_I}$ ($u_{S\alpha_{(t_s+T_s)}}$, $u_{S\beta_{(t_s+T_s)}}$), and the i^{st} NPC available vector $\mathbf{V_i} = [u_{S\alpha_i}, u_{S\beta_i}]$. It gives the information of the optimal-vector $\mathbf{V_I}$ deviation from the possible vector $\mathbf{V_i}$.

$$e_{U_{V_i}} = \sqrt{\left(u_{S\alpha_{(t_s+T_s)}} - u_{S\alpha_i}\right)^2 + \left(u_{S\beta_{(t_s+T_s)}} - u_{S\beta_i}\right)^2} \tag{21}$$

Moreover, the error $e_{I_{V_i}}$, given by (22), is the converter i^{st} DC-bus current vector I_{V_i} deviation from the optimal current vector $\mathbf{I_U}$, which is necessary to balance the capacitor voltages. From (18) and (19):

$$e_{I_{V_i}} = \sqrt{\sum_{n=1}^{4} \left(I_{U_n} - I_{V_{in}}\right)^2} \tag{22}$$

The phase current control is further associated with the weight $W_I(i_{Sk})$ of the cost functional (20) given in (23), showing that it depends on the current tracking error. In (23), ρ_I is a constant for all possible vectors and is used to match current error units, which are weighted with voltage error units.

$$W_I(i_{Sk}) = \rho_I \left(\left(i_{\alpha\,ref} - i_{\alpha_{t_s}}\right)^2 + \left(i_{\beta\,ref} - i_{\beta_{t_s}}\right)^2 \right) \tag{23}$$

If only AC current control was required, a constant weight $W_I(i_{Sk})$ in (20) would be enough. However, since it is also necessary to balance the capacitor voltages, it is better to consider a quadratic form (23) of $W_I(i_{Sk})$ in the cost functional, in order to give greater weight to the current error when bigger tracking errors occur.

The DC capacitor voltage balance is not the main purpose of NPC converter control, but it is nevertheless an essential task to enable the NPC correct operation. Thus, in the cost functional (20), the weight $W_U(u_{C_n})$ imposes the need to balance the capacitor voltages. It is given by (24) as a quadratic function of the capacitors' voltage tracking errors sum, where ρ_C is considered to be a constant value.

$$W_U(u_{C_n}) = \rho_C \left(\sum_{n=1}^{4} \left| u_{Cref} - u_{C_n} \right| \right)^2 \tag{24}$$

The variable weighting strategy, $W_I(i_{Sk})$, and $W_U(u_{C_n})$, give greater attention, either to the current control or to DC-bus voltages balancing control as a function of tracking errors, without needing to compute the controlled variable values for every possible converter vector. This flexibility allows covering a larger range of NPC operating conditions.

The cost functional (20) is calculated for each NPC possible vector V_i, including the redundant vectors. The selected vector is the one that scores the minimum value for the cost functional $f_C(V_i)$.

4. Simulation and Experimental Results

The proposed system simulations and experimental results, shown in the following points, were obtained using a 230 V ac/600 V dc/230 V ac five level NPC back-to-back prototype, shown in Figure 4. This prototype uses 48 IGBTs (Semikron Elektronik Gmbh & Co., Nuremberg, Germany)

as controlled power semiconductors. Both five level NPC converters are controlled using just one Power PC-based board (DS1103 from dSPACE GmbH, Paderborn, Germany) with a 32 µs sampling time, which performs sampling and calculations, and outputs semiconductor signals. The system parameters are presented in Table 1.
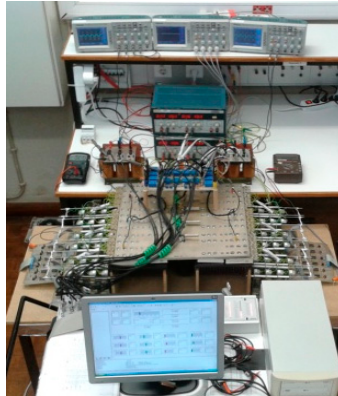

Figure 4. Experimental set-up including the five level NPC back-to-back converter and the DSP-based controllers.

Table 1. System parameters.

Symbol	Description	Value
C_1, C_2, C_3, C_4	DC-bus capacitors	4.7 mF
f_R, f_V	Fundamental grid frequencies	50 Hz
L	Coupling inductors	8 mH
R	Coupling inductors resistance	0.1 Ω
T_s	Sampling time	32 µs
u_{dc}	DC-bus voltage	600 V
u_{GR}, u_{GV}	AC grid voltages	230 V
ρ_C	Capacitors voltage error weights	5
ρ_i	Current error weights	1

4.1. Current Control

Table 2 presents the steady state operation conditions used in the experimental result shown in Figure 5. This figure shows the phase current i_{SV1} experimental result and the respective frequency spectrum. From Figure 5, it is possible to see that the output phase currents exhibit the fundamental component at 50 Hz and also a spread spectrum with a maximum frequency around 5 kHz. This maximum frequency is well above each semiconductor switching frequency, since the output switching frequency is the contribution of the eight IGBTs of each one of the three converter legs.

Table 2. Operation conditions of Figure 5.

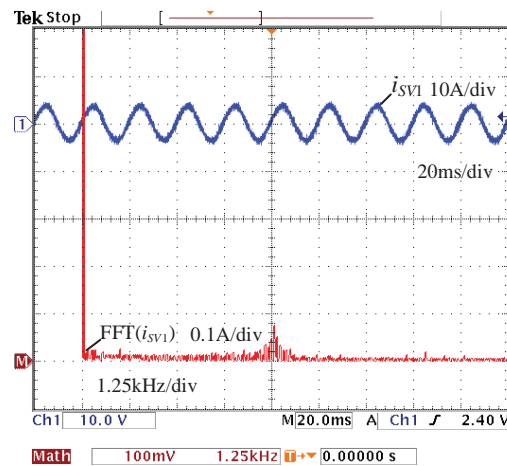| Figure	u_{GR}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
5	230 V	0	600 V	−5 A	0	230 V

Figure 5. Phase current control experimental result. CH1: i_{SV1}, 10 A/div, 20 ms/div; M: i_{SV1} frequency spectrum, 100 mA/div, 1.25 kHz/div.

Table 3 presents the operation conditions used to obtain the simulation results of Figures 6a and 7a, and the corresponding experimental results shown in Figures 6b and 7b. These figures show the phase current i_{SV1} control during a step in the i_{SVd} and i_{SVq} reference, respectively.

Table 3. Operation conditions of Figures 6 and 7.

Figure	u_{GR}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
6	230 V	0	600 V	Step: 5 A to −5 A	0	230 V
7	230 V	0	600 V	−4A	Step: 5 A to −5 A	230 V
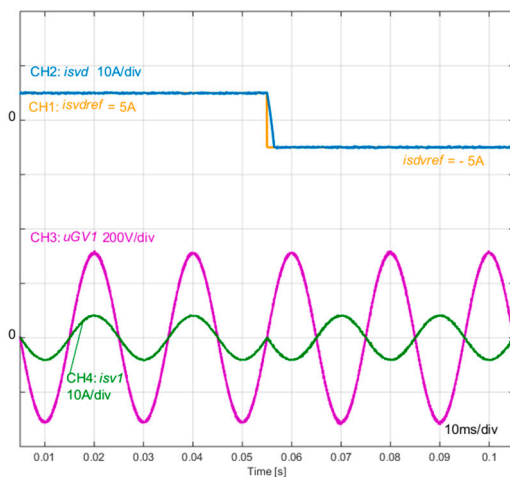
(**a**)
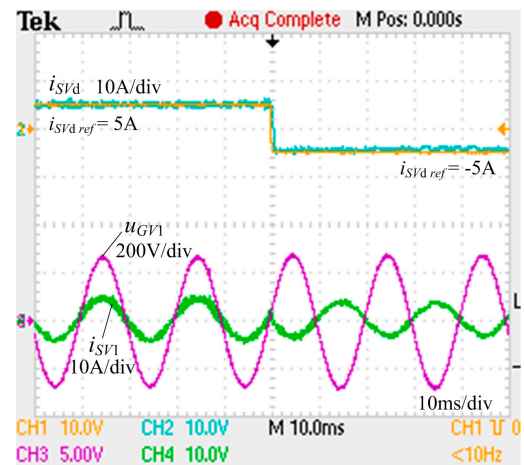
(**b**)

Figure 6. Phase current control: (**a**) Simulation result, CH1: i_{SVdref}, 10 A/div; CH2: i_{SVd}, 10 A/div; CH3: u_{GV1}, 200 V/div; CH4: i_{SV1}, 10 A/div; 10 ms/div; (**b**) Experimental result, CH1: i_{SVdref}, 10 A/div; CH2: i_{SVd}, 10 A/div; CH3: u_{GV1}, 200 V/div; CH4: i_{SV1}, 10 A/div; 10 ms/div.
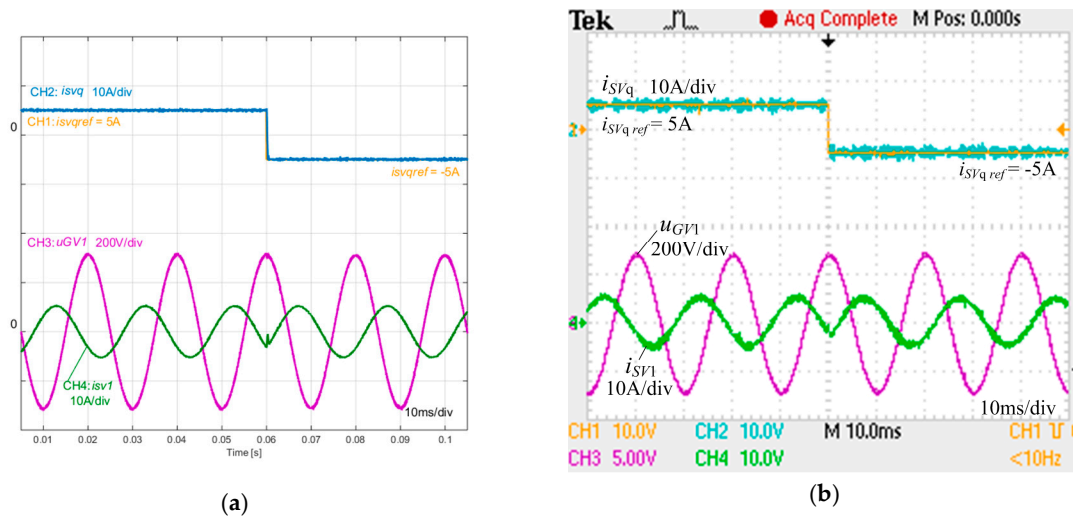
Figure 7. Phase current control: (**a**) Simulation result, CH1: i_{SVqref}, 10 A/div; CH2: i_{SVq}, 10 A/div; CH3: u_{GV1}, 200 V/div; CH4: i_{SV1}, 10 A/div; 10 ms/div; (**b**) Experimental result, CH1: i_{SVqref}, 10 A/div; CH2: i_{SVq}, 10 A/div; CH3: u_{GV1}, 200 V/div; CH4: i_{SV1}, 10 A/div; 10 ms/div.

From Figures 6 and 7, it can be seen that the backward Euler stabilized control strategy accurately tracks the current references in a steady state or during a step in the i_{SVd} or i_{SVq} reference, respectively. The measured current ripple was less than 0.25 A in 5 A (<5%).

The time evolution of the capacitor voltages during the step transitions of Figures 6 and 7 are presented in Figure 8a,b respectively. From Figure 8, it can be seen that the deviation of the capacitor voltages, $u_{C1\ldots4}$, is around 1.5 V over 150 V (1%).
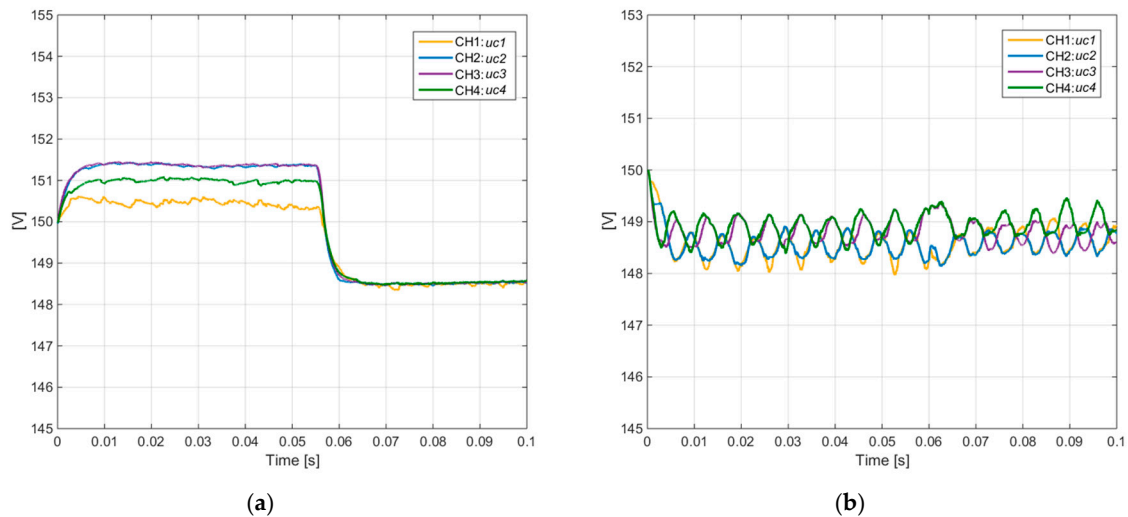

Figure 8. Capacitor voltage balancing during the step transition of: (**a**) Figure 6 and (**b**) Figure 7, CH1: u_{C1}; CH2: u_{C2}; CH3: u_{C3}; CH4: u_{C4}; 1 V/div; 10 ms/div.

The proposed control strategy achieves high output modulation indexes, $m_o = \hat{u}_{GV}/u_{dc}$, even in the most difficult operation conditions for a NPC back-to-back connection with an active load, that is, with no active power exchange [4]. Table 4 shows the operation conditions of the simulation results presented in Figure 9, and displays the 1st harmonic $u_{GV12\text{-}1h}$ of the output line-to-line voltage.

Table 4. Operation conditions of Figure 9.

Figure	u_{GR}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
9	230 V	0	600 V	0	Step: 5 A to −5 A	230 V
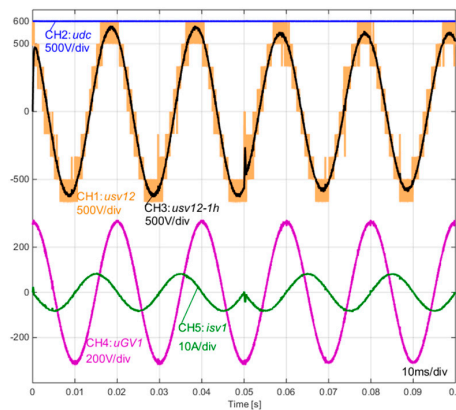
Figure 9. First harmonic of the u_{GV} line to line voltage simulation result. CH1: u_{SV12}, 500 V/div; CH2: u_{dc}, 500 V/div; CH3: $u_{SV12\text{-}1h}$, 500 V/div; CH4: u_{GV1}, 200 V/div; CH5: i_{SV1}, 10 A/div; 10 ms/div.

The simulation results of Figure 9 were obtained using a modulation index around m_o = 0.93. This result clearly shows the limits extension of the proposed control strategy, when compared with redundant vector-based strategies as sinusoidal pulse width modulation (SPWM) or space vector modulation (SVM) [3,4] (the theoretical maximum output modulation index is around 0.6).

4.2. DC-bus Voltage Control and Capacitors Voltage Balancing

DC-bus voltage control robustness is verified by applying a grid side voltage sag perturbation of a 25% nominal voltage, for which the operation conditions are presented in Table 5 and the results are shown in Figure 10. It can be seen that the DC-bus voltage remains almost constant through a sag perturbation on the main grid voltage. The maximum voltage disturbance measured was 50 V in 600 V (<9%).

Table 5. Operation conditions of Figure 10.

Figure	u_{GR1}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
10	230 V | 170 V | 230 V	0	600 V	−5 A	0	230 V
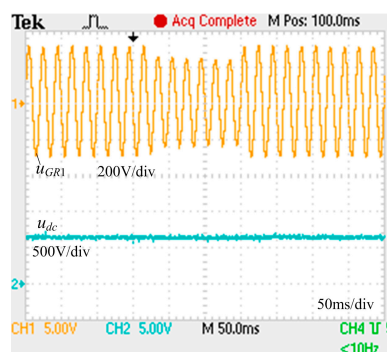
Figure 10. DC-bus voltage control experimental result, CH1: u_{GR1}, 200 V/div; CH2: u_{dc}, 500 V/div; 50 ms/div.

The voltage balancing of the capacitors is tested by restarting the voltage balancing algorithm, which means that $\rho_C \neq 0$, after a time interval without considering it ($\rho_C = 0$). The operating conditions are presented in Table 6 and the results are shown in Figure 11. From Figure 11, it can be seen that the four capacitor voltages $u_{C1\ldots4}$ deviate from the reference during the time interval without voltage balancing. After restarting the voltage balancing algorithm, the backward Euler stabilized control strategy has the capability to rapidly restore the capacitor voltage balance.

Table 6. Operation conditions of Figure 11.

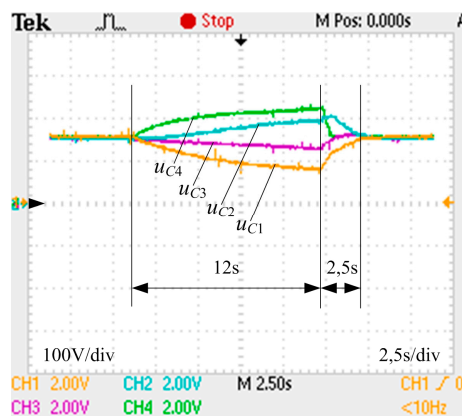| Figure	ρ_C	u_{GR1}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
11	15 | 0 | 15	230 V	0	600 V	−2.5 A	0	230 V

Figure 11. Capacitor voltage balancing experimental result, CH1: u_{C1}; CH2: u_{C2}; CH3: u_{C3}; CH4: u_{C4}; 100 V/div; 2.5 s/div.

4.3. Power Flow Control

Several conditions can be imposed in order to test power flow control. Figures 12 and 13 show the i_{SVd} reference, phase current, and u_{dc} voltage for two different power flow conditions, presented in Table 7.
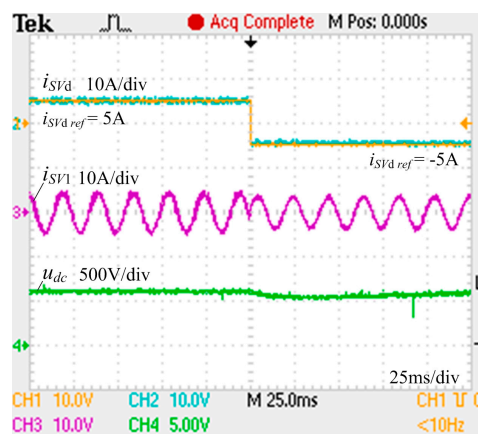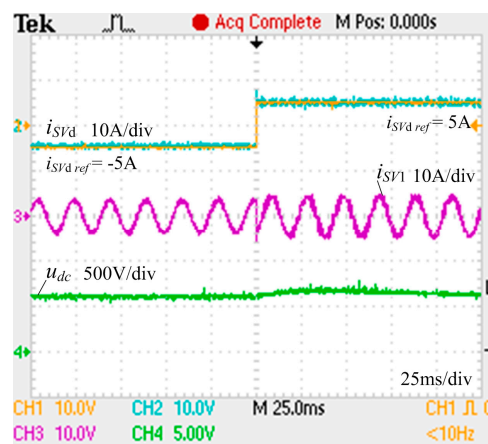

Figure 12. DC-bus voltage and phase current experimental result. CH1: i_{SVdref}, 10 A/div; CH2: i_{SVd}, 10 A/div; CH3: i_{SV1}, 10 A/div; CH4: u_{dc}; 500 V/div; 25 ms/div.

Figure 13. DC-bus voltage and phase current experimental result. CH1: i_{SVdref}, 10 A/div; CH2: i_{SVd}, 10 A/div; CH3: i_{SV1}, 10 A/div; CH4: u_{dc}, 500 V/div; 25 ms/div.

Table 7. Operation conditions of Figures 12 and 13.

Figure	u_{GR}	i_{SRq}	u_{dc}	i_{SVd}	i_{SVq}	u_{GV1}
11	230 V	0	600 V	Setp: 5 A to -5 A	0	230 V
12	230 V	0	600 V	Setp: -5 A to 5 A	0	230 V

From Figures 12 and 13, it is possible to see the u_{dc} recovery after a negative or positive step in active power flow, respectively. The experimental results obtained attest the good performance of the proposed control strategy.

From [19,21,24], the comparison presented in Table 8 can be obtained. Although the results are not directly comparable, since some of them refer to three-level converters, while the herein results are for five-level converters, it can be said that the backward Euler-based controller shows results which are better than PI controllers and are comparable to the best results obtained by advanced controllers.

Table 8. Backward Euler stabilized controller compared with existing control methods.

Method	Proportional Integral	Proportional Integral-Resonant	Sliding Mode	Predictive Optimum	Fast Predictive	Backward Euler
THD of AC currents	5.8%	7.5%	7%	4.6%	1.5%	<1.5%
DC-bus voltage unbalance	8%	-	-	-	1%	1%

5. Conclusions

The proposed backward Euler stabilized control strategy based on a generalized model of a five level NPC back-to-back converter, is able to control both the converter AC currents and to balance the four capacitor voltages.

From the active and reactive power flow of the convertors, in addition to the DC-bus voltage references, the control strategy computes, using the stable backward Euler approach, the optimum voltage or current vectors required to reach the references in the next time step. The selection of the converter output voltage vector is done by minimizing a variable weight cost functional within a sampling period. The minimum value of the cost functional gives the converter output voltage vector. The modified cost functional with variable weight allows converter control in a wide range of operating conditions.

Simulation and experimental results were obtained using a 230 V ac/600 V dc/230 V ac five level NPC back-to-back prototype. Both NPC converters are controlled with one Power PC-based board (DS1103) with a 32 μs sampling time.

The results demonstrate the feasibility and robustness of the proposed control strategy, achieving a very good compromise covering the main tasks: AC current tracking errors were lower than 5% and the DC-bus capacitor voltage balancing was within 10%. When compared with redundant vector-based control techniques, the proposed control strategy shows the extension of the modulation index, from 0.6 to 0.93.

Author Contributions: M. Chaves, J. F. Silva and E. Margato conceived the theory and designed the experiments; M. Chaves performed the experiments; M. Chaves, S. F. Pinto and J. Santana analyzed the data; M. Chaves, J. F. Silva, S. F. Pinto J. and J. Santana wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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