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Output Voltage Quality Evaluation of Stand-alone Four-Leg Inverters Using Linear and Non-Linear Controllers

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Academic Editor: José Gabriel Oliveira Pinto
Received: 7 February 2017; Accepted: 29 March 2017; Published: 9 April 2017

Abstract: This paper presents the design and experimental voltage quality evaluation of controllers for the output voltages of 3-phase four-leg voltage source inverters. These inverters are needed in stand-alone power systems to supply linear and non-linear, balanced or unbalanced loads with constant RMS value voltages at fixed frequency. Comparisons include closed loop outer voltage controllers based on predictive, sliding mode and decoupled proportional-integral controllers in *dqo* synchronous space, fitted with an inner hysteretic current loop vector controller in $\alpha\beta\gamma$ space. The 3-phase four-leg VSI output voltages waveform quality is analysed under unbalanced and non-linear loads.

Keywords: stand-alone four-leg inverter; non-linear voltage vector modulator; voltage waveform quality

1. Introduction

Many electric power systems, such as distributed generation systems, variable frequency fed stand-alone power systems, uninterruptible power supplies and active filters need the use of power electronic converters. These power converters, in a back-to-back connection, can output sinusoidal voltages with precise amplitude frequency, even if the stand-alone generator is operating at variable speed (frequency) to maximise its efficiency. Voltage source inverters (VSI) are commonly used to transfer power between a DC system to an AC system or to work as back-to-back power electronic converter to connect AC systems with different frequencies [1].

In three-phase low-voltage electric systems a neutral wire is usually needed to provide a current path for linear/non-linear unbalanced loads or to feed single-phase loads. Therefore, the 3-phase VSI must have an extra wire connection to the load neutral, becoming a four-wire inverter.

Four-wire inverters are capable of supplying unbalanced and/or non-linear loads connected to stand-alone power supply systems. Besides, they accept input power at any frequency from a rectifier, which is important to allow variable frequency generators. This solution avoids the use of the electric transformer Δ-Yg to obtain an access to neutral point [2,3]. The neutral wire can be formed from the inverter using three different topologies:

- 3-phase 4-wire. The neutral point is connected to midpoint of the DC-link capacitors [3–5];
- 3-phase four-leg. With an additional inverter leg enabling the neutral voltage control [6–8];
- a combination of DC split capacitors and the neutral leg. The control of the neutral point is decoupled from the control of the 3-phase VSI [9].

The first solution uses the 3-phase inverter that can be controlled as three independent single-phase inverters. The disadvantage for the split capacitor converter is the large and expensive DC-link capacitors needed to maintain acceptable voltage ripple level across the DC-link capacitors in case of a large zero-sequence current due to unbalanced or non-linear load [6]. However, this topology has advantages, saving two power semiconductors and reducing control complexity [3]. The four-leg VSI solution requires two additional power switches, but it offers advantages, such as an increased maximum output voltage value, a reduction of neutral currents and the possibility of neutral voltage control [6]. In the third solution, the neutral point is still provided by two split capacitors and the fourth leg is really an active filter independent from the 3-phase legs. Thus, the fourth leg is controlled to cancel the zero-sequence current in unbalanced or non-linear loads, so that the neutral current does not flow through the DC-link capacitors. This approach needs a smaller DC-link capacitance for the same voltage ripple. However, it still suffers from insufficient use of the DC-link voltage as the first topology [10]. Considering the merits and demerits of topologies for the 3-phase VSIs, in this study the four-leg VSI is considered for their advantages to high-performance applications, where a good power quality might be required, or when sensitive electronics equipment are used as four-leg VSI loads [10].

The four-leg VSI applicability to stand-alone power systems should take into account the control of the DC-link voltage, since the load transients on AC side may cause disturbances in the four-leg VSI DC side [11]. Based on the stand-alone power sources that feed the four-leg inverter, a short-term or a long-term response energy storage system [12,13], should be considered to minimize the effect of disturbance transients analyzed in DC-link and to allow the four-leg inverter correct operation. In this paper, the control of DC voltage side is not presented, but it uses a supercapacitor energy storage system [14], that keeps the DC voltage within a maximum deviation of 4% from its nominal value, during the presented transient tests [15].

Considering performance, this paper presents the converter model and designs, evaluates and compares output voltage control loops based on predictive, sliding mode and proportional-integral controllers in dqo synchronous space. An internal hysteretic current loop vector controller in $\alpha\beta\gamma$ space is common to all the voltage controllers. The paper is organized as follows: Section II presents the four-leg VSI modelling. The four-leg VSI current loop vector controller in $\alpha\beta\gamma$ space is described in section III and voltage controllers are presented and discussed in section IV. In section V a performance evaluation of four-leg VSI with unbalanced and non-linear loads is presented. The paper closes with the conclusions and future work on this subject.

2. Four-Leg VSI Modelling

The 3-phase four-leg VSI supplied by a constant DC voltage, u_{DC}, and the output LC filter are show in Figure 1. The outputs of four-leg VSI are denoted by phases a, b, c and the neutral n terminals and the LC filter output terminals denoted by A, B, C, and N (neutral). The three-phase LC filter reduces the output waveform carrier frequency components content. The semiconductors S_{1k} and S_{2k} are considered to be ideal. Their states can be represented by a leg switching variable, γ_k, where $k = \{a, b, c, n\}$ (1).

$$\delta_k = \begin{cases} 0 \Rightarrow S_{1k} = 0 \text{ and } S_{2k} = 1 \\ 1 \Rightarrow S_{1k} = 0 \text{ and } S_{2k} = 0 \end{cases}, k = \{a, b, c, n\} \quad (1)$$

The voltages u_a, u_b, u_c, u_n measured between the terminals a, b, c, n and the negative DC-link of the four-leg VSI, can be expressed as in (2).

$$u_k = \gamma_k u_{DC} \quad (2)$$

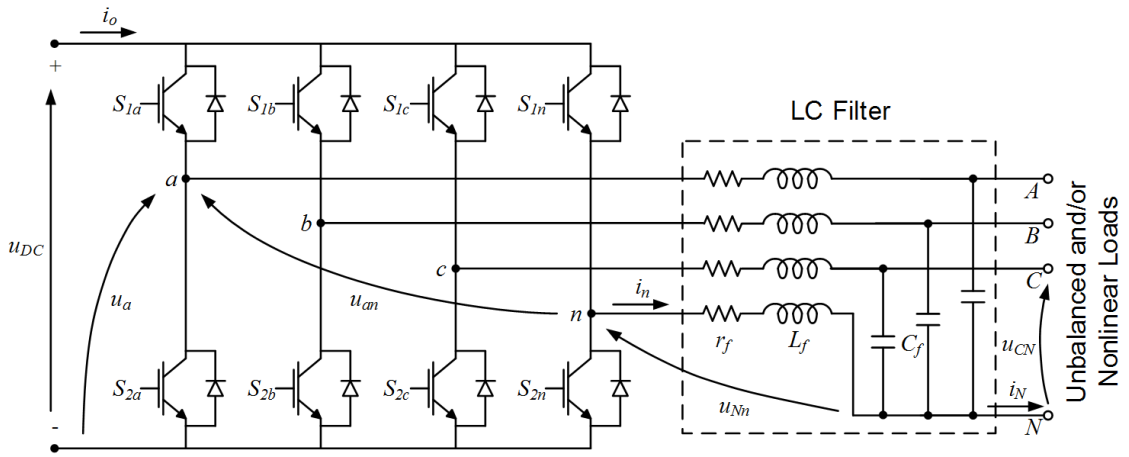


Figure 1. Three-phase four-leg VSI and output LC filter.

The phase voltages of the four-leg inverter, u_{an}, u_{bn}, u_{cn} are expressed in matrix form:

$$\begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = u_{DC} \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} \gamma_a \\ \gamma_b \\ \gamma_c \\ \gamma_n \end{bmatrix} \tag{3}$$

The state-space matrix equations to calculate the four-leg VSI currents, i_a, i_b and i_c, can be outlined as (4).

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -\frac{r_f}{L_f} \mathbf{I_3} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L_f^{-1} \begin{bmatrix} u_{an} - u_{AN} - u_{Nn} \\ u_{bn} - u_{bN} - u_{Nn} \\ u_{cn} - u_{cN} - u_{Nn} \end{bmatrix} \tag{4}$$

In (4), r_f and L_f represent, respectively, the LC filter parasite resistance and inductance per phase. The i_a, i_b, i_c and i_n represents, respectively, the four-leg VSI currents flowing in outer direction of the a, b, c, and n terminals. The u_{AN}, u_{BN}, u_{CN} are the three phase-neutral load voltages and u_{Nn} the voltage drop on neutral inductance filter. The $\mathbf{I_3}$ represents the 3 by 3 identity matrix. The phase-neutral u_{AN}, u_{BN}, u_{CN} voltages are derived from capacitor voltages equations in state-space form (5).

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = \frac{1}{C_f} \begin{bmatrix} i_a - i_A \\ i_b - i_B \\ i_c - i_C \end{bmatrix} \tag{5}$$

In (5), i_{ABC} represents the 3-phase load currents and C_f is the LC filter capacitance. For unbalanced loads the neutral currents, i_n and i_N, are obtained from Kirchhoff's first law of four-leg VSI currents circuit analysis (6).

$$\begin{aligned} i_n &= -\left(i_a + i_b + i_c\right) \\ i_N &= -\left(i_A + i_B + i_C\right) \end{aligned} \tag{6}$$

The DC-link current, i_o, depends of the switching state of each VSI leg, γ_k, and the output currents, by (7).

$$i_o = \gamma_a i_a + \gamma_b i_b + \gamma_c i_c + \gamma_n i_n \tag{7}$$

3. Current Loop Vector Controller

3.1. Four-Leg VSI Output Voltage Vectors in Stationary αβγ Reference Frame

Using the Concordia matrix transformation [16], the voltages quantities in $\alpha\beta\gamma$ stationary reference frame, u_α, u_β and u_γ are obtained. Depending on the γ_k state values, the four-leg VSI has 2^4 possible states. Figure 2 presents the voltage vectors in $\alpha\beta\gamma$ space, $V_j(\gamma_n, \gamma_c, \gamma_b, \gamma_a)$, where $j = \{0, 1, 2, ..., 15\}$ represents the voltage vector number. The projection of the all voltages vectors in $\alpha\beta$ plane match the well-known 3-leg VSI eight output voltages plane.

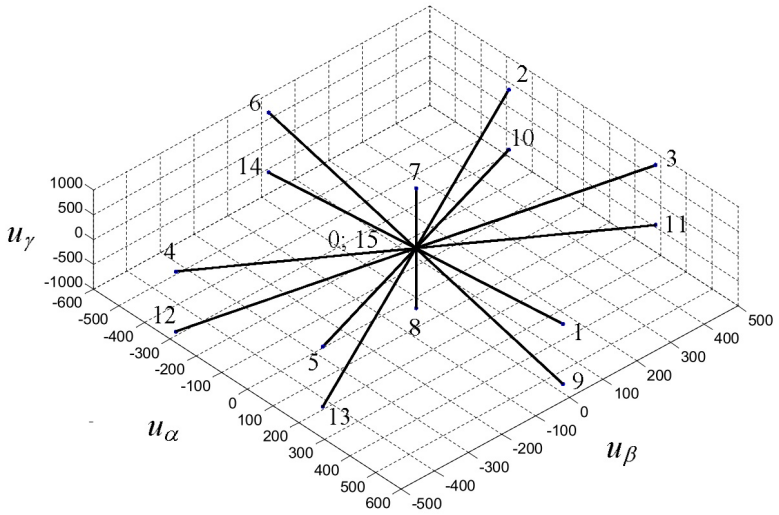


Figure 2. Four-leg output voltage vectors in $\alpha\beta\gamma$ space.

3.2. Current Loop Vector Controller

For short circuit protection and power limitation, an inner current control loop is adopted with a vector control strategy on the stationary α, β, γ space reference. The outer synchronous *dqo* frame voltage loops generate constant output voltages with constant frequency to supply both linear/non-linear, balanced/unbalanced loads, Figure 3.

The current loop vector controller (CVC) for the four-leg VSI is derived from the previously proposed vector current control for 3-phase 3-leg VSIs under balanced loads, that selects a suitable vector out of the 2^3 possible voltage vectors in the $\alpha\beta$ plane reference [14,15]. This technique is here extended to the 3-phase four-leg VSI, considering now the 2^4 $u_\alpha, u_\beta, u_\gamma$ voltage vectors.

The input references currents, i_d^*, i_q^*, and i_o^*, are transformed to new input reference currents, i_α^*, i_β^*, and i_γ^*, using the $dqo - \alpha\beta\gamma$ rotational matrix transformation [16]. The angular electrical speed and position are represented by, ω_e and θ_e, respectively. The measured four-leg VSI output currents are also transformed to $\alpha\beta\gamma$ coordinates using the Concordia transformation matrix. Comparing the references and output currents the errors of each $\alpha\beta\gamma$ components, $e_{i\alpha}$, $e_{i\beta}$ and $e_{i\gamma}$, are obtained (8).

$$e_{i\kappa} = i_\kappa^* - i_\kappa \ , \ \kappa \in \{\alpha, \beta, \gamma\} \tag{8}$$

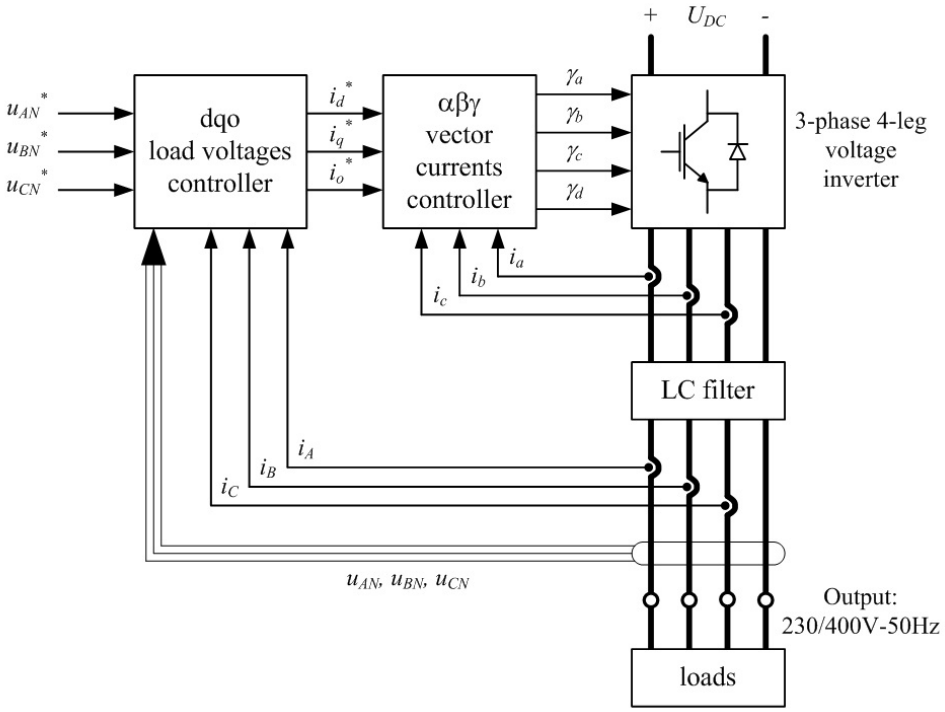


Figure 3. The 3-phase four-leg VSI and their main control blocks.

The CVC uses three hysteretic comparators to evaluate the current errors in three discrete values: negative, null and positive (9).

$$\delta_\kappa = \begin{cases} 1 & \text{if} \quad e_{i\kappa} > +\Delta \\ 0 & \text{if} \quad -\Delta < e_{i\kappa} < +\Delta \\ -1 & \text{if} \quad e_{i\kappa} < -\Delta \end{cases} \tag{9}$$

In (9), Δ is the hysteresis band width and δ_κ the output values of hysteretic comparators, δ_α, δ_β and δ_γ. Equation (4) can be written in a compact form using $\alpha\beta\gamma$ coordinates from the Concordia transformation matrix:

$$u_\kappa = Ri_\kappa + L\frac{\mathrm{d}i_\kappa}{\mathrm{d}t} - v_\kappa \ , \ \kappa \in \{\alpha, \beta, \gamma\} \tag{10}$$

The CVC control strategy is described by (11). The selection of the $\alpha\beta\gamma$ voltage vector is obtained by the needed $\alpha\beta\gamma$ current time derivatives, according to (10).

$$\delta_\kappa = \begin{cases} 1 & \Rightarrow & i_\kappa^* > i_\kappa & \Rightarrow & \frac{\mathrm{d}i_\kappa}{\mathrm{d}t} > 0 & \Rightarrow & u_\kappa > 0 \\ 0 & \Rightarrow & i_\kappa^* \approx i_\kappa & \Rightarrow & \frac{\mathrm{d}i_\kappa}{\mathrm{d}t} \approx 0 & \Rightarrow & u_\kappa = 0 \\ -1 & \Rightarrow & i_\kappa^* < i_\kappa & \Rightarrow & \frac{\mathrm{d}i_\kappa}{\mathrm{d}t} < 0 & \Rightarrow & u_\kappa < 0 \end{cases} \tag{11}$$

Table 1 presents the voltage vector selection, based on the analysis of the current errors. In some cases more than one vector can be selected. The voltage vector decision, in the case where more than one vector is available, is solved considering the sum of two comparators output states with two different hysteretic levels, large and narrow, $\delta_{L\kappa}$ and $\delta_{N\kappa}$, respectively, with $\kappa \in \{\alpha, \beta, \gamma\}$. Figure 4 the $\alpha\beta\gamma$ vector currents controller using 3-level hysteretic comparators, δ_κ, as a sum of large and narrow 2-level hysteretic comparators, $\delta_{L\kappa}$ and $\delta_{N\kappa}$, respectively [17]. In (12), this approach is shown to solve the multiple voltage vectors decision, using an example of Table 1 where $(\delta_\alpha = 0) \wedge (\delta_\beta = -1) \wedge (\delta_\gamma = 0)$.

Table 1. Voltage vector selection.

δ_γ	δ_β	δ_α	**Vector** j
−1	−1	−1	12
−1	−1	0	12; 13
−1	−1	1	13
−1	0	−1	14
−1	0	0	8
−1	0	1	9
−1	1	−1	10
−1	1	0	10; 11
−1	1	1	11
0	−1	−1	4; 12
0	−1	0	5; 12; 4; 13
0	−1	1	5; 13
0	0	−1	0; 15; 6; 14
0	0	0	0; 15
0	0	1	0; 15; 1; 9
0	1	−1	2; 10
0	1	0	2; 11; 3; 10
0	1	1	3; 11
1	−1	−1	4
1	−1	0	4; 5
1	−1	1	5
1	0	−1	6
1	0	0	7
1	0	1	1
1	1	−1	2
1	1	0	2; 3
1	1	1	3

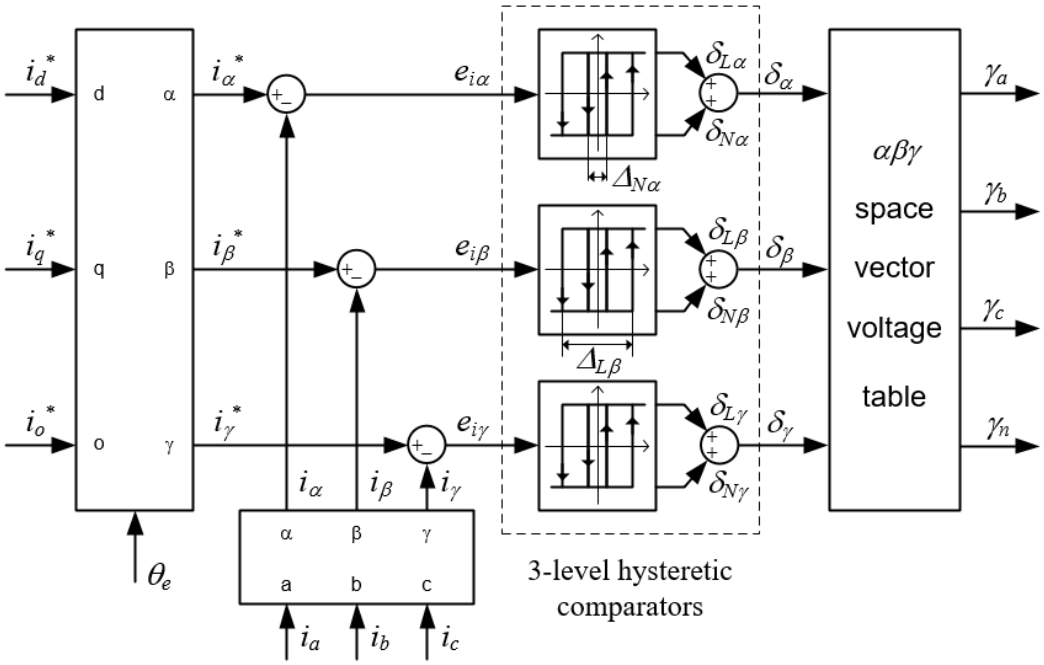


Figure 4. The $\alpha\beta\gamma$ vector currents controller using 3-level hysteretic comparators.

$$\left.\begin{array}{l}\delta_{L\alpha}>0\Rightarrow\delta_{N\alpha}<0\Rightarrow\frac{\mathrm{d}i_{\alpha}}{\mathrm{d}t}<0\\ \delta_{L\gamma}>0\Rightarrow\delta_{N\gamma}<0\Rightarrow\frac{\mathrm{d}i_{\gamma}}{\mathrm{d}t}<0\end{array}\right\}\Rightarrow V_{12}$$
$$\left.\begin{array}{l}\delta_{L\alpha}>0\Rightarrow\delta_{N\alpha}<0\Rightarrow\frac{\mathrm{d}i_{\alpha}}{\mathrm{d}t}<0\\ \delta_{L\gamma}<0\Rightarrow\delta_{N\gamma}>0\Rightarrow\frac{\mathrm{d}i_{\gamma}}{\mathrm{d}t}>0\end{array}\right\}\Rightarrow V_{4}$$
$$\left.\begin{array}{l}\delta_{L\alpha}<0\Rightarrow\delta_{N\alpha}>0\Rightarrow\frac{\mathrm{d}i_{\alpha}}{\mathrm{d}t}>0\\ \delta_{L\gamma}<0\Rightarrow\delta_{N\gamma}>0\Rightarrow\frac{\mathrm{d}i_{\gamma}}{\mathrm{d}t}>0\end{array}\right\}\Rightarrow V_{13}$$
$$\left.\begin{array}{l}\delta_{L\alpha}<0\Rightarrow\delta_{N\alpha}>0\Rightarrow\frac{\mathrm{d}i_{\alpha}}{\mathrm{d}t}>0\\ \delta_{L\gamma}>0\Rightarrow\delta_{N\gamma}<0\Rightarrow\frac{\mathrm{d}i_{\gamma}}{\mathrm{d}t}<0\end{array}\right\}\Rightarrow V_{13} \quad (12)$$

The condition $(\delta_{\alpha}=0)\wedge(\delta_{\beta}=0)\wedge(\delta_{\gamma}=0)$ implies the decision of the null voltage vectors, 0 or 15, to minimize the switching frequency, reducing the four-leg VSI switching losses. A simple algorithm to minimize the semiconductors commutations can be applied. The current error output states and the switching frequency of semiconductor devices depend on the hysteretic comparator window width. Reducing the hysteretic window leads to reduced current errors (ripple), but increases the semiconductor switching frequency. The optimum value of the width of hysteresis window should be balanced for currents admissible ripple and power converter switching losses.

Figure 5 shows the simulation of the 3-phase four-leg VSI currents with CVC. Unbalanced currents reference and linear loads were considered to obtain these results. The phase and neutral current references, i_a^*, i_b^*, i_c^* and i_n^*, respectively, are enclosed by the corresponding output currents ripple of the four-leg VSI.

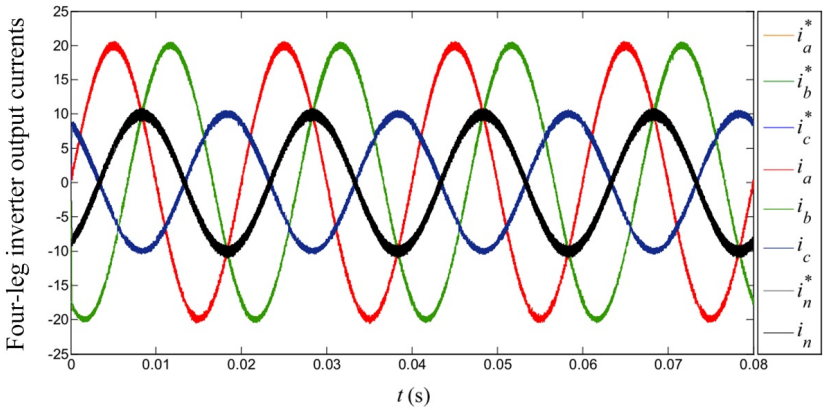


Figure 5. Simulation result of 3-phase four-leg VSI with $\alpha\beta\gamma$ vector currents controller with current references to unbalanced load.

4. Load Voltage Control

This section explains the design of optimal load voltage controllers that preserve the constant magnitude phase difference and frequency of symmetrical 3-phase sinusoidal load voltages. Starting from the load voltages dynamic model, a non-linear voltage controller is deduced from two control methods: the predictive control (Section 4.1) and the sliding mode control (Section 4.2); and for comparison purposes the classical PI controller (Section 4.3). Considering the Blondel-Park matrix transformation, $\mathbf{C}(\theta_e)$ [16], and using the compact form relations (13), the load voltages dynamic model in (5), are expressed in the synchronous dqo frame reference, by (14).

$$\begin{bmatrix} u_d & u_q & u_o \end{bmatrix}^{\mathsf{T}} = \mathbf{C}(\theta_e)^{\mathsf{T}} \begin{bmatrix} u_{AN} & u_{BN} & u_{CN} \end{bmatrix}^{\mathsf{T}}$$
$$\begin{bmatrix} i_d & i_q & i_o \end{bmatrix}^{\mathsf{T}} = \mathbf{C}(\theta_e)^{\mathsf{T}} \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^{\mathsf{T}} \quad (13)$$
$$\begin{bmatrix} i_{Ld} & i_{Lq} & i_{Lo} \end{bmatrix}^{\mathsf{T}} = \mathbf{C}(\theta_e)^{\mathsf{T}} \begin{bmatrix} i_A & i_B & i_C \end{bmatrix}^{\mathsf{T}}$$

$$\begin{aligned} \frac{\mathrm{d}u_d}{\mathrm{d}t} &= \omega_e u_q + \frac{1}{C_f} i_d - \frac{1}{C_f} i_{Ld} \\ \frac{\mathrm{d}u_q}{\mathrm{d}t} &= -\omega_e u_d + \frac{1}{C_f} i_q - \frac{1}{C_f} i_{Lq} \\ \frac{\mathrm{d}u_o}{\mathrm{d}t} &= \frac{1}{C_f} i_o - \frac{1}{C_f} i_{Lo} \end{aligned} \tag{14}$$

In (14), the voltages u_d, u_q, u_o, and the currents i_d, i_q, i_o, represent, respectively, the u_{an}, u_{bn}, u_{cn} and i_a, i_b, i_c, four-leg VSI outputs voltages and currents, in *dqo* coordinates. In same way, i_{Ld}, i_{Lq}, i_{Lo}, represent the 3-phase line loads currents i_A, i_B, i_C.

4.1. Load Voltage Optimal Predictive Control

The main goal of Optimal Predictive Control (OPC), is to estimate the values of the *dqo* frame CVC current references, i_d^*, i_q^*, i_o^*, that minimize voltage errors [17,18]. From the four-leg inverter output voltages dynamic model, described by (14), system stability conditions for predictive control are defined (15).

$$\begin{aligned} & e_{um} = u_m^* - u_m \simeq 0 \\ & e_{um} \frac{\mathrm{d}e_{um}}{\mathrm{d}t} < 0 \qquad\qquad , m \in \{d, q, o\} \\ & \frac{\mathrm{d}e_{um}}{\mathrm{d}t} = -\alpha_{um} e_{um} \end{aligned} \tag{15}$$

In (15), e_{um}, u_m^* represent the voltage errors vector and the voltage references vector, respectively. The α_{um} is a vector with the *dqo* controllability constants. Manipulating (15) together with (14) and considering $\alpha_{ud} = \alpha_{uq} = \alpha_{uo} = \alpha_u$, the load voltages control laws are obtained (16).

$$\begin{aligned} i_d^* &= C_f \frac{u_d^* - u_d}{\alpha_u^{-1}} + C_f \frac{\mathrm{d}u_d^*}{\mathrm{d}t} - C_f \omega_e u_q + i_{Ld} \\ i_q^* &= C_f \frac{u_q^* - u_q}{\alpha_u^{-1}} + C_f \frac{\mathrm{d}u_q^*}{\mathrm{d}t} + C_f \omega_e u_d + i_{Lq} \\ i_o^* &= C_f \frac{u_o^* - u_o}{\alpha_u^{-1}} + C_f \frac{\mathrm{d}u_o^*}{\mathrm{d}t} + i_{Lo} \end{aligned} \tag{16}$$

4.2. Load Voltage Sliding Mode Control

To design load voltage sliding mode controllers (SMC) able to ensure sinusoidal load voltages, sliding mode surfaces, must be obtained from the load voltage dynamic model (14) [17,19]. The three sliding surfaces, $S(e_{um}, t)$ [20,21], are expressed based on *dqo* frame voltage errors (17).

$$S(e_{um}, t) = e_{um} + \beta_{um} \frac{\mathrm{d}e_{um}}{\mathrm{d}t} = 0 \quad , m \in \{d, q, o\} \tag{17}$$

In (17) the β_{um} gains are related to the first order errors decay to zero [22]. Substituting (14) in the load voltages sliding mode surfaces (17), and considering $\beta_{ud} = \beta_{uq} = \beta_{uo} = \beta_u$, the control laws are obtained (18).

$$\begin{aligned} i_d^* &= C_f \frac{u_d^* - u_d}{\beta_u} + C_f \frac{\mathrm{d}u_d^*}{\mathrm{d}t} - C_f \omega_e u_q + i_{Ld} \\ i_q^* &= C_f \frac{u_q^* - u_q}{\beta_u} + C_f \frac{\mathrm{d}u_q^*}{\mathrm{d}t} + C_f \omega_e u_d + i_{Lq} \\ i_o^* &= C_f \frac{u_o^* - u_o}{\beta_u} + C_f \frac{\mathrm{d}u_o^*}{\mathrm{d}t} + i_{Lo} \end{aligned} \tag{18}$$

Comparing the SMC with OPC, it can be seen that the control laws of (18) and (16), respectively, are similar. Both non-linear controllers, SMC and OPC, lead to the same control solution if $\beta_{um} = \alpha_{um}^{-1}$. Also in SMC and OPC, the AC phase-neutral load voltages references, u_{AN}^*, u_{BN}^*, u_{CN}^*, are a balanced system, the *dqo* frame load voltages references, u_{dqo}^*, are constant in time. Then, the derivatives terms of load voltages references can be neglected in the steady-state.

To avoid large outputs of the derivative term given at high frequency or noise, from (18), the derivative term is modified by using a first-order high-pass filter to apply the derivative action only to low and medium frequencies [23]. For digital signal implementation of the output voltage non-linear output controller, from (16) or (18), a discrete-time model of the CVC current references is used (19).

$$\begin{aligned} i_d^*(t_{s+1}) &= C_f \frac{u_d^*(t_{s+1}) - u_d(t_s)}{\Delta t_u} - C_f \omega_e u_q(t_s) + i_{Ld}(t_s) \\ i_q^*(t_{s+1}) &= C_f \frac{u_q^*(t_{s+1}) - u_q(t_s)}{\Delta t_u} + C_f \omega_e u_d(t_s) + i_{Lq}(t_s) \\ i_o^*(t_{s+1}) &= C_f \frac{u_o^*(t_{s+1}) - u_o(t_s)}{\Delta t_u} + i_{Lo}(t_s) \end{aligned} \tag{19}$$

In (19), t_s and t_{s+1}, are the actual and the next time sampling step Δt_u, respectively. The non-linear controller laws considers that the sampled *dqo* frame load voltages, $u_d(t_s)$, $u_q(t_s)$, $u_o(t_s)$, will follow their voltages references, $u_d(t_{s+1})$, $u_q(t_{s+1})$, $u_o(t_{s+1})$, in one voltage control loop sampling time, Δt_u. The actual time line load currents are represented in *dqo* frame by i_{Ld}, i_{Lq}, i_{Lo}.

As can be seen from (14) the direct and quadrature axes are coupled through $\omega_e C_f$ term. The non-linear controller (19) uses decoupling terms to cancel this coupling. The currents, i_{Ld}, i_{Lq} and i_{Lo} are measured and used to calculate the current references, i_d^*, i_q^*, i_o^*.

4.3. Load Voltage Decoupled PI Control

To use simple PI controllers it is necessary to decouple the cross coupling terms of the load voltage dynamic model (14). This can be done with two auxiliary variables [18], h_d and h_q, defined by (20).

$$\begin{aligned} h_d &= i_d + C_f \omega_e u_q \\ h_q &= i_q - C_f \omega_e u_d \end{aligned} \tag{20}$$

Substituting (20) in (14), a decoupled model for the load voltages control can be obtained and the PI controllers, $C_m(s)$, with proportional and integral gains, K_{pm} and K_{im}, respectively, could be designed for each *dqo* frame control loop in the frequency-domain, taking into account a first order dynamics CVC model, $\frac{h_m(s)}{h_m^*(s)}$, with unitary gain and T_d as the dominant pole of average delay time, due the switching period of four-leg inverter, and $m \in \{d, q, o\}$, Figure 6.

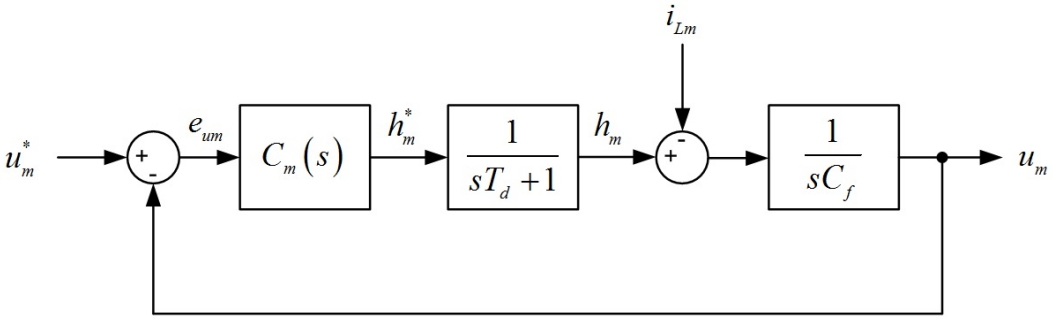


Figure 6. Block diagram of closed loop four-leg inverter output voltage control, considering the decoupled PI controllers.

Two implementations of decoupled PI (DPI) controllers are considered the common implementation given by (21) and an alternative PI controller implementation, where the proportional gain, K_{pm} is applied only to the output signal (22).

$$h_m^* = K_{pm}(u_m^* - u_m) + \frac{K_{im}}{s}(u_m^* - u_m) \tag{21}$$

$$h_m^* = -K_{pm} u_m + \frac{K_{im}}{s}(u_m^* - u_m) \tag{22}$$

The closed loop transfers functions of four-leg inverter output voltage, $\frac{u_m(s)}{u_m^*(s)}$, considering the two DPI approaches of (21) and (22) are given by (23) and (24), respectively.

$$\frac{u_m(s)}{u_m^*(s)} = \frac{s\frac{K_{pm}}{C_f T_d} + \frac{K_{im}}{C_f T_d}}{s^3 + s^2\frac{1}{T_d} + s\frac{K_{pm}}{C_f T_d} + \frac{K_{im}}{C_f T_d}} \tag{23}$$

$$\frac{u_m(s)}{u_m^*(s)} = \frac{\frac{K_{im}}{C_f T_d}}{s^3 + s^2\frac{1}{T_d} + s\frac{K_{pm}}{C_f T_d} + \frac{K_{im}}{C_f T_d}} \tag{24}$$

The transfer function between the disturbance and the output voltage, $\frac{u_m(s)}{i_{Lm}(s)}$, is given by (25).

$$\frac{u_m(s)}{i_{Lm}(s)} = -\frac{s\frac{sT_d+1}{C_f T_d}}{s^3 + s^2\frac{1}{T_d} + s\frac{K_{pm}}{C_f T_d} + \frac{K_{im}}{C_f T_d}} \tag{25}$$

From (24) or (25), the PI gains, K_{pm} and K_{im}, of each dqo closed loop transfer function, $\frac{u_m(s)}{u_m^*(s)}$, are obtained by the ITAE criteria (integral function of time multiplied by the absolute magnitude of the error) in order to allow good disturbance rejection, considering the third-order system optimum coefficients for a step input [23] (26).

$$\begin{aligned} K_{pm} &= \frac{2.15 C_f T_d}{(1.75T_d)^2} \\ K_{im} &= \frac{C_f T_d}{(1.75T_d)^3} \end{aligned} \quad , m \in \{d, q, o\} \tag{26}$$

Figure 7 presents the step responses for both DPI controllers taking as an example the u_q output voltage loop control. The usual PI controller presents a large overshoot, 46%, and the modified PI reduces the overshoot to 2%. The settling time is very close for both PI controllers, 1.5 ms and 1.3 ms, respectively. The disturbance time recovery is the same for both PI controllers, 1.5 ms.

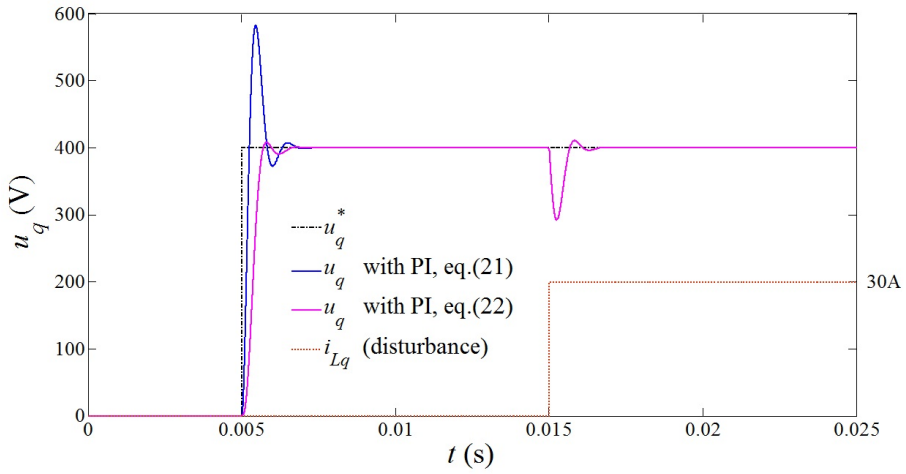


Figure 7. Closed-loop step response of decoupled PI controller.

Considering the alternative PI controller (23), the control laws for i_d^*, i_q^*, i_o^*, are obtained by inversion of decoupling variables, h_d and h_q (27).

$$\begin{aligned} i_d^* &= -K_{pd}u_d + K_{id}\int\left(u_d^* - u_d\right)\mathrm{d}t - C_f\omega_e u_q \\ i_q^* &= -K_{pq}u_q + K_{iq}\int\left(u_q^* - u_q\right)\mathrm{d}t + C_f\omega_e u_d \\ i_o^* &= -K_{po}u_o + K_{io}\int\left(u_o^* - u_o\right)\mathrm{d}t \end{aligned} \tag{27}$$

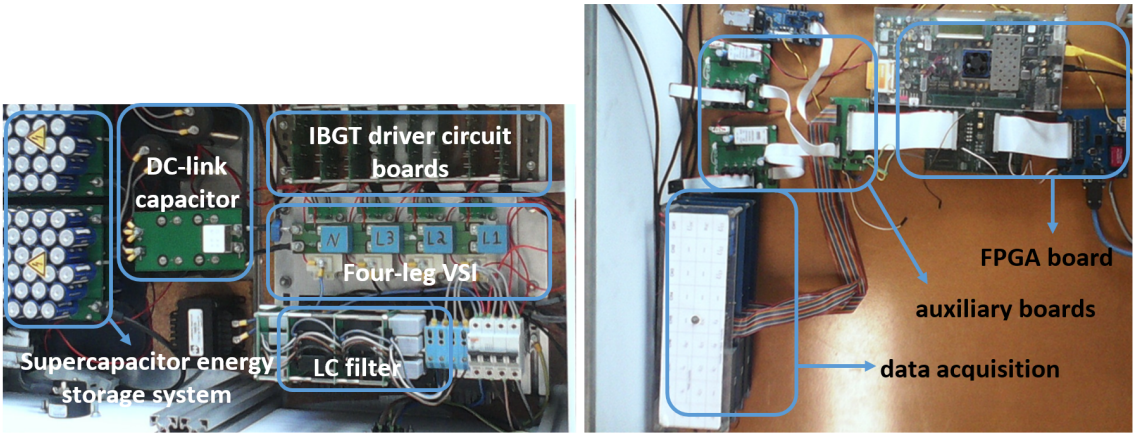
For the practical implementation, the PI controllers should have an anti-windup system to prevent the accumulation of integral errors when the currents limiters are active [23].

5. Performance Analysis of Four-Leg VSI

For comparison purposes a 3-phase four-leg VSI up to 20 kVA, with power factor of 0.8 lagging and an output sinusoidal voltage of 400 V–50 Hz was considered. The experimental results were obtained from a four-leg VSI laboratory prototype with the following parameters: $u_{DC} = 650$ V; $r_f = 220$ mΩ; $L_f = 3.7$ mH; $C_f = 40$ μF; hysteresis bands widths, $\Delta(\delta_{N\kappa}) = 0.2$ A, $\Delta(\delta_{L\alpha}) = 2$ A, $\Delta(\delta_{L\beta}) = 8$ A, $\Delta(\delta_{L\gamma}) = 5$ A; $\omega_e = 100\pi$ rads^{-1}; $T_d = 100$ μs; $\Delta t_u = 2$ μs; $K_{pm} = 0.28$; $K_{im} = 746$.

The four-leg VSI laboratory prototype, Figure 8, was developed using SKM200 half-bridge IGBT modules and the double driver SKHI 23/12R both from SEMIKRON (SEMIKRON International GmbH, Nuremberg, Germany). The control system was implemented in a FPGA development board Virtex® 6 (Xilinx Inc., San Jose, CA, USA) and the control algorithms for CVC and output voltage controllers (non-linear and linear) were developed in high-level programming language System Generator for DSP™ (Xilinx Inc., San Jose, CA, USA) under MATLAB® (The MathWorks Inc., Natick, MA, USA) and Simulink® (The MathWorks Inc., Natick, MA, USA) environments.

The data acquisition system is based on analog-digital converter ADC7609 (Analog Devices Inc, Norwood, MA, USA) and the currents and voltages were measured, respectively, through the Hall effect sensors LA100-P/SP3 and LV25-P/SP5 from LEM® (LEM Holding SA, Fribourg, Switzerland).



(a) View of the implemented four-leg VSI (b) View of the implemented control system

Figure 8. View of the four-leg VSI laboratorial setup.

The 3-phase four-leg voltage inverter output voltage waveform quality evaluation was divided into steady-state and dynamic response tests [24,25]. To the evaluation of experimental results of the four-leg inverter at steady-state operation, the power quality monitoring Fluke 435 (Fluke Corporation, Everett, WA, USA) was used.

5.1. Steady-State Performance Analysis

The steady-state performance analysis is obtained considering three performance criterion: the voltage regulation, the voltage total harmonic distortion and the voltage imbalance [24,25]. Voltage regulation, $V_R(\%)$, is a quantity to evaluate the ability of the bus to supply the load currents without changing its voltage amplitude [25]. The total harmonic distortion is the most common harmonic index used to indicate the harmonic content of a distorted waveform [25]. The total voltage harmonic distortion, THD_V, is defined as the rms of the harmonics, V_h, expressed in percentage of the fundamental voltage component. The voltage imbalance (or unbalance) refers to the deviation of phase voltages from their rated values with respect to magnitude and phase. One of the methods

for characterization of unbalance in power systems is done using the symmetrical components [26]. The symmetrical components of output voltages are described by vector sum of the three systems of 3-phase quantities referred as the positive, negative and zero sequence components [16]. For power quality evaluation, the voltage imbalance index can be defined in two components, V_{imb}^{-} and V_{imb}^{0}, that relate the steady-state output voltage negative and zero sequences components in percentage of the positive sequence component of the output voltage, respectively [27,28].

Figure 9 shows the four-leg inverter steady-state response when it is supplying a balanced linear load obtained from a three-phase resistors bank. Using the same resistive load bank, but with one of the phases disconnected, the steady-state response of the four-leg inverter to an unbalanced linear load is presented in Figure 10. The Table 2 presents the obtained performance analysis results of the four-leg VSI output voltages with linear loads.

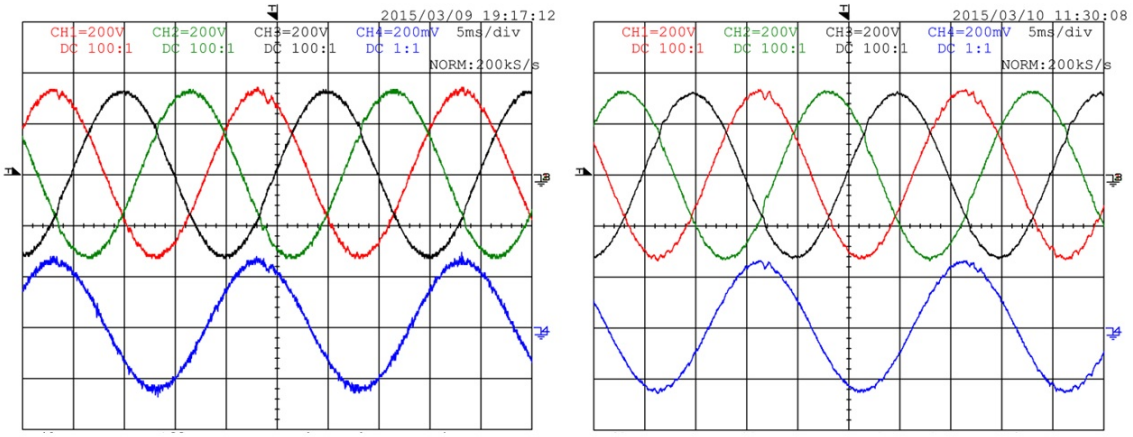


Figure 9. Steady-state balanced linear loads. Experimental results of the output voltages (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_A, 20 A/div).

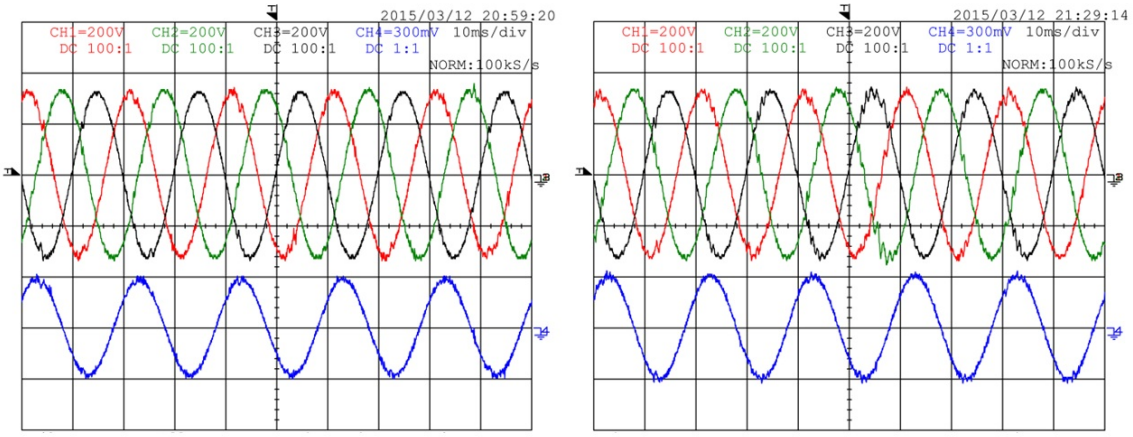


Figure 10. Steady-state unbalanced linear loads. Experimental results of the output voltages (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_A, 30 A/div).

Table 2. Steady-State performance results of the four-leg VSI with linear loads.

	Balanced Linear Loads		Unbalanced Linear Loads	
	OPC/SMC	**DPI**	**OPC/SMC**	**DPI**
Voltage deviation	±1.1%	±1.2%	±1.3%	±1.6%
THD_v	1.6%	1.8%	1.9%	2.2%
V_{imb}^{-} ; V_{imb}^{0}	0.7%; 0.4%	1.0%; 0.4%	1.0%; 0.5%	1.2%; 0.6%

Comparing the experimental results of two types of output voltage controllers, non-linear (OPC/SMC) and linear (DPI), there is a better voltage waveform quality obtained by the OPC/SMC. This is due to the higher dynamic response speed of the output currents compared with DPI.

Considering the experimental results with balanced and unbalanced linear loads, the performance analysis of four-leg inverter at steady-state operation shows that the voltage deviation value is ±1.3%. There is a THD_V up to 2%, and the voltage imbalance indexes, V_{imb}^{-} and V_{imb}^{0}, are up to 1.0% and 0.5%, respectively.

To evaluate the output voltage waveforms quality when the four-leg inverter supplies non-linear loads, two electrical circuits that uses diode bridges rectifiers, Figure 11, were considered. Figure 11a presents the balanced non-linear load tested and Figure 11b the unbalanced non-linear load that can be used as phase-neutral or as phase-phase load.

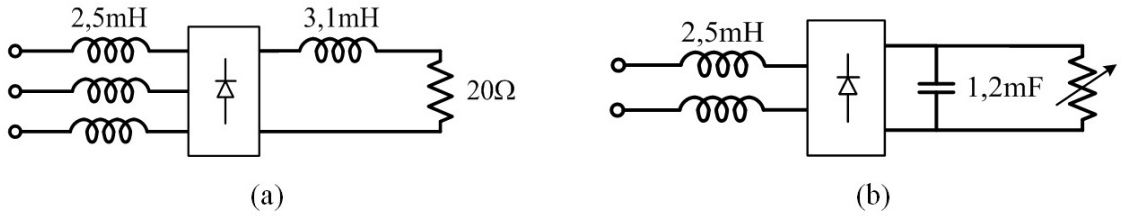


Figure 11. Non-linear loads considered. (**a**) Balanced non-linear load; and (**b**) unbalanced non-linear load.

Figures 12 and 13 presented the steady-state experimental results to evaluate the output voltage waveform quality of the four-leg inverter with balanced (12.7 kW) and unbalanced non-linear loads (phase-neutral, 3.5 kW), respectively. The Table 3 presents the obtained performance analysis results of the four-leg VSI output voltages with non-linear loads.

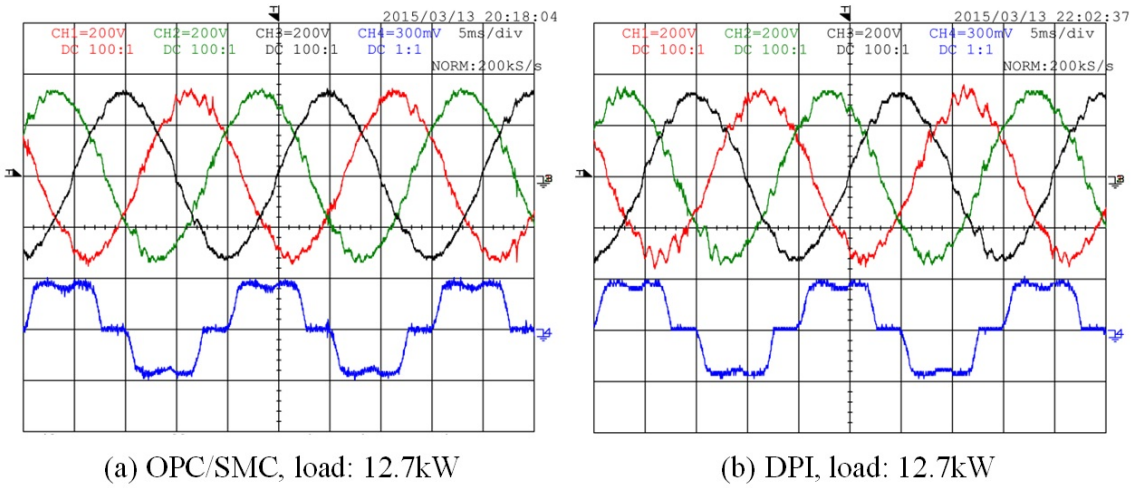
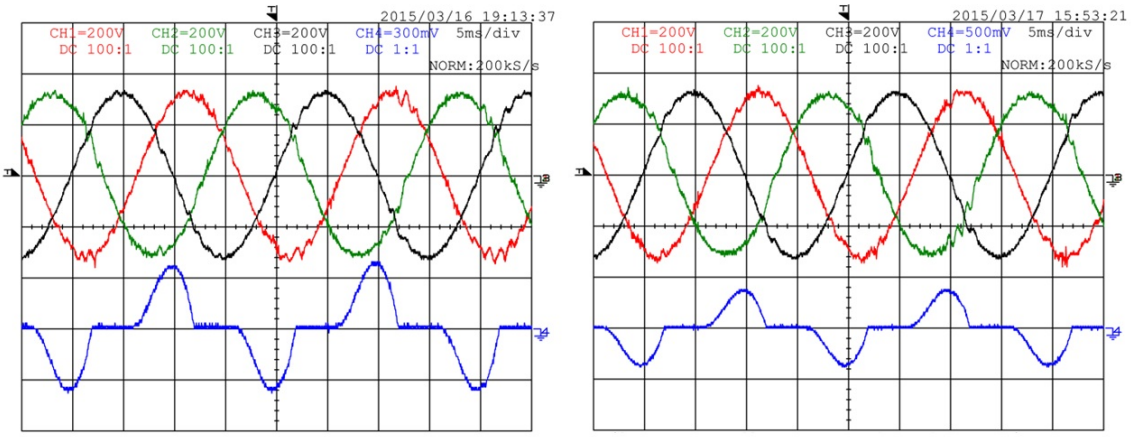


Figure 12. Steady-state balanced non-linear loads. Experimental results of the output voltages (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_B, 30 A/div).

The four-leg inverter analysis with non-linear loads shows that the output voltages waveforms maintain the desired amplitude and frequency, however, the ripple increases regarding the experimental results with linear loads. However, with non-linear a higher similarity is verified in the results between the OPC/SMC and DPI controllers.

Considering the experimental results with non-linear loads, the performance analysis of four-leg inverter at steady-state operation shows that the voltage deviation is ±1.6%. There is a THD_V up to 3%, and the voltage imbalance indexes, V_{imb}^{-} and V_{imb}^{0}, are up to 1.6% and 0.5%, respectively.



(a) OPC/SMC, load: 3.5kW, CH4: 30A/div (b) DPI, load: 3.5kW, CH4: 50A/div

Figure 13. Steady-state unbalanced non-linear loads: experimental results of the output voltages (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current, CH4.

Table 3. Steady-state performance results of the four-leg VSI with non-linear loads.

	Balanced Non-Linear Loads		**Unbalanced Non-Linear Loads**	
	OPC/SMC	**DPI**	**OPC/SMC**	**DPI**
Voltage deviation	±1.4%	±1.5%	±1.6%	±1.7%
THD_v	2.8%	3.3%	3.0%	2.9%
V_{imb}^{-} ; V_{imb}^{0}	1.3% ; 0.4%	1.3% ; 0.4%	1.6% ; 0.5%	1.7% ; 0.6%

5.2. Dynamic Response Performance Analysis

For the dynamic response performance analysis, the instantaneous sag caused by an impact loading, Figure 14, was considered. To determine the dynamic response, two quantities are measured: the voltage notch amplitude, V_{not}, and its time duration, Δt [29].

Figure 15 shows a transient test with the four-leg inverter, when from no-load state is turned on a balanced linear load of 12.3 kW, obtained from three-phase resistance. The disturbance in the output voltages waveform has relative amplitude of 26.2% and occurs during 1ms, Figure 15a. Depending of the instant that the load is connected, the voltage disturbance could be imperceptible, as it is seen in Figure 15b, when tested with DPI controller. Figure 15c,d presents the energy storage system transient response to keep constant the DC-link voltage, u_{DC} through the supercapacitors current, i_{SC}.

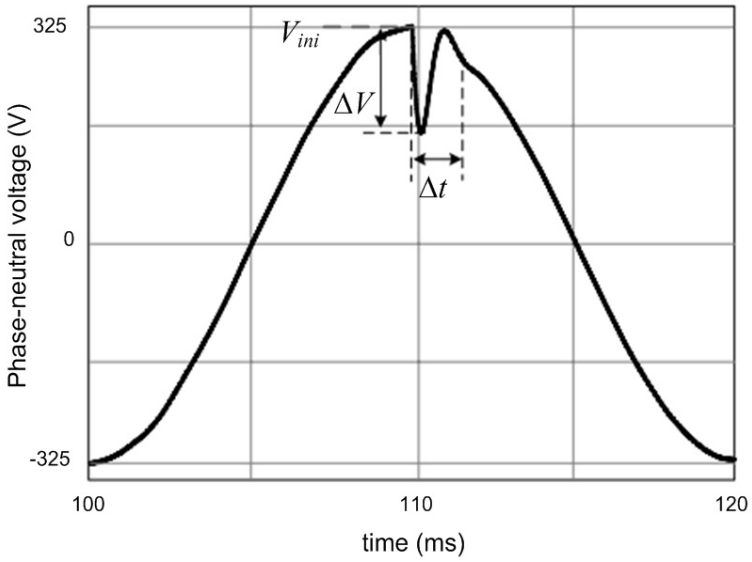


Figure 14. Example of dynamic voltage response analysis due a load transient (modified from [29]).

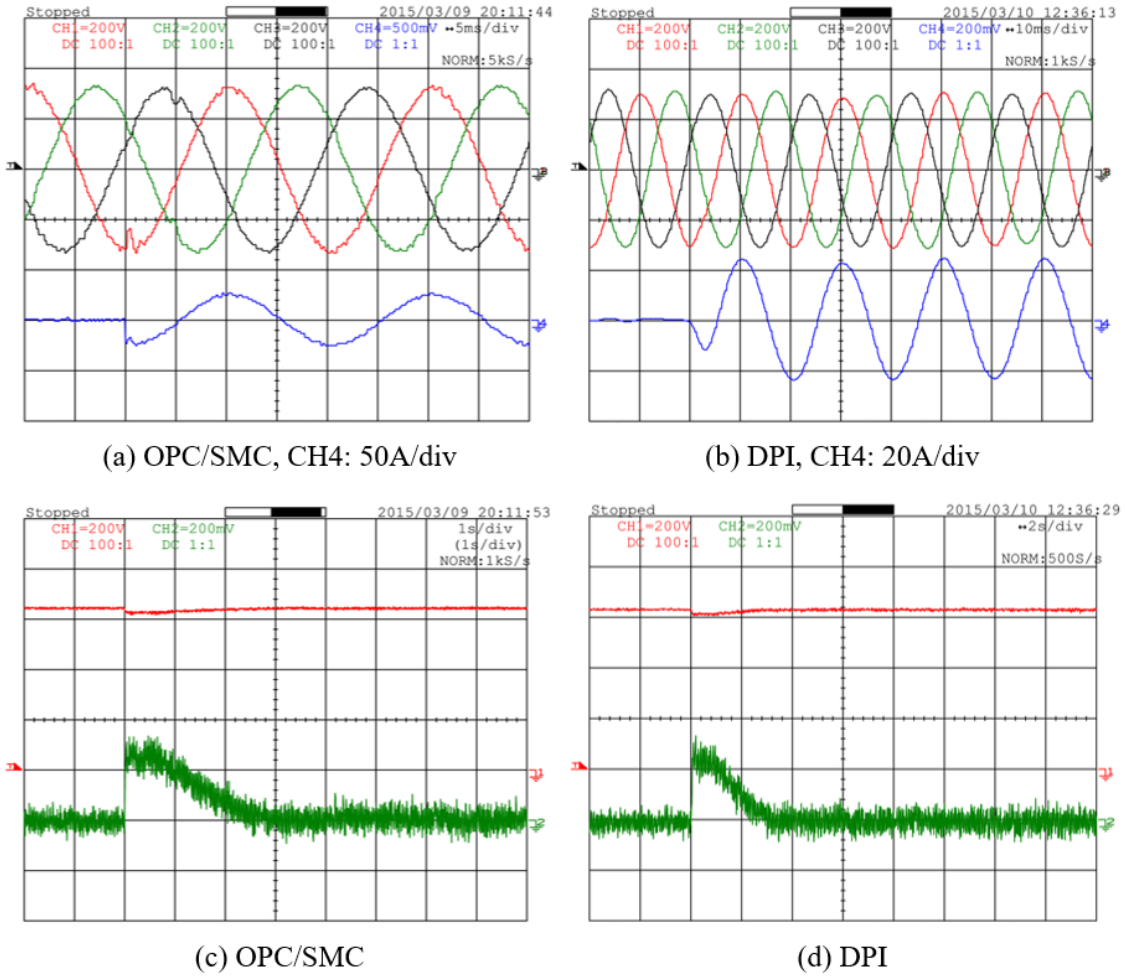
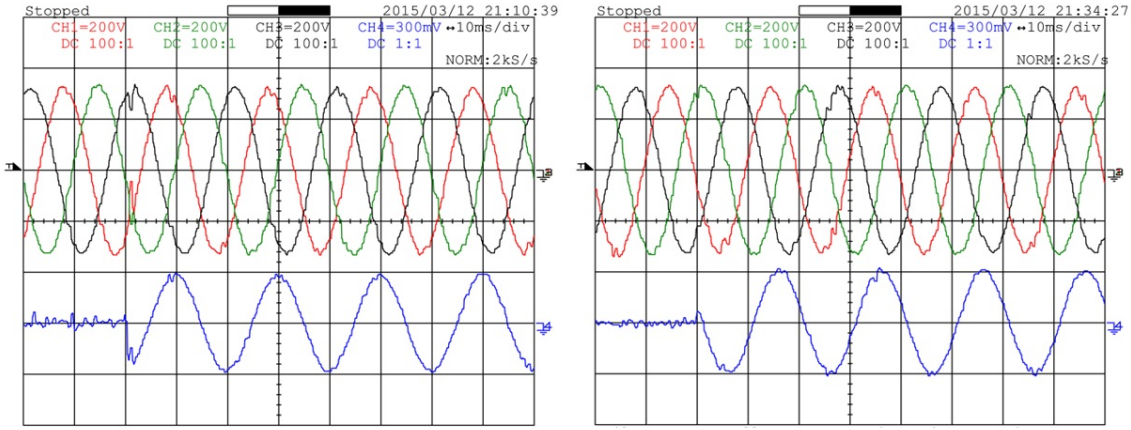


Figure 15. Transient of balanced linear load of 12.3 kW: (**a**,**b**) experimental dynamic voltage response (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_A); and (**c**,**d**) transient in DC-link side (CH1: u_{DC}; CH2: i_{SC}, 20 A/div).

Figure 16 shows the transient test with unbalanced linear load of 8.1 kW, related to the circuit of Figure 11b connected into two output phases. The disturbance in the output voltage waveform presents relative amplitude of 71.8% with a duration of 1.8 ms, which occurred in the test of OPC/SMC, Figure 16a.

Figure 17 presents the direct starting of a three-phase induction motor of 7.5 kW, 400 V–50 Hz and one pair poles. In this laboratory test the current limiters of output voltage controllers, OPC/SMC and DPI, were set to ±30 A.



(a) OPC/SMC (b) DPI

Figure 16. Transient of unbalanced linear load of 8.1 kW: experimental dynamic voltage response (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_A, 30 A/div).

Analyzing the experimental results shown in Figure 17, during the direct starting transient of the three-phase induction motor, there is a sag in the three-phase voltages applied to the motor, comparing with the voltages reference values. This voltage sag is due to the action of the inverter current limiter, I_{dmax}, I_{qmax} and I_{omax}, presented in the output voltages controllers that prevents overcurrents in the four-leg inverter outputs. It is noted that the temporal evolution of the voltages and currents responses is very similar between the OPC/SMC and DPI controllers.

Figure 18 shows the transient test of a balanced non-linear load of 12.7 kW connection (the three-phase diode bridge rectifier load type of Figure 11a). It is noted a small disturbance in output voltages, more visible in the experimental results of the DPI output voltage controller, Figure 18b. Figure 18c,d present the energy storage system transient response to keep constant the DC-link voltage, u_{DC} through the supercapacitors current, i_{SC}.

The load type used in this experimental test has electrolytic capacitors in the DC side, which are initially discharged. Thus, when the load transient of this load type occurs, despite the reduced value of its power in continuous operation, has a considerable disturbance in the output voltage waveforms, due to the current required to initially charge the output load capacitors.

Comparing the experimental results of output voltages controllers, OPC/SMC and DPI, the disturbance caused by the unbalanced non-linear load connection transient is solved in one period time of AC output voltages, to either non-linear and linear controllers.

Figure 19 presents the transient test of the unbalanced non-linear load of 3.5 kW connection (the phase-neutral diode bridge rectifier load of Figure 11b).

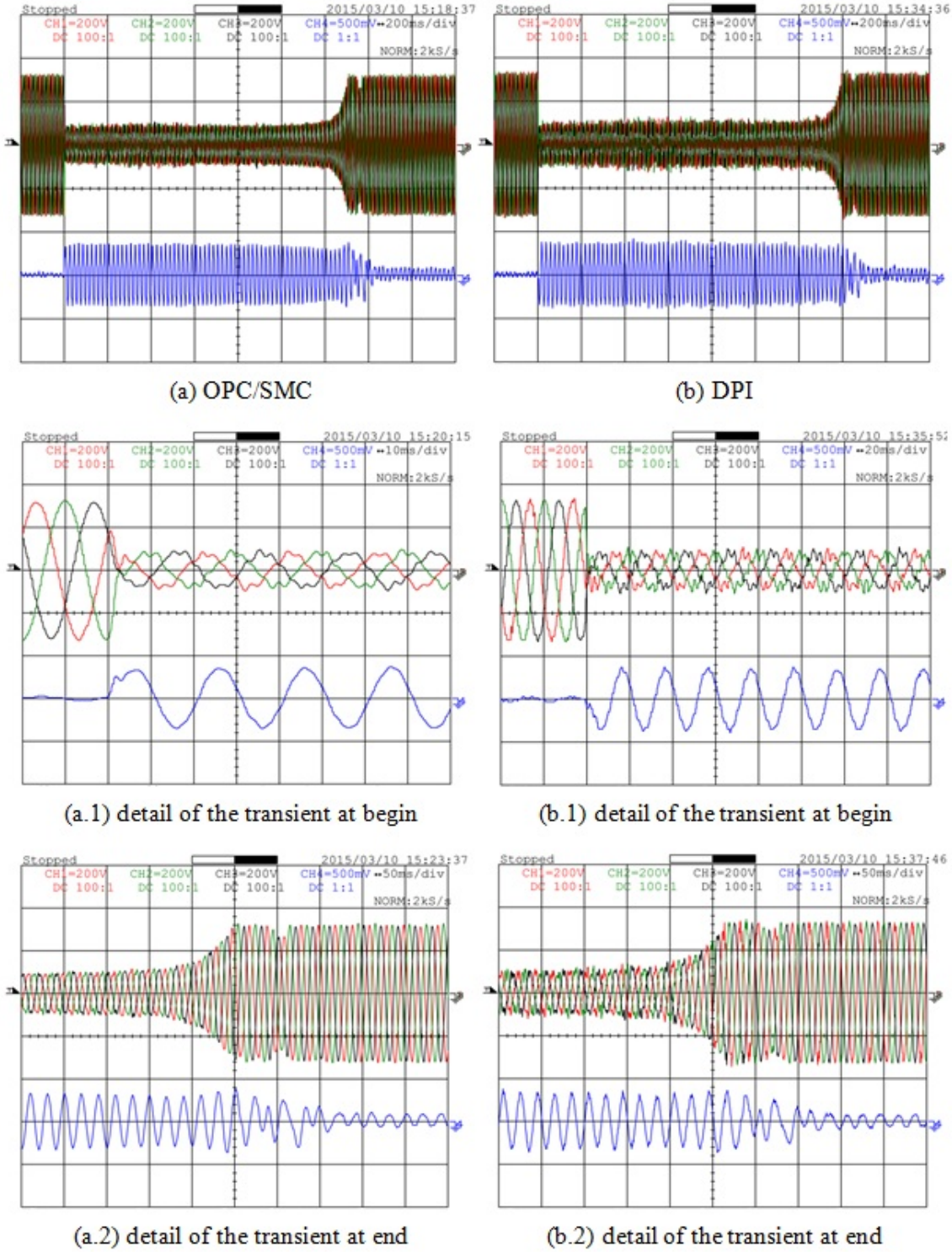


Figure 17. Direct on-line starting of a 3-phase induction motor: experimental dynamic voltage response (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_A, 50 A/div).

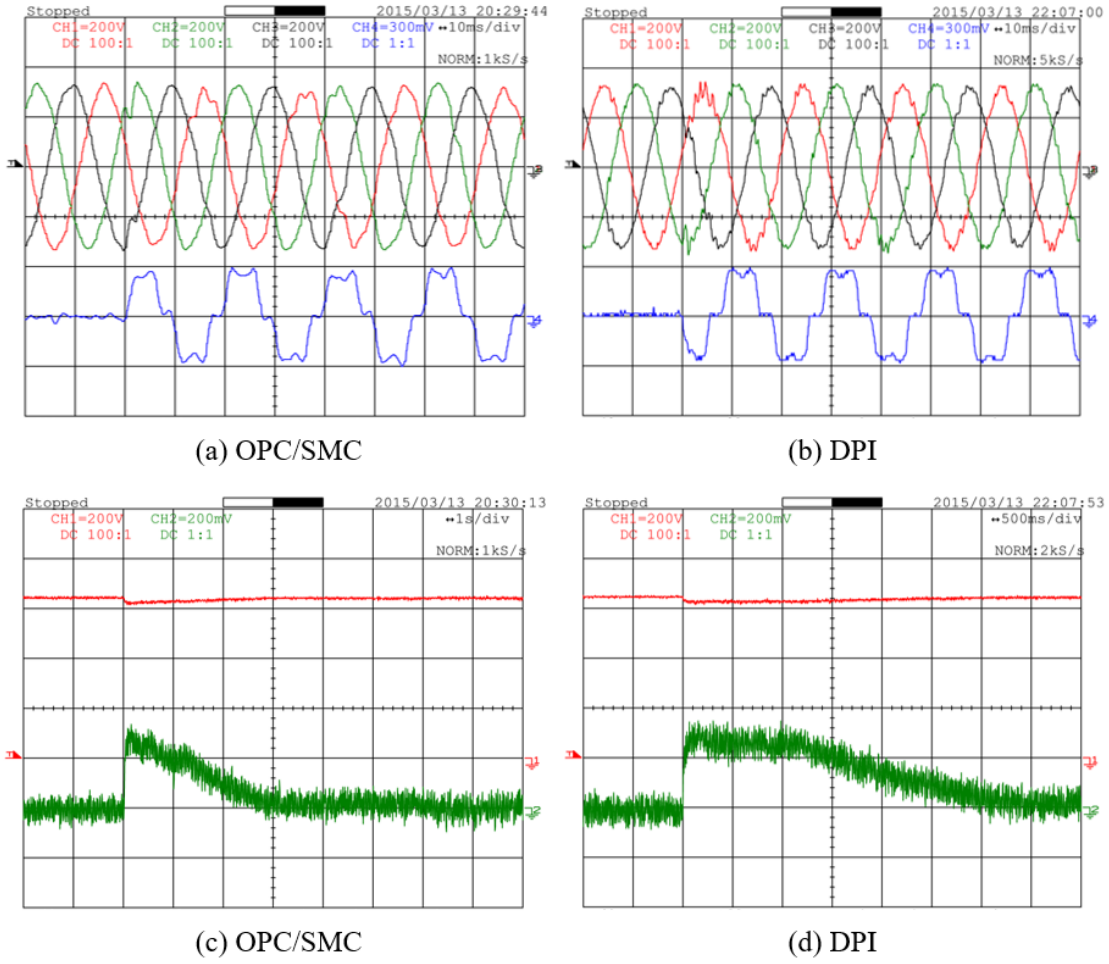


Figure 18. Transient test of 12.7 kW balanced non-linear load: (**a**,**b**) experimental dynamic voltage response (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: i_B, 30 A/div); and (**c**,**d**) transient in DC-link side (CH1: u_{DC}; CH2: i_{SC}, 20 A/div).

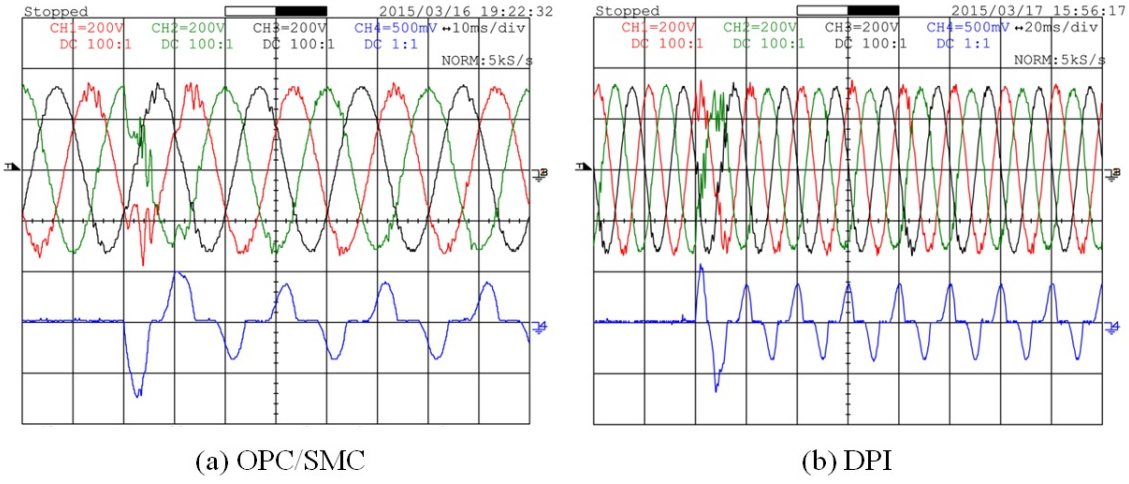


Figure 19. Transient test of 3.5 kW unbalanced non-linear load. Experimental dynamic voltage response (CH1: u_{AN}; CH2: u_{BN}; CH3: u_{CN}) and phase current (CH4: 50 A/div).

6. Conclusions

This paper presented the design of current and voltage controllers for three-phase four-leg VSI. Predictive, sliding mode and decoupled PI controllers performance were designed, tested and results evaluated. The OPC, SMC and DPI controllers, together with the inner hysteretic current loop vector controller in $\alpha\beta\gamma$ space, lead to a variable switching frequency of the four-leg VSI with timely and precise control actions, determined by the control laws of each controller and the allowed currents ripple. The computational resources required to implement the linear and non-linear outer voltage controllers are similar. However, the development of the high-level programming language for non-linear controllers was realized in a more straightforward way, while the programming of the linear controller, due to the need of the anti-windup system, introduces some complexity in the PI controller, to enable it to operate correctly with high load currents.

The steady-state and dynamic performance analysis of the stand-alone four-leg inverter were measured experimentally. In steady-state, the output voltage RMS value presents a root-mean-square voltage deviation of $\pm 1.6\%$ with respect to a voltage reference of 230 V. There is a THD_V, less than 3% for the measured loads and voltages imbalance indices, V_{imb}^{-} and V_{imb}^{0}, less than 1.6% and 0.5%, respectively.

The dynamic response performance analysis was measured experimentally, by analysing transients created by different types of loads. The results showed the four-leg inverter ability to hold load transients, in general, eliminating voltages notches in less than a half of the voltage waveform period. In the case of load transients that require high currents for a short period of time, the currents are limited to admissible current values by decreasing the output voltages when the current limiters stay active.

Globally, the tests with non-linear output voltage controllers, OPC and SMC, demonstrates a slightly better performance in the output voltages waveform quality than DPI. Overall, the experimental results confirm the output voltage waveform quality characteristics of the four-leg inverter to use in stand-alone power systems with linear and nonlinear, balanced and unbalanced loads.

Acknowledgments: Authors thank to Converte® (Lisboa, Portugal) for the engineering support on functional prototype assembly. This work was supported in part by national funds through Fundação para a Ciência e Tecnologia (FCT) with reference UID/CEC/50021/2013.

Author Contributions: Ricardo Luís performed the experiments, analyzed the data and wrote the manuscript. José Fernando Silva supervised the research, providing guidance and key suggestions. José Carlos Quadrado revised text to the manuscript draft versions. All authors revised and approved the publication of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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