energies

MDPI

Article

An Isolated Three-Port Bidirectional DC-DC Converter with Enlarged ZVS Region for HESS Applications in DC Microgrids

Cheng-Shan Wang [1], Wei Li [1], Yi-Feng Wang [1,*], Fu-Qiang Han [1], Zhun Meng [1] and Guo-Dong Li [2]

[1] School of Electrical Engineering and Automation, Tianjin University, Tianjin 300072, China; cswang@tju.edu.cn (C.-S.W.); liweitju@hotmail.com (W.L.); hanxinyu@tju.edu.cn (F.-Q.H.); quakermaster@hotmail.com (Z.M.)

[2] Electric Power Research Institute, State Grid Tianjin Electric Power Company, Tianjin 300384, China; tjLGD@163.com

* Correspondence: wayif@tju.edu.cn; Tel.: +86-022-2740-1479

Academic Editor: Gabriele Grandi
Received: 15 February 2017; Accepted: 24 March 2017; Published: 1 April 2017

Abstract: In this paper, a two-stage three-port isolated bidirectional DC-DC converter (BDC) for hybrid energy storage system (HESS) applications in DC microgrids is proposed. It has an enlarged zero-voltage-switching (ZVS) region and reduced power circulation loss. A front-end three-phase interleaved BDC is introduced to the supercapacitor (SC) channel to compensate voltage variations of SC. Consequently, wide ZVS range and reduced circulation power loss for SC and DC bus ports are achieved under large-scale fluctuating SC voltage. Furthermore, a novel modified pulse-width-modulation (PWM) and phase-shift (PHS) hybrid control method with two phase-shift angles is proposed for BA port. And it contributes to an increasing number of switches operating in ZVS mode with varying battery (BA) voltage. Phase shift control with fixed driving frequency is applied to manage power flow. The ZVS range as well as the current stress of resonant tanks under varying port voltages is analyzed in detail. Finally, a 1 kW prototype with peak efficiency of 94.9% is built, and the theoretical analysis and control method are verified by experiments.

Keywords: hybrid energy storage system; there-port isolated converter; series resonant BDC; phase shift control; hybrid control method

1. Introduction

The development and utilization of renewable energy have turned out to be new solutions for the worldwide energy depletion and environmental pollution problems [1]. In order to achieve efficient utilization of distributed energy generations, DC microgrid has become a research focus in recent years [2–4]. However, the output of several renewable energy sources is intermittent and time-varying, and the load demand is uncertain [5]. Therefore, storage units are usually used to balance the power supplies and loads in DC microgrids. Several studies use hybrid energy storage systems (HESSs), which are composed of SC and BA, to improve stability and reliability of DC microgrid [6–8]. Numerous literatures have researched on energy management and power sharing strategy of HESS in DC microgrid [9–16]. While, the design of interface converters between HESS and DC microgirds is still considered as an emerging area of research.

Three-port BDC, which integrates SC and BA converters into one dual-input converter, will assist to improve the efficiency, power density and control coordination of HESS converters. Many three-port BDCs have been reported in literatures. According to the connection methods, three-port BDCs can be

categorized into three types: non-isolated, partly-isolated and isolated converters. Typical structures of three-port BDCs are shown in Figure 1 [17].

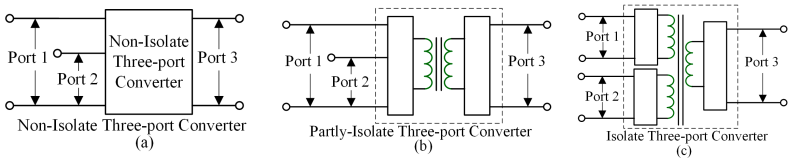


Figure 1. Typical structure of three-port converter: (**a**) non-isolated; (**b**) partly-isolated; (**c**) isolated.

Figure 1a shows the diagram of non-isolated three-port converter [18,19], and Figure 1b presents the topology of partly-isolated converter [20–22]. The common shortcomings of non-isolated and partly-isolated three-port converters are the lack of complete electrical isolation among three ports, and being unable to cope with wide operating voltage ratio. For the HESS application, security is of great importance, and thus, electrical isolation is essential. In consequence, the isolated structure shown in Figure 1c is adopted in this article [23,24].

Numerous isolated three-port DC-DC converters have been proposed to integrate two energy sources into one dual-input converter. The three-port triple-active-bridge (TAB) converter shown in Figure 2, as the most widely disseminated isolated three-port topology, attracts a lot of attentions from researchers [23–29]. In [26], a TAB converter is used to deal with a hybrid energy source consisting of full cell and super capacitor. It appears that TAB converter has attractive features of galvanic isolation, bidirectional power flow, ZVS operation and phase shift control with fixed switching frequency. However, power transfer among three ports in TAB is coupled, therefore, decoupling control algorithm is required. What's more, the power transmission of TAB topology is inversely proportional to the impedance of inductance. While, the inductance of TAB is inherent greater than the leakage inductor of transformer. In case of high power levels, switching frequency has to be reduced to get realizable inductance value. In [26–29] the driving frequency are all 20 kHz, and this will be detrimental for realizing high power density.

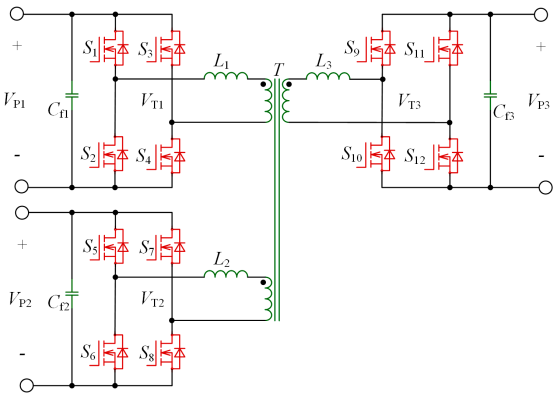


Figure 2. Topology of the isolated three-port BDC based on transformer and inductor.

In order to solve problems of TAB mentioned above, a series-resonant (SR) based converter is proposed in [30]. The impedance of SR tank is determined by value of inductor and capacitor together with the switching frequency. Therefore, it can operate at higher frequency under high power level. In [31,32], renewable source, battery and load are integrated to a three-port SR BDC. The driving frequency is 100 kHz, which is apparently higher than 20 kHz of TAB as shown in [26–29]. What's more, power flow among three ports can be controlled independently since there are only two SR tanks. Nevertheless, the three-port SR BDC still suffers disadvantages including losing ZVS operation and increased current stress under wide voltage variations. However, previously published works

mainly concentrated on the operating characteristics of SR BDC with fixed port voltages. The methods, which can enlarge ZVS region and reduce circulation power loss under varying port voltages, are still considered as emerging area of research.

Two methods for enlarging ZVS range and decreasing power circulation loss under DAB and TAB topologies are reported in [33–36]. One method is to adopt improved control algorithm. Literature [34] has presented an improved modulation control approach, where two phase-shift angles are employed to minimize the switching losses for DAB under light load. Another alternative method is to use a front-end converter to keep input voltage of bridge constant, as suggested in [36]. These two methods effectively improve the characteristics of TAB converters with wide voltage variations. Unfortunately, few of literatures have ever investigated the validity of these two methods in three-port SR BDC under varying port voltages.

Based on the SR BDC, this article proposes a two-stage three-port BDC to integrate HESS and DC microgrid. The subject of this paper is to enlarge the ZVS operating range and to reduce the circulation power loss of the proposed three-port SR BDC. Then, by comprehensively considering the large SC's and small BA's voltage fluctuation ranges, two different methods are adopted in SC and BA channels respectively. For the SC channel, a three-phase interleaved BDC is introduced to convert the widely fluctuating V_{SC} to a fixed voltage $V_{dc\text{-}link}$. This method guarantees the unity voltage gain between SC and DC bus ports. The BDC adopts the interleaved structure to improve the power level of the BDC, and to reduce the SC current ripple as well as the inductor size [37,38]. Additionally, a PWM and PHS (PWM-PHS) control method is developed to enlarge ZVS operating range when the voltage gain between DC bus and BA ports is greater than 1. The control objectives of three-port SR BDC and there-phase interleaved BDC are to maintain the DC bus voltage and dc-link voltage stable respectively. Finally, a prototype platform is built to verify the feasibility of the proposed topology. The structure of this article is organized as followings: the topology of proposed converter is given in Section 2. Operating principles are introduced in Section 3. Section 4 explains the variation of ZVS region and the peak value of resonant current under varying voltage gain. Principles of the proposed PWM-PHS control method are also introduced in Section 4. Finally, the experimental results are presented in Section 5, while the conclusion is drawn in Section 6. The main contributions of this paper are summarized below:

(1) A new two-stage three-port isolated BDC topology is proposed to integrate SC and BA.
(2) Methods to enlarge ZVS region and to reduce power circulation loss for three-port SR BDC under varying port voltages are first investigated.
(3) A front-end converter in SC channel is introduced to keep input of full bridge constant. For BA channel, PWM-PHS control method is developed to improve the characteristics of the proposed three-port BDC.
(4) By adopting the two-stage structure, all switches of SC and DC bus ports have realized ZVS with variable V_{SC}. By applying the proposed PWM-PHS control method, two more switches of BA port realize ZVS even under the worst input voltage condition of M_{BA} = 1.15.

2. Proposed System

The overall structure of the proposed two-stage three-port BDC is shown in Figure 3. It contains two parts: a three-port SR BDC and a three-phase interleaved BDC. Three-port SR BDC is presented to maintain DC bus voltage stable and to control power transmission among three ports. The function of three-phase interleaved BDC is converting the widely fluctuating super capacitor voltage V_{sc} to a constant voltage $V_{dc\text{-}link}$.

2.1. Three-Port SR BDC

The three-port SR BDC is composed of a three-winding transformer, three full bridges and two SR tanks formed by C_{r1}, L_{r1} and C_{r2}, L_{r2} respectively. The three-winding transformer provides electrical

isolation among three ports. What's more it has inherent bidirectional power flow characteristic, since all power switches of three full bridges are MOSFETs. The converter works at a constant switching frequency f_s, which is above the resonant frequency of SR tanks. As a consequence, it works only in continuous current mode. Phase shift control method is implemented, the amount and direction of transmitted power are controlled by the phase shift angles. All the switches of the three full bridges work with 50% duty cycle.

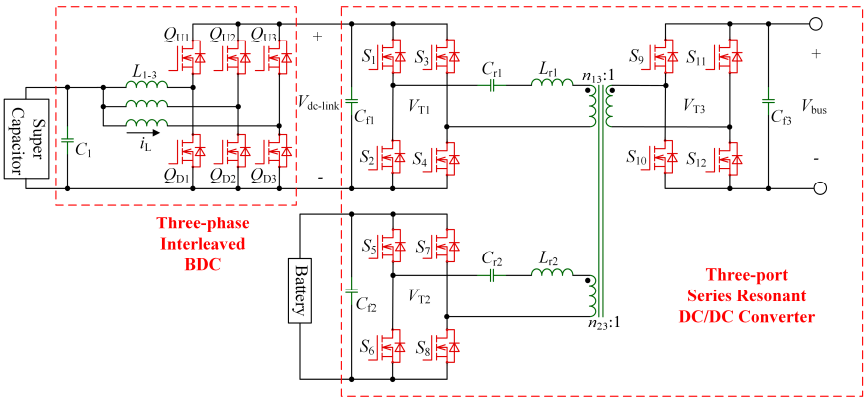


Figure 3. Topology of the proposed HESS bidirectional DC/DC system.

Through theoretical analysis, the three-port SR BDC is shown to have the best operating characteristics such as maximum ZVS operating region, reduced current stress and cutoff current only under unity voltage gain among three ports. Whereas, the voltage of SC has a large fluctuation range with the change of residual energy. To solve the contradictions of the varying V_{SC} and the best operating voltage gain restraint of SR BDC, a three-phase interleaved BDC is applied in the system. The interleaved BDC is used to convert the widely fluctuating SC voltage to a fixed voltage $V_{dc\text{-}link}$. However, the fluctuation range of battery voltage is relatively small, the method of converting the battery voltage to a fixed voltage by increasing a BDC converter is not the best solution. In addition, a new PWM-PHS hybrid control strategy which has two phase-shift angles is proposed to improve the operation characteristics of battery channel under a variation range of voltage gain. The proposed control method can increase the number of MOSFETs operating in ZVS.

The features of the three-port SR BDC are:

(1) Three-port structure with transformer coupling reduces amount of power switches, increases power density.
(2) Power flow between BA port and DC bus port, SC port and DC bus port are bidirectional.
(3) Centralized control method of power flow by changing the direction and magnitude of the phase shift angles between three ports is applied.
(4) Three-phase interleaved BDC is introduced in the SC channel to keep voltage gain M_{SC} = 1, which guarantee best operating characteristics of SC channel of SR BDC.
(5) PWM-PHS hybrid control strategy is proposed for the BA channel to increase the number of switches, which can achieve ZVS, under a variation voltage V_{BA}.

2.2. Three-Phase Interleaved BDC

A three-phase interleaved BDC is introduced to the SC channel of SR BDC to convert the widely fluctuating SC voltage V_{SC} to a fixed voltage $V_{dc\text{-}link}$. The SC is connected to the low-voltage side, and the SR BDC is placed on the high-voltage side. When energy flows from SC to the SR BDC, it works at boost mode, and conversely, it works under buck mode.

A non-isolated bidirectional buck/boost converter topology is adopted in this paper. In order to achieve high efficiency and high power density, the converter is designed to operate in discontinuous

conducting mode (DCM), such that all the switches realize ZVS, and the buck/boost inductors are minimized. However, the DCM also has the drawback of large current ripple. To reduce current ripple, the interleaved multi-phase structure is introduced to reduce current ripple. All of the interleaved channels adopt the same control strategy, while hold a phase shift of $\pi/3$ in driving signal from each other. As a consequence, the inductor currents of three phases are shifted by $\pi/3$. Hence, with interleaved inductor currents, the ripple current of SC is minimized. The features of the three-phase interleaved BDC are:

(1) The structure is simple, and it combines a boost converter together with a buck converter connected in antiparallel.
(2) Three-phase interleaved structure is adopted to reduce current ripple, improve power level and reduce current stress of the converter.
(3) It works under DCM, which can reduce the inductance value.
(4) Two MOSFETs of one phase-leg conduct complementarily, and the inductor operates under DCM condition, and thus ZVS of MOSFETs is achieved.

3. Operating Analysis

In this section, operating principles of three-port SR BDC and three-phase interleaved BDC are introduced respectively. For the three-port SR BDC, relationship between phase shift angle and power transmission is deduced. What's more, ZVS soft-switching realizing region and current stress of the resonant tank are analyzed in detail. For three-phase interleaved BDC, the operating principle as well as the inductance designing method is introduced.

3.1. Operating Principle of Three-Port SR BDC

The proposed three-port SR BDC is shown in Figure 4. It is composed of three full bridges, a three-winding transformer, two SR tanks formed by C_{r1} and L_{r1}, C_{r2} and L_{r2}, and filter capacitors C_{f1}–C_{f3}. Port 1 is connected to SC through a three-phase interleaved BDC, port 2 is and port 3 are BA port and DC bus respectively. Phase shift method is applied among three ports to control the direction and magnitude of the power transmission, all the switches of the converter are driven at 50% duty cycle. Since the voltage of three ports are constant dc, V_{T1}, V_{T2} and V_{T3} are square-waves with amplitudes of $\pm V_{\text{dc-link}}$, $\pm V_{BA}$ and $\pm V_{\text{bus}}$ respectively. In the subsequent analysis, phase shift angles of SC and BA ports are defined as φ_1 and φ_2, which are shown in Figure 4. They control the phase shift between the square-wave outputs of the active bridges. The phase shifts φ_1 and φ_2 are considered positive if V_{T1} and V_{T2} lead V_{T3}, and conversely, φ_1 and φ_2 are considered negative.

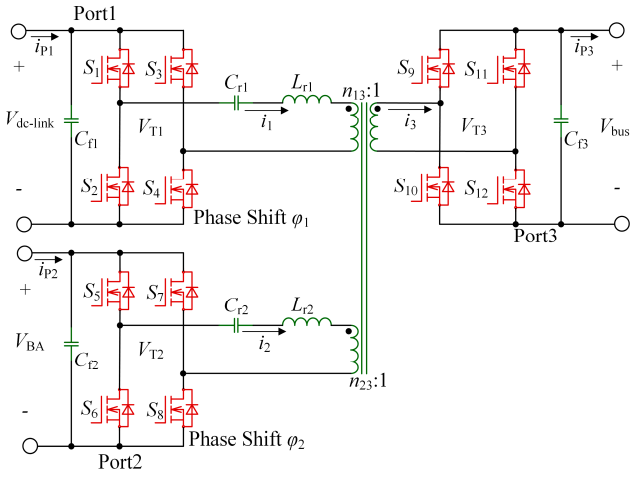


Figure 4. Structure of the three-port SR BDC.

3.1.1. Operating Mode Analysis

The operating principles when both SC and BA ports are providing energy to DC bus port are analyzed. In this condition both φ_1 and φ_2 are positive. The theoretical waveforms, when $\varphi_1 > \varphi_2 > 0$, are shown in Figure 5.

There are 18 different intervals in one switching cycle. Dead time is considered in the analysis, however, the charging and discharging intervals of snubber capacitors are very small, and they can be neglected.

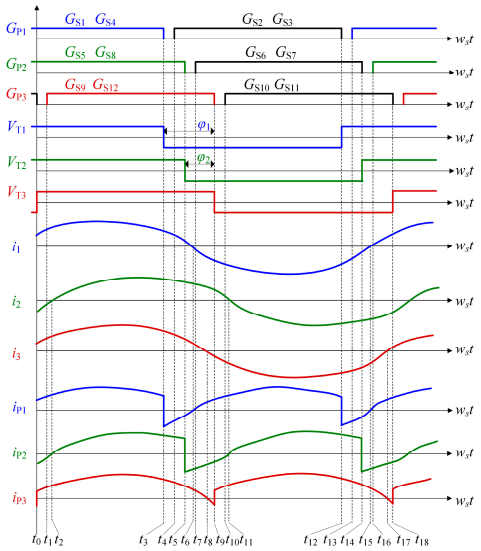


Figure 5. Theoretical waveforms of the three-port SR BDC.

Interval 1 (t_0–t_1): S_1 and S_4, S_5 and S_8 are on. This interval is dead time of port 3 and all the switches of port 3 are off. Since i_3 is positive, i_3 flows through the anti-parallel diodes of S_9 and S_{12}. i_1 flows through S_1 and S_4, and i_2 flows through S_5 and S_8. This interval ends at t_1, when S_9 and S_{12} are turned on.

Interval 2 (t_1–t_2): S_1 and S_4, S_5 and S_8, S_9 and S_{12} are on. This interval ends when i_2 increases to zero. The anti-parallel diodes of S_9 and S_{12} conduct prior to the main switches, thus, S_9 and S_{12} are turned on with ZVS. The operating characteristics of port 1 and 2 are exactly same with interval 1.

Interval 3 (t_2–t_3): This interval begins at t_2 when i_2 increases to zero, and it ends when switches S_1 and S_4 are turned off. During this interval, S_1 and S_4 of port 1, S_5 and S_8 of port 2 and S_9 as well as S_{12} of port 3 are on. i_1, i_2 and i_3 are positive and flow through S_1 and S_4, S_5 and S_8, and S_9 and S_{12} respectively.

Interval 4 (t_3–t_4): This interval is dead time of port 1 and all the switches of port 1 are off. i_1 is positive, so i_1 flows through the anti-parallel diodes of S_2 and S_3. During this interval, i_2 and i_3 flow through S_5 and S_8, and S_9 and S_{12} respectively. This interval ends when S_2 and S_3 are turned on.

Interval 5 (t_4–t_5): At t_4, S_2 and S_3 are turned on, and this interval ends when S_5 and S_8 are turned off. Since the anti-parallel diodes conduct before main switches of S_2 and S_3, S_2 and S_3 are turned on with ZVS. The operating characteristics of port 2 and 3 are identical with interval 4.

Interval 6 (t_5–t_6): At t_5, switches S_5 and S_8 are turned off, this interval ends when i_1 decreases to zero. This interval is dead time of port 2 and all the switches of port 2 are off. i_2 is positive, hence i_2 flows through the anti-parallel diodes of S_6 and S_7. i_1 and i_3 flow through S_2 and S_3, and S_9 and S_{12} respectively.

Interval 7 (t_6–t_7): This interval begins at t_6 when i_1 decreases to zero, and it ends when S_6 and S_7 are turned on. The difference between interval 7 and 6 is that the direction of i_1 changes. i_2 still flows through the anti-parallel diodes of S_6 and S_7.

Interval 8 (t_7–t_8): At t_7, S_6 and S_7 are turned on, and this interval ends when i_3 decreases to zero. The anti-parallel diodes conduct ahead the main switches of S_6 and S_7, therefore, S_6 and S_7 are turned on with ZVS. The operating characteristics of port 1 and 3 are exactly same with interval 7.

Interval 9 (t_8–t_9): This interval begins at t_8 when i_3 decreases to zero, and it ends when S_9 and S_{12} are turned off. The difference between interval 9 and 8 is that the direction of i_3 changes. The operating characteristics of port 1 and 2 are exactly the same with interval 8.

Interval 10 (t_9–t_{10}): This interval is dead time of port 3. Because i_3 is negative, so i_3 flows through the anti-parallel diodes of S_{10} and S_{11}. During this interval, i_1 and i_2 flow through S_2 and S_3, and S_6 and S_7 respectively. This interval ends when S_{10} and S_{11} are turned on.

Interval 11 (t_{10}–t_{11}): At t_{10}, S_{10} and S_{11} are turned on, and this interval ends when i_2 decreases to zero. The anti-parallel diodes conduct before main switches of S_{10} and S_{11}, so that S_{10} and S_{11} are turned on with ZVS. The operating characteristics of port 1 and 2 are exactly same with interval 10.

Interval 12 (t_{11}–t_{12}): This interval begins at t_8 when i_2 decreases to zero, and it ends when S_2 and S_3 are turned off. The difference between interval 12 and 11 is that the direction of i_2 changes.

Interval 13 (t_{12}–t_{13}): This interval is dead time of port 1. During this interval, i_1 is negative, so i_1 flows through the anti-parallel diodes of S_1 and S_4. i_2 and i_3 flow through S_6 and S_7, and S_{10} and S_{11} respectively. This interval ends when S_1 and S_4 are turned on.

Interval 14 (t_{13}–t_{14}): At t_{13}, S_1 and S_4 are turned on and this interval ends at t_{14} when S_6 and S_7 are turned off. The anti-parallel diodes conduct prior to the main switches of S_1 and S_4, so S_1 and S_4 are turned on with ZVS. The operating characteristics of port 2 and 3 are exactly same with interval 13.

Interval 15 (t_{14}–t_{15}): This interval is dead time of port 2. During this interval, i_2 is negative, thus i_2 flows through the anti-parallel diodes of S_5 and S_8. i_1 and i_3 flow through S_1 and S_4, and S_{10} and S_{11} respectively. This interval ends at t_{15} when i_1 increases to zero.

Interval 16 (t_{15}–t_{16}): This interval begins at t_{15} when i_1 increases to zero and ends when S_5 and S_8 are turned on. This interval is still dead time of port 2. The difference between interval 16 and 15 is that the direction of i_1 changes.

Interval 17 (t_{16}–t_{17}): This interval begins at t_{16} when S_5 and S_8 are turned on, and ends when i_3 increases to zero. Because the anti-parallel diodes conduct prior to the main switches of S_5 and S_8, so S_5 and S_8 are turned on with ZVS. The operating characteristics of port 1 and 3 are exactly same with interval 16.

Interval 18 (t_{17}–t_{18}): This interval begins at t_{17} when i_3 increases to zero, and ends when S_{10} and S_{11} are turned off. The difference between interval 18 and 17 is that the direction of i_3 changes.

3.1.2. Analysis for Voltage Source Load

This section analyzes the relationship between phase shift angle and power transmission, ZVS soft-switching realizing condition and peak current of the resonant tank under a given voltage source load.

The equivalent circuits of the three-port SR BDC are shown in Figure 6. In Figure 6a the output of three active bridges are represented by square waves V_{T1}, V_{T2} and V_{T3} respectively, and in Figure 6b V_{T3} of port 3 is transferred to port 1 and port 2 according to the transformer ratio.

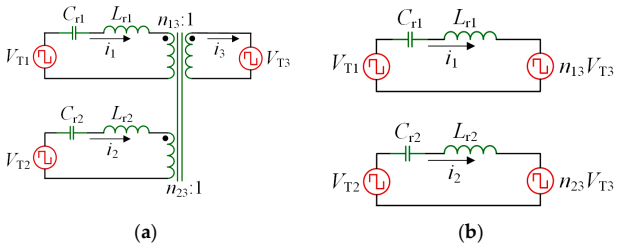


Figure 6. Equivalent circuits for analysis: (**a**) equivalent circuit of three-port SR BDC; (**b**) transformer equivalent model.

In the proposed three-port SR BDC, $L_{r1} = L_{r2} = L_r$, $C_{r1} = C_{r2} = C_r$, and the resonant frequency of SR tanks are f_r. The operating frequency of three ports is f_s, which is greater than f_r, and the corresponding angular velocity is ω_s. Then the impedance value of two resonant tanks can be given by:

$$X = \omega_s L_r - \frac{1}{\omega_s C_r} \tag{1}$$

The Fundamental Harmonics Approximation (FHA) method is a commonly used approach for steady-state analysis in resonant-type converters. And the accuracy level of the results obtained from FHA is acceptable for our work. To simplify the analysis procedure, all harmonics except fundamental component of all voltages and currents are neglected. $V_{T1,1}$, $V_{T2,1}$ and $V_{T3,1}$ are the fundamental components of square waves V_{T1}, V_{T2} and V_{T3}, and phase shift angles between port 1 and port 3, port 2 and port 3 are φ_1 and φ_2 respectively. Using the Fourier series, $V_{T1,1}$, $V_{T2,1}$ and $V_{T3,1}$ are shown as follows:

$$V_{T1,1} = \frac{4V_{\text{dc-link}}}{\pi} \sin(\omega_s t + \varphi_1) \tag{2}$$

$$V_{T2,1} = \frac{4V_{BA}}{\pi} \sin(\omega_s t + \varphi_2) \tag{3}$$

$$V_{T3,1} = \frac{4V_{\text{bus}}}{\pi} \sin \omega_s t \tag{4}$$

The variables M_{SC} and M_{BA} are defined as the voltage gain between port 1 and port 3, port 2 and port 3 respectively. They are given by (5) and (6):

$$M_{SC} = \frac{n_{13} V_{\text{bus}}}{V_{\text{dc-link}}} \tag{5}$$

$$M_{BA} = \frac{n_{23} V_{\text{bus}}}{V_{BA}} \tag{6}$$

Resonant currents of three ports can be obtained as follows:

$$i_1(t) = \frac{V_{T1,1} - n_{13} V_{T3,1}}{jX} = \frac{4V_{\text{dc-link}}}{\pi X} \left[\sin(\omega_s t + \varphi_1 - 90^\circ) - M_{SC} \sin(\omega_s t - 90^\circ) \right] \tag{7}$$

$$i_2(t) = \frac{V_{T2,1} - n_{23} V_{T3,1}}{jX} = \frac{4V_{BA}}{\pi X} \left[\sin(\omega_s t + \varphi_2 - 90^\circ) - M_{BA} \sin(\omega_s t - 90^\circ) \right] \tag{8}$$

$$i_3(t) = n_{13} i_1(t) + n_{23} i_2(t) \tag{9}$$

Switches in port 1 and port 2 can realize ZVS only when the resonant tank currents lag their applied square wave voltages. While for port 3, the defined positive current direction is contrary to port 1 and 2, the condition for ZVS realization is that the resonant current leads its applied square wave voltage. Then the constraint conditions for ZVS of port 1–3 can be given by (10)–(12) respectively:

$$i_1\left(-\frac{\varphi_1}{t}\right) = \frac{4V_{\text{dc-link}}}{\pi X} (M_{SC} \cos \varphi_1 - 1) < 0 \tag{10}$$

$$i_2\left(-\frac{\varphi_2}{t}\right) = \frac{4V_{BA}}{\pi X} (M_{BA} \cos \varphi_2 - 1) < 0 \tag{11}$$

$$i_3(0) = n_{13} \frac{4V_{\text{dc-link}}}{\pi X} (M_{SC} - \cos \varphi_1) + n_{23} \frac{4V_{BA}}{\pi X} (M_{BA} - \cos \varphi_2) > 0 \tag{12}$$

By calculating the maximum value of $i_1(t)$ and $i_2(t)$, the peak current of two resonant tanks can be derived as:

$$i_{1\max} = \frac{4V_{\text{dc-link}}}{\pi X} \sqrt{1 + {M_{SC}}^2 - 2M_{SC} \cos \varphi_1} \tag{13}$$

$$i_{2\max} = \frac{4V_{\mathrm{BA}}}{\pi X}\sqrt{1 + {M_{\mathrm{BA}}}^2 - 2M_{\mathrm{BA}}\cos\varphi_2} \tag{14}$$

The transferred power from SC and BA ports to the bus port can be calculated as follows:

$$P_1 = \frac{1}{2\pi}\int_0^{2\pi} V_{\mathrm{T1}}(t)\cdot i_1(t)d(\omega_s t) = \frac{8{V_{\text{dc-link}}}^2 M_{\mathrm{SC}}}{\pi^2 X}\sin\varphi_1 \tag{15}$$

$$P_2 = \frac{1}{2\pi}\int_0^{2\pi} V_{\mathrm{T2}}(t)\cdot i_2(t)d(\omega_s t) = \frac{8{V_{\mathrm{BA}}}^2 M_{\mathrm{BA}}}{\pi^2 X}\sin\varphi_2 \tag{16}$$

Equations (15) and (16) indicate that the power transferred from SC and BA ports to the DC bus port are proportional to the sinusoidal values of φ_1 and φ_2 respectively. It is obviously that the power transmission is positive when φ_1 and φ_2 values are positive, and conversely the power flow is negative.

3.1.3. Analysis for Resistive Load

This section explains the relationship of voltage gain, power transmission and phase shift angles under a resistive load. If the DC bus port is connected to a pure resistive load, the output voltage V_{bus} needs to be derived. According to superposition theorem, in the three-port SR BDC with linear resistive load, the output voltage V_{bus} can be divided into two parts: V_{busSC} and V_{busBA}. V_{busSC} and V_{busBA} are output voltage values when only one of the two inputs works alone. M_{busSC} and M_{busBA} are the corresponding voltage gain, and are given by:

$$M_{\mathrm{busSC}} = \frac{n_{13}V_{\mathrm{busSC}}}{V_{\text{dc-link}}} \tag{17}$$

$$M_{\mathrm{busBA}} = \frac{n_{23}V_{\mathrm{busBA}}}{V_{\mathrm{BA}}} \tag{18}$$

Under specific output voltage value and phase shift angles conditions, the transferred power is given in (15) and (16), no matter what kind of load is connected to the DC bus port. If the load resistance is defined as R_{L}. Combing (15) and (16), the output power P_1 and P_2, when $V_{\text{dc-link}}$ and V_{BA} work alone, can be given by:

$$P_1 = \frac{{V_{\mathrm{busSC}}}^2}{R_{\mathrm{L}}} = \frac{8{V_{\text{dc-link}}}^2 M_{\mathrm{busSC}}}{\pi^2 X}\sin\varphi_1 \tag{19}$$

$$P_2 = \frac{{V_{\mathrm{busBA}}}^2}{R_{\mathrm{L}}} = \frac{8{V_{\mathrm{BA}}}^2 M_{\mathrm{busBA}}}{\pi^2 X}\sin\varphi_2 \tag{20}$$

By combing (17)–(20), the voltage gain M_{busSC} and M_{busBA} can be given as follows:

$$M_{\mathrm{busSC}} = \frac{8{n_{13}}^2 R_{\mathrm{L}}}{\pi^2 X}\sin\varphi_1 \tag{21}$$

$$M_{\mathrm{busBA}} = \frac{8{n_{23}}^2 R_{\mathrm{L}}}{\pi^2 X}\sin\varphi_2 \tag{22}$$

According to the superposition theorem, the output voltage V_{bus} with resistive R_{L} can be given by:

$$V_{\mathrm{bus}} = \frac{8n_{13}R_{\mathrm{L}}}{\pi^2 X}\sin\varphi_1 V_{\text{dc-link}} + \frac{8n_{23}R_{\mathrm{L}}}{\pi^2 X}\sin\varphi_2 V_{\mathrm{BA}} \tag{23}$$

3.2. Operating Principle of Three-Phase Interleaved BDC

The operating principles of the three-phase interleaved BDC are analyzed in this section. The proposed three-phase interleaved BDC is shown in Figure 7. When power transfers from SC

to the dc-link, it works under boost mode and switches Q_{D1}–Q_{D3} are main switches. If direction of power transfer is reversed, the BDC works under buck mode and switches Q_{U1}–Q_{U3} are main switches. L_1–L_3 are buck/boost inductors, C_1 and C_{f1} are filter capacitors. By adopting three-phase interleaving structure, current ripple of SC port can be minimized and thus the required filter capacitance can be reduced.

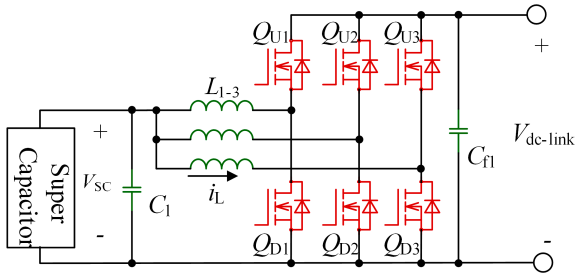


Figure 7. Circuit diagram of the proposed three-phase interleaved BDC.

For the proposed three-phase interleaved BDC, switches of one phase leg conduct complementarily, and the inductor current can go through from positive to negative and then raise to positive. This will ensure all the switches realize ZVS turn on.

The three-phase interleaved channels adopt the same control strategy, but hold a phase shift of $\pi/3$ in driving signal. In order to simplify the analysis, the operating characteristics of single phase are introduced. Circuit diagram of single phase is shown in Figure 8, and theoretical waveforms under boost mode are shown in Figure 9.

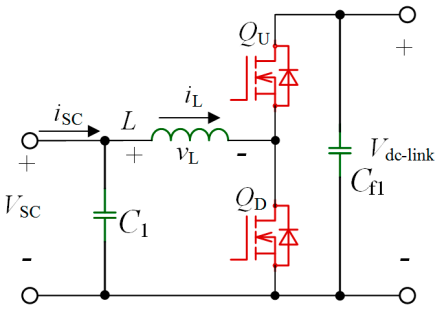


Figure 8. Circuit diagram of single phase.

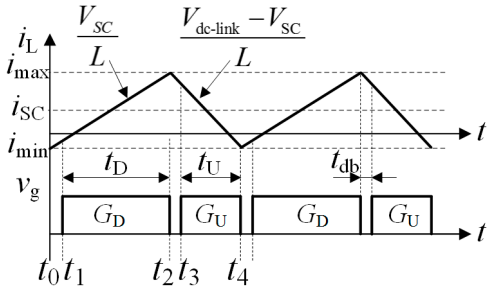


Figure 9. Theoretical waveforms of single phase under boost mode.

The parameters are defined as follows: V_{SC} and $V_{dc\text{-}link}$ are the voltage of SC and dc-link; i_L and v_L are voltage and current of the buck/boost inductor L; i_{max} and i_{min} are the maximum and minimum value of i_L respectively; Δi is the variation of i_L during one switching cycle; i_{SC} is the current of SC. t_{db} is dead band time; T_s is switching period; t_D and t_U are the conducting time of Q_U and Q_D separately.

For single-phase BDC, there are four different intervals in one switching cycle. Same as the above analysis of three-port SR BDC, dead time is considered, while charging and discharging intervals of snubber capacitors are neglected.

Interval 1 (t_0–t_1): This interval is dead band time, both Q_U and Q_D are off, and it ends when Q_D is turned on. During this interval, $i_L < 0$ and it flows through the anti-parallel diode of Q_D. If the conduction voltage drop of anti-parallel diode is neglected, $v_L = V_{SC}$ and i_L increases linearly.

Interval 2 (t_1–t_2): During this interval, Q_D is on and Q_U is off, i_L flows through Q_D. Since the anti-parallel diodes conduct prior to the main switches of Q_D, thus it is turned on with ZVS. Same as interval 1, i_L increases linearly.

Interval 3 (t_2–t_3): This interval is also dead band time, both Q_U and Q_D are off, and it ends when Q_U is turned on. Different from interval 1, during this interval $i_L > 0$, so it flows through the anti-parallel diode of Q_U. $v_L = V_{SC} - V_{dc\text{-}link}$ and this value is less than zero, so i_L decreases linearly.

Interval 4 (t_3–t_4): During this interval, Q_U is on and Q_D is off. i_L flows through Q_U. Same as interval 3, i_L decreases linearly. Since the anti-parallel diodes conduct before main switches of Q_U, it is turned on with ZVS.

Compared to t_D and t_U, t_{db} can be ignored, so Δi can be derived as follows:

$$\Delta i = \frac{V_{SC}}{L} \cdot \frac{V_{dc\text{-}link} - V_{SC}}{V_{dc\text{-}link}} \cdot T_S \tag{24}$$

To maintain ZVS switching of Q_U and Q_D, it must be ensured that $i_{max} > 0$ and $i_{min} < 0$.

4. ZVS Region Analysis and Proposed Method for Expanding ZVS Realization Range

Since the transformer voltage of port 3 is clamped by the output voltage V_{bus}, so there is no direct energy interaction between port 1 and port 2. Thus, the three-port SR BDC can be decomposed into two single input SR BDCs. The ZVS realization and current stress of single channel SR BDC can provide reference for the three-port SR BDC. To simplify the analysis, the ZVS realization region and current stress of single channel SR BDC are analyzed in this section.

4.1. ZVS Region and Current Stress Analysis of Single Channel SR BDC

Through (10)–(12), the ZVS constraint conditions for primary-side and secondary-side can be simplified as follows:

$$\text{Primary-side} : M\cos\varphi - 1 < 0 \tag{25}$$

$$\text{Secondary-side} : M - \cos\varphi > 0 \tag{26}$$

The ZVS regions of primary and secondary sides of single channel SR BDC are shown in Figure 10a,b, respectively. Figure 10a shows that when $M < 1$ all switches of primary side can realize ZVS, while as shown in Figure 10b, switches of secondary side can only realize ZVS when φ is greater than a certain value. When $M > 1$ situations are just contrary to situations when $M < 1$. It can be obtained that, the ZVS realization regions of primary and secondary sides change reversely under varying M. So during the design process, M should be as close to 1 as possible, and $M = 1$ is the best choice to achieve ZVS for all the switches of primary and secondary sides.

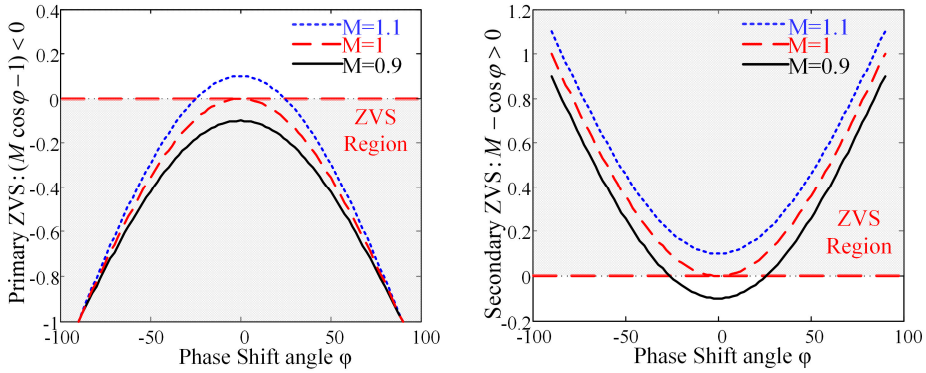


Figure 10. ZVS range of single channel SR BDC versus phase shift angel φ under different M: (**a**) primary side; (**b**) secondary side.

Before analyzing the peak value of resonant current under varying M, it must be noticed that phase shift angles to transfer same power under different M are varying. If we suppose that the phase shift angle under unity voltage gain (M = 1) is φ, and the phase shift angel to transfer same power under varying M is α. The relationship between φ and α is shown in (27) and (28). It is shown in (13) and (14) that with certain input voltage, resonant parameters and switching frequency, the peak value of resonant current is directly proportional to N which is shown in (29). The diagrams of N under $M < 1$ and $M > 1$ are shown in Figure 11a,b, respectively:

$$\frac{8{V_{\text{dc-link}}}^2}{\pi^2 X}\sin\varphi = \frac{8{V_{\text{dc-link}}}^2 M}{\pi^2 X}\sin\alpha \tag{27}$$

$$\alpha = \arcsin\frac{\sin\varphi}{M} \tag{28}$$

$$\begin{aligned} i_{\max} &= \tfrac{4V_{\text{dc-link}}}{\pi X} \times N \\ N &= \sqrt{1 + M^2 - 2M\cos\alpha} \end{aligned} \tag{29}$$

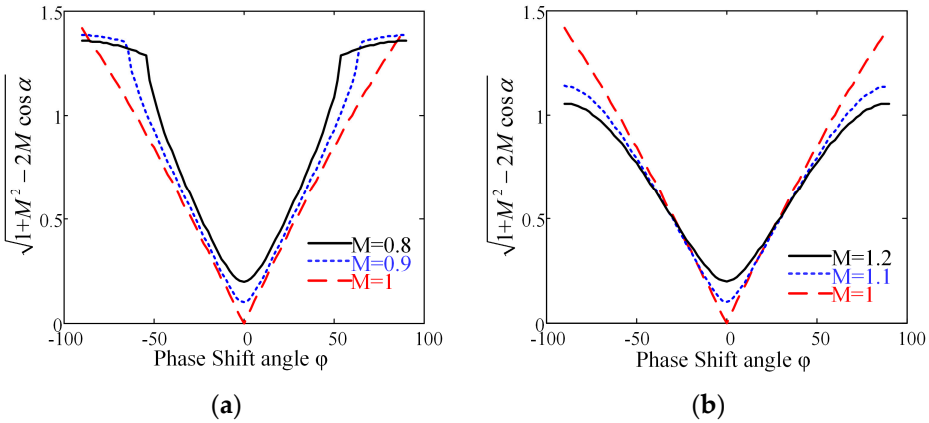


Figure 11. Peak current of single channel SR BDC versus phase shift angel φ under different M: (**a**) $M < 1$; (**b**) $M > 1$.

Figure 11 shows that, when $M < 1$, the peak current of resonant tanks increases with the decreases of M in a large range. While when $M > 1$, the peak current increases with the increases of M in a certain range. In the design process, the phase shift must be limited in a relatively small range to restrict

cut off current of switches. So, from the point of limiting peak value of resonant current, M should be designed as close to 1 as possible. And $M = 1$ is the best choice to achieve minimize peak value of resonant current. Through the analysis above, both M_{SC} and M_{BA} should be designed to be 1 to achieve best operating characteristics. While the voltages of SC and BA are all not fixed value. To solve this problem, different methods for two channels are proposed.

(1) For the SC channel, the voltage has a large variation range, and can't get an ideal operating state only by reasonable parameters design. Therefore, a three-phase interleaved BDC is introduced between SC and port 1 of the three-phase SR BDC. The interleaved BDC is used to convert the widely fluctuating V_{SC} to a fixed $V_{dc\text{-}link}$, and thus ensuring $M_{SC} = 1$.

(2) Since voltage variation scale is relatively small for the BA channel, it is not essential to add BDC converter as SC channel does. A new PWM-PHS control strategy is proposed for the BA channel. The newly proposed control method has two phase shift angles for modulation, and can increase number of MOSFETs which can realize ZVS.

4.2. Proposed PWM and Phase Shift Hybrid Control Strategy

The difference of the newly proposed PWM-PHS control strategy and the traditional phase shift control method is that there are two phase-shift angles to modulate for the BA channel. This can provide more control flexibility, and can increase the number of ZVS switches under a wide variation of V_{BA}. In this method, two switches in each phase leg also work complementary with 50% duty cycle. The two phase legs of BA port are defined as phase leg A and phase leg B, and corresponding phase shift angles are represented as φ_{2A} and φ_{2B} respectively. The phase shift angles between two legs is δ, $\varphi_{2B} = \varphi_{2A} - \delta$. While, when S5 and S7, or S6 and S8 conduct together, the instantaneous value of V_{T2} is zero, so the pulse width of is not 180° any more. The pulse width of the newly proposed control method is $(180 - \delta)°$, so it can be regarded as the combination of PWM and PHS control. The theoretical waveforms for the BA channel under PWM-PHS control strategy is shown in Figure 12.

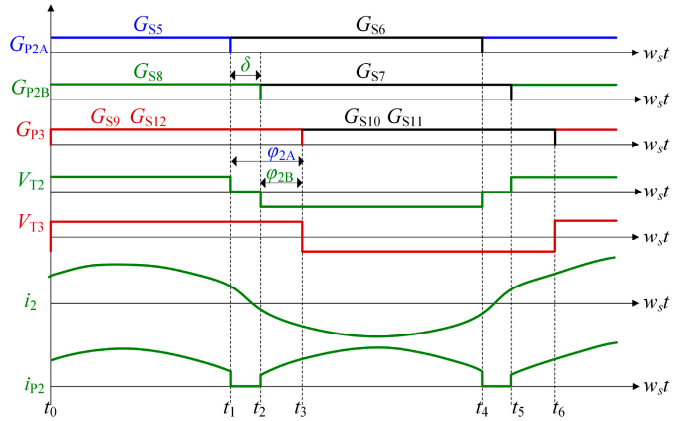


Figure 12. Theoretical waveforms for BA channel under PWM-PHS control method with $M_{BA} = 1.15$.

The fundamental components of square waves V_{T2} under PWM-PHS control method can be shown as (30). Referring to the analysis above, the resonant current and power transmission value of port 2 under PWM-PHS control method can be shown as (31) and (32) respectively:

$$V_{T2,1} = \frac{2V_{BA}}{\pi}[\sin(\omega_s t + \varphi_{2A}) + \sin(\omega_s t + \varphi_{2B})] \tag{30}$$

$$i_2(t) = \frac{2V_{BA}}{\pi X}\left[\sin(\omega_s t + \varphi_{2A} - 90^\circ) + \sin(\omega_s t + \varphi_{2B} - 90^\circ) - 2M_{BA}\sin(\omega_s t - 90^\circ)\right] \tag{31}$$

$$P_2 = \frac{4{V_{BA}}^2 M_{busBA}}{\pi^2 X}(\sin\varphi_{2A} + \sin\varphi_{2B}) = \frac{4{V_{BA}}^2 M_{busBA}}{\pi^2 X}[\sin\varphi_{2A} + \sin(\varphi_{2A} - \delta)] \tag{32}$$

The ZVS constraint conditions for phase leg A and B of primary side and secondary side can be shown as follows:

$$\text{Primary-side leg A}: \quad i_2\left(-\frac{\varphi_{2A}}{t}\right) = \frac{2V_{BA}}{\pi X}(2M_{BA}\cos\varphi_{2A} - 1 - \cos\delta) < 0 \tag{33}$$

$$\text{Primary-side leg B}: \quad i_2\left(-\frac{\varphi_{2B}}{t}\right) = \frac{2V_{BA}}{\pi X}[2M_{BA}\cos(\varphi_{2A} - \delta) - \cos\delta - 1] < 0 \tag{34}$$

$$\text{Secondary-side}: \quad i_2(0) = \frac{2V_{BA}}{\pi X}(2M_{BA} - \cos\varphi_{2A} - \cos\varphi_{2B}) > 0 \tag{35}$$

Equations (26) and (35) show that when $M_{BA} > 1$, all switches of secondary side can realize ZVS under traditional control method and the newly proposed PWM-PHS control method. Therefore, only the ZVS realization conditions for the primary side are analyzed. The designed maximum value of M_{BA} is 1.15, and the following analysis is under condition of $M_{BA} = 1.15$.

To transfer same power under traditional phase shift control method and newly proposed PWM-PHS control method, phase shift angles of φ_2, φ_{2A} and δ should satisfy the constraint condition shown in (36) and (37). The diagram of ZVS operating range of primary side phase leg A and B for the variation of δ under $M_{BA} = 1.15$ is given in Figure 13:

$$\frac{8{V_{BA}}^2 M_{busBA}}{\pi^2 X}\sin\varphi_2 = \frac{4{V_{BA}}^2 M_{busBA}}{\pi^2 X}[\sin\varphi_{2A} + \sin(\varphi_{2A} - \delta)] \tag{36}$$

$$\varphi_{2A} = \arcsin\left[\frac{\sin\varphi_2}{\cos(0.5\delta)}\right] + \frac{\delta}{2} \tag{37}$$

Figure 13a,c shows the ZVS range of phase leg A and B in the primary side, Figure 13b,d is the zoom-in diagrams of Figure 13a,c, respectively. The enlarged ZVS range of phase leg A and B are defined as η and γ respectively. Figure 13 shows that the ZVS range of phase leg A and B can be enlarged with the increase of δ. The enlarged ZVS range of phase leg A and B are represented in Figure 13b,d. During η and γ, the ZVS MOSFETs number of primary side under traditional phase shift control ($\delta = 0$) is 0, while the ZVS MOSFETs number under PWM-PHS control ($\delta \neq 0$) is 2.

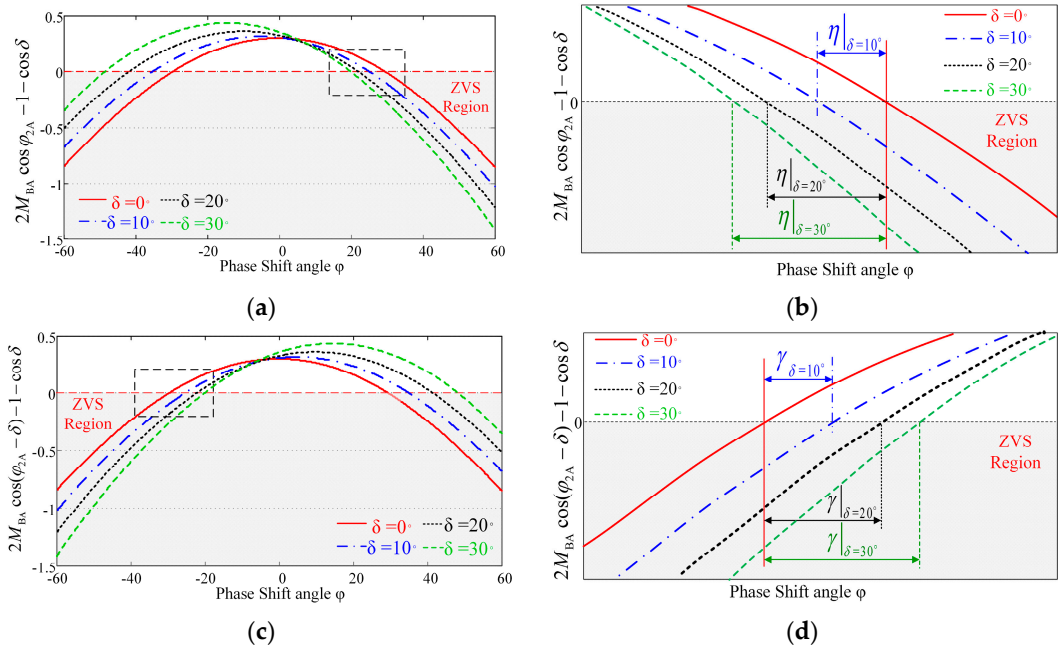


Figure 13. Soft switching range of primary side for variation of δ under $M_{BA} = 1.15$: (**a**) phase leg A; (**b**) zoom-in figure of (**a**); (**c**) phase leg B; (**d**) zoom-in figure of (**c**).

The theoretical analysis results prove that the proposed PWM-PHS control method can increase the number of MOSFETs which can realize ZVS under specific power condition.

4.3. Control Strategy of the Proposed Two-Stage Three-Port BDC

Through the proposed two-stage three-port BDC, HESS is integrated to the DC bus of DC microgrid. The proposed three-port BDC is composed of two parts: three-port SR BDC and three-phase interleaved BDC. The control target of three-port SR BDC is to keep DC bus voltage constant by compensating the mismatch between generation and demand. Meanwhile, the control objective of the three-phase interleaved BDC is converting the widely fluctuating SC voltage V_{sc} to a constant voltage $V_{dc\text{-}link}$. The control scheme for the proposed two-stage three-port BDC is shown in Figure 14.

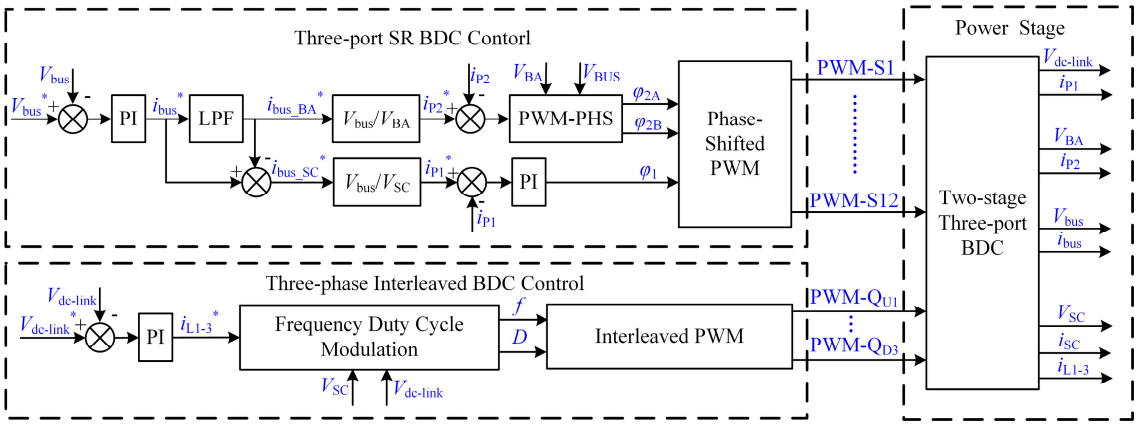


Figure 14. Control scheme for the proposed two-stage three-port BDC.

The basic idea of the three-port SR BDC is that the battery supports slow transients, and SC supports fast transients. The control structure has an inner current loop as well as an outer control loop for voltage stabilization. The bus voltage V_{bus} is compared with the reference voltage V_{bus}*, and the deviation of voltage is tracked by the voltage PI controller to produce the total current reference i_{bus}*. By using a low-pass filter (LPF), the total current is divided into a dynamic component i_{bus_SC}* and an average component i_{bus_BA}*. Then, the reference currents of SC and BA are derived as i_{P1}* and i_{P2}* respectively. Through the inner current loops, phase shift angles are adjusted to maintain a constant DC bus voltage.

The control objective of the three-phase interleaved BDC is to keep the dc-link voltage constant. Same with the control method of three-port SR BDC, $V_{dc\text{-}link}$ is compared with reference voltage $V_{dc\text{-}link}$*. The current reference is obtained through the outer voltage loop. Combining the current reference and voltage values, the driving frequency f and duty ratio D are deduced. Through the interleaved PWM generator, driving signals of three-phase interleaved BDC are acquired.

5. Experimental Results

To verify the validity of theoretical analyses, a 1 kW prototype was built in the laboratory. The MOSFETs adopted in the system are C3M0065090D units from CREE (Durham, NC, USA). The control platform is a TMS320F28379D from Texas Instruments (Dallas, TX, USA). Based on the theoretical analysis above, a set of optimized parameters of the proposed system are selected and shown in Table 1.

Table 1. Parameters of the proposed system.

Converter Parameter	Value
Resonant Inductor L_{r1} and L_{r2}	15 μH
Resonant Capacitors C_{r1} and C_{r2}	141 nF
Transformer turns ratio n_{13}:n_{23}:1	0.425:0.51:1
Port 1 voltage $V_{dc\text{-}link}$	85 V
Port 2 voltage V_{BA}	90 V–102 V
Port 3 voltage V_{bus}	200 V
Voltage Gain M_{SC}	1
Voltage Gain M_{BA}	1–1.15
Super Capacitor Voltage V_{SC}	30 V–75 V
Buck/Boost Inductor of BDC L	15 μH

5.1. SC and BA Charging Mode

For the SC and BA charging mode, a 200 V voltage source is provided for port 3, port 1 and port 2 are connected to resistive loads of 15 Ω, in this experiment V_{T1} and V_{T2} lag V_{T3}. Port 1 and 2 are entirely independent from each other. The concrete data of this experiment are as follows: input voltage V_{bus} = 200 V, output voltage $V_{dc\text{-}link}$ = 84 V, driving frequency f_s = 130 kHz, $\varphi_1 = -18.5°$, $\varphi_2 = -20°$; V_{BA} = 102 V, $P_1 = -458.2$ W, $P_2 = -684.5$ W, $P_3 = -1204.3$ W. The efficiency is 94.9%. $M_{SC} = M_{BA} = 1$, thus all switches of 3 ports can realize ZVS. The required phase shift angles to realize $M_{SC} = M_{BA} = 1$ are compared in Table 2. It is proved that the experimental results are consistent with theoretical analysis.

Table 2. Comparison of φ_1 and φ_2 under theoretical calculation and experiment.

Method	φ_1	φ_2
Theoretical Calculation	−19.1°	−19.1°
Experiment	−18.5°	−20°

Figure 15 shows the waveforms of resonant currents of the three-port SR BDC.

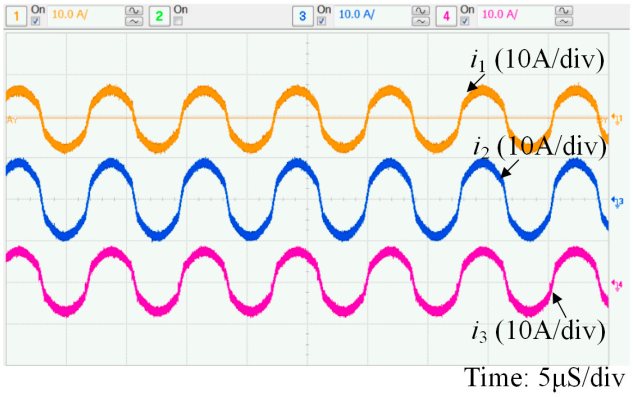


Figure 15. Waveforms of resonant currents of three ports under SC and BA charging mode.

Figure 16 shows the waveforms of resonant currents and transformer voltages of three ports. Figure 16a,b show the operating waveforms of port 1, such as resonant current i_1, drain-source voltage and driving voltage of S1 v_{DS_S1} and v_{G_S1}. Figure 16b is the zoom-in waveforms of Figure 16a, from it we can see that the MOSFETs of port 1 can realize ZVS. Figure 16c,d show the operating waveforms of port 2, resonant current i_2, drain-source voltage and driving voltage of S_5 v_{DS_S5} and v_{G_S5}. Figure 16e,f

show waveforms of port 3. It is shown that MOSFETs of port 2 and 3 can realize ZVS under SC and BA charging mode with $M_{SC} = M_{BA} = 1$.

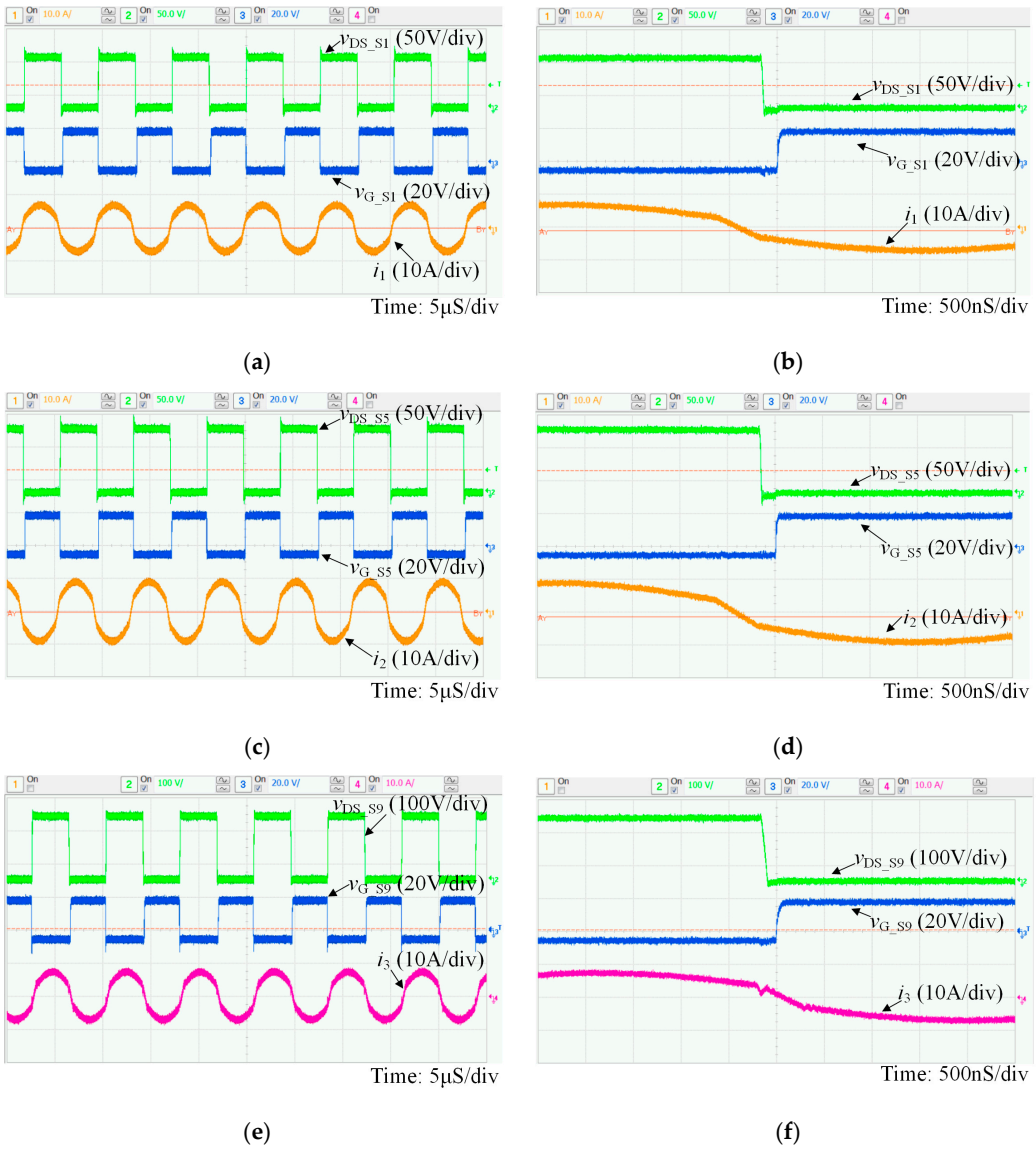


Figure 16. Experimental results of three-port SR BDC under SC and BA charging mode: (**a**,**b**) SC port; (**c**,**d**) BA port; (**e**,**f**) DC bus port.

5.2. SC and BA Discharging Mode

In the SC and BA discharging mode, two voltage sources are connected to SC and BA port respectively, a resistive load of 40 Ω is connected to port 3. Power is transferred from port 1 and 2 to port 3. Both M_{busSC} and M_{busBA} are designed as 0.5. The concrete data of this experiment are as follows: input voltage $V_{SC} = 30$ V, $V_{BA} = 102$ V, $V_{dc\text{-}link} = 85$ V, output voltage $V_{bus} = 200$ V; driving frequency $f_s = 130$ kHz, $\varphi_1 = 18.2°$, $\varphi_2 = 13.4°$; $P_1 = 521.5$ W, $P_2 = 533.9$ W, $P_3 = 993.1$ W. The efficiency of two stage three-port BDC is 94.1%. All switches of three ports can realize ZVS.

The required phase shift angles to realize $M_{busBA} = M_{busSC} = 0.5$ are compared in Table 3. It is proved that the experimental results are consistent with theoretical analysis. For the three-phase interleaved BDC, inductor currents i_{L1}–i_{L3} and $V_{dc\text{-}link}$ are shown in Figure 17, and they are completely consistent with the theoretical analysis waveforms.

Table 3. Comparison of φ_1 and φ_2 under theoretical calculation and experiment.

Method	φ_1	φ_2
Theoretical Calculation	19.8°	13.6°
Experiment	18.2°	13.4°

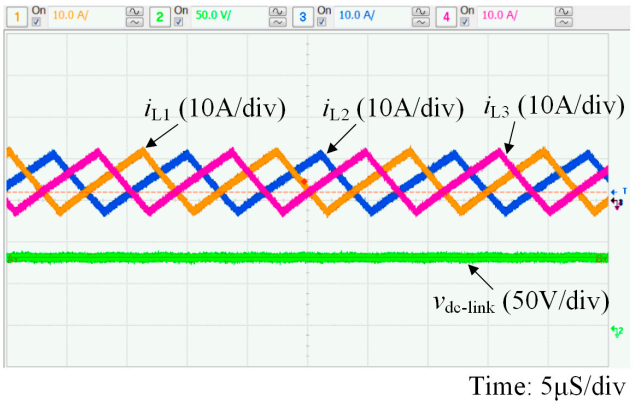


Figure 17. Waveforms of three-phase interleaved BDC.

Figure 18 shows the waveforms of resonant currents of three ports. Figure 19a shows i_1, v_{DS_S1} and v_{G_S1} of port 1. Figure 19c shows i_2, v_{DS_S5} and v_{G_S5} of port 2. Figure 19e shows i_3, v_{DS_S9} and v_{G_S9} of port 3. Figure 19b,d,f is enlarged waveforms of Figure 19a,c,e. The waveforms of three ports are consistent with analysis above, and all MOSFETs of three-ports can realize under conditions when $M_{SC} = M_{BA} = 1$.

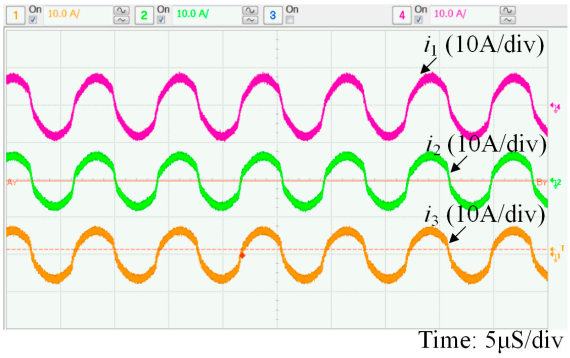
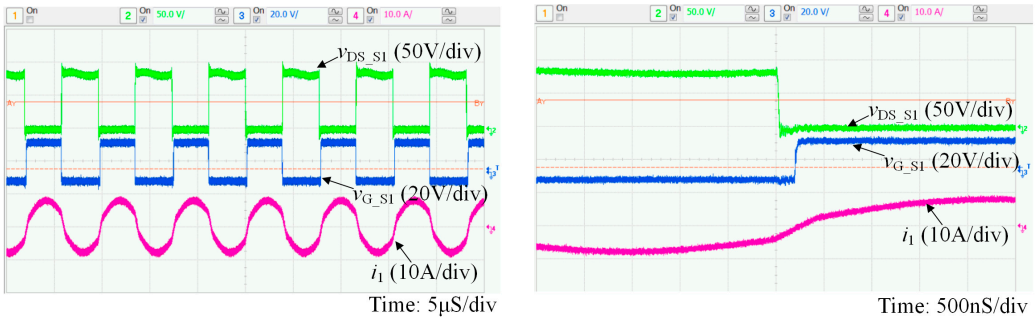


Figure 18. Waveforms of resonant currents of three ports and transformer port voltages.



(**a**) (**b**)

Figure 19. *Cont.*

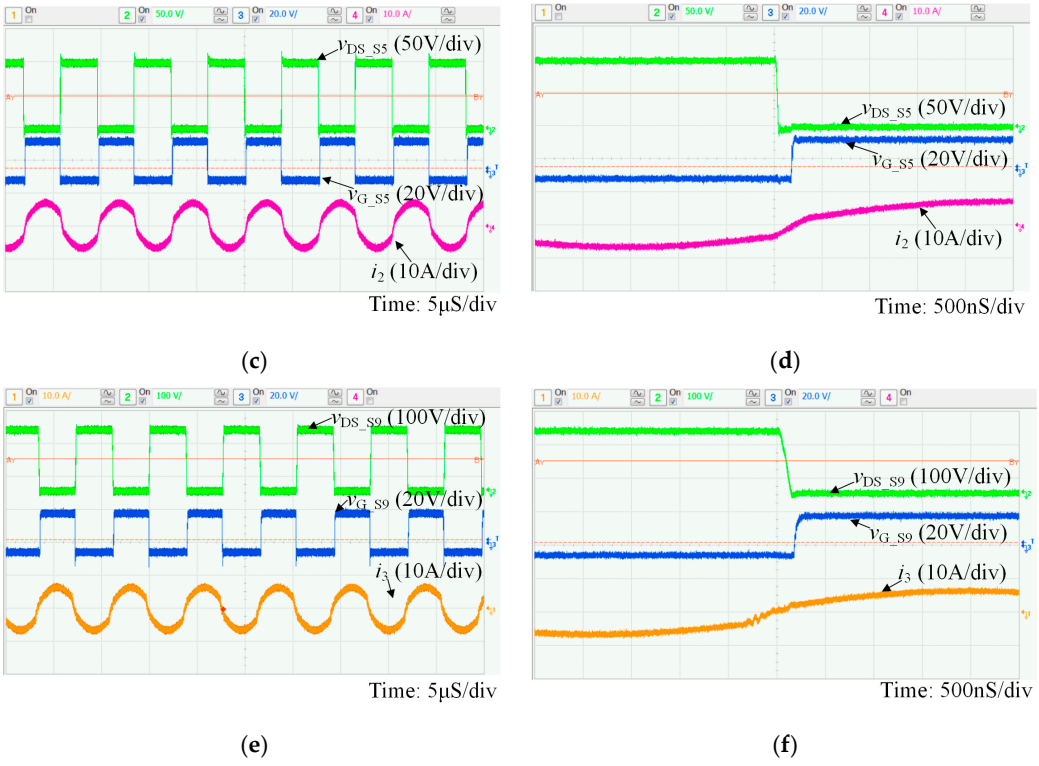


Figure 19. Experimental results of three-port SR BDC under SC and BA charging mode: (**a**,**b**) SC port; (**c**,**d**) BA port; (**e**,**f**) DC bus port.

5.3. Proposed PWM-PHS Control Method

The effectiveness of proposed PWM-PHS control method is verified based on the BA channel for battery discharging mode. A 80 Ω resistive load is connected to port 3. The operating parameters are defined as follows: V_{BA} = 45 V, V_{bus} = 100 V, M_{BA} = 1.15. Two groups of contrast experiment are done, two groups adapt traditional phase-shift and the newly proposed PWM-PHS control method, respectively.

The operating parameters under traditional phase shift control method are as follows: driving frequency f_s = 130 kHz, φ_{2A} = φ_{2B} = 23.4°, P_2 = 138.3 W, P_3 = 124.6 W, the efficiency is 90.1%. Figure 20a,c shows the operating waveforms of port 2 and 3. Resonant current i_2, drain-source voltage and driving voltage of S5 and S9 are given. Figure 20b,d is enlarged waveforms of Figure 20a,c. Experimental results show that MOSFETs of BA port can't realize ZVS, MOSFETs of DC bus port operate under ZVS when M_{BA} = 1.15.

As shown in Figure 20a,b, MOSFETs of BA port can't realize ZVS, drive signal of *S*5 turns positive before the output capacitor of *S*5 gets fully discharged. Parasitic ringing, which is due to oscillation between output capacitance of *S*5 and parasitic inductance present in the converter layout, occurs during turn-on switching transient. In Figure 20c,d, output capacitor is fully discharged before driving signal turns positive. Consequently, ZVS is achieved for MOSFETs of DC bus port, and parasitic ringing is avoided.

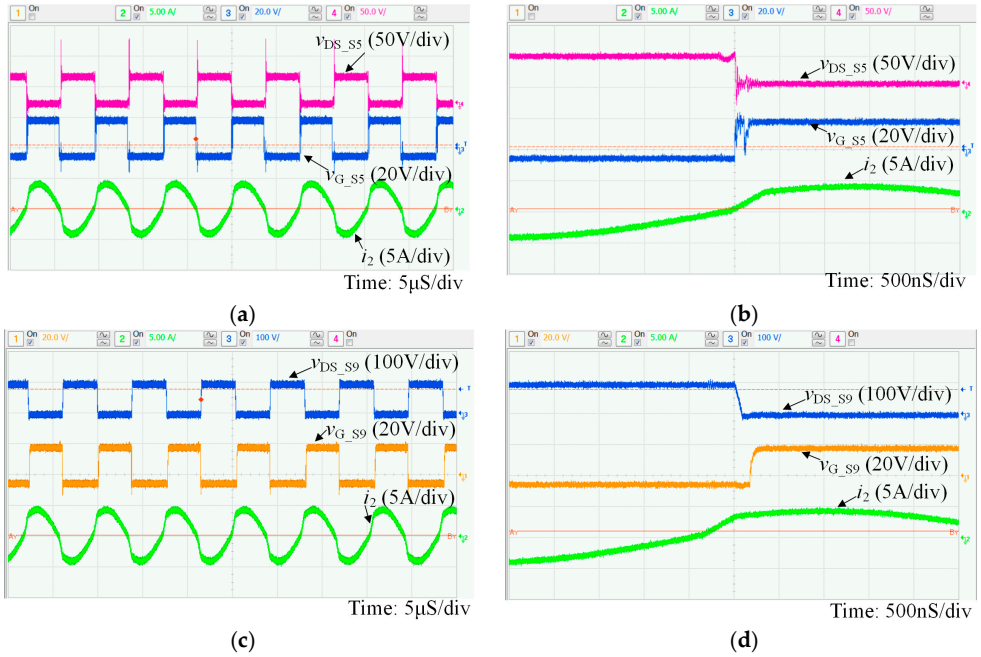


Figure 20. Experimental results of BA channel using phase-shift control method under M_{BA} = 1.15: (**a**,**b**) BA port; (**c**,**d**) DC bus port.

The operating parameters under phase shift control method are as follows: driving frequency f_s = 130 kHz, φ_{2A} =35.8°, φ_{2B} = 10.8°, P_2 = 134.8 W, P_3 = 125 W, the efficiency is 92.7%. The efficiency is relatively low since the power level is low.

Figure 21a,c shows the operating waveforms of phase leg A and B of port 2 respectively. Figure 21e shows waveforms of port 3. Resonant current i_2, drain-source voltage and driving voltage of S5, S7 and S9 are given. Figure 21b,d,f is enlarged waveforms of Figure 21a,c,e. Experimental results show that MOSFETs of phase A of BA port realize ZVS, MOSFETs of phase B of BA port can't realize ZVS, MOSFETs of DC bus port achieve ZVS operating when M_{BA} = 1.15.

Like the conditions shown in Figure 20a,b, MOSFETs of phase B can't realize ZVS, and parasitic ringing presents during the turn-on switching transients. The experimental results above show that, when using traditional phase shift control method, only four switches can realize ZVS, and the efficiency is 90.1%. While, by adopting the newly proposed, the number of switches which can realize ZVS increases to 6, and the efficiency increases to 92.7%. The experimental results are consistent with theoretical analysis. It is proved that the PWM-PHS control method can improve operating characteristics of SR BDC under the condition of $M_{BA} > 1$.

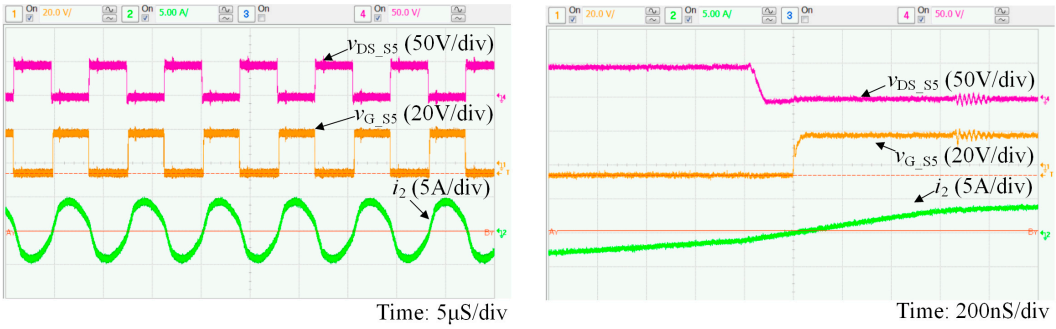


Figure 21. *Cont.*

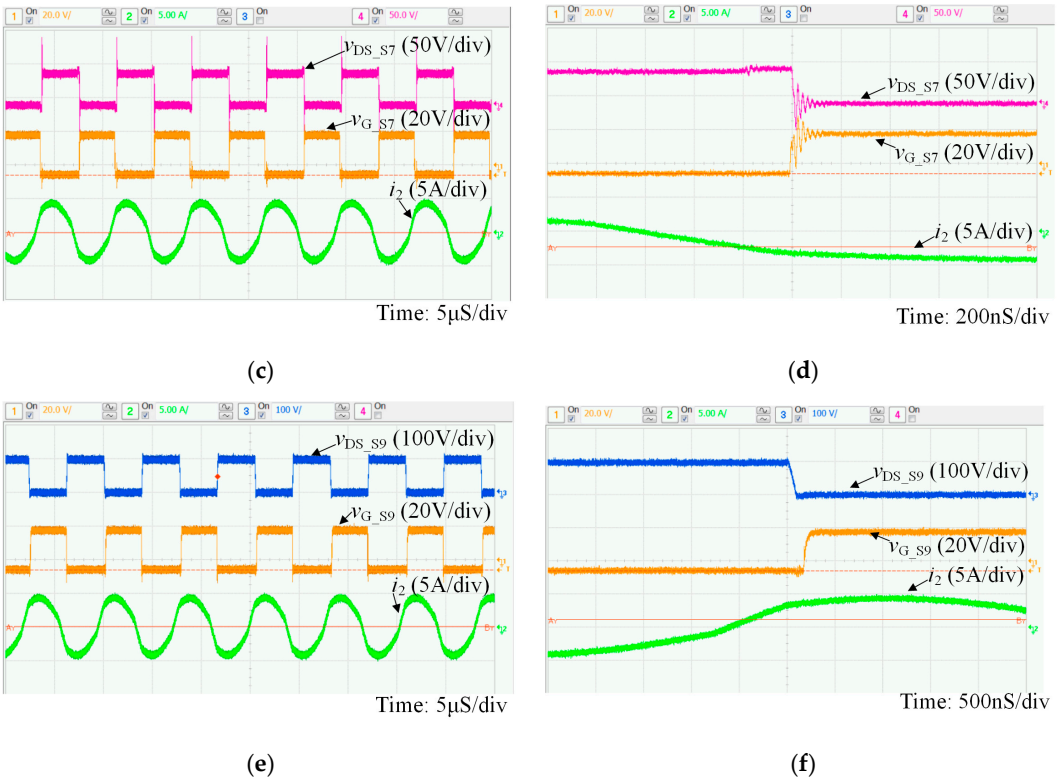


Figure 21. Experimental results of BA channel using PWM-PHS control method under M_{BA} = 1.15: (**a**,**b**) phase leg A of BA port; (**c**,**d**) phase leg B of BA port; (**e**,**f**) DC bus port.

6. Conclusions

In this paper, a two-stage three-port BDC is fabricated to interface SC and BA with the DC microgrid. It is composed of a three-port SR BDC and a three-phase interleaved BDC. The particular two-stage structure makes it possible to handle wide voltage variations at SC port, and will ensure unity voltage gain between SC and DC bus ports. In addition, a PWM-PHS hybrid control method is applied on the BA channel. The proposed control method contributes to an increasing number of switches operating under ZVS under variable voltage gain. Together with the proposed PWM-PHS control strategy, the proposed BDC acquires optimized operation characteristics with both enlarged ZVS range and reduced power circulation loss. Finally, a 1 kW prototype is built, and the efficiency of SC and BA charging and discharging mode are 94.9% and 94.1% respectively. The experimental results validate that all switches of SC and DC bus ports can realize ZVS under varying V_{SC}. With the proposed topology and PWM-PHS control method, two more switches of BA port achieve ZVS even under the worst input condition of M_{BA} = 1.15.

Acknowledgments: This research was supported by the National High Technology Research and Development Program of China (863 Program) (Grant: 2015AA050603) and supported by Tianjin Municipal Science and Technology Commission (Grant: 14ZCZDGX00035). The authors would also like to thank the anonymous reviewers for their valuable comments and suggestions to improve the quality of the paper.

Author Contributions: Cheng-Shan Wang, Wei Li and Yi-Feng Wang designed the main parts of the study, including the circuit simulation model, topology innovation and simulation development. Fu-Qiang Han and Zhun Meng helped in the hardware development and experiment. Guo-Dong Li were also responsible for writing the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Marzband, M.; Ardeshiri, R.R.; Moafi, M.; Uppal, H. Distributed generation for economic benefit maximization through coalition formation based on Game Theory. *Int. Trans. Electr. Energy Syst.* **2017**, 1–16. [CrossRef]
2. Han, Y.; Chen, W.; Li, Q. Energy Management Strategy Based on Multiple Operating States for a Photovoltaic/Full Cell/Energy Storage DC Microgrid. *Energies* **2017**, *10*, 136. [CrossRef]
3. Liu, J.; Zhang, L. Strategy Design of Hybrid Energy Storage System for Smoothing Wind Power Fluctuations. *Energies* **2016**, *9*, 991. [CrossRef]
4. Marzband, M.; Ghazimirsaeid, S.S.; Uppal, H.; Fernando, T. A real-time evaluation of energy management systems for smart hybrid home Microgrids. *Electr. Power Syst. Res.* **2017**, *143*, 624–633. [CrossRef]
5. Marzband, M.; Moghaddam, M.M.; Akorede, M.F.; Khomeyrani, G. Adaptive load shedding scheme for frequency stability enhancement in microgrids. *Electr. Power Syst. Res.* **2016**, *140*, 78–86. [CrossRef]
6. Xu, Q.; Hu, X.; Wang, P.; Xiao, J.; Tu, P.; Wen, C.; Lee, M.Y. A Decentralized Dynamic Power Sharing Strategy for Hybrid Energy Storage System in Autonomous DC Microgrid. *IEEE Trans. Ind. Electr.* **2016**. [CrossRef]
7. Kollimalla, S.K.; Mishra, M.K.; Ukil, A.; Gooi, H.B. DC Grid Voltage Regulation Using New HESS Control Strategy. *IEEE Trans. Sustain. Energy* **2016**, *8*, 772–781. [CrossRef]
8. Jin, Z.; Hou, M.; Dong, F.; Li, Y. A New Control Strategy of DC Microgrid with Photovoltaic Generation and Hybrid Energy Storage. In Proceedings of the IEEE PES Asia-Pacific Power and Energy Conference, Xi'an, China, 25–28 October 2016; pp. 434–438.
9. Marzband, M.; Alavi, H.; Ghazimirsaeid, S.S.; Uppal, H.; Fernando, T. Optimal Energy Management System Based on Stochastic Approach for a Home Microgrid with Integrated Responsive Load Demand and Energy Storage. *Sustain. Cities Soc.* **2017**, *28*, 256–264. [CrossRef]
10. Marzband, M.; Parhizi, N.; Savaghebi, M.; Guerrero, J.M. Distributed Smart Decision-Making for a Multi-microgrid System Based on a Hierarchical Interactive Architecture. *IEEE Trans. Energy Convers.* **2016**, *31*, 637–648. [CrossRef]
11. Marzband, M.; Azarinejadian, F.; Savaghebi, M.; Guerrero, M. An Optimal Energy Management System for Islanded Microgrids Based on Multiperiod Artificial Bee Colony Combined With Markov Chain. *IEEE Syst. J.* **2015**, *100*, 1–11. [CrossRef]
12. Marzband, M.; Yousefnejad, E.; Sumper, A.; Domínguez-García, J.L. Real Time Experimental Implementation of Optimum Energy Management System in Standalone Microgrid by Using Multi-layer Ant Colony Optimization. *Int. Trans. Electr. Energy Syst.* **2016**, *75*, 265–274. [CrossRef]
13. Marzband, M.; Ghadimi, M.; Sumper, A.; Domínguez-García, J.L. Experimental validation of a real-time energy management system using multi-period gravitational search algorithm for microgrids in islanded mode. *Appl. Energy* **2014**, *128*, 164–174. [CrossRef]
14. Marzband, M.; Parhizi, N.; Adabi, J. Optimal energy management for stand-alone microgrids based on multi-period imperialist competition algorithm considering uncertainties: Experimental validation. *Int. Trans. Electr. Energy Syst.* **2016**, *26*, 1358–1372. [CrossRef]
15. Marzband, M.; Sumper, A.; Ruiz-Álvarez, A.; Domínguez-García, J.L. Experimental evaluation of a real time energy management system for stand-alone microgrids in dayahead markets. *Appl. Energy* **2013**, *106*, 365–376. [CrossRef]
16. Marzband, M.; Sumper, A.; Domínguez-García, J.L.; Gumara-Ferret, R. Experimental Validation of a Real Time Energy Management System for Microgrids in Islanded Mode Using a Local Day-Ahead Electricity Market and MINLP. *Energy Convers. Manag.* **2013**, *76*, 314–322. [CrossRef]
17. Zhang, N.; Sutanto, D.; Muttaqi, K.M. A review of topologies of three-port DC–DC converters for the integration of renewable energy and energy storage system. *Renew. Sustain. Energy Rev.* **2016**, *56*, 388–401. [CrossRef]
18. Chien, L.J.; Chen, C.C.; Chen, J.F.; Hsieh, Y.P. Novel Three-Port Converter with High-Voltage Gain. *IEEE Trans. Power Electron.* **2014**, *29*, 4693–4703. [CrossRef]
19. Lai, C.M.; Yang, M.J. A High-Gain Three-Port Power Converter with Fuel Cell, Battery Sources and Stacked Output for Hybrid Electric Vehicles and DC-Microgrids. *Energies* **2016**, *9*, 180. [CrossRef]
20. Hu, Y.; Xiao, W.; Cao, W.; Ji, B. Three-Port DC–DC Converter for Stand-Alone Photovoltaic Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 3068–3076. [CrossRef]

21. Wang, Z.; Li, H. An Integrated Three-Port Bidirectional DC-DC Converter for PV Application on a DC Distribution System. *IEEE Trans. Power Electron.* **2013**, *28*, 4612–4624. [CrossRef]
22. Sun, X.; Shen, Y.; Li, W. A Novel LLC Integrated Three-port DC-DC Converter for Stand-alone PV/Battery System. In Proceedings of the IEEE Transportation Electrification Conference and Expo, Asia-Pacific, Beijing, China, 31 August–3 September 2014; pp. 1–6.
23. Duarte, J.L.; Hendrix, M.; Simões, M.G. Three-Port Bidirectional Converter for Hybrid Fuel Cell Systems. *IEEE Trans. Power Electron.* **2007**, *22*, 480–487. [CrossRef]
24. Phattanasak, M.; Gavagsaz-Ghoachani, R.; Martin, J.P.; Pierfederici, S. Flatness Based control of an Isolated Three-port Bidirectional DC-DC converter for a Fuel cell hybrid source. In Proceedings of the IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011; pp. 977–984.
25. Fontana, C.; Buja, G.; Bertoluzzo, M.; Kumar, K. Power and control characteristics of an isolated three-port DC-DC converter under DCM operations. In Proceedings of the Annual Conference of the IEEE Industrial Electronics Society, Florence, Italy, 24–27 October 2016; pp. 4211–4216.
26. Phattanasak, M.; Gavagsaz-Ghoachani, R.; Martin, J.P.; Nahid-Mobarakeh, B. Control of a Hybrid Energy Source Comprising a Fuel Cell and Two Storage Devices Using Isolated Three-Port Bidirectional DC–DC Converters. *IEEE Trans. Ind. Appl.* **2015**, *51*, 491–497. [CrossRef]
27. Wang, L.; Wang, Z.; Li, H. Asymmetrical Duty Cycle Control and Decoupled Power Flow Design of a Three-port Bidirectional DC-DC Converter for Fuel Cell Vehicle Application. *IEEE Trans. Power Electron.* **2012**, *27*, 891–904. [CrossRef]
28. Wang, Z.; Liu, B.; Zhang, Y.; Cheng, M.; Chu, K.; Xu, L. The Chaotic-Based Control of Three-Port Isolated Bidirectional DC/DC Converters for Electric and Hybrid Vehicles. *Energies* **2016**, *9*, 83. [CrossRef]
29. Ling, Z.; Wang, H.; Yan, K.; Gan, J. Optimal Isolation Control of Three-Port Active Converters as a Combined Charger for Electric Vehicles. *Energies* **2016**, *9*, 715. [CrossRef]
30. Li, X.; Bhat, A.K.S. Analysis and Design of High-Frequency Isolated Duan-Bridge Series Resonant DC/DC Converter. *IEEE Trans. Power Electron.* **2010**, *25*, 850–862.
31. Krishnaswami, H.; Mohan, N. Three-Port Series-Resonant DC-DC Converter to Interface Renewable Energy Sources with Bidirectional Load and Energy Storage Ports. *IEEE Trans. Power Electron.* **2009**, *24*, 2289–2297. [CrossRef]
32. Shreelekha, K.; Arulmozhi, S. Multiport isolated bidirectional DC-DC converter interfacing battery and supercapacitor for hybrid energy storage application. In Proceedings of the International Conference on Electrical, Electronics, and Optimization Techiniques, Chennai, India, 3–5 March 2016; pp. 2763–2768.
33. Tao, H.; Kotsopoulos, A.; Duarte, J.L.; Hendrix, M.A.M. Transformer-Coupled Multiport ZVS Bidirectional DC–DC Converter with Wide Input Range. *IEEE Trans. Power Electron.* **2008**, *23*, 771–781. [CrossRef]
34. Oggier, G.; Garcia, G.O.; Oliva, A. Switching Control Strategy to Minimize Dual Active Bridge Converter Losses. *IEEE Trans. Power Electron.* **2009**, *24*, 1826–1838. [CrossRef]
35. Xu, D.; Zhao, C.; Fan, H. A PWM Plus Phase-Shift Control Bidirectional DC-DC Converter. *IEEE Trans. Power Electron.* **2004**, *19*, 666–675. [CrossRef]
36. Tao, H.; Duarte, J.L.; Hendrix, M.A.M. Three-Port Triple-Half-Bridge Bidirectional Converter with Zero-Voltage Switching. *IEEE Trans. Power Electron.* **2008**, *23*, 782–792.
37. Baek, J.-B.; Choi, W.-I.; Cho, B.-H. Digital Adaptive Frequency Modulation for Bidirectional DC-DC Converter. *IEEE Trans. Power Electron.* **2013**, *60*, 5167–5176. [CrossRef]
38. Nandankar, P.V.; Rothe, J. Hihgly efficient discontinuous mode interleaved DC-DC converter. In Proceedings of the International Conference on Electrical, Electronics, and Optimization Techiniques, Chennai, India, 3–5 March 2016; pp. 476–481.