energies

MDPI

Article

A Novel High Step-Up DC-DC Converter with Coupled Inductor and Switched Clamp Capacitor Techniques for Photovoltaic Systems

Yong-Seng Wong [1,2], Jiann-Fuh Chen [1,*], Kuo-Bin Liu [2] and Yi-Ping Hsieh [3]

1 Department of Electrical Engineering, National Cheng Kung University, No. 1 University Road, Tainan 701, Taiwan; wochenseng@gmail.com
2 Power Supply Group, National Synchrotron Radiation Research Center, 101, Hsin-Ann Road, Hsinchu 300, Taiwan; kbl@nsrrc.org.tw
3 Mission Critical Infrastructure Solutions Business Unit, Delta Electronics INC, 39 Section 2, Huan-dong Road, Shanhua Township, Tainan 741, Taiwan; kyo124718@yahoo.com.tw
* Correspondence: chenjf@mail.ncku.edu.tw; Tel.: +886-6-275-7575 (ext. 62353)

Academic Editors: Jih-Sheng (Jason) Lai and Frede Blaabjerg
Received: 9 September 2016; Accepted: 10 March 2017; Published: 16 March 2017

Abstract: In this study, a novel high step-up DC-DC converter was successfully integrated using coupled inductor and switched capacitor techniques. High step-up DC-DC gain was achieved using a coupled inductor when capacitors charged and discharged energy, respectively. In addition, energy was recovered from the leakage inductance of the coupled inductor by using a passive clamp circuit. Therefore, the voltage stress of the main power switch was almost reduced to $1/7\ V_o$ (output voltage). Moreover, the coupled inductor alleviated the reverse-recovery problem of the diode. The proposed circuit efficiency can be further improved and high voltage gain can be achieved. The operation principle and steady-state analysis of the proposed converter were discussed. Finally, a hardware prototype circuit with input voltage of 24 V, output voltage of up to 400 V, and maximum power of 150 W was constructed in a laboratory; the maximum efficiency was almost 96.2%.

Keywords: high voltage gain; switch-clamp capacitor; power generation; energy conversion

1. Introduction

In recent years, air pollution and energy shortage have become major national concerns. When the global temperature increases by 1 °C, the sea level will increase by 2.3 m [1]. This phenomenon will considerably affect human life and safety. Therefore, previous studies have attempted to find a solution, hoping to solve the problems of air pollution, global warming, and energy shortage by using highly efficient renewable energy systems. The current more mature and widely used renewable energy sources include solar, wind, and tidal energy sources [2–4]. Often these renewable energy sources have low-voltage output and must pass through a set of high boost converter circuits to increase the voltage, and then through a DC-AC inverter to convert AC voltage from the main supply in parallel. Therefore, a DC-DC high boost ratio circuit affects the overall efficiency of the system [5–8].

The conventional DC-DC boost circuit is not applied in high boost ratio applications. In an ideal scenario, when the duty cycle in a conventional boost circuit increases to 1 (unity), the boost conversion ratio reaches infinity. However, high step-up gain is limited by the capacitor, inductor main power switch, and resistance, because electromagnetic interference and reverse-recovery issues are encountered at extreme duty cycles. Moreover, the leakage inductance of the transformer will cause high power dissipation and high voltage spikes on the main power switch. Therefore, a main power switch with high stress voltage must be selected because of excessive cost and space issues. Therefore,

many studies have developed a new architecture to overcome the shortcomings of a conventional boost circuit. In particular, switch capacitor [9–13], coupled inductor [14–21], and voltage lift [22,23] techniques have been proposed. A coupled inductor step-up circuit with a simple inductive winding structure was used to achieve low voltage stress of the main switch and a high voltage conversion ratio. Therefore, this architecture is commonly used. However, the main drawback of this architecture is that the coupled inductor has a considerable leakage inductance; this leakage inductance and parasitic capacitance on the switch will resonate and cause voltage spikes. To solve the problems caused by leakage inductance, capacitors, resistors, and diodes comprising a snubber circuit can be used; however, the energy is consumed in the resistance, thus reducing circuit efficiency. Switched capacitor and voltage lift technology can achieve a high boost ratio function but the main switch suffers a high transient current, and the conduction loss is increased. A switched-clamp capacitor can store energy when the switch is turned on. When the power is switched off afterwards, the energy in the capacitor is delivered to the output loading. However, the electric system prevents current flow and no direct conduction path is permitted. The voltage lift technique is similar the Cuk converter or the single-ended primary inductor converter (SEPIC) converter, the energy transfer from one inductor via the intermediate capacitor and then to the other inductor. Therefore, the transferred energy is mainly determined by the capacitance, thus causing the current stress on the capacitor to be serious. The coupled-inductor technique can achieve high step-up gain by adjusting the turn ratio. However, the inductor leakage issue relates to the voltage spike on the power switch. Therefore, this study used a coupled inductor step-up circuit with a clamp circuit, which absorbed energy from the leakage inductor of the coupled inductor and supply the energy back to the output terminal of the capacitor during the next period [24,25]. Using a clamp circuit prevents spikes on the switch, and the main switch voltage stress is clamped at a voltage of $1/7\ V_o$. Moreover, the booster-circuit integrates a boost-flyback converter with switched capacitor architecture to achieve a high step-up ratio. This circuit has boost and flyback type features. When the switch is turned on, the first boost stage is similar to a boost converter combined with a switched capacitor converter. Conversely, when the switch is turned off, the second boost stage is similar to the flyback and switched capacitor converters [26–34]. The new proposed converter architecture can achieve a high step-up ratio by adjusting the duty cycle; a clamp circuit is used for energy recovery by the leakage inductor of the coupled inductor to achieve high efficiency and step-up ratio.

2. Operation Principle of the Proposed Converter

Figure 1 illustrates the proposed converter circuit topology, where the DC input voltage is V_{in}, main switch is S, and coupled inductors are N_p and N_s.

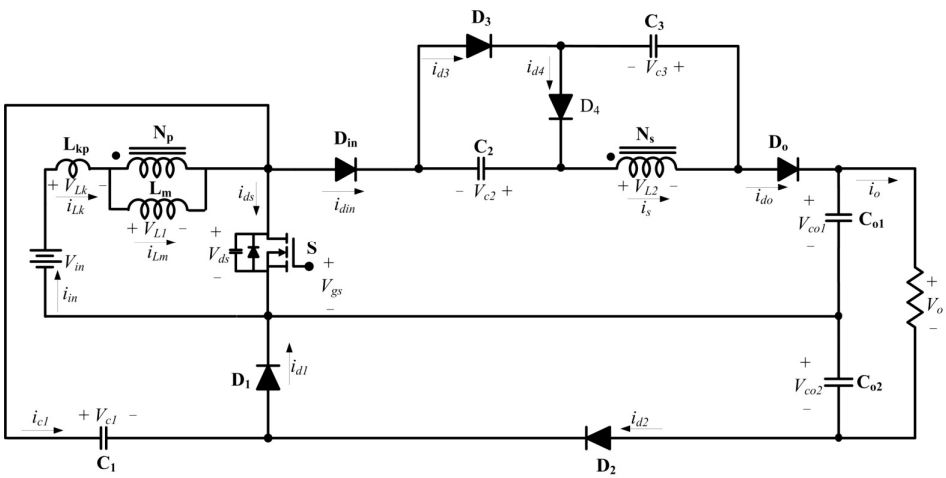


Figure 1. Circuit configuration of the proposed converter.

The clamp circuit has two diodes D_1 and D_2 and a capacitor C_1. The step-up circuit has two diodes D_3 and D_4 and two capacitors C_2 and C_3. The equivalent circuit of the coupled inductor comprises the leakage inductor L_k, magnetizing inductor L_m, and an ideal transformer with turn numbers N_p and N_s of the primary and secondary windings, respectively. To simplify the analysis of the circuit operation principles, the following conditions were assumed:

- Capacitors C_1–C_3 and C_{o1}–C_{o2} are sufficiently large. Therefore, V_{c1}–V_{c3} and V_{co1}–V_{co2} are considered constant during an operation.
- Power devices are ideal components, and the parasitic capacitors of power devices are not neglected.
- The magnetizing inductance is L_m and leakage inductance is L_k; the coupling coefficient of the coupled inductor is k and is equal to $L_m/(L_m+L_k)$.
- The turn ratio n is equal to N_s/N_p.
- The proposed converter operation can be divided into the continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The detail analysis is as follows:

2.1. CCM Operation

Figure 2 shows the main component current and voltage waveforms of the proposed converter during CCM operation.

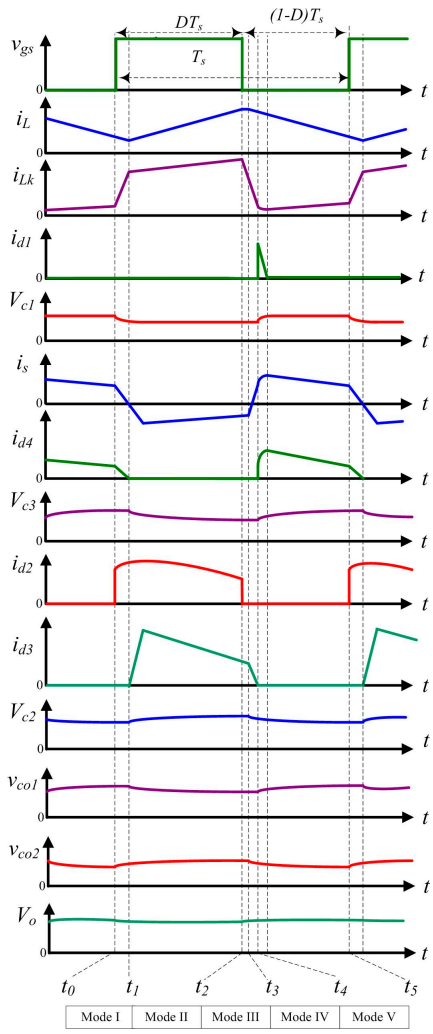


Figure 2. Key components current and voltage waveforms of the proposed converter at CCM.

This CCM operation can be divided into five operating modes as follows:

Mode I [t_0, t_1]: During this time interval, the power switch S is turned on, and D_2, D_4, D_{in}, and D_o are forward-biased. The equivalent circuit is shown in Figure 3a. The primary-side leakage magnetizing current i_{Lk} increases linearly, and the DC source V_{in} supplies energy to the magnetizing inductor L_m. The secondary-side leakage inductor current i_s supplies energy to the capacitor C_3, and V_{c3} is approximately equal to nV_{L1}. The clamp capacitor C_1 supplies energy to the high voltage output capacitor C_{o2}. When i_s equals zero at $t = t_1$, this operation mode is terminated.

Mode II [t_1, t_2]: The switch S is still turned on, and D_3 is forward-biased. The equivalent circuit is shown in Figure 3b. The DC source V_{in} supplies energy to the magnetizing inductor L_m. The secondary-side capacitor C_2 is charged by the coupled inductor and capacitor C_3. V_{c3} is approximately equal to $V_{c2} - nV_{L1}$. The output capacitors C_{o1} and C_{o2} provide energy to the output load. This operating mode is terminated when the switch S is turned off at $t = t_2$.

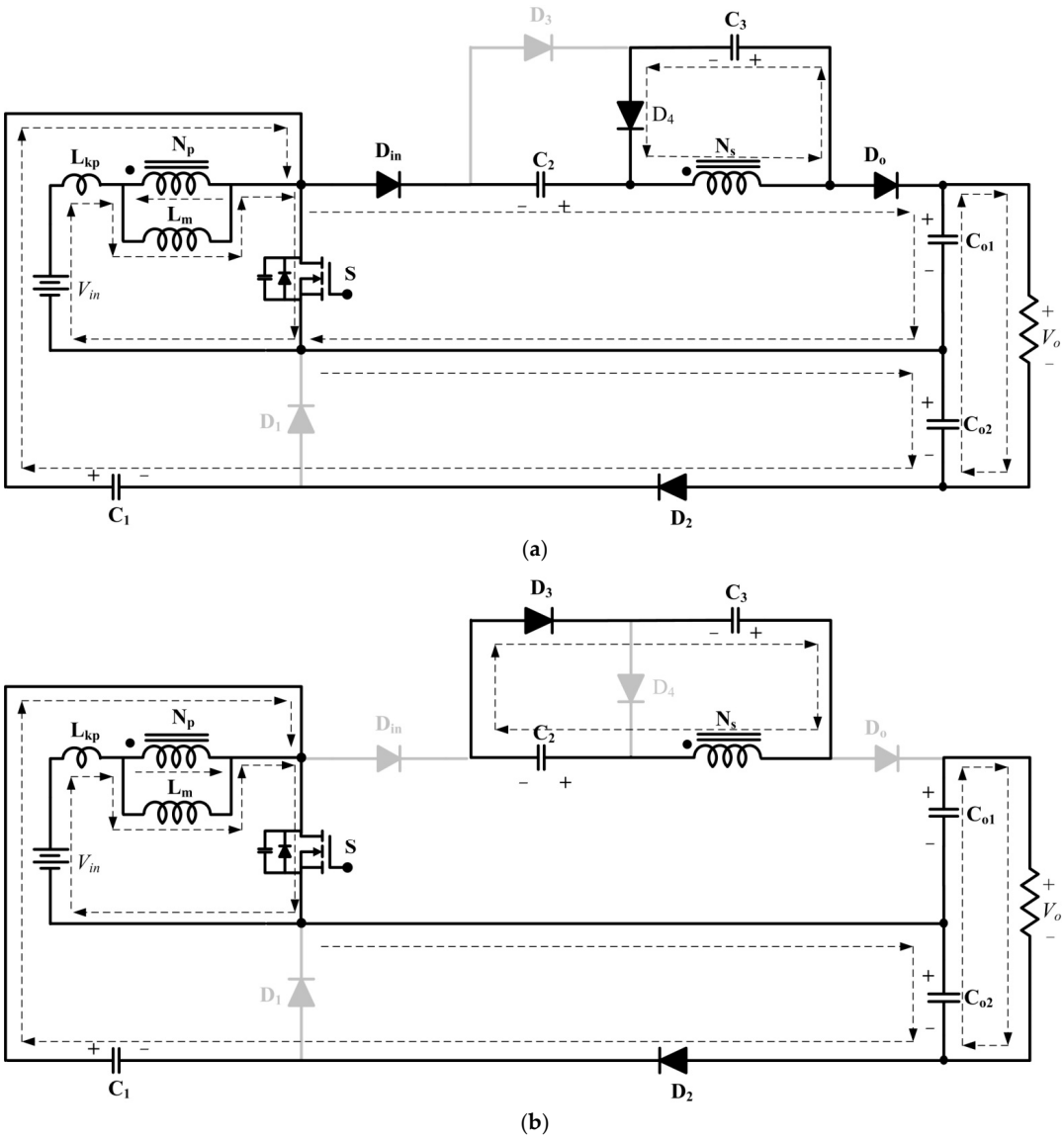


Figure 3. Operating modes at CCM during a switching period (Switch turn on). (**a**) Modes I; (**b**) Modes II.

Mode III [t_2, t_3]: At $t = t_2$, the switch S is turned off, and D_3 is forward-biased. The equivalent circuit is shown in Figure 4a. The parasitic capacitor C_{ds} of the main power switch S is charged rapidly by the leakage inductor L_k and magnetizing inductor L_m. The secondary-side capacitor C_2 is charged by the coupled inductor and capacitor C_3. The output capacitors C_{o1} and C_{o2} provide energy to the load.

Mode IV [t_3, t_4]: At $t = t_3$, the switch S is turned off, and D_1 and D_3 are forward-biased. The equivalent circuit is shown in Figure 4b. The passive clamp capacitor C_1 is charged by the leakage inductor L_k and magnetizing inductor L_m; the leakage inductor L_k is recovered and i_{Lk} decreases rapidly. The capacitor C_2 is charged continuously by the coupled inductor and capacitor C_3. This mode is terminated at $t = t_4$ until the secondary-side current i_s equals zero. Therefore, D_3 is turned off and D_4, D_{in}, and D_o are turned on.

Mode V [t_4, t_5]: At $t = t_4$, the switch S is turned off, and D_1, D_4, D_{in}, and D_o are forward-biased. The equivalent circuit is shown in Figure 4c. The coupled inductor, DC source V_{in}, and capacitor C_2 are connected to supply energy to the high-output voltage side capacitor C_{o1} and load. This mode is terminated at $t = t_5$, and the power switch S is turned on again during the next mode.

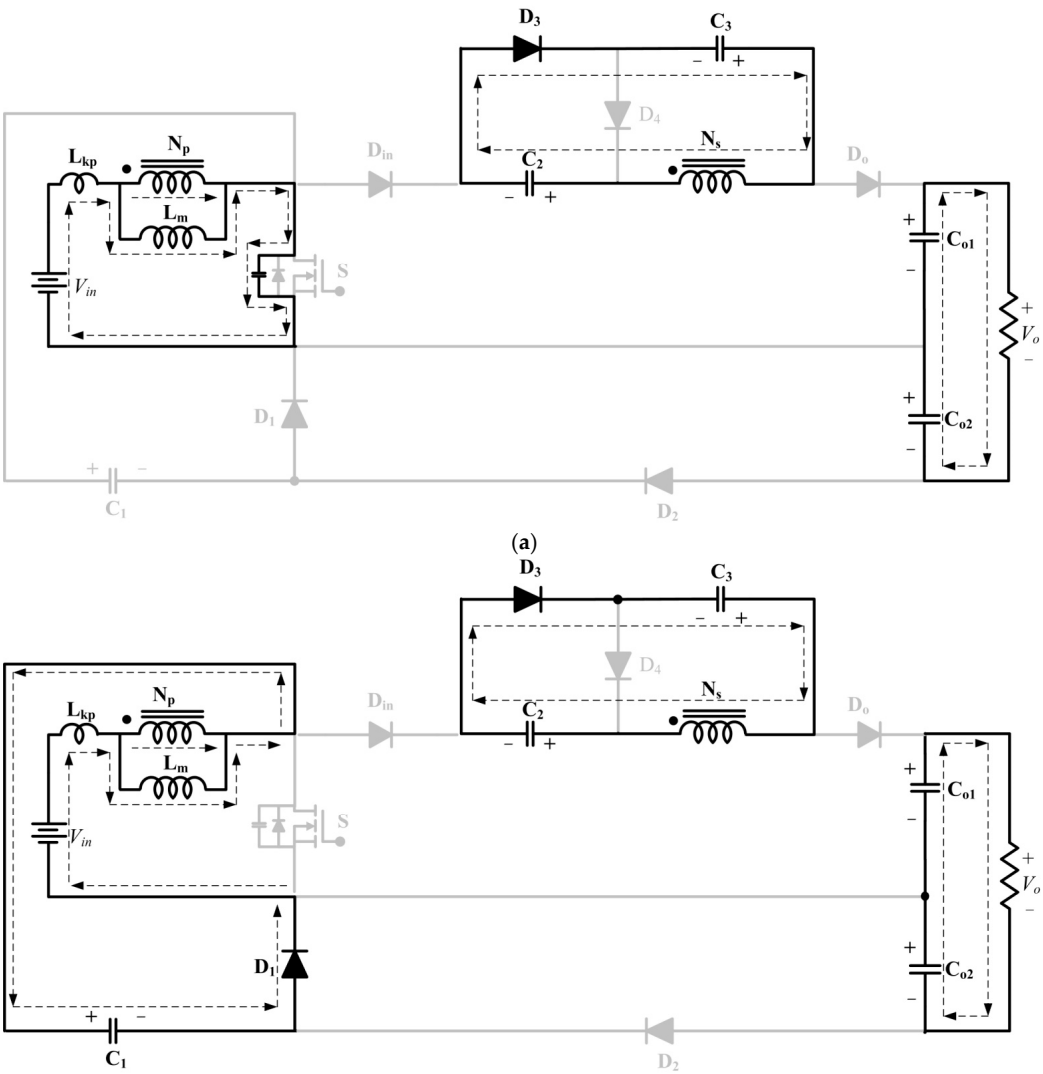
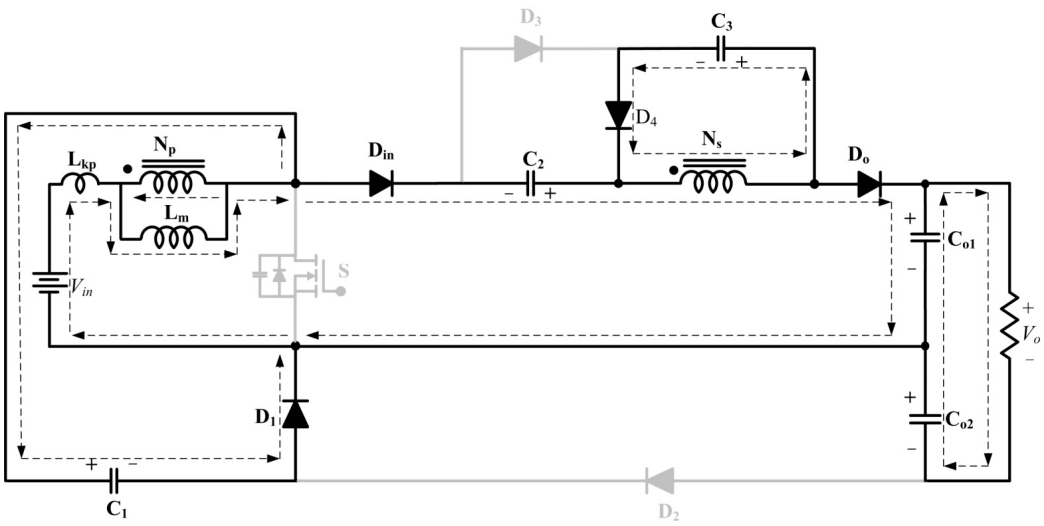


Figure 4. *Cont.*



(**c**)

Figure 4. Operating modes at CCM during a switching period (Switch turn off). (**a**) Modes III; (**b**) Modes IV; and (**c**) Modes V.

2.2. DCM Operation

Figure 5 shows the major component current and voltage waveforms of the proposed converter during the DCM operation. To simplify the analysis, the leakage inductor L_k of the coupled inductor is neglected during the DCM operation.

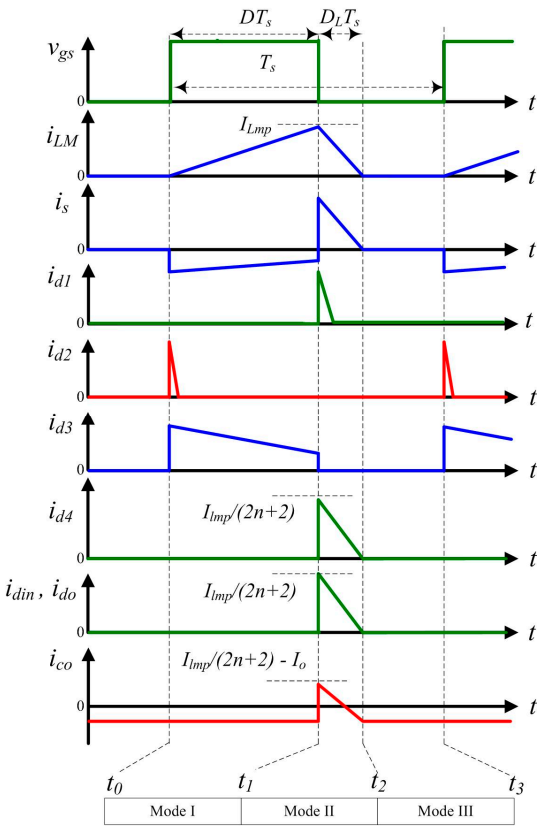


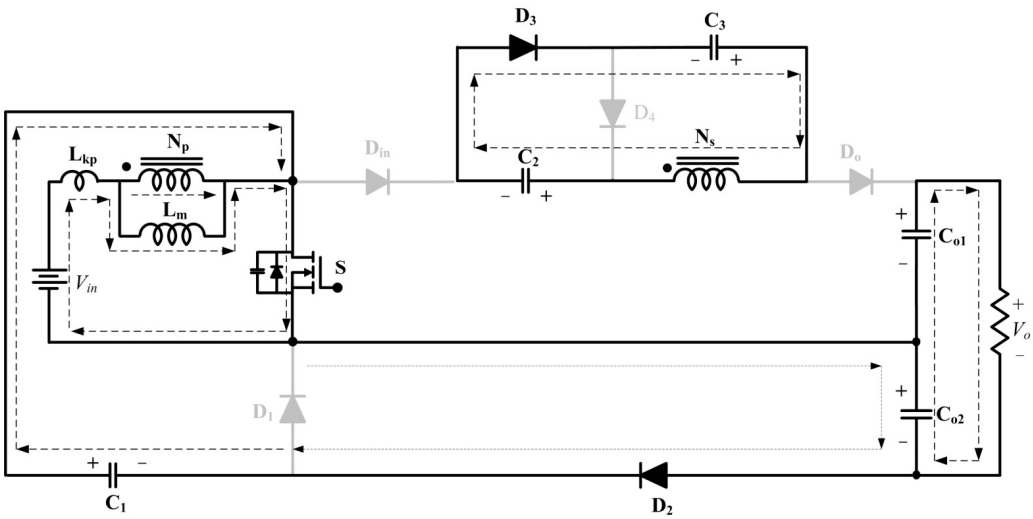
Figure 5. Key components current and voltage waveforms of the proposed converter at DCM operation.

Figure 6 shows the modes I–III operating stages. The operating modes are explained as follows:

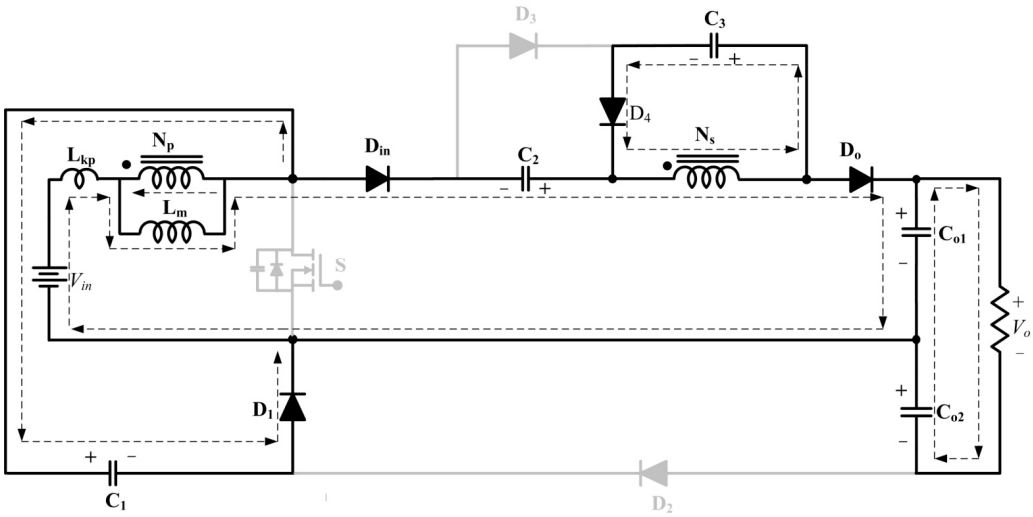
Mode I [t_0, t_1]: During this time interval, the power switch S is turned on, and D_2 and D_3 are forward-biased. The equivalent circuit is shown in Figure 6a. The primary current i_{Lm} increases linearly, and the DC source V_{in} supplies energy to the magnetizing inductor L_m. The secondary-side coupled inductor in series with the capacitor C_3 supplies energy to the capacitor C_2. The output capacitors C_{o1} and C_{o2} provide energy to the output load. The main switch S is turned off at $t = t_1$, and this operation mode is terminated.

Mode II [t_1, t_2]: During this time interval, the main switch S is turned off, and D_1, D_4, D_{in}, and D_o are forward-biased. The equivalent circuit is shown in Figure 6b. The magnetizing inductor L_m, DC source V_{in}, and capacitor C_2 are charged by D_{in} and D_o and supply energy to the output capacitor C_{o1}. The magnetizing energy of L_m is transferred to capacitor C_3 by coupled inductor. This operating mode is terminated when the energy stored in L_m is depleted at $t = t_2$.

Mode III [t_2, t_3]: During this time interval, the main switch S is turned off. The equivalent circuit is shown in Figure 6c. The output capacitors C_{o1} and C_{o2} provide energy to the output load. This mode is terminated at $t = t_3$, and the main switch S is turned on again during the next mode.

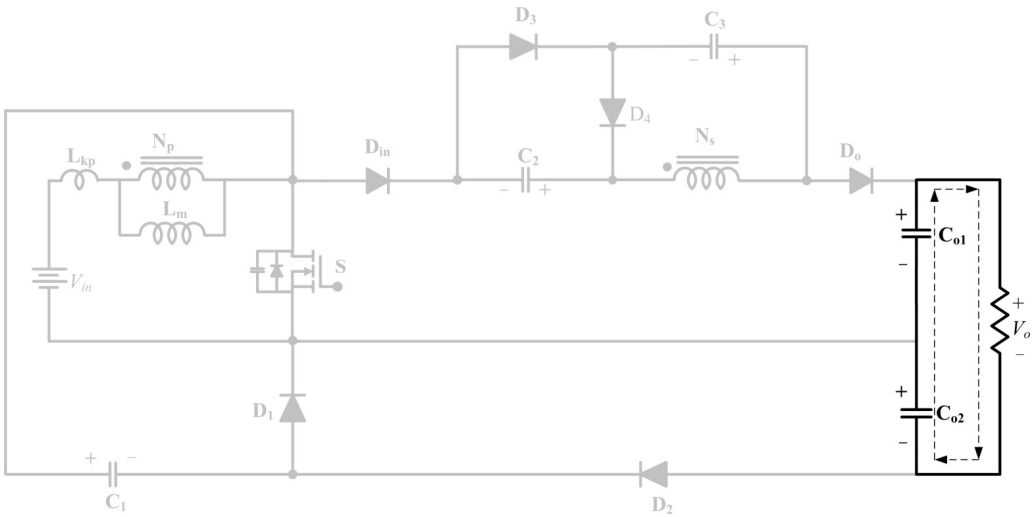


(**a**)



(**b**)

Figure 6. *Cont.*



(**c**)

Figure 6. Operating modes at DCM during a switching period. (**a**) Modes I; (**b**) Modes II; and (**c**) Modes III.

3. Steady-State Analysis of the Proposed Converter

3.1. CCM Operation

The turn ratio is defined as:

$$n = \frac{N_s}{N_p} \tag{1}$$

The coupling coefficient k of the coupled inductor is defined as:

$$k = \frac{L_m}{L_m + L_k} \tag{2}$$

Modes I, III, and IV, which have considerably short time durations, are ignored to simplify the steady state analysis; only modes II and V of the CCM operation are considered.

The voltage stresses of V_{Lk}, V_{L1}, and V_{L2} at mode II can be derived on the basis of Figure 3b.

$$V_{Lk}^{II} = \frac{L_{k1}}{L_m + L_{k1}} V_{in} = (1-k)V_{in} \tag{3}$$

$$V_{L1}^{II} = \frac{L_m}{L_m + L_{k1}} V_{in} = kV_{in} \tag{4}$$

$$V_{L2}^{II} = nV_{L1}^{II} = nkV_{in} \tag{5}$$

According to the volt–second balance principle and L_k, N_p, and N_s, the following equations are obtained:

$$\int_0^{DT_s} V_{Lk}^{II} \mathrm{d}t + \int_{DT_s}^{T_s} V_{Lk}^{V} \mathrm{d}t = 0 \tag{6}$$

$$\int_0^{DT_s} V_{L1}^{II} \mathrm{d}t + \int_{DT_s}^{T_s} V_{L1}^{V} \mathrm{d}t = 0 \tag{7}$$

$$\int_0^{DT_s} V_{L2}^{II} \mathrm{d}t + \int_{DT_s}^{T_s} V_{L2}^{V} \mathrm{d}t = 0 \tag{8}$$

By substituting (3)–(5) into (6)–(8), the voltage stresses of V_{Lk}, V_{L1}, V_{L2}, and V_o at mode V can be expressed as:

$$V_{Lk}^{V} = \frac{-D(1-k)}{(1-D)} V_{in} \tag{9}$$

$$V_{L1}^{V} = -\frac{Dk}{1-D} V_{in} \tag{10}$$

$$V_{L2}^{V} = -\frac{nDk}{1-D} V_{in} \tag{11}$$

$$V_o = 2V_{c1} + V_{c2} - V_{L2}^{V} \tag{12}$$

The capacitor C_2 is charged in mode II, and the capacitors C_1 and C_3 are charged in mode V. The voltage stress across capacitors C_1, C_2, and C_3 can be represented on the basis of Figures 3b and 4c.

$$V_{c3} = -V_{L2}^{V} = \frac{nDk}{1-D} V_{in} \tag{13}$$

$$V_{c2} = V_{L2}^{II} + V_{c3} \tag{14}$$

By substituting (5) and (13) into (14), the voltage stresses of the capacitors C_1 and C_2 are expressed as:

$$V_{c2} = \frac{nk}{1-D} V_{in} \tag{15}$$

$$\begin{aligned} V_{c1} &= V_{in} - V_{Lk}^{V} - V_{L1}^{V} \\ &= (1 + \frac{Dk}{(1-D)} + \frac{D(1-k)}{(1-D)}) V_{in} \end{aligned} \tag{16}$$

By substituting (11), (15), and (16) into (12), the voltage gain is developed as:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2 + nk + nDk}{1-D} \tag{17}$$

Assume k is equal to 1 and neglect the leakage inductor of the coupled inductor. At k = 1, the ideal voltage gain can be derived as:

$$M_{\mathrm{CCM}} = \frac{2 + n + nD}{1-D} \tag{18}$$

Table 1 and Figure 7 are shows the voltage gain of the proposed converter and those of previous converters during the CCM operation under coupling coefficient equal to 1. According to this Figure 7, the voltage gain of the proposed converter is higher than those of the previous converters with the same duty cycle. Proposed converter has achieved high step–up ratio and the efficiency of proposed converter is higher than those of the previous converter, except that the converters [9,29]. The converter [9] has high efficiency but voltage stress of the switch is high, the peak voltage of V_{ds} is appropriately 71V during the switch-off period and large coupled inductor size is ETD-59. The low efficiency in converter [29] under 150w and maximum output voltage is 200 V lesser than proposed converter.

Table 1. Comparison of the proposed converter compared with some of the previous converters. NA: Not showing efficiency in reference paper.

Converters	No. of Components	Efficiency	V_{in}/V_{out}	Voltage Gain ($M_{\mathrm{CCM}} = V_o/V_{in}$)
proposed converter	6 diodes, 5 capacitors	96.20%	V_{in} = 24 V, V_o = 400 V	$M_{\mathrm{CCM}} = \frac{2+n+nD}{1-D}$
[6]	3 diodes, 3 capacitors	NA	V_{in} = 48 V, V_o = 380 V	$M_{\mathrm{CCM}} = \frac{1+n}{1-D}$

Table 1. *Cont.*

Converters	No. of Components	Efficiency	V_{in}/V_{out}	Voltage Gain ($M_{CCM} = V_o/V_{in}$)
[8]	4 diodes, 4 capacitors	95.88%	V_{in} = 24 V, V_o = 400 V	$M_{CCM} = \frac{1+n+nD}{1-D}$
[9]	4 diodes, 4 capacitors	96.70%	V_{in} = 24 V, V_o = 400 V	$M_{CCM} = \frac{2+n}{1-D} + n$
[19]	5 diodes, 4 capacitors	95.70%	V_{in} = 24 V, V_o = 200 V	$M_{CCM} = n\frac{1+D}{1-D}$
[22]	5 diodes, 3 capacitors	96.20%	V_{in} = 24 V, V_o = 200 V	$M_{CCM} = \frac{n(2-D)}{1-D}$
[29]	5 diodes, 3 capacitors	96.50%	V_{in} = 27–37.5 V, V_o = 200 V	$M_{CCM} = \frac{2+n}{2(1-D)}$
[31]	3 diodes, 3 capacitors	95.20%	V_{in} = 27–36.5 V, V_o = 200 V	$M_{CCM} = (1+n) + \frac{1}{1-D} + \frac{D}{1-D}n$

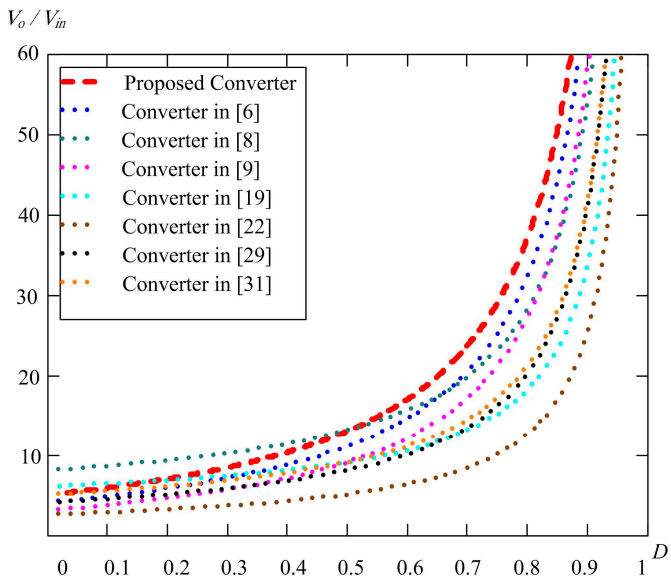


Figure 7. Duty ratio versus voltage gain of the proposed converter compared with previous converters, condition is CCM operation under $k = 1$ and $n = 3$.

3.2. DCM Operation

The DCM operation can be divided into three modes. Figure 5 shows the main component current and voltage waveforms. Figure 6 shows the proposed converter during different modes of the DCM operation. The mode I operation is shown in Figure 6a; the main power switch S is turned on. Therefore, the voltage stresses V_{L1} and V_{L2} can be expressed as:

$$V_{L1}^{I} = V_{in} \tag{19}$$

$$V_{L2}^{I} = nV_{in} \tag{20}$$

The magnetizing inductor peak current can be expressed as:

$$I_{Lmp} = \frac{V_{in}}{Lm} DT_s \tag{21}$$

Therefore, the voltage stresses of the capacitors C_2, C_{o1}, and C_{o2} can be expressed as:

$$V_{c2} = V_{L2}^{I} + V_{c3} \tag{22}$$

$$V_{co2} = V_{c1} \tag{23}$$

$$V_{co1} = V_o - V_{c1} \tag{24}$$

Figure 6b illustrates the mode II operation; the main power switch S is turned off. Therefore, the voltage stresses during mode II can be expressed as:

$$V_{L1}^{II} = V_{in-} V_{c1} \tag{25}$$

$$V_{L2}^{II} = 2V_{c1} + V_{c2} - V_o \tag{26}$$

$$V_{L2}^{II} = -V_{c3} \tag{27}$$

Figure 6c illustrates the mode III operation; the main power switch S is turned off. The capacitors C_{o1} and C_{o2} supply energy to the load, and the voltage stresses of V_{L1} and V_{L2} are expressed as:

$$V_{L1}^{III} = V_{L2}^{III} = 0 \tag{28}$$

By applying the volt–second balance principle to the coupled inductor, the following equations can be obtained:

$$\int_0^{DT_s} V_{L1}^{I} \mathrm{d}t + \int_{DT_s}^{(D+D_L)T_s} V_{L1}^{II} \mathrm{d}t + \int_{(D+D_L)T_s}^{T_s} V_{L1}^{III} \mathrm{d}t = 0 \tag{29}$$

$$\int_0^{DT_s} V_{L2}^{I} \mathrm{d}t + \int_{DT_s}^{(D+D_L)T_s} V_{L2}^{II} \mathrm{d}t + \int_{(D+D_L)T_s}^{T_s} V_{L2}^{III} \mathrm{d}t = 0 \tag{30}$$

By substituting (20), (27), and (28) into (30), the voltage across capacitor C_3 can be expressed as:

$$V_{c3} = \frac{nD}{D_L} V_{in} \tag{31}$$

Similarly, by substituting (19), (25), and (28) into (29) and (22), (27), and (28) into (30), the stress voltages of capacitors C_1 and C_2 can be expressed as:

$$V_{c1} = \frac{D + D_L}{D_L} V_{in} \tag{32}$$

$$V_{c2} = (n + \frac{nD}{D_L}) V_{in} \tag{33}$$

By substituting (20), (26), (28), (32), and (33) into (30), the voltage gain of the proposed converter during the DCM can be expressed as:

$$V_o = [\frac{2D}{D_L}(1+n) + (n+2)]\ V_{in} \tag{34}$$

$$D_L = \frac{2D(1+n)V_{in}}{V_o - (2+n)V_{in}} \tag{35}$$

On the basis of Figure 5, the average current value i_{co1}, can be expressed as:

$$i_{co1} = \frac{1}{2} D_L \frac{I_{Lmp}}{2+2n} - I_o \tag{36}$$

In the steady state, i_{co1} is equal to zero and (21), (35), and $i_{co1} = 0$ can be substituted into (36). Therefore, (37) can be obtained as:

$$\frac{D^2(n+1){V_{in}}^2 T_s}{[V_o - (n+2)V_{in}] \cdot (2n+2) \cdot Lm} = \frac{V_o}{R} \tag{37}$$

The time constant of the magnetizing inductance is defined as:

$$\tau_{Lm} \stackrel{\text{def}}{=} \frac{Lm}{RT_s} \tag{38}$$

By substituting (38) into (37), the voltage gain can be obtained as follows:

$$M_{\text{DCM}} = \frac{V_o}{V_{in}} = \frac{2n+2}{2} + \sqrt{\frac{(2n+2)^2}{4} + \frac{D^2(n+1)}{(2n+2)\cdot\tau_{Lm}}} \tag{39}$$

3.3. Boundary Operating Condition between the CCM and the DCM

While operating the proposed converter in boundary-condition mode the voltage gain is equal for CCM and DCM operations. Based on (18) and (39), the time constant τ_{LmB} of the boundary normalized magnetizing inductor can be expressed as:

$$\tau_{LmB} = \frac{\frac{D^2(n+1)}{2n+2}}{\left[\left(\frac{2+n+nD}{1-D}\right) - \frac{2n+2}{2}\right]^2 - \frac{(2n+2)^2}{4}} \tag{40}$$

Figure 8 shows the curve of τ. The proposed converter is operated in the CCM when τ is higher than i_{LmB}. Otherwise, the proposed converter is operated in the DCM.

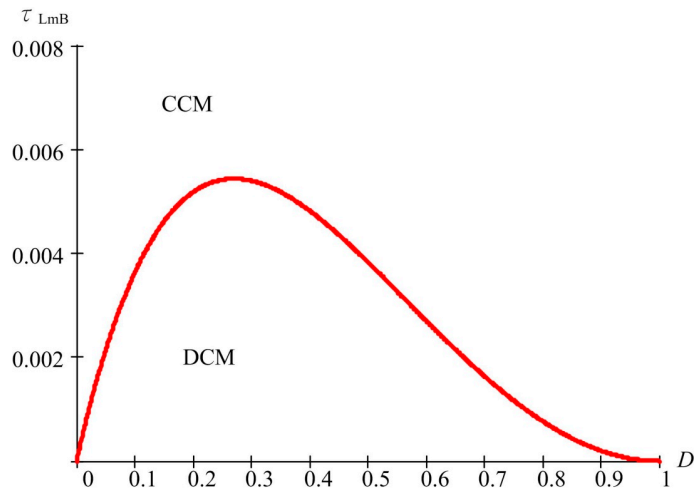


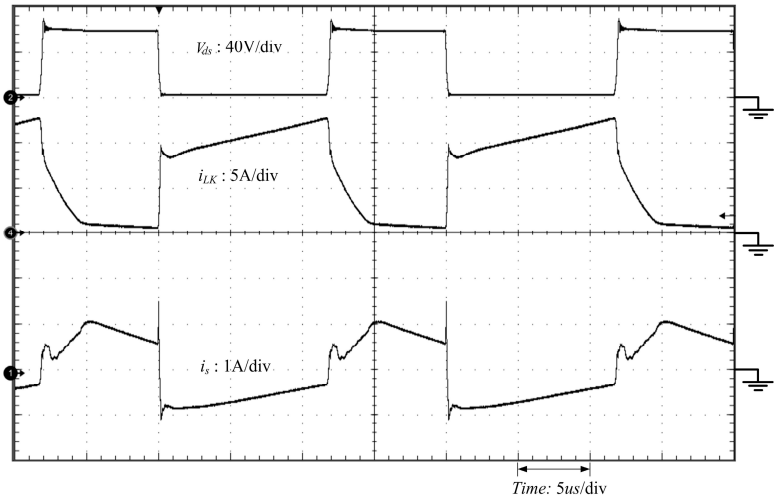
Figure 8. Duty ratio versus τ_{LmB} at boundary condition of the proposed converter under n = 3.

4. Design and Experiment of the Proposed Converter

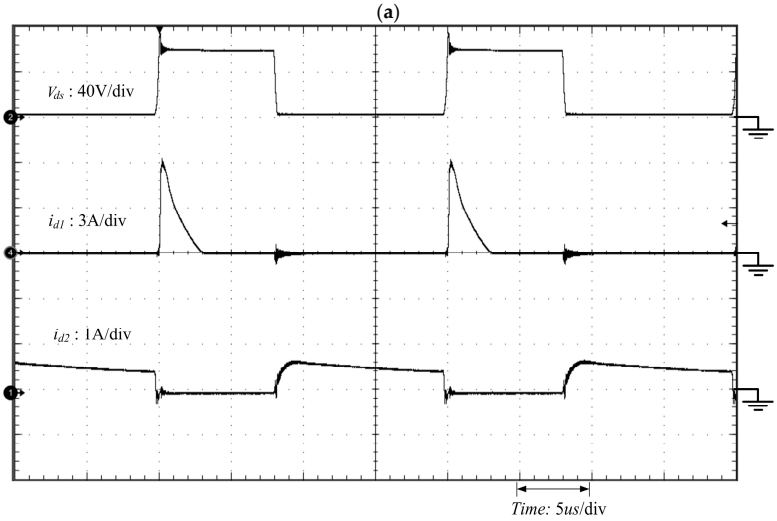
To test and measure the proposed converter performance, a prototype circuit of the proposed converter at 150 W was constructed in the laboratory. The main specifications are as follows:

Input DC voltage V_{in}: 24 V.
Output DC voltage V_o : 400 V.
Maximum output power: 150 W.
Switch frequency: 50 kHz.
Switch: IXTH130N10T.
Diodes: D_1–D_3, D_o: DSEI 30-10A; D_{in} and D_4: 25JPE40.
Capacitors: C_1 and C_{co2}: 100 μ/100 V, C_2: 100 μ/250 V, C_3: 100 μ/100 V, and C_{o1}: 220 μ/400 V aluminium capacitors.
Transformer: ETD-49 core PC-32, N_p:Ns = 1:3, L_m = 32 μH and L_k = 0.22 μH; k = 0.993.

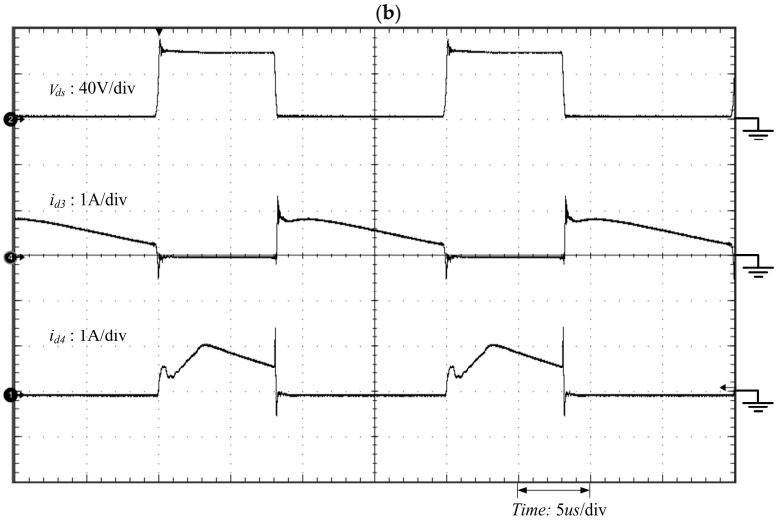
Figure 9a illustrates the secondary current i_s, primary-side leakage magnetizing current i_{Lk}, and drain to source voltage of the main power switch at full load P_o = 150 W and V_{in} = 24 V. The waveform of the secondary current i_s of the coupled inductor shows that the proposed circuit does not have zero current when the switch is turned on in the CCM. Figure 9b shows the waveforms of i_{d1} and i_{d2}.



(**a**)

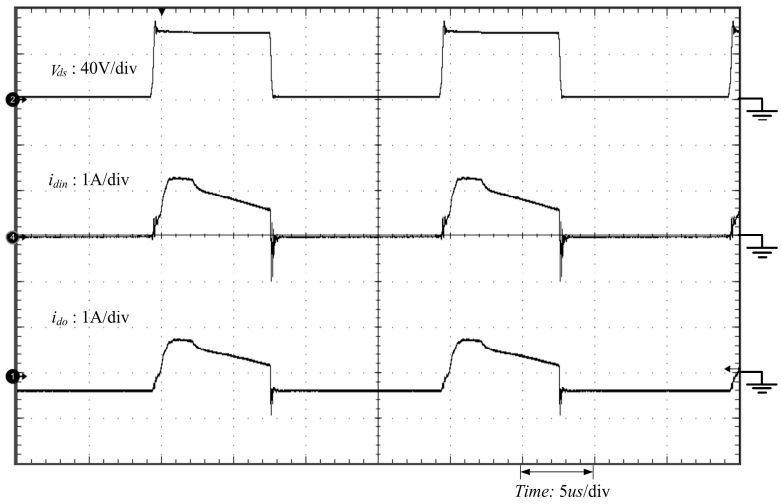


(**b**)



(**c**)

Figure 9. *Cont.*

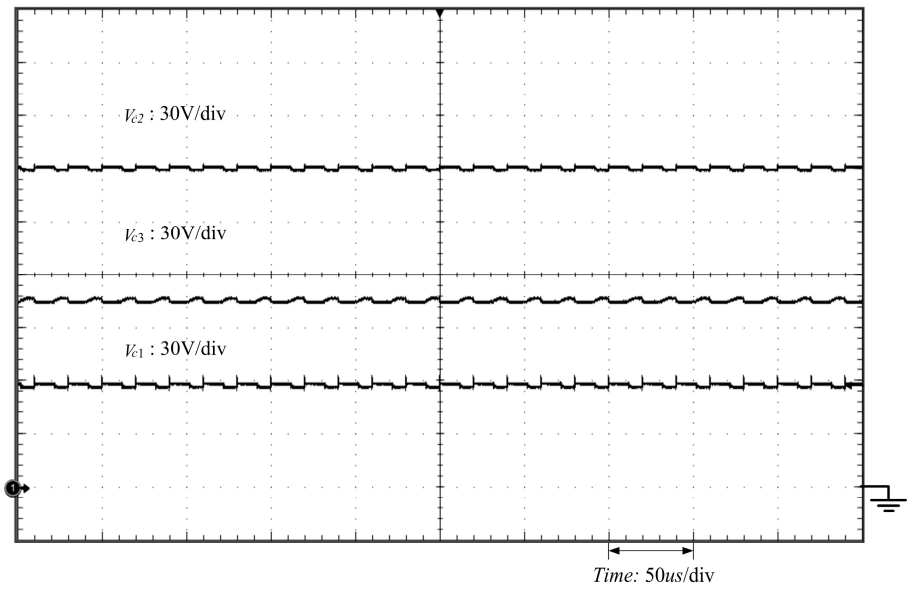


(**d**)

Figure 9. Experiment waveform under full-load P_o = 150 W. (**a**) Measured waveforms of V_{ds}, i_{Lk} and i_s; (**b**) Measured waveforms of V_{ds}, i_{d1} and i_{d2}; (**c**) Measured waveforms of V_{ds}, i_{d3} and i_{d4}; and (**d**) Measured waveforms of V_{ds}, i_{din} and i_{do}.

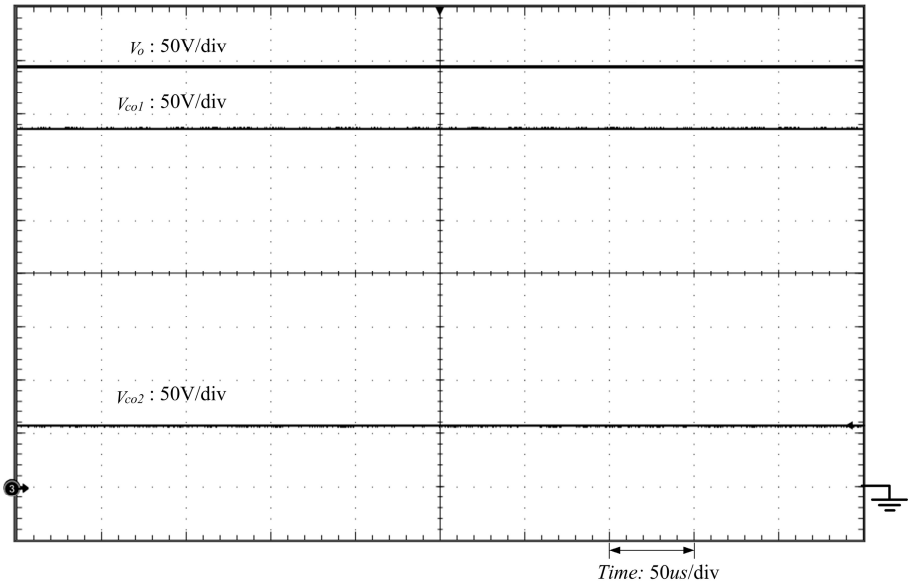
The current of the capacitor C_1 flows to D_2 and energy is transferred to the capacitor C_{o2} when the switch is turned on. The capacitor C_1 absorbs energy from V_{in} and parasitic capacitor on the switch when the switch is turned off. Figure 9c shows the waveforms of i_{d3} and i_{d4}; C_2 and C_3 are charged by the DC source V_{in} and secondary-side coupled inductor. Figure 9d shows the waveforms of i_{din} and i_{do}. The energy of V_{in} though C_{in} transfers to the step up circuit and current flow to D_o and is released to output capacitors.

Figure 10a shows that V_{c1}, V_{c2}, and V_{c3} satisfy (14), (15), and (17). Figure 10b shows the input and output voltages of capacitors C_{o1} and C_{o2}. Figure 11 illustrates the efficiency of the proposed converter at 20–150 W loads, and the maximum efficiency is 96.2% at 60 W.



(**a**)

Figure 10. *Cont.*



(**b**)

Figure 10. Experiment waveform under full-load P_o = 150 W. (**a**) Measured waveforms of v_1, v_2 and v_3; (**b**) Measured waveforms of V_{co1}, V_{co2} and V_o.

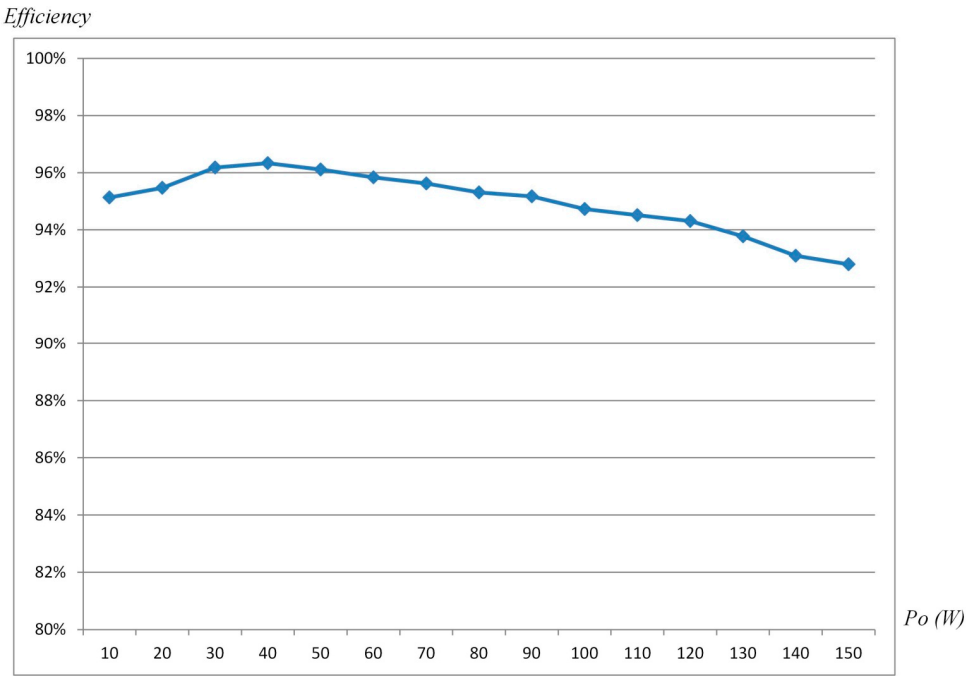


Figure 11. Efficiency of proposed converter.

5. Conclusions

This study successfully integrated the proposed converter by using the coupled inductor and high step-up circuit. High voltage gain was achieved using the coupled inductor when the capacitor charged and discharged energy. For this paper is integrated coupled inductor and switch capacitor to achieve a high step-up voltage gain without extreme duty cycle. In addition, energy was recovered from the leakage inductor of the coupled inductor by using a passive clamp circuit. The primary-leakage inductor recovered the energy function, and the switch clamp capacitor reduced the voltage spike of

the switch. Therefore, when low conducting resistance $R_{ds(on)}$ and low voltage stresses component were selected, the main power switch loss was reduced. Finally, a prototype circuit of the proposed converter with an input voltage of 24 V converted to an output voltage of 400 V and maximum power 150 W was constructed in the laboratory. The experimental results proved the high efficiency and voltage gain of the proposed converter. Moreover, it was proved that the main switch stress voltage is clamped by the capacitor C_1.

Acknowledgments: This work were supported in part by the National Synchrotron Radiation Research Center and Ministry of Science and Technology, China, through grant numbers MOST 105-2199-M-006-004 and MOST 104-2221-E-006-073-MY3.

Author Contributions: Yong-Seng Wong and Jiann-Fuh Chen conceived and designed the experiments; Yong-Seng Wong performed the experiments; Yong-Seng Wong, Yi-Ping Hsieh and Jiann-Fuh Chen analyzed the data; Kuo-Bin Liu contributed reagents/materials/analysis tools; Yong-Seng Wong wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Anders, L.; Peter, U.C.; Ben, M.; Glenn, A.M.; David, P.; Valentina, R.; Alexander, R. The multimillennial sea-level commitment of global warming. *Proc. IEEE Natl. Acad. Sci. USA* **2016**, *110*, 13745–13750.
2. Wei, C.L.; Shih, M.H. Design of a switched-capacitor DC-DC converter with a wide input voltage range. *IEEE Trans. Circuits Syst. I* **2013**, *60*, 1648–1656. [CrossRef]
3. Chang, C.H.; Chang, E.C.; Cheng, H.L. A high-efficiency solar array simulator implemented by an LLC resonant DC-DC converter. *IEEE Trans. Power Electron.* **2013**, *28*, 3039–3046. [CrossRef]
4. Shen, J.M.; Jou, H.L.; Wu, J.C. Novel transformerless grid-connected power converter with negative grounding for photovoltaic generation system. *IEEE Trans. Power Electron.* **2012**, *27*, 1819–1829. [CrossRef]
5. Zhang, L.; Sun, K.; Feng, L.L.; Wu, H.F.; Xing, Y. A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters. *IEEE Trans. Power Electron.* **2013**, *28*, 730–739. [CrossRef]
6. Baek, J.W.; Ryoo, M.H.; Kim, T.J.; Yoo, D.W.; Kim, J.S. High boost converter using voltage multiplier. In Proceedings of the 31st Annual Conference of IEEE Industrial Electronics Society (IECON 2005), Raleigh, NC, USA, 6–10 November 2005; pp. 567–572.
7. Wai, R.J.; Duan, R.Y. High-efficiency power conversion for low power fuel cell generation system. *IEEE Trans. Power Electron.* **2005**, *20*, 847–856. [CrossRef]
8. Hsieh, Y.P.; Chen, J.F.; Liang, T.J.; Yang, L.S. Novel high step-up DC-DC converter for distributed generation system. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1473–1482. [CrossRef]
9. Hsieh, Y.P.; Chen, J.F.; Liang, T.J.; Yang, L.S. Analysis and implementation of a novel single-switch high step-up DC-DC converter. *IET Power Electron.* **2012**, *5*, 11–21. [CrossRef]
10. Ajami, A.; Ardi, H.; Farakhor, A. A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *IEEE Trans. Power Electron.* **2015**, *30*, 4255–4263. [CrossRef]
11. Luo, F.L.; Ye, H. Positive output multiple-lift push-pull switched-capacitor Luo-converters. *IEEE Trans. Ind. Electron.* **2004**, *51*, 594–602. [CrossRef]
12. Abutbul, O.; Gherlitz, A.; Berkovih, Y.; Ioinovici, A. Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit. *IEEE Trans. Circuits Syst. I* **2003**, *50*, 1098–1102. [CrossRef]
13. Hsieh, Y.P.; Chen, J.F.; Liang, T.J.; Yang, L.S. Novel high step up DC-DC converter with coupled-inductor and switched-capacitor techniques. *IEEE Trans. Ind. Electron.* **2012**, *59*, 998–1007. [CrossRef]
14. Axelrod, B.; Berkovich, Y. Switched coupled-inductor cell for DC-DC converters with very large conversion ratio. *IET Power Electron.* **2011**, *4*, 309–315.
15. Duan, R.Y.; Lee, J.D. High-efficiency bidirectional DC-DC converter with coupled inductor. *IET Power Electron.* **2012**, *5*, 115–123. [CrossRef]
16. Changchien, S.K.; Liang, T.J.; Chen, J.F.; Yang, L.S. Step-up DC-DC converter by coupled inductor and voltage-lift technique. *IET Power Electron.* **2013**, *3*, 369–378. [CrossRef]
17. Hsieh, Y.P.; Chen, J.F.; Yang, L.S.; Wu, C.Y.; Liu, W.S. High-conversion-ratio bidirectional DC-DC converter with coupled inductor. *IEEE Trans. Ind. Electron.* **2014**, *61*, 210–222. [CrossRef]

18. Zhao, Q.; Lee, F.C. High-efficiency, high Step-up DC-DC converters. *IEEE Trans. Power Electron.* **2003**, *18*, 65–73. [CrossRef]
19. Lee, J.H.; Liang, T.L.; Chen, J.F. Isolated coupled-inductor-integrated DC-DC converter with nondissipative snubber for solar energy applications. *IEEE Trans. Ind. Electron.* **2014**, *61*, 3337–3348. [CrossRef]
20. Hsieh, Y.P.; Chen, J.F.; Liang, T.J.; Yang, L.S. Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques for a sustainable energy system. *IEEE Trans. Power Electron.* **2011**, *26*, 3481–3490. [CrossRef]
21. Siwakoti, Y.P.; Blaabjerg, F.; Loh, P.C. Ultra-step-up DC-DC converter with integrated autotransformer and coupled inductor. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 1872–1877.
22. Liang, T.J.; Lee, J.H.; Chen, S.M.; Chen, J.F.; Yang, L.S. Novel isolated high step-up DC-DC converter with voltage lift. *IEEE Trans. Power Electron.* **2013**, *60*, 1483–1491. [CrossRef]
23. Chen, Y.T.; Tsai, M.H.; Liang, R.H. DC-DC converter with high voltage gain and reduce switch stress. *IET Power Electron.* **2014**, *7*, 2564–2571. [CrossRef]
24. Lin, B.R.; Dong, J.Y. Analysis and implementation of an active clamping zero-voltage turn-on switching/zero-current turn-off switching converter. *IET Power Electron.* **2010**, *3*, 429–437. [CrossRef]
25. Zhao, Q.; Tao, F.; Hu, Y.; Lee, F.C. Active-clamp DC/DC converters using magnetic switches. In Proceedings of the Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2001), Anaheim, CA, USA, 4–8 March 2002; pp. 946–952.
26. Tseng, K.C.; Liang, T.J. Analysis of integrated boost-flyback step-up converter. *IEEE Proc. Inst. Elect. Eng. Electric. Power Appl.* **2005**, *151*, 217–225.
27. Wai, R.J.; Duan, R.Y.; Jheng, K.H. High-efficiency bidirectional DC-DC converter with high-voltage gain. *IET Power Electron.* **2012**, *5*, 173–184. [CrossRef]
28. Kuo, P.H.; Liang, T.J.; Tseng, K.C.; Chen, J.F.; Chen, S.M. An isolated high step-up forward/flyback active-clamp converter with output voltage lift. In Proceedings of the 2010 IEEE Energy Conversion Congress and Exposition (ECCE), Atlanta, GA, USA, 12–16 September 2010; pp. 542–548.
29. Wai, R.J.; Liu, L.W.; Duan, R.Y. High-efficiency voltage-clamped DC-DC converter with reduced reverse-recovery current and switch-Voltage stress. *IEEE Trans. Ind. Electron.* **2006**, *53*, 272–280.
30. Wu, T.F.; Lai, Y.S.; Hung, J.C.; Chen, Y.M. Boost converter with coupled inductors and buck-boost type of active clamp. *IEEE Trans. Ind. Electron.* **2008**, *55*, 154–162. [CrossRef]
31. Wai, R.J.; Lin, C.Y.; Duan, R.Y.; Chang, Y.R. High-efficiency DC-DC converter with high voltage gain and reduced switch stress. *IEEE Trans. Ind. Electron.* **2007**, *54*, 354–364. [CrossRef]
32. Muhammad, M.; Armstrong, M.; Elgendy, M.A. A nonisolated interleaved boost converter for high-voltage gain applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 352–362. [CrossRef]
33. Muhammad, M.; Armstrong, M.; Elgendy, M. Non-isolated DC-DC converter for high-step-up ratio applications. In Proceedings of the 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, Switzerland, 8–10 September 2015; pp. 1–10.
34. Muhammad, M.; Armstrong, M.; Elgendy, M.A. Non-isolated, high gain, boost converter for power electronic applications. In Proceedings of the 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, UK, 19–21 April 2016.