energies

MDPI

Article

An Efficient Phase-Locked Loop for Distorted Three-Phase Systems

Yijia Cao [1], Jiaqi Yu [1], Yong Xu [1], Yong Li [1,*] and Jingrong Yu [2]

[1] College of Electrical and Information Engineering, Hunan University, Changsha 410082, China; yijiacao@hnu.edu.cn (Y.C.); yujq629@hnu.edu.cn (J.Y.); xuyong@hnu.edu.cn (Y.X.)

[2] School of Information Science and Engineering, Central South University, Changsha 410083, China; Jingrong@csu.edu.cn

* Correspondence: yongli@hnu.edu.cn

Academic Editor: José Gabriel Oliveira Pinto

Received: 6 December 2016; Accepted: 20 February 2017; Published: 27 February 2017

Abstract: This paper proposed an efficient phase-locked loop (PLL) that features zero steady-state error of phase and frequency under voltage sag, phase jump, harmonics, DC offsets and step-and ramp-changed frequency. The PLL includes the sliding Goertzel discrete Fourier transform (SGDFT) filter-based fundamental positive sequence component separator (FPSCS), the synchronous-reference-frame PLL (SRF-PLL) and the secondary control path (SCP). In order to obtain an accurate fundamental positive sequence component, SGDFT filter is introduced as it features better filtering ability at the frequencies that are integer times of fundamental frequency. Meanwhile, the second order Lagrange-interpolation method is employed to approximate the actual sampling number including both integer and fractional parts as grid frequency may deviate from the rated value. Moreover, an improved SCP with single-step comparison filtering algorithm is employed as it updates reference angular frequency according to the FPSC, which promises a zero steady-state error of phase and improves the frequency tracking speed. In this paper, the mathematical model of the proposed PLL is constructed, its stability is analyzed. Also, design procedure of the control parameters is presented. The effectiveness of the proposed PLL is confirmed by experimental results and comparison with advanced pre-filtering PLLs.

Keywords: distorted grid conditions; SGDFT; Lagrange-interpolation method; frequency adaption; SCP

1. Introduction

The information about instantaneous grid voltage phase and frequency are usually obtained via phase lock loop (PLL), which is of vital importance to maintain synchronization and stable operation for grid-connected power electronic devices [1–5]. Recently, the presence of DC offsets and harmonics in grid voltages caused by measurement devices, nonlinear loads and grid faults throws down a new challenge to the synchronization technique [6].

Synchronous-reference-frame PLL (SRF-PLL) is probably the most popular synchronization technique under ideal grid condition [7,8]. However, the disturbance rejection capability of SRF-PLL is poor for unbalanced voltages, harmonics, step-and ramp-changed frequency and DC offsets. Under unbalanced condition, the fundamental negative sequence component imposes the second harmonic ripple on variables in dq axis. Under polluted condition, the nth order harmonic components of input voltages become $(n-1)$th harmonics (if it is a positive sequence harmonic) or $(n+1)$th harmonics (if it is a negative sequence harmonic) in dq axis [9]. Especially, DC offsets become fundamental component in dq axis. Under step-and ramp-changed frequency, there is an error between

the reference angular frequency and the actual one. As a result, the SRF-PLL cannot track phase and frequency precisely.

To solve this problem, numerous advanced PLLs have been intensively studied [10–27]. The improved methods generally fall into two classes. One representative method is the in-loop filtering technique which adds various specific filters in the phase control loop, such as adaptive notch filter-based PLL [10], moving average filter-based PLL (MAF-PLL) [11], Type-1 PLL [12], *dq*-frame delayed signal cancellation operator based-PLL [13] and the variable sampling period filter based PLL (VSPF-PLL) [14]. These PLLs show satisfactory performances but they are not applicable to the situation where precise fundamental positive sequence component (FPSC) is needed.

The other method is the pre-filtering technique which employs various filters to extract FPSC from the non-ideal voltages [15–27]. References [15,16] present a multiple complex-coefficient filter-based (MCCF) synchronization technique with no need of the symmetrical component method and rotating frame transformations. Reference [17] proposes a generalized second-order and third-order complex-vector filter based on reference [15] for better dynamic performance and higher harmonic attenuation, but DC offsets of input signal are not considered. Moreover, as CCF gives relatively limited gains for each order harmonics especially for DC offsets, it cannot maintain tracking precision of grid phase under harmonics and DC offsets. As a representative pre-filtering SRF-PLL, second-order generalized integrator-based (SOGI) PLL is presented in [16] and improved in references [19,20]. Dual SOGI in [18] is the building block of the quadrature signal generator (QSG) and offers harmonic blocking capability to the system. References [19,20] make SOGI-PLL frequency adaptive by adding a harmonic decoupling network and an angular frequency feed forward loop, respectively. Consequently, the SOGI-based PLLs exhibit a relatively precise and frequency-adaptive response under unbalanced condition, but they also cannot track the phase precisely under harmonics and DC offsets due to similar filtering characteristics with CCF based PLL. The moving average filter-based (MAF) pre-filtering PLL has precise accuracy under unbalanced and heavily polluted conditions when the filtering window width is integer times of the input AC signal's period [21]. The filtering window width in [22,23] is set to one time of the input AC signal's period in *dq* axis, which can eliminate DC offsets of input signal. But this will give one period delay and increase the response time. References [24] proposes a generalized delay signal cancelation-based (GDSC) pre-filtering PLL, which can eliminate the negative-sequence component and any given harmonics under unbalanced voltages, harmonics and DC offsets. References [25–27] focus on the frequency-adaptive scheme of GDSC-PLL. They all track frequency precisely and give an acceptable response time when input frequency varies. However, it bears burdensome digital computation time, as it needs 4 to 5 cascaded DSC modules to suppress all-field harmonics. Furthermore, the aforementioned pre-filtering PLLs give steady-state error on estimated phase when input signal's frequency varies due to the fixed reference angular frequency. Thus, some improved PLLs adopt a secondary control path (SCP) for better tracking accuracy [28,29]. But the reference angular frequency is calculated directly from the input signals without pre-filter, which would make the reference angular frequency inaccuracy and consequently mislead the detected frequency under variable frequency.

With the aim of further improvement in tracking accuracy and disturbance rejection capability under unbalanced voltages, harmonics, step-and ramp-changed frequency and DC offsets, an improved PLL based on sliding Goertzel discrete Fourier transform (SGDFT) pre-filter is proposed. The FPSC is extracted by SGDFT pre-filter as it features unit gain on specified frequency and negative infinite gain on other frequencies; Second order Lagrange-interpolation method is used to approximate the actual sample number as grid frequency may deviate from the normal value; In order to obtain an accurate reference angular frequency, the extracted FPSC is adopted as the input of SCP rather than the one without being pre-filtered. Meanwhile, single-step comparison filtering algorithm is proposed according to the SCP characteristics, which gives lower delay and higher accuracy on the calculation of reference angular frequency than traditional low pass filter (LPF). By means of these

schemes, zero steady-state error and rapid transient response in phase and frequency are guaranteed under distorted conditions.

The rest of this paper is organized as follows: Section 2 analyzes the SGDFT filter characteristics. Section 3 proposes the new PLL structure and its mathematical model. Section 4 describes the design and implementation method. The comparative experimental results of five PLLs obtained from the prototype comprised of signal generator and digital signal processor (DSP) TMS320F28335 control board are given in Section 5. Finally, the conclusions are drawn in Section 6.

2. SGDFT Overview

The quadrature signal generator (QSG) is widely used in pre-filtering PLL. However, it has limited performance under polluted condition, since the separated FPSCs still contain harmonics. The SGDFT filter is derived from the standard DFT equation and commonly used to compute DFT spectra [30]. Compared with QSG, it has better filtering ability at the frequencies that are integer times of fundamental frequency. The transfer function $H_{\mathrm{SGDFT}}(z)$ and the structure of SGDFT filter are shown in Equation (1) and Figure 1, respectively.

$$H_{\mathrm{SGDFT}}(z) = \frac{(1 - \mathrm{e}^{-j2k\pi/N} z^{-1})(1 - z^{-N})}{1 - 2\cos(2k\pi/N) z^{-1} + z^{-2}} \tag{1}$$

where k is frequency domain index and N is the sampling number.

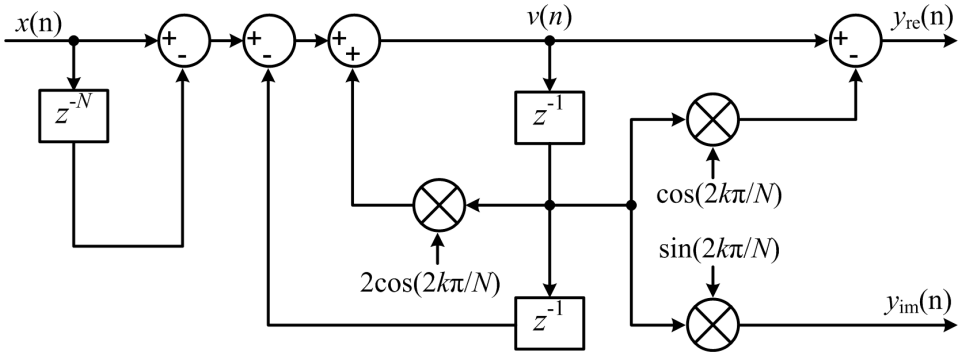

Figure 1. Block diagram description of SGDFT.

Figure 2 shows the frequency response and z-domain zero/pole of SGDFT. As shown in Figure 2a, $H_{\mathrm{re}}(z)$ and $H_{\mathrm{im}}(z)$ are the real and imaginary part of $H_{\mathrm{SGDFT}}(z)$, while $G_{\mathrm{d}}(s)$ and $G_{\mathrm{q}}(s)$ represent the transfer function of QSG in d and q axis, respectively. The magnitude of the four transfer functions are all 0 dB at the fundamental frequency f_0 = 50 Hz. It is shown that the frequency response of SGDFT is same with QSG except at the frequencies that are integer times of f_0. Meanwhile, SGDFT has much smaller gain than QSG at the integer multiple of f_0, which means that SGDFT has better filtering ability than QSG under polluted condition. In Figure 2b, there are 256 zeros (blue circle) of the transfer function equally spaced around the unit circle on z-domain. Moreover, it has two conjugate poles (red cross) cancelling zeros at $z = \mathrm{e}^{\pm j2\pi/256}$. Thus, one can conclude that SGDFT can calculate the fundamental coefficient of the input signal precisely. Therefore, SGDFT is introduced to separate the FPSC.

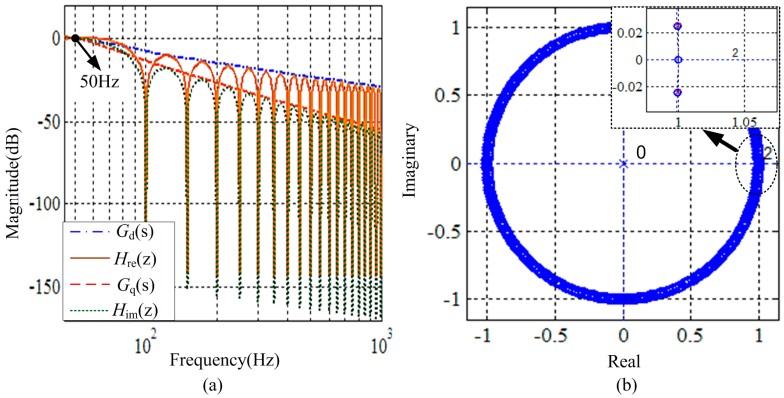

Figure 2. Frequency response and z-domain zero/pole of SGDFT when k = 1, N = 256. (**a**) Real and imaginary frequency response of SGDFT; (**b**) z-domain zero/pole.

3. The Proposed PLL

The block diagram of the proposed PLL is shown in Figure 3. This PLL structure consists of three main parts: FPSCS, SRF-PLL and SCP. The FPSCS module uses SGDFT filter and the symmetrical component method to separate the FPSC precisely even under distorted conditions. Considering that the practical grid frequency may deviate from the rated value, Lagrange-interpolation method is adopted to approximate the actual sampling number N_r, in order to make the SGDFT filter effective under variable frequency. The SCP module updates reference angular frequency, which improves its tracking performance.

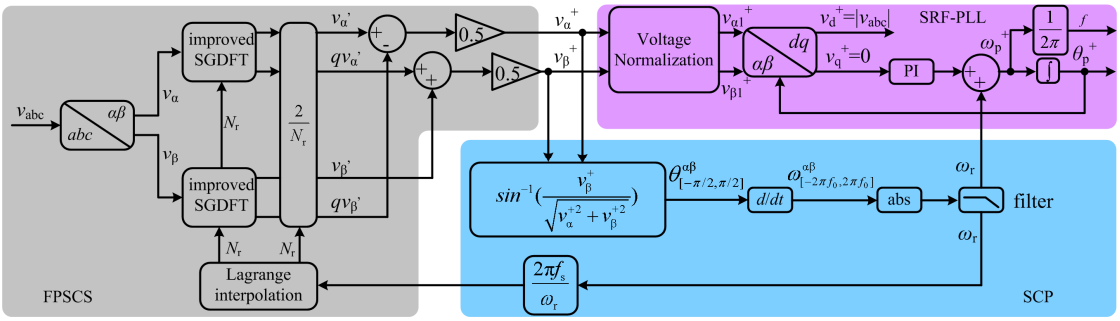

Figure 3. Block diagram of the proposed PLL.

3.1. SGDFT-Based FPSCS

The SGDFT structure is shown in Figure 1. v_α and v_β are input signals in two-phase stationary frame. v'_α and qv'_α are the filtered direct and quadrature parameters of v_α. v'_β and qv'_β are the filtered direct and quadrature parameters of v_β. v^+_α and v^+_β are FPSC in two-phase stationary frame, $v^+_{\alpha1}$ and $v^+_{\beta1}$ are normalized FPSC. The FPSC v^+_α and v^+_β in αβ axis are obtained by:

$$\begin{bmatrix} v^+_\alpha \\ v^+_\beta \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v'_\alpha - qv'_\beta \\ qv'_\alpha + v'_\beta \end{bmatrix} \tag{2}$$

In practical power system, the grid frequency f_0 is a time-varying parameter. The problem arises when f_0 cannot be divisible by the sampling frequency f_s, i.e., the order N_r would not be a integer and can be described as $N_r = N_a + D$, where N_a = floor (N_r) is the integer and $D = N_r - N_a$ ($0 \le D < 1$) is the fractional part. Thus, the delay is given as: $z^{-Nr} = z^{-Na}z^{-D}$. The Lagrange-interpolation method is introduced because it is an effective way to approximate the fractional delay for FIR filter design [31]. The fraction delay z^{-D} can be approximated by:

$$z^{-D} \approx \sum_{k=0}^{n} \mathrm{H}(k) z^{-k} \qquad k = 0, 1, \cdots, n \tag{3}$$

The coefficients H(k) are calculated as:

$$\mathrm{H}(k) = \prod_{\substack{i=0 \\ i \neq k}}^{n} \frac{D-i}{k-i} \qquad k = 0, 1, \cdots, n \tag{4}$$

Specifically, the case n = 1 corresponds to the linear interpolation and the two coefficients are H(0) = 1 − D and H(1) = D. Figure 4 shows the frequency responses of Lagrange-interpolating fraction delay z^{-D} at different D values.

In Figure 4, the fractional D are 0.3 (red line), 0.5 (green line) and 0.75 (blue line) for validation. It shows that the magnitude of fraction delay with n = 2 (dashed line) is closer to the case with D = 0 (the real value), meanwhile the phase has smaller change at different D values than n = 1 (solid line). The magnitude of fraction delay with the order n = 3 is close to the case with D = 0 while it exceeds the unit amplitude, which may introduce stability problem. Moreover, the fraction delay with the order n = 3 consumes more addition and multiplication operations than n = 2. Considering these two aspects, n = 2 is chosen to be the Lagrange interpolation order. Hence, the corresponding fractional delay is:

$$z^{-N_r} = \mathrm{H}(0) z^{-N_a} + \mathrm{H}(1) z^{-N_a - 1} + \mathrm{H}(2) z^{-N_a - 2} \tag{5}$$

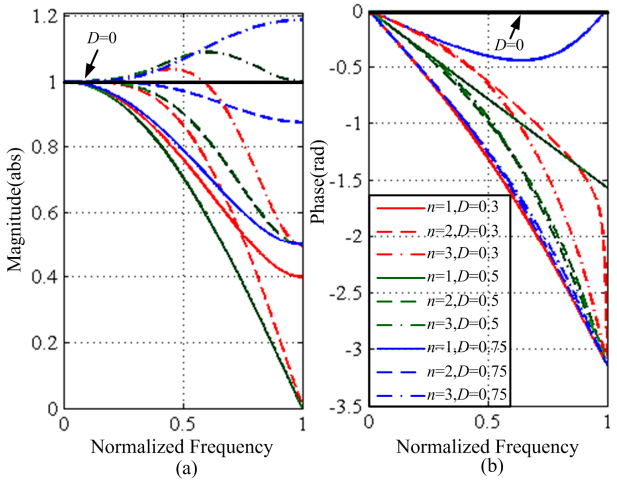

Figure 4. Frequency responses of Lagrange-interpolating fraction delay. (**a**) Magnitude responses; (**b**) Phase responses.

Therefore, the structure of SGDFT can be improved, as shown in Figure 5.

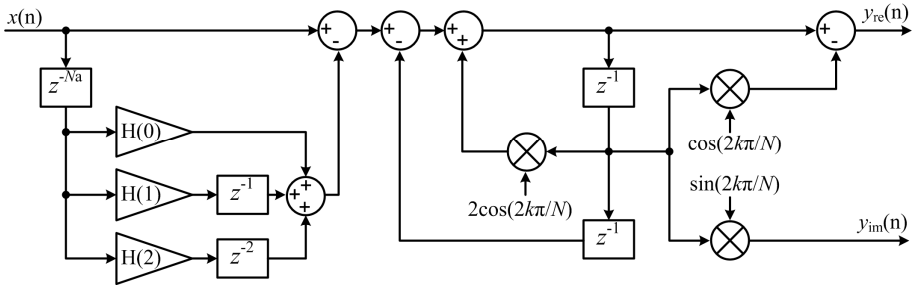

Figure 5. The improved structure of SGDFT.

3.2. Description of SCP

The secondary control path is introduced to improve the transient response rate. Moreover, it updates the reference angular frequency to decrease phase error under variable frequency.

In reference [28], the phase $\theta \in [-\pi/2, \pi/2]$ can be deduced as $\theta = \tan^{-1}(v_\beta^+/v_\alpha^+)$. However, *arctangent* function gives rapid change at $\pm n\pi/2$, which results in differential errors in digital implementation. Therefore, this paper uses *arcsin* function to calculate the phase. Besides, an *abs* function is adopted to regulate the negative angular frequency. In order to eliminate the digital differential error in the regulated angular frequency, the single-step comparison filter is realized as follows:

$$\omega_r(k_n) = \{\omega(k_n) \geq \omega(k_n - 1)\}?\{\omega_r(k_n) = \omega(k_n)\}:\{\omega_r(k_n) = \omega(k_n - 1)\} \tag{6}$$

where k_n is the current cycle counter. Both the differential part $\mathrm{d}/\mathrm{d}t$ and Equation (6) need one control period delay, thus its transfer function can be described as $G_f(s) = 1/(2T_s s + 1)$. As analyzed in Section 2, the model of SGDFT is equivalent to QSG. Thus, the pre-filtering stage small signal model in the proposed PLL can be used as $G_o(s) = \omega_o/(s + \omega_o)$, where ω_o equals to $0.707\omega_r$. Therefore, the secondary control path transfer function is $\omega_r(s) = G_o(s) \times G_f(s) \times \omega(s)$.

Moreover, the introduction of SCP changes the type and pole-zero location of tracking loop [29]. Thus, the voltage normalization part is employed to remove this adverse effect. It can be achieved as:

$$\begin{cases} v_{\alpha 1}^+ = \dfrac{v_\alpha^+}{\sqrt{v_\alpha^{+2}+v_\beta^{+2}}} \\ v_{\beta 1}^+ = \dfrac{v_\beta^+}{\sqrt{v_\alpha^{+2}+v_\beta^{+2}}} \end{cases} \text{ or } \begin{cases} v_{\alpha 1}^+ = \dfrac{v_\alpha^+}{0.5(\sqrt{v_\alpha'^2+qv_\alpha'^2}+\sqrt{v_\beta'^2+qv_\beta'^2})} \\ v_{\beta 1}^+ = \dfrac{v_\beta^+}{0.5(\sqrt{v_\alpha'^2+qv_\alpha'^2}+\sqrt{v_\beta'^2+qv_\beta'^2})} \end{cases} \tag{7}$$

3.3. Proposed PLL Model

According to the aforementioned deduction, the small-signal model and equivalent model of the proposed PLL are shown in Figure 6.

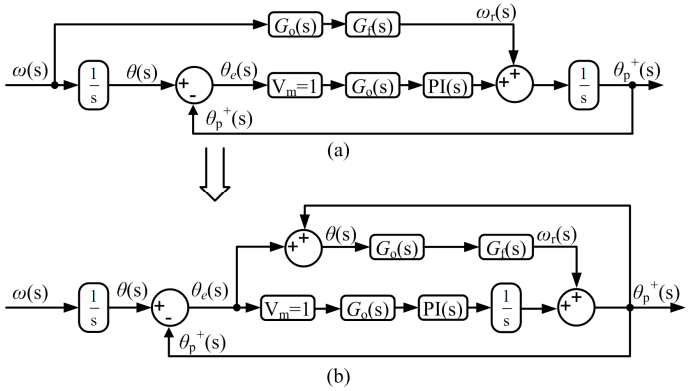

Figure 6. Small-signal model of the proposed PLL. (**a**) Original model; (**b**) Equivalent model.

It can be deduced from Figure 6b as:

$$\theta_p^+(s) = \underbrace{V_m G_o(s) G_{PI}(s) \frac{1}{s}}_{G_a(s)} \theta_e(s) + G_o(s) G_f(s) \left\{ \theta_e(s) + \theta_p^+(s) \right\} \tag{8}$$

Then the open-loop transfer function can be obtained as:

$$G_{ol}(s) = \frac{\theta_p^+(s)}{\theta_e(s)} = \frac{G_o(s) G_f(s) + G_a(s)}{1 - G_o(s) G_f(s)} \tag{9}$$

The term $G_o(s) \times G_f(s)$ can be replaced by $G_e(s) = 1/(T_e s + 1)$ because these two terms are small inertial elements, where T_e is the equivalent delay that equals to $2T_s + 1/\omega_o$. Therefore, the complete open-loop and closed-loop transfer functions are:

$$G_{ol}(s) = \frac{\theta_p^+(s)}{\theta_e(s)} = \frac{s^3 + s^2\omega_o(1 + k_p T_e) + s\omega_o(k_p + k_i T_e) + \omega_o k_i}{T_e s^3(s + \omega_o)} \tag{10}$$

$$G_{cl}(s) = \frac{\theta_p^+(s)}{\theta(s)} = \frac{s^3 + s^2\omega_o(1 + k_p T_e) + s\omega_o(k_p + k_i T_e) + \omega_o k_i}{s^4 T_e + s^3(1 + \omega_o T_e) + s^2\omega_o(1 + k_p T_e) + s\omega_o(k_p + k_i T_e) + \omega_o k_i} \tag{11}$$

4. Systematic Design Approach

The aim of this section consists of four aspects: parameter design guidelines for the proposed PLL, system stability analysis, study of bandwidth and dynamic responses, and discrete implementation method.

4.1. Parameters Design

It can be seen from Equation (10) that the open-loop transfer function is a four-order expression. Thus, zero-pole cancellation which is convenient for parameters design is adopted to simplify the system. Suppose that numerator polynomial has three real zeros, and one of them equals to ω_o. Thus, the open-loop transfer function would be:

$$G_{ol}(s) = \frac{(s + \omega_{z1})(s + \omega_{z2})(s + \omega_o)}{T_e s^3(s + \omega_o)} \tag{12}$$

It has been proved that the coincident zeros (i.e., $\omega_{z1} = \omega_{z2}$) can provide a higher stability margin than the spread ones [32]. Thus, combining Equations (10), (12) and $\omega_{z1} = \omega_{z2} = \omega_z$, Equation (10) can be rewritten as:

$$G_{ol}(s) = \frac{(s + \omega_z)^2}{T_e s^3} = \frac{s^2 + \omega_o k_p T_e s + k_i}{T_e s^3} \tag{13}$$

where k_p and k_i are the proportional and integral parameters of PI regulator shown in Figure 6. From Equation (13), the phase margin (PM) and the crossover frequency ω_c of the proposed PLL can be determined as:

$$\begin{aligned} PM &= -90^\circ + 2\tan^{-1}(h) \\ \omega_c &= \frac{1}{T_e \sin^2(\tan^{-1}(h))} \end{aligned} \tag{14}$$

where $\omega_c = h\omega_z$. Figure 7 illustrates that PM is a function of h.

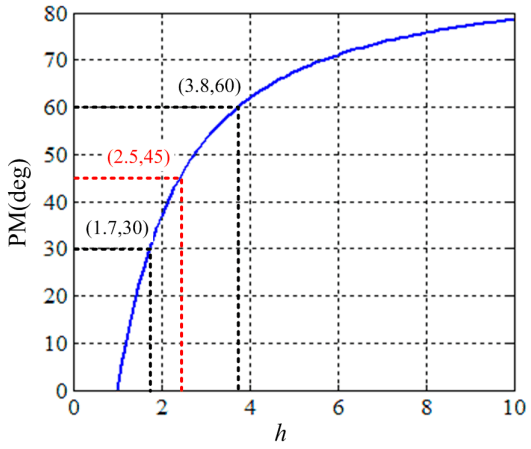

Figure 7. PM is a function of h.

The PM within the range of 30°~60° is the recommended range for stable operation [32]. Generally, PM = 45° is selected, which corresponds to h = 2.5, as shown in Figure 7. When h = 2.5, it can be derived that ω_c = 246.8 rad/s, ω_z = 98.7 rad/s, $k_p = 2\omega_z/(\omega_o \times T_e)$ = 189.2 and $k_i = \omega_z^2$ = 9746 according to Equations (13) and (14).

4.2. System Stability

It is known that the introduction of SCP aggravates the stability problem as the voltage amplitude V_m changes the zeros of the open-loop and closed-loop transfer function. Thus, the voltage normalization is utilized to remove this effect. From Equations (10) and (11), it can be seen that V_m is no longer an influence factor. According to the analysis in Section 4.1, the open-loop bode plots are shown in Figure 8.

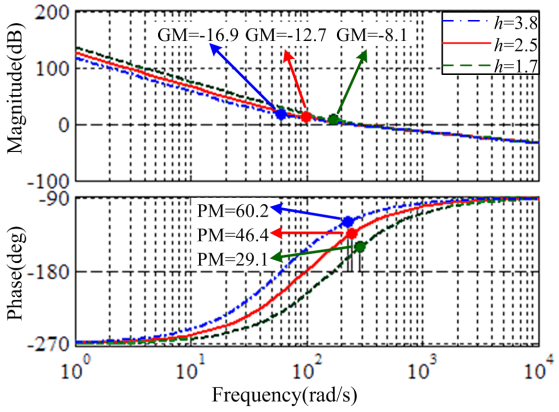

Figure 8. Open-loop bode plots of the proposed PLL.

It can be observed that the gain margin (GM) is between 8.1 and 16.9 dB within the PM range of 29.1°~60.2°, which are coincide with the aforementioned calculation. Therefore, one can conclude that the design guideline for the proposed PLL gives satisfactory PM and GM.

4.3. Bandwidth and Dynamic Response Evaluation

In order to analyze the bandwidth of the proposed PLL, the closed-loop bode plots of SRF-PLL, DSOGI-PLL and the proposed PLL are drawn. From Figure 9, it can be seen that the proposed PLL obtains wider bandwidth than the other two PLLs.

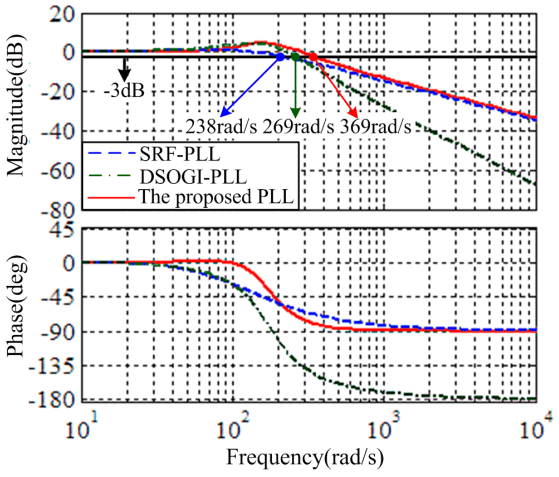

Figure 9. Closed-loop Bode plots of three kinds of PLL for h = 2.5.

The dynamic responses of the proposed PLL are evaluated by the unit step and ramp response. The corresponding transient responses are shown in Figure 10. It can be seen that the settling time are about 2 fundamental periods in these two conditions. Also, the steady-state value of unit step response equals to 1, and ramp response tracks the input ramp function $1/s^2$ precisely. These results validate that the proposed PLL obtains good dynamic performance.

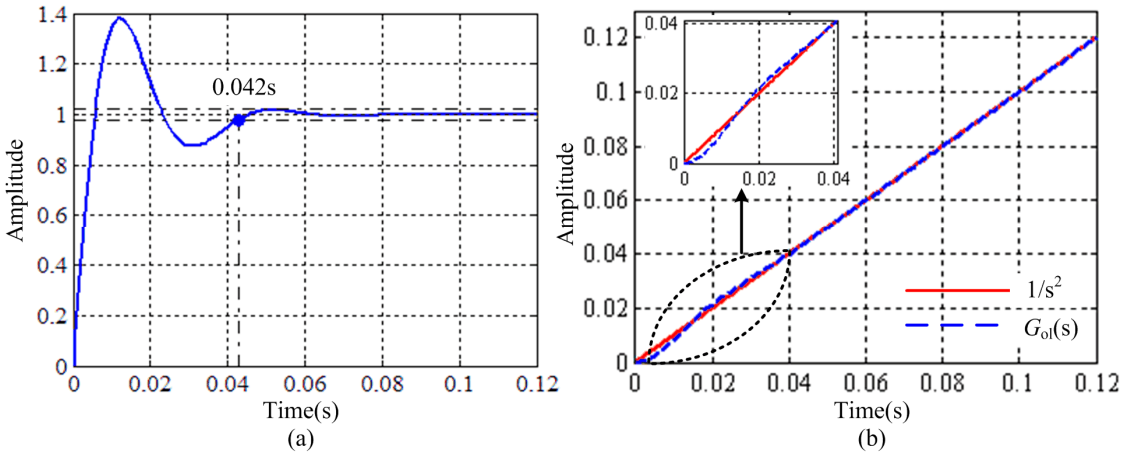

Figure 10. Transient response of closed-loop transfer function for $h = 2.5$. (**a**) The unit step response; (**b**) The unit impulse response.

4.4. Discrete Implementation of the Proposed PLL

Performance of the proposed PLL highly depends on digital discretization approach. The Tustin with pre-warping method ($s = \frac{\omega_1}{\tan(0.5\omega_1 T_s)}\frac{z-1}{z+1}$) gives better accuracy and frequency characteristics than the forward Euler and the backward Euler methods [33]. It is worth noting that SRF-PLL is regulated in q-axis. Therefore, $\omega_1 = 0$ and Tustin with pre-warping method has the same effect as Tustin (trapezoidal) method ($s = \frac{2}{T_s}\frac{z-1}{z+1}$). The discretization implementations of the proposed PLL are shown in Table 1. It is worth noting that n means the current period and y means α or β.

Table 1. The digital implementation.

	Discretization Expression	Difference Equation Implementations
SGDFT	$N_r(z) = \frac{2\pi f_s}{\omega_r(z)z^{-1}}$ $y(z) = \frac{(1-\cos(2k\pi/N_r)z^{-1})(1-z^{-N_r})}{1-2\cos(2k\pi/N_r)z^{-1}+z^{-2}}x(z)$ $qy(z) = \frac{\sin(2k\pi/N_r)z^{-1}(1-z^{-N_r})}{1-2\cos(2k\pi/N_r)z^{-1}+z^{-2}}x(z)$	$N_r(n) = \frac{2\pi f_s}{\omega_r(n-1)}$ $v(n) = 2\cos(2k\pi/N_r)v(n-1) - v(n-2) + x(n) - x(n-N_r)$ $y(n) = v(n) - \cos(2k\pi/N_r)v(n-1)$ $qy(n) = \sin(2k\pi/N_r)v(n-1)$
SRF-PLL	$v^+_{\alpha 1}(z) = v^+_\alpha(z)/\sqrt{v^{+2}_\alpha(z) + v^{+2}_\beta(z)}$ $v^+_{\beta 1}(z) = v^+_\beta(z)/\sqrt{v^{+2}_\alpha(z) + v^{+2}_\beta(z)}$ $v^+_q(z) = -\sin(\theta^+_p(z)z^{-1})v^+_{\alpha 1}(z) + \cos(\theta^+_p(z)z^{-1})v^+_{\beta 1}(z)$ $\omega^+_p(z) = v^+_q(z)\left[k_p + k_i T_s(1+z^{-1})/(2-2z^{-1})\right] + \omega_r(z)$ $\theta^+_p(z) = T_s(1+z^{-1})/(2-2z^{-1})\omega^+_p(z)$	$v^+_{\alpha 1}(n) = v^+_\alpha(n)/\sqrt{v^{+2}_\alpha(n) + v^{+2}_\beta(n)}$ $v^+_{\beta 1}(n) = v^+_\beta(n)/\sqrt{v^{+2}_\alpha(n) + v^{+2}_\beta(n)}$ $v^+_q(n) = -\sin(\theta^+_p(n-1))v^+_{\alpha 1}(n) + \cos(\theta^+_p(n-1))v^+_{\beta 1}(n)$ $\omega^+_p(n) = \omega^+_p(n-1) + \omega_r(n) - \omega_r(n-1) + v^+_q(n)(k_p + k_i T_s/2) - v^+_q(n-1)(k_p - k_i T_s/2)$ $\theta^+_p(n) = \theta^+_p(n-1) + T_s/2\left[\omega^+_p(n) + \omega^+_p(n-1)\right]$
SCP	$\theta^+_{\alpha\beta}(z) = v^+_\alpha(z)/\sqrt{v^{+2}_\alpha(z) + v^{+2}_\beta(z)}$ $\omega^+_{\alpha\beta}(z) = (2-2z^{-1})/(T_s + T_s z^{-1})\theta^+_{\alpha\beta}(z)$ $\omega_r(z) = \left\|\omega^+_{\alpha\beta}(z)\right\| LPF(z)$	$\theta^+_{\alpha\beta}(n) = v^+_\alpha(n)/\sqrt{v^{+2}_\alpha(n) + v^{+2}_\beta(n)}$ $\omega^+_{\alpha\beta}(n) = \omega^+_{\alpha\beta}(n-1) + \frac{2}{T_s}\left[\theta^+_{\alpha\beta}(n) - \theta^+_{\alpha\beta}(n-1)\right]$ $\omega_r(n) = \left\|\omega^+_{\alpha\beta}(n)\right\| LPF(n)$

5. Experimental Validation

The aim of this section is to evaluate the performance of the proposed PLL by extensive experimental studies under distorted conditions. The experimental setup presented in Figure 11

consists of signal generator and digital signal processor (DSP) TMS320F28335 control board. Throughout the experimental studies, the voltage benchmark is 311 V and the grid fundamental frequency f_0 is 50 Hz. The PI parameters in control loop are: k_p = 189.2 k_i = 9746 and the sampling frequency f_s is 12.8 kHz. In addition, three phase DC offsets (0.1 p.u., −0.1 p.u. and 0.1 p.u.) caused by measurement devices are considered all the time in the rest experiments. The detailed distorted conditions performed in experiments are summarized as follows:

Condition I: An asymmetric voltage sags (0.1, 0.2 and 0.3 p.u.) at t = 30 ms.
Condition II: An asymmetric phase jumps (10°, 20°, and 30°) at t = 40 ms.
Condition III: 5th and 7th order harmonics (0.2 and 0.1 p.u.) emerge at t = 50 ms.
Condition IV: Grid frequency jumps from 50 to 55 Hz at t = 60 ms.
Condition V: Grid frequency ramp change occurs at t = 100 ms with ramp rate of 20 Hz/s.

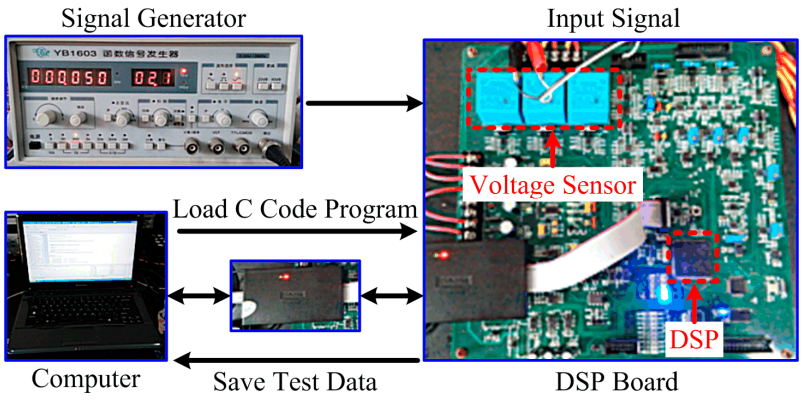

Figure 11. The experimental platform.

5.1. Experimental Results of the Proposed PLL under Distorted Conditions

The main variables of the proposed PLL are displayed: three-phase voltage (v_{abc}); FPSCs in two-phase stationary frame (v_α^+ and v_β^+); phase angle of fundamental positive sequence voltages (θ_p^+); calculated reference angular frequency (ω_r); detected grid frequency (f_m); estimated phase error ($\Delta\theta$); detected frequency error (Δf). The settling time is the time required for the response curve to reach and stay within certain range of 98% steady-state value for $\Delta\theta$ and Δf, respectively. Figure 12 shows the experimental results of the proposed PLL performed under voltage sag (condition I), phase jump (condition II), harmonics (condition III), and step-changed frequency (condition IV).

As can be seen in Figure 12, v_α^+ and v_β^+ give same amplitude and $\pi/2$ angle difference, which means the FPSCs are extracted accurately under conditions I–IV. As SGDFT needs one cycle to collect data, v_α^+ and v_β^+ become stable after one cycle when disturbances occur at t = 30 ms, t = 40 ms, t = 50 ms and t = 60 ms. Besides, it is worth noticing that θ_p^+ and v_α^+ reach the maximum simultaneously and f_m is in accordance with f_0 in steady-state regardless of the distorted conditions.

The performance of the proposed PLL under ramp-changed frequency (condition V) is also evaluated. The corresponding experimental results are shown in Figure 13. It can be observed that f_m tracks the ramp change of f_0 with a small error. In addition, f_m gives obvious overshoot at the start and end of ramp change, as SGDFT cannot give correct reference during its settling process. The detailed steady-state and dynamic performance indexes under conditions I–V are shown in the next section.

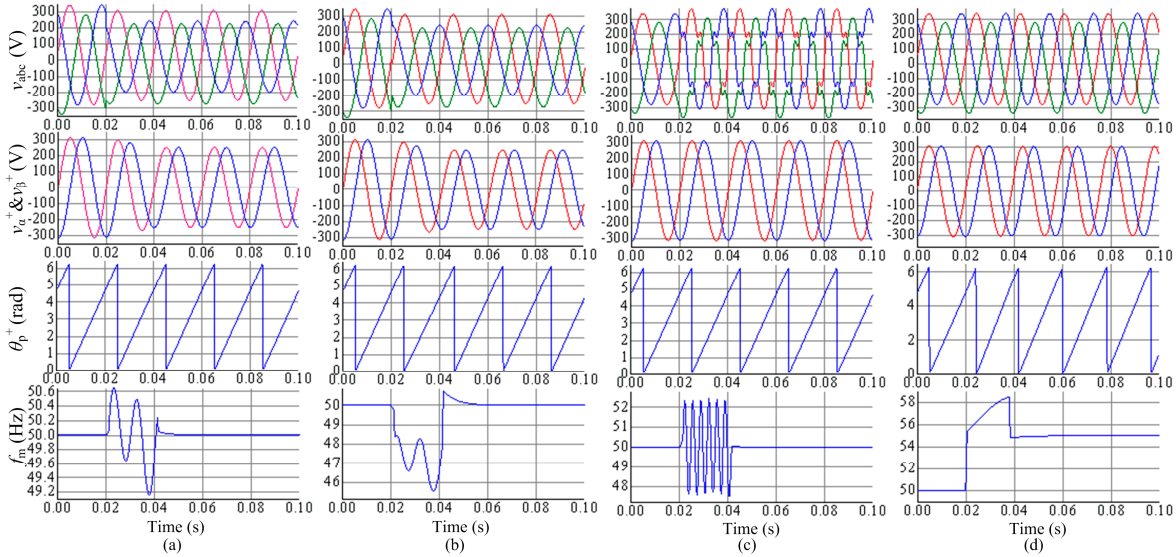

Figure 12. The experimental results under conditions I–IV. (**a**) Voltage sag; (**b**) Phase jump; (**c**) Harmonics; (**d**) Step-changed frequency.

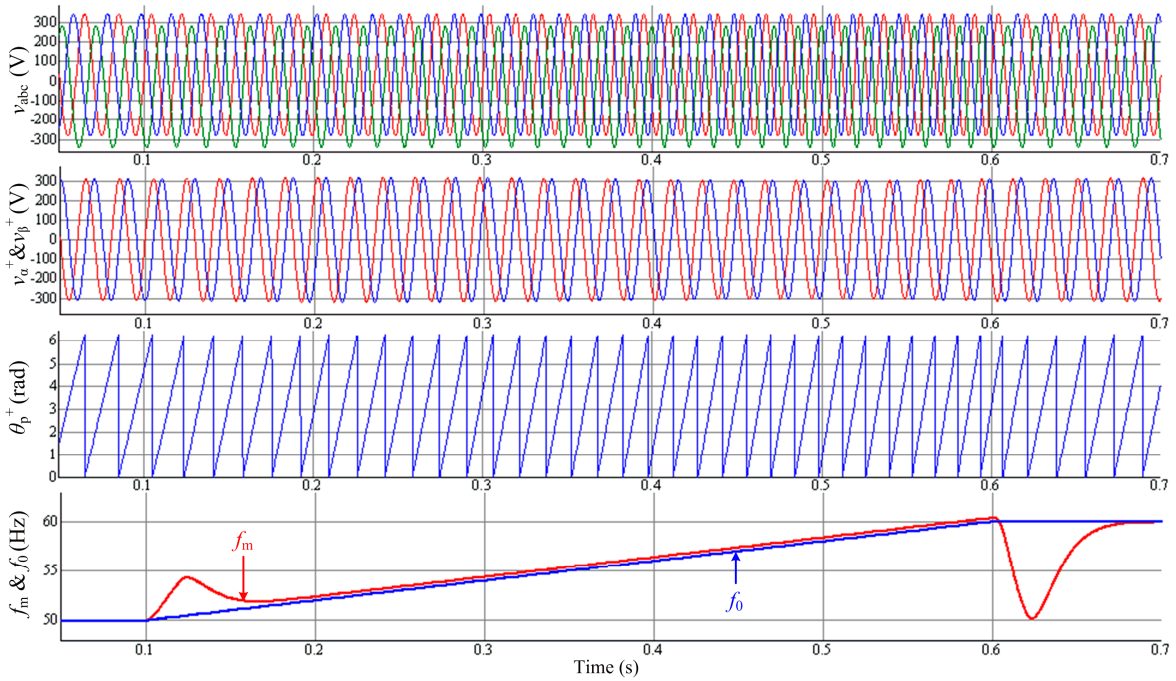

Figure 13. The experimental results under ramp-changed frequency.

5.2. Experimental Results Compared with Other Pre-Filtered PLLs

The effectiveness of the proposed PLL is further confirmed by comparing its performance with MCCF-PLL, DSOGI-PLL, PMAF-PLL and GDSC-PLL in [15,18,21,24], respectively. In order to allow a fair evaluation, the PI parameters of the above four PLLs are regulated according to the tunning methods in the corresponding articles. The PI parameters of the above four PLLs are: k_{p1} = 141.1 k_{i1} = 9952, k_{p2} = 222 k_{i2} = 6169, k_{p3} = 390 k_{i3} = 40,426, and k_{p4} = 266 k_{i4} = 35,530, respectively. The comparative tracking performance under conditions I–V are shown in Figures 14 and 15. Besides, the relevant data are summarized in Table 2.

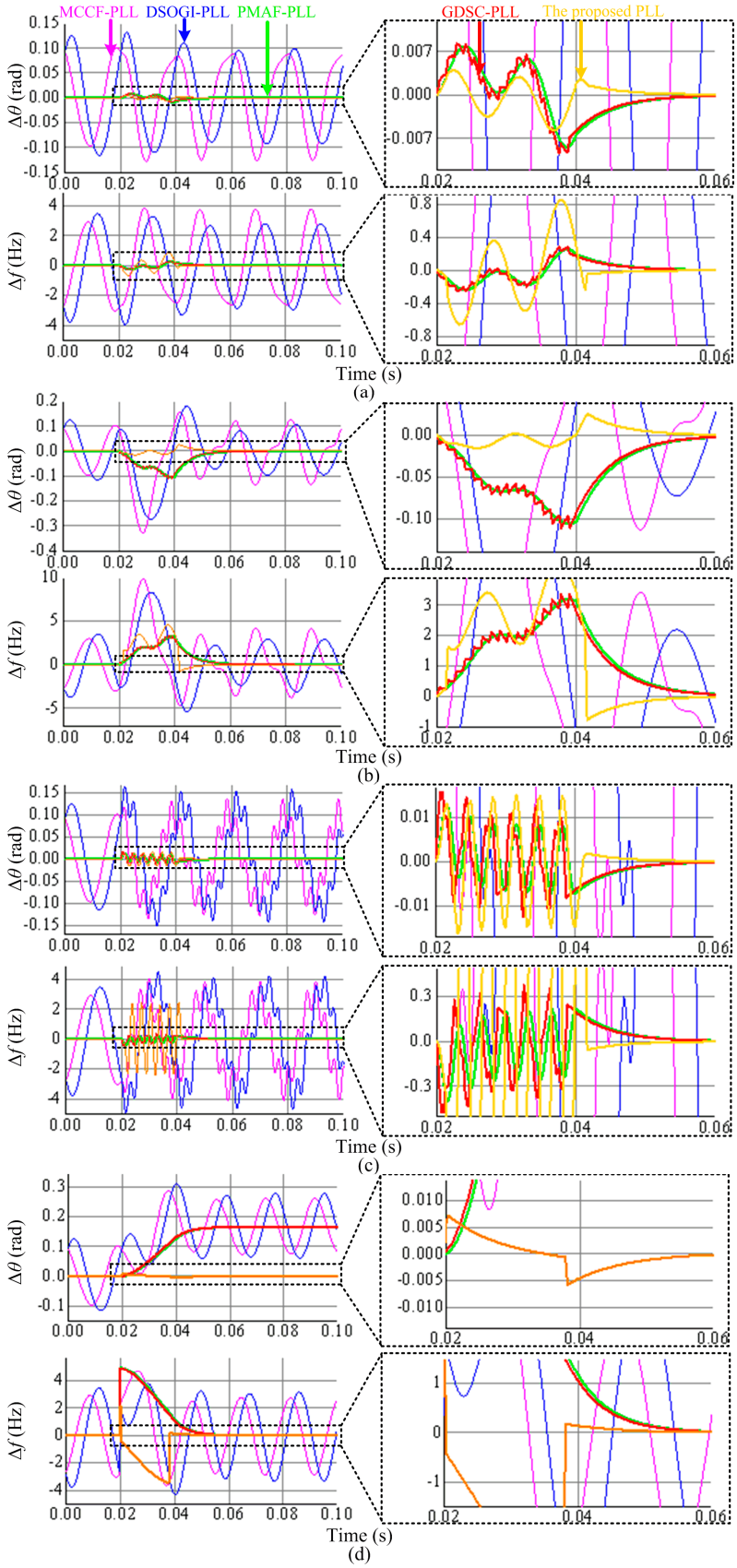

Figure 14. The comparative experimental results under conditions I–IV. (**a**) Voltage sag; (**b**) Phase jump; (**c**) Harmonics; (**d**) Step-changed frequency.

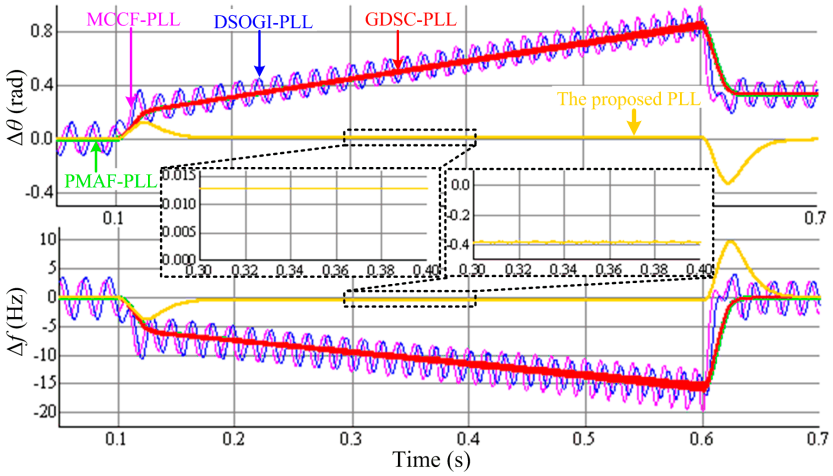

Figure 15. The comparative experimental results under ramp-changed frequency.

Table 2. Dynamic performance index.

Performance Index	Conditions	MCCF-PLL		DSOGI-PLL		PMAF-PLL		GDSC-PLL		Proposed PLL	
		Δθ	Δ*f*	Δθ	Δ*f*	Δθ	Δ*f*	Δθ	Δ*f*	Δθ	Δ*f*
Settling Time (ms)	I	≈30	≈33	≈40	≈40	≈36	≈31	≈35	≈30	≈25	≈23
	II	≈36	≈38	≈41	≈42	≈40	≈40	≈39	≈39	≈30	≈30
	III	≈30	≈35	≈38	≈39	≈34	≈34	≈33	≈33	≈30	≈28
	IV	≈31	≈32	≈38	≈40	≈41	≈36	≈40	≈35	≈35	≈25
	V	-	-	-	-	-	-	-	-	≈50	≈50
Overshoot (rad, Hz)	I	≈0.14	≈4	≈0.14	≈4	≈0.01	≈0.3	≈0.01	≈0.3	≈0.006	≈0.9
	II	≈0.32	≈10	≈0.28	≈7	≈0.11	≈3.1	≈0.11	≈3.1	≈0.03	≈4.5
	III	≈0.14	≈4	≈0.16	≈4.1	≈0.01	≈0.31	≈0.012	≈0.31	≈0.012	≈2.1
	IV	≈0.29	≈4.1	≈0.31	≈4.1	≈0.18	≈5	≈0.18	≈5	≈0.006	≈3.8
	V	-	-	-	-	-	-	-	-	≈0.18	≈4.5
Steady-state value (rad, Hz)	I	≈0.13	≈3.9	≈0.1	≈2.9	0	0	0	0	0	0
	II	≈0.13	≈4	≈0.1	≈3.5	0	0	0	0	0	0
	III	≈0.14	≈4	≈0.15	≈4.5	0	0	0	0	0	0
	IV	≈0.28	≈3	≈0.29	≈3.5	≈0.17	0	≈0.17	0	0	0
	V	-	-	-	-	-	-	-	-	≈0.013	≈0.39

DC offsets are considered in all conditions in Table 2.

It can be seen from Figure 14 that only MCCF-PLL and DSOGI-PLL contain obvious fundamental component in Δθ and Δ*f* as their pre-filters are not effective for DC offsets. Also, it is clear that Δθ and Δ*f* of MCCF-PLL and DSOGI-PLL are strongly distorted under heavily polluted condition due to their limited filtering characteristic for harmonics. As shown in Figure 14a–c, PMAF-PLL, GDSC-PLL and the proposed PLL have satisfactory disturbance rejection ability for DC offsets, voltage sag, phase jump and harmonics. However, PMAF-PLL and GDSC-PLL give obvious Δθ steady-state errors in Figure 14d. Moreover, in Figure 15 MCCF-PLL, DSOGI-PLL, PMAF-PLL and GDSC-PLL cannot track ramp-changed frequency accurately as their reference angular frequency is not updated with input signal's frequency. It is clear that the proposed PLL is effective under DC offsets, voltage sag, phase jump, harmonics, step- and ramp-changed frequency.

In Table 2, the performance indexes of the first four PLLs under condition V is not provided as they cannot track the ramp-changed frequency stably. Moreover, the steady-state values of MCCF-PLL and DSOGI-PLL refer to the peak value because they both contain fundamental components.

As summarized in Table 2, DSOGI-PLL gives the maximal settling time overall. The settling time of PMAF-PLL and GDSC-PLL are almost same. They are slightly smaller than DSOGI-PLL. MCCF-PLL tracks relatively faster than the previous PLLs. The proposed PLL gives the least settling time of Δθ

and Δf under conditions I–IV and it needs about 2.5 cycles to track the ramp-changed frequency as SGDFT needs one cycle to collect data when the periodical signals change.

MCCF-PLL and DSOGI-PLL give obvious overshoots due to the existed DC offsets. The $\Delta\theta$ overshoots of PMAF-PLL and GDSC-PLL are smaller than the first two PLLs. It is worth noticing that the proposed PLL gives the smallest $\Delta\theta$ overshoot but it cause a slight increase in the overshoot of Δf under conditions I–IV. In addition, the proposed PLL gives acceptable overshoot in $\Delta\theta$ and Δf under condition V.

MCCF-PLL and DSOGI-PLL have obvious fundamental components of $\Delta\theta$ and Δf under steady-state condition, while the other three PLLs can obtain zero steady-state error of $\Delta\theta$ and Δf under conditions I–IV except for $\Delta\theta$ of PMAF-PLL and GDSC-PLL under condition IV. Moreover, the proposed PLL gives the smallest steady-state values of $\Delta\theta$ and Δf.

We can conclude from the experimental results in Figures 12–15 and Table 2 that, (1) Like PMAF-PLL and GDSC-PLL, the proposed PLL has good disturbance rejection capability of DC offsets; (2) Only the proposed PLL can solve the ramp-changed frequency problem due to its improved SCP; (3) The proposed PLL can obtain the least settling time of phase and frequency under conditions I–IV; (4) The proposed PLL gives the least overshoot of phase and the third small overshoot of frequency under conditions I–IV; (5) The proposed PLL almost obtains zero stead-state error of phase and frequency.

6. Conclusions

This paper presents an efficient PLL based on SGDFT filter and the improved SCP. SGDFT filter is employed to enhance separation accuracy of FPSC under distorted conditions. Lagrange-interpolation method is applied to remove the adverse effect of the fractional delay when the sampling number is not integer. The improved SCP is employed to promise precise phase estimation and enables the PLL tracking reference frequency rapidly. Comparative experimental results demonstrate that the proposed PLL can achieve zero steady-state error in phase and frequency with a rapid speed compared with the other four PLLs. Meanwhile, it has satisfactory disturbance rejection capability under unbalanced voltages, harmonics, step-and ramp-changed frequency and DC offsets.

Acknowledgments: This work was supported in part by the national Natural Science Foundation of China (NSFC) under Grant 61233008 and 51520105011, and in part by the Special Project of Hunan Province of China under Grant 2015GK1002 and 2015RS4022.

Author Contributions: Yijia Cao proposed the original idea, Jiaqi Yu carried out the main research tasks, Yong Xu and Yong Li carried out the experiments. Jiaqi Yu and Jingrong Yu wrote the full manuscript and supervised the experiments.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hadjidemetriou, L.; Kyriakides, E.; Yang, Y.; Blaabjerg, F. A synchronization method for single-phase grid-tied inverters. *IEEE Trans. Power Electron.* **2016**, *31*, 2139–2149. [CrossRef]
2. Zhang, G.Q.; Wang, G.L.; Xu, D.G.; Zhao, N.N. Adaline network based PLL for position sensorless interior permanent magnet synchronous motor drives. *IEEE Trans. Power Electron.* **2016**, *31*, 1450–1460. [CrossRef]
3. Li, Y.; Liu, Q.Y.; Hu, S.J.; Liu, F.; Cao, Y.J.; Luo, L.F.; Rehtanz, C. A virtual impedance comprehensive control strategy for the controllably inductive power filtering system. *IEEE Trans. Power. Electron.* **2017**, *32*, 920–926. [CrossRef]
4. Li, Y.; Peng, Y.J.; Liu, F.; Sidorov, D.; Liang, C.G.; Luo, L.F.; Cao, Y.J. A controllably inductive filtering method with transformer-integrated linear reactor for power quality improvement of shipboard power system. *IEEE Trans. Power Deliv.* **2016**, *99*, 1–9. [CrossRef]
5. Zhang, D.L.; Wang, Y.J.; Hu, J.B.; Ma, S.C.; He, Q.; Guo, Q. Impacts of PLL on the DFIG-based WTG's electromechanical response under transient conditions: Analysis and modeling. *CSEE J. Power Energy Syst.* **2016**, *2*, 30–39. [CrossRef]

6. Golestan, S.; Freijedo, F.D.; Guerrero, J.M. A systematic approach to design high-order phase-locked loops. *IEEE Trans. Power Electron.* **2016**, *30*, 4013–4019. [CrossRef]
7. Kaura, V.; Blasko, V. Operation of phase locked loop system under distorted utility conditions. *IEEE Trans. Ind.* **1997**, *33*, 58–63. [CrossRef]
8. Blaabjerg, F.; Teodorescu, R.; Liserre, M.; Timbus, A.V. Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1398–1409. [CrossRef]
9. Subramanian, C.; Kanagaraj, R. Rapid tracking of grid variables using prefiltered synchronous reference frame PLL. *IEEE Trans. Instrum. Meas.* **2015**, *64*, 1826–1836. [CrossRef]
10. Lee, K.J.; Lee, J.P.; Shin, D.; Yoo, D.W.; Kim, H.J. A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS. *IEEE Trans. Ind. Electron.* **2014**, *61*, 292–301. [CrossRef]
11. Wang, L.; Jiang, Q.; Hong, L.C. A novel three-phase software phase-locked loop based on frequency-locked loop and initial phase angle detection phase-locked loop. In Proceedings of the IECON 2012 38th Annual Conference on IEEE Industrial Electronics Society, Montreal, QC, Canada, 25–28 October 2012; pp. 150–155.
12. Kanjiya, P.; Khadkikar, V.; El Moursi, M.S. A novel type-1 frequency-locked loop for fast detection of frequency and phase with improved stability margins. *IEEE Trans. Power Electron.* **2016**, *31*, 2550–2561. [CrossRef]
13. Wang, Y.F.; Li, Y.W. Analysis and digital implementation of cascaded delayed-signal-cancellation PLL. *IEEE Trans. Power Electron.* **2011**, *26*, 1067–1080. [CrossRef]
14. Carugati, I.; Maestri, S.; Donato, P.G.; Carrica, D.; Benedetti, M. Variable sampling period filter PLL for distorted three-phase systems. *IEEE Trans. Power Electron.* **2012**, *27*, 321–330. [CrossRef]
15. Guo, X.Q.; Wu, W.Y.; Chen, Z. Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks. *IEEE Trans. Power Electron.* **2011**, *58*, 1194–1204. [CrossRef]
16. Li, W.W.; Ruan, X.B.; Bao, C.L.; Pan, D.H.; Wang, X.H. Grid synchronization systems of three-phase grid-connected power converters: A complex-vector-filter perspective. *IEEE Trans. Ind. Electron.* **2014**, *61*, 1855–1870. [CrossRef]
17. Ohori, K.; Hattori, N.; Funaki, T. Phase-locked loop using complex-coefficient filters for grid-connected inverter. *Electr. Eng. Jpn.* **2014**, *189*, 52–60. [CrossRef]
18. Rodríguez, P.; Teodorescu, R.; Candela, I.; Timbus, A.V.; Blaabjerg, M.L.F. New Positive-sequence Voltage Detector for Grid Synchronization of Power inverters under Faulty Grid Conditions. In Proceedings of the 2006 37th IEEE Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006; pp. 1–7.
19. Rodriguez, P.; Luna, A.; Candela, I.; Mujal, R.; Teodorescu, R.; Blaabjerg, F. Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions. *IEEE Trans. Ind. Electron.* **2011**, *58*, 127–138. [CrossRef]
20. Xiao, F.; Dong, L.; Li, L.; Liao, X. A frequency-fixed SOGI-based PLL for single-phase grid-connected converters. *IEEE Trans. Power Electron.* **2017**, *32*, 1713–1719. [CrossRef]
21. Golestan, S.; Guerrero, J.M.; Vidal, A. PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement. *IEEE Trans. Power Electron.* **2016**, *31*, 4013–4019. [CrossRef]
22. Robles, E.; Pou, J.; Ceballos, S.; Zaragoza, J.; Martin, J.L.; Ibanez, P. Frequency-adaptive stationary-reference-frame grid voltage sequence detector for distributed generation systems. *IEEE Trans. Ind. Electron.* **2011**, *58*, 4275–4287. [CrossRef]
23. Robles, E.; Ceballos, S.; Pou, J.; Martín, J.L.; Zaragoza, J.; Ibañez, P. Variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a phase-locked loop. *IEEE Trans. Power Electron.* **2010**, *25*, 2552–2563. [CrossRef]
24. Neves, F.A.S.; Cavalcanti, M.C.; de Souza, H.E.P.; Bradaschia, F.; Bueno, E.J.; Rizo, M. A generalized delayed signal cancellation method for detecting fundamental-frequency positive-sequence three-phase signals. *IEEE Trans. Power Deliv.* **2010**, *25*, 1816–1825. [CrossRef]
25. Wang, Y.F. Grid synchronization PLL based on cascaded delayed signal cancellation. *IEEE Trans. Ind. Electron.* **2013**, *60*, 645–658. [CrossRef]
26. Batista, Y.N.; de Souza, H.E.P.; Neves, F.A.S.; Filho, R.F.D.; Bradaschia, F. Variable-structure generalized delayed signal cancellation PLL to improve convergence time. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7146–7150. [CrossRef]

27. Neves, F.A.S.; de Souza, H.E.P.; Cavalcanti, M.C.; Bradaschia, F.; Bueno, E.J. Digital filters for fast harmonic sequence component separation of unbalanced and distorted three-phase signals. *IEEE Trans. Ind. Electron.* **2012**, *59*, 3847–3859. [CrossRef]
28. Liccardo, F.; Marino, P.; Raimondo, G. Robust and fast three-phase PLL tracking system. *IEEE Trans. Ind. Electron.* **2011**, *58*, 221–231. [CrossRef]
29. Rani, B.I.; Aravind, C.K.; Ilango, G.S.; Nagamani, C. A three phase PLL with a dynamic feed forward frequency estimator for synchronization of grid connected converters under wide frequency variations. *Int. J. Electr. Power Energy Syst.* **2012**, *41*, 63–70. [CrossRef]
30. Jacobsen, E.; Lyons, R. The sliding DFT. *IEEE Signal Process. Mag.* **2003**, *20*, 74–80.
31. Laakso, T.I.; Valimaki, V.; Karjalainen, M. Splitting the unit delay [FIR/all pass filters design]. *IEEE Signal Process. Mag.* **1996**, *13*, 30–60. [CrossRef]
32. Golestan, S.; Monfared, M.; Freijedo, F.D.; Guerrero, J.M. Dynamics assessment of advanced single-phase PLL structures. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2167–2176. [CrossRef]
33. Yepes, A.G.; Freijedo, F.D.; Doval-Gandoy, J. Effects of discretization methods on the performance of resonant controllers. *IEEE Trans. Power Electron.* **2010**, *25*, 1692–1712. [CrossRef]