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Near State Vector Selection-Based Model Predictive Control with Common Mode Voltage Mitigation for a Three-Phase Four-Leg Inverter

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Abstract: A high computational burden is required in conventional model predictive control, as all of the voltage vectors of a power inverter are used to predict the future behavior of the system. Apart from that, the common mode voltage (CMV) of a three-phase four-leg inverter utilizes up to half of the DC-link voltage due to the use of all of the available voltage vectors. Thus, this paper proposes a near state vector selection-based model predictive control (NSV-MPC) scheme to mitigate the CMV and reduce computational burden. In the proposed technique, only six active voltage vectors are used in the predictive model, and the vectors are selected based on the position of the future reference vector. In every sampling period, the position of the reference current is used to detect the voltage vectors surrounding the reference voltage vector. Besides the six active vectors, one of the zero vectors is also used. The proposed technique is compared with the conventional control scheme in terms of execution time, CMV variation, and load current ripple in both simulation and an experimental setup. The LabVIEW Field programmable gate array rapid prototyping controller is used to validate the proposed control scheme experimentally, and demonstrate that the CMV can be bounded within one-fourth of the DC-link voltage.

Keywords: near state vector selection based model predictive control; common mode voltage; ripple content; execution time; computational burden and three phase four leg inverter

1. Introduction

Photovoltaic (PV) energy has become an attractive renewable energy source due to its user-friendly operation, straightforward structure, easy installation, and close setup to the user. In PV energy conversion and distribution systems, three-phase four-leg inverters are becoming popular in specific applications such as standalone [1] and Uninterruptible power supply (UPS) systems [2], as well as in islanded mode when the grid supply has failed [3]. A standalone PV system has to provide uninterrupted and balanced/unbalanced power for utilities such as data communication, aircraft, home appliances, satellite stations, and railway systems [4]. However, delivering an unbalanced load is a commercial and industrial issue in an energy conversion system. A four-wire three-leg inverter can be used to deliver unbalanced power, but it has the drawback of low utilization DC-link voltage. The potential difference between the star point and the midpoint of DC-link capacitors is forced to zero; therefore, the star point of the load is not free [5,6]. Thus, four-leg inverters have been introduced

that can provide zero sequence paths, and are thus preferred over three-leg inverters to distribute power to the balanced/unbalanced loads. Moreover, three-phase four-leg inverters can overcome the low voltage DC-link utilization of the three-phase four-wire system [7]. Due to the additional leg, the control vectors increase from 8 (2^3) to 16 (2^4), which increases the number of switching actions in every switching period [8–10]. However, the common mode voltage (CMV) between the load-neutral point and the midpoint of the DC-link capacitors of the three-phase four-leg inverter causes radiation in the electromagnetic interference, system losses, and threats to personal safety [11].

In order to overcome these problems, the CMV has to be mitigated or reduced. This can be achieved actively or passively. In active mitigation, active circuits such as transistors and capacitors are used. Meanwhile, passive components are used in passive mitigation [12]. Owing to hardware additions or modifications, these methods lead to increases in size and higher costs, and thus cannot be directly applicable to high-voltage systems. Thus, research is progressing towards software invention or modification through improving the control algorithm. The improvement in software can be divided into two main types. The first type is achieved with a modulation-based control algorithm. In a three-phase four-leg inverter, CMV can be kept constant at $\pm \frac{v_{dc}}{2}$ (v_{dc} is the DC-link voltage) by improving the modulation mode with the Boolean logic function [13]. A pulse width modulation (PWM) block that avoids the zero-voltage vector has been introduced to alleviate the CMV in [14]. A control scheme with six switching states for the three-phase four-leg inverter is proposed to ensure the zero CMV in [15]. However, this switching scheme cannot be practically implemented for the unbalanced condition due to the utilization of the restricted voltage vector in a conventional method. The aforementioned PWM-based control algorithms consist of a modulation stage and an inner control loop with proportional–integral (PI) controllers. In the second type of improvement scheme, an easier and more powerful control method, the finite control set model predictive control (FCS-MPC) is used. The FCS-MPC considers a finite number of valid switching states to predict the behavior of the system through a discrete model in every sampling period [16–19]. The FCS-MPC uses a cost function to carry out the optimization in the prediction. The predefined cost function is used to compare each prediction with its respective reference, and the switching state that produces the minimum value of the cost function is applied to the inverter. This process is repeated in every sampling period as mentioned in [9,20–22], and thus, no modulation stage is required in this technique. The implementation of the FCS-MPC is very easy and simple, and it has fast a dynamic response in spite of its constraints and nonlinearity inclusion [8,23–25]. However, since the FCS-MPC algorithm predicts the control variables based on the system model, it puts a high computational burden on the controller [20,26,27]. This FCS-MPC-based control technique also can be used to restrict the CMV within $\pm \frac{v_{dc}}{6}$ by utilizing six non-zero voltage vectors in the three-phase three-leg inverter [28]. The FCS-MPC method can reduce the CMV and control the load current for the three-phase three-leg inverter, as mentioned in [28–30]. Meanwhile, in [29], the load current ripple and CMV are reduced, but the process of selecting two non-zero voltage vectors in each sampling period and determining each vector duration is very complex. This greatly increases the computation complexity. Guo et al. [31] proposed the use of four non-zero voltage vectors in order to reduce the CMV for three-phase three-leg inverters to $\pm \frac{v_{dc}}{6}$, but the complicated switching selection between opposite voltage vectors increases the switching losses. In [32], the CMV factor is inserted into the cost function in order to reduce the CMV, but this increases the ripple content in the load current. In recent works, there is a lack of CMV mitigation with reduced computational burden, and most of the research studies have focused on the three-phase three-leg inverter. Thus, further research work is required for the three-phase four-leg inverter.

In this paper, a near state vector selection-based MPC (NSV-MPC) is proposed in order to reduce the CMV with reduced computational burden for a three-phase four-leg inverter. Based on near state voltage vector, a cost function is used in the predictive model to determine the optimal switching voltage vector from the vectors that surround the future reference voltage vector. The reference voltage vector and its NSV are determined by the future reference currents. In order to reduce the CMV, the zero-switching voltage vector has to be eliminated from the switching state, because it is

causing a high CMV. Thus, only six switching states are required to predict the future voltage vector. Consequently, only six repeated iterations are required in every sampling period, which reduces the computational burden.

The rest of this paper is structured as follows: the mathematical models for the inverter-load system are derived in Section 2. Then, the model predictive control for three-phase four-leg inverter is explained in Section 3, and the proposed control technique is described in Section 4. The proposed system is then validated through simulation, and the experimental results are given in Section 5. Afterwards, the robustness and performance analysis are discussed in Section 6. Then, the appropriate conclusions are drawn in Section 7.

2. Three-Phase Four-Leg Inverter Model

A three-phase four-leg inverter topology with the output resistive-inductive (R-L) filter is shown in Figure 1. The neutral leg in the inverter topology is used to control the zero-sequence current. The neutral inductor is introduced in the fourth leg to attenuate the switching current ripple to be the same as the other legs. Besides, the neutral inductor limits the fault current during short circuit or unbalanced loading conditions [15,33]. Therefore, neutral inductance L_{fn} is connected at the neutral leg in the practical applications [34,35].

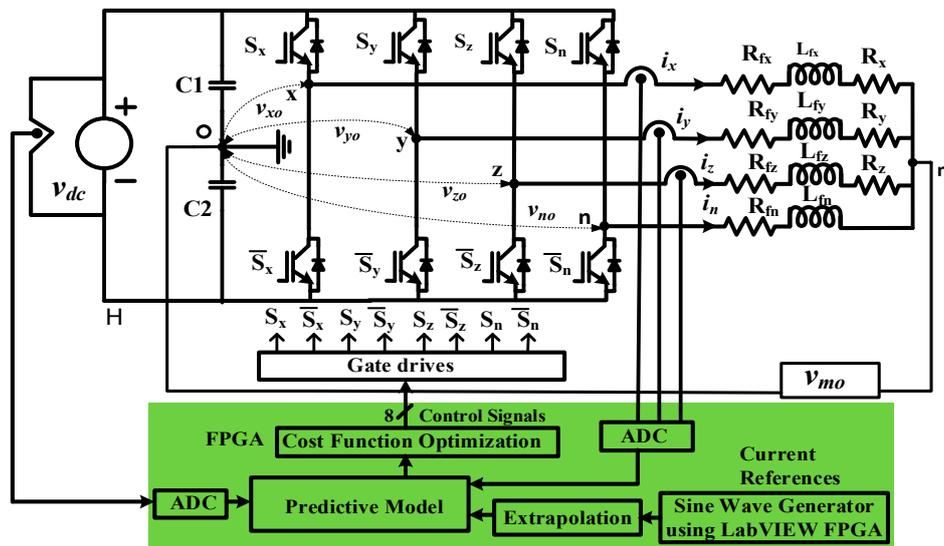


Figure 1. Three-phase four-leg inverter with a field programmable gate array (FPGA) control block.

The paired insulated-gate bipolar transistor (IGBT) switches in each of the four legs turn on and off in a complementary mode. If the upper switch of one leg is turned on, the lower one is turned off, and vice versa. The CMV is the potential difference between the midpoint of the DC-link capacitors and the load-neutral point (v_{mo}), as shown in Figure 1. The CMV can be expressed in terms of the voltage on each leg, as shown in [36]:

$$v_{mo} = \frac{v_{xo} + v_{yo} + v_{zo} + v_{no}}{4} \tag{1}$$

where v_{xo} , v_{yo} , v_{zo} , and v_{no} are the voltages between the terminal and the midpoint of the DC-link. Based on the switching states, the phase voltages can have either voltages level $+\frac{v_{dc}}{2}$ or $-\frac{v_{dc}}{2}$. Therefore, depending on the 16 switching states of the three-phase four-leg inverter, the CMV can have the values $\pm\frac{v_{dc}}{2}$, 0, and $\pm\frac{v_{dc}}{4}$.

According to Kirchhoff's voltage law, the inverter's output voltages can be written as follows:

$$v = \left(R_f + R \right) i + L_f \frac{di}{dt} + v_{mH} \tag{2}$$

where:

$$\begin{aligned} \mathbf{v} &= \begin{bmatrix} v_{xH} & v_{yH} & v_{zH} & v_{nH} \end{bmatrix}^T \\ \mathbf{i} &= \begin{bmatrix} i_x & i_y & i_z & i_n \end{bmatrix}^T \\ R_f + R &= \begin{bmatrix} R_{fx} + R_x & R_{fy} + R_y & R_{fz} + R_z & R_{fn} \end{bmatrix}^T \\ L_f &= \begin{bmatrix} L_{fx} & L_{fy} & L_{fz} & L_{fn} \end{bmatrix}^T \\ i_n + i_x + i_y + i_z &= 0 \end{aligned}$$

where, \mathbf{v} is the load voltage vector, \mathbf{i} is the load vector current, R_f is the filter resistance, R is the load resistance, L_f is the filter inductance, and v_{mH} is the voltage between the load-neutral and the DC-link negative point (H).

The voltages of each leg from the DC-link negative point (H) can be written as:

$$v_{jH} = S_j v_{dc}, \quad j = x, y, z, n \quad (3)$$

where v_{dc} is the DC-link voltage, and S_j is the switching state of leg j . The derivative from Equation (2) can be written in continuous form in terms of the load current vector, as shown in Equation (4):

$$\frac{d\mathbf{i}}{dt} = \frac{1}{L_f} \left[(\mathbf{v} - v_{mH}) - (R_f + R)\mathbf{i} \right] \quad (4)$$

The load-neutral voltage (v_{mH}) can be expressed from Equations (3) and (4) as:

$$v_{mH} = L_{eq} v_{dc} \sum_{k=x,y,z,n} \frac{S_k}{L_{fk}} - L_{eq} \sum_{k=x,y,z,n} \frac{R_{fk} + R_k}{L_{fk}} i_k \quad (5)$$

with $L_{eq} = \left(\frac{1}{L_{fx}} + \frac{1}{L_{fy}} + \frac{1}{L_{fz}} + \frac{1}{L_{fn}} \right)^{-1}$.

The system state space representation from Equation (2) is as follows, as seen in [26]:

$$\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \quad \mathbf{y} = \mathbf{C}\mathbf{x} \quad (6)$$

with $\mathbf{x} = \begin{bmatrix} i_x & i_y & i_z \end{bmatrix}^T$ and $\mathbf{u} = \begin{bmatrix} v_{xn} & v_{yn} & v_{zn} \end{bmatrix}^T$, where \mathbf{x} is the state variable vector, \mathbf{u} is the input variable vector, and \mathbf{y} is the output variable vector. Matrix \mathbf{A} , \mathbf{B} , and \mathbf{C} are as follows:

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{fX}+R_X}{L_{fX}} + \frac{L_{eq}}{L_{fX}} \begin{pmatrix} \frac{R_{fX}+R_X}{L_{fX}} \\ -\frac{R_{fn}}{L_{fn}} \end{pmatrix} & \frac{L_{eq}}{L_{fX}} \begin{pmatrix} \frac{R_{fy}+R_y}{L_{fy}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} & \frac{L_{eq}}{L_{fX}} \begin{pmatrix} \frac{R_{fz}+R_z}{L_{fz}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} \\ \frac{L_{eq}}{L_{fy}} \begin{pmatrix} \frac{R_{fx}+R_x}{L_{fx}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} & -\frac{R_{fy}+R_y}{L_{fy}} + \frac{L_{eq}}{L_{fy}} \begin{pmatrix} \frac{R_{fy}+R_y}{L_{fy}} \\ -\frac{R_{fn}}{L_{fn}} \end{pmatrix} & \frac{L_{eq}}{L_{fy}} \begin{pmatrix} \frac{R_{fz}+R_z}{L_{fz}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} \\ \frac{L_{eq}}{L_{fz}} \begin{pmatrix} \frac{R_{fx}+R_x}{L_{fx}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} & \frac{L_{eq}}{L_{fz}} \begin{pmatrix} \frac{R_{fy}+R_y}{L_{fy}} - \frac{R_{fn}}{L_{fn}} \end{pmatrix} & -\frac{R_{fz}+R_z}{L_{fz}} + \frac{L_{eq}}{L_{fz}} \begin{pmatrix} \frac{R_{fz}+R_z}{L_{fz}} \\ -\frac{R_{fn}}{L_{fn}} \end{pmatrix} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} \frac{v_{dc}}{L_{fx}} \left(1 - \frac{L_{eq}}{L_{fx}} \right) & -\frac{v_{dc}}{L_{fx}} \frac{L_{eq}}{L_{fy}} & -\frac{v_{dc}}{L_{fx}} \frac{L_{eq}}{L_{fz}} \\ -\frac{v_{dc}}{L_{fy}} \frac{L_{eq}}{L_{fx}} & \frac{v_{dc}}{L_{fy}} \left(1 - \frac{L_{eq}}{L_{fy}} \right) & -\frac{v_{dc}}{L_{fy}} \frac{L_{eq}}{L_{fz}} \\ -\frac{v_{dc}}{L_{fz}} \frac{L_{eq}}{L_{fx}} & -\frac{v_{dc}}{L_{fz}} \frac{L_{eq}}{L_{fy}} & \frac{v_{dc}}{L_{fz}} \left(1 - \frac{L_{eq}}{L_{fz}} \right) \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}.$$

3. Model Predictive Control Method of Three-Phase Four-Leg Inverter

In order to implement the FCS-MPC algorithm on a microprocessor-based hardware, the discrete model has to be used in the analysis of the FCS-MPC algorithm. In the digital implementation, a discrete time model is used to predict the future current's value at a sampling interval (k). The inverter output current i at k th and $(k + 1)$ th instant with sampling time T_s can be calculated by using the solution of Equation (6) at the initial and final time as follows:

$$\mathbf{i}((k + 1)T_s) = e^{\mathbf{A}(k+1)T_s}\mathbf{i}(0) + e^{\mathbf{A}(k+1)T_s} \int_0^{(k+1)T_s} e^{-\mathbf{A}\tau} \mathbf{B}\mathbf{v}(\tau) d\tau \quad (7)$$

$$\mathbf{i}(kT_s) = e^{\mathbf{A}kT_s}\mathbf{i}(0) + e^{\mathbf{A}kT_s} \int_0^{kT_s} e^{-\mathbf{A}\tau} \mathbf{B}\mathbf{v}(\tau) d\tau \quad (8)$$

$\mathbf{i}((k + 1)T_s)$ can be obtained by solving Equations (7) and (8) as below:

$$\mathbf{i}((k + 1)T_s) = e^{\mathbf{A}T_s}\mathbf{i}(kT_s) + e^{\mathbf{A}(k+1)T_s} \left[\int_0^{(k+1)T_s} e^{-\mathbf{A}\tau} \mathbf{B}\mathbf{v}(\tau) d\tau - \int_0^{kT_s} e^{-\mathbf{A}\tau} \mathbf{B}\mathbf{v}(\tau) d\tau \right] \quad (9)$$

Then, Equation (10) is obtained by changing the variable of integration in Equation (9):

$$\mathbf{i}((k + 1)T_s) = e^{\mathbf{A}T_s}\mathbf{i}(kT_s) + \mathbf{A}^{-1}(\mathbf{G} - \mathbf{I}_{3 \times 3})\mathbf{B}\mathbf{v}(k + 1)T_s \quad (10)$$

The output current can be obtained at $(k + 1)$ th from Equation (10) as:

$$\mathbf{i}(k + 1) = \mathbf{G}\mathbf{i}(k) + \mathbf{Q}\mathbf{v}(k + 1) \quad (11)$$

where:

$$\mathbf{G} = e^{\mathbf{A}T_s}$$

$$\mathbf{Q} = \mathbf{A}^{-1}(\mathbf{G} - \mathbf{I}_{3 \times 3})\mathbf{B}$$

The identity matrix $\mathbf{I}_{3 \times 3}$, the inverse of matrix \mathbf{A} , and matrices \mathbf{G} and \mathbf{Q} are calculated offline in MATLAB (R2014a, MathWorks, Natick, MA, USA). The load current and DC-link voltage are required to predict the output current.

Each predicted future current is compared with its respective current reference in order to select the optimal switching state by using the cost function according to the following equation:

$$g_a(k + 1) = |\mathbf{i}^*(k + 1) - \mathbf{i}(k + 1)|$$

$$= |\mathbf{i}_x^*(k + 1) - \mathbf{i}_x(k + 1)| + |\mathbf{i}_y^*(k + 1) - \mathbf{i}_y(k + 1)| + |\mathbf{i}_z^*(k + 1) - \mathbf{i}_z(k + 1)| \quad (12)$$

The Sinusoidal current references are obtained by Sine Wave Generator using LabVIEW field programmable gate array (FPGA) at k th instant. Then, the required extrapolation can be achieved by using the fourth-order Lagrange extrapolation method [20].

$$\mathbf{i}^*(k + 1) = 4\mathbf{i}^*(k) - 6\mathbf{i}^*(k - 1) + 4\mathbf{i}^*(k - 2) - \mathbf{i}^*(k - 3) \quad (13)$$

When the sampling period is very small ($T_s < 20 \mu\text{s}$), no extrapolation is required. In that case, $\mathbf{i}^*(k + 1) = \mathbf{i}^*(k)$. The fourth leg has to change the switching state according to the switching state changes of three phases in order to control the zero-sequence current. Hence, the changing rate of the switching state in the fourth leg is higher, and it operates at a higher switching frequency as compared

with the average switching frequency. Therefore, the switching loss of the fourth leg is higher. In order to compensate for the losses caused by the neutral-leg switching frequency, its constrain has been included in the cost function as follows:

$$g_b(k + 1) = w_{swc} \times swc_n \tag{14}$$

where w_{swc} is the weighting factor. The guidelines of weighting factor selection have been given in [37]. Equation (14) must be achieved in order to improve the performance in reference current tracking and reduce the switching losses. Hence, w_{swc} is important in order to empirically achieve the improvement in performance. The number of switching in the fourth leg can be achieved as follows [38]:

$$swc_n = |S_n(k + 1) - S_n(k_{opt})| \tag{15}$$

where $S_n(k + 1)$ is the predicted neutral leg gate signal, and $S_n(k_{opt})$ is the optimal gate signal in the previous sample, k . The objective of Equation (15) is to force the predicted switching signal to remain at the same signal as the previous state. Then, the overall cost function can be expressed as follows:

$$g(k + 1) = g_a(k + 1) + g_b(k + 1) \tag{16}$$

The objective of this cost function is to optimize the error close towards zero.

4. Near State Vector Selection-Based Model Predictive Control

The lines to neutral voltages for all of the 16 switching vectors of a three-phase four-leg inverter are shown in Table 1. The lines to neutral voltages are transformed from abc into $\alpha\beta\gamma$ coordinates by using Equation (17). The results of the transformation are shown in Table 2.

$$T = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{17}$$

Table 1. The switching states with phase voltages in the abc coordinate.

Switching States	Phase Voltage in abc Coordinate			Switching States	Phase Voltage in abc Coordinate		
	v_{xn}	v_{yn}	v_{zn}		v_{xn}	v_{yn}	v_{zn}
PPPP	0	0	0	PPPN	v_{dc}	v_{dc}	v_{dc}
NNNP	$-v_{dc}$	$-v_{dc}$	$-v_{dc}$	NNNN	0	0	0
PNNP	0	$-v_{dc}$	$-v_{dc}$	PNNN	v_{dc}	0	0
PPNP	0	0	$-v_{dc}$	PPNN	v_{dc}	v_{dc}	0
NPNP	$-v_{dc}$	0	$-v_{dc}$	NPNN	0	v_{dc}	0
NPPP	$-v_{dc}$	0	0	NPPN	0	v_{dc}	v_{dc}
NNPP	$-v_{dc}$	$-v_{dc}$	0	NNPN	0	0	v_{dc}
PNPP	0	$-v_{dc}$	0	PNPN	v_{dc}	0	v_{dc}

Table 2. The switching states with phase voltages in the $\alpha\beta\gamma$ coordinate.

Switching States	Phase Voltage in $\alpha\beta\gamma$ Coordinate			Switching States	Phase Voltage in $\alpha\beta\gamma$ Coordinate		
	v_α	v_β	v_γ		v_α	v_β	v_γ
PPPP	0	0	0	PPPN	0	0	v_{dc}
NNNP	0	0	$-v_{dc}$	NNNN	0	0	0
PNNP	$\frac{2v_{dc}}{3}$	0	$-\frac{2v_{dc}}{3}$	PNNN	$\frac{2v_{dc}}{3}$	0	$\frac{v_{dc}}{3}$
PPNP	$\frac{v_{dc}}{3}$	$\frac{v_{dc}}{\sqrt{3}}$	$-\frac{v_{dc}}{3}$	PPNN	$\frac{v_{dc}}{3}$	$\frac{v_{dc}}{\sqrt{3}}$	$\frac{2v_{dc}}{3}$
NPNP	$-\frac{v_{dc}}{3}$	$\frac{v_{dc}}{\sqrt{3}}$	$-\frac{2v_{dc}}{3}$	NPNN	$-\frac{v_{dc}}{3}$	$\frac{v_{dc}}{\sqrt{3}}$	$\frac{v_{dc}}{3}$
NPPP	$-\frac{2v_{dc}}{3}$	0	$-\frac{v_{dc}}{3}$	NPPN	$-\frac{2v_{dc}}{3}$	0	$\frac{2v_{dc}}{3}$
NNPP	$-\frac{v_{dc}}{3}$	$-\frac{v_{dc}}{\sqrt{3}}$	$-\frac{2v_{dc}}{3}$	NNPN	$-\frac{v_{dc}}{3}$	$-\frac{v_{dc}}{\sqrt{3}}$	$\frac{v_{dc}}{3}$
PNPP	$\frac{v_{dc}}{3}$	$-\frac{v_{dc}}{\sqrt{3}}$	$-\frac{v_{dc}}{3}$	PNPN	$\frac{v_{dc}}{3}$	$-\frac{v_{dc}}{\sqrt{3}}$	$\frac{2v_{dc}}{3}$

vector. Therefore, two sets (Set-*a* and Set-*b*) of four switching vectors are selected in each sector. It is clear that two switching vectors (*PNNP* and *PNNN*) are chosen in both sets. Hence, there are six different switching vectors in one sector.

The voltage vector closest to the reference voltage vector is selected by evaluating the six active vectors through the predictive model mentioned in Section 3. The optimal voltage vector is selected from the six active vectors by using the cost function in Equation (15).

The model predictive control technique based on the near state voltage vector can be employed to find the closest voltage vector, which reduces the error between the desired and reference currents. From the predefined sectors, the proposed control method predicts the reference vector in each sampling time. Six active vectors are selected from the 14 active vectors that surround the reference vector based on the near state vectors listed in Table 3. This ensures that the CMV is confined within $\pm \frac{v_{dc}}{4}$, and at the same time reduces the computational burden, as only six active vectors are used, instead of 14 vectors. However, this increases the ripple content marginally in the load current as conventional MPC. In order to overcome the problem, one zero vector—either *PPPP* or *NNNN*—can be used together with the six active vectors at each control cycle, and this causes the CMV to vary between $+\frac{v_{dc}}{4}$ and $-\frac{v_{dc}}{2}$ or $-\frac{v_{dc}}{4}$ and $+\frac{v_{dc}}{2}$. Therefore, seven voltage vectors are selected to determine the voltage vector that is closest to the reference vector in the proposed NSV-MPC. In both cases, the computational burden is also reduced due to the reduction of switching vectors from 16 to six (considering only active vectors), and seven (including one zero vector), as shown Figure 3. As a result, NSV-MPC demonstrates the better performance with reduced computational burden.

Table 3. Corresponding common mode voltage (CMV) based on the near state vector (NSV) of each sector.

SECTOR I						SECTOR II							
	<i>PNPP</i>	<i>PNNP</i>	<i>PNNN</i>	<i>PPNN</i>	<i>PNNP</i>		<i>PNNP</i>	<i>PPNP</i>	<i>PPNN</i>	<i>NPNN</i>	<i>PNNN</i>	<i>PNPP</i>	
v_{xo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{xo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	
v_{yo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{yo}	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	
v_{zo}	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{zo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	
v_{no}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{no}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	
v_{mo}	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	0	0	v_{mo}	0	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	$-\frac{v_{dc}}{4}$	0	
SECTOR III						SECTOR IV							
	<i>PPNP</i>	<i>NPNP</i>	<i>NPNN</i>	<i>NPPN</i>	<i>PPNN</i>	<i>NPPP</i>		<i>NPNP</i>	<i>NPPP</i>	<i>NPPN</i>	<i>NNPN</i>	<i>NPNN</i>	<i>NNPP</i>
v_{xo}	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{xo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$
v_{yo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{yo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$
v_{zo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{zo}	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$
v_{no}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{no}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$
v_{mo}	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	0	0	$\frac{v_{dc}}{4}$	v_{mo}	0	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	$-\frac{v_{dc}}{4}$	0
SECTOR V						SECTOR VI							
	<i>NPPP</i>	<i>NNPP</i>	<i>NNPN</i>	<i>PNPN</i>	<i>NPPN</i>	<i>PNPP</i>		<i>NNPP</i>	<i>PNPP</i>	<i>PNPN</i>	<i>PNNN</i>	<i>NNPN</i>	<i>PNPP</i>
v_{xo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{xo}	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$
v_{yo}	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	v_{yo}	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$
v_{zo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{zo}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$
v_{no}	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	v_{no}	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$
v_{mo}	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	0	0	$\frac{v_{dc}}{4}$	v_{mo}	0	$\frac{v_{dc}}{4}$	0	$-\frac{v_{dc}}{4}$	$-\frac{v_{dc}}{4}$	0

A step-by-step implementation procedure for NSV-MPC is summarized below:

- Step 1. Measure the load currents $i(k)$ and calculate the reference currents $i^*(k + 1)$ by using Equation (13)
- Step 2. Identify the sector on the $\alpha\beta$ plane in the $\alpha\beta\gamma$ coordinate and the corresponding voltage vectors at every sampling period.
- Step 3. Predict the future voltage vector for all of the possible switching states from the identified sector from Table 3.
- Step 4. Predict the load currents $i(k + 1)$ of all of the possible switching states from the identified sector at the next sampling time by using Equation (11).

- Step 5. Evaluate the cost function $g(k+1)$ by using Equation (16).
 Step 6. Select the switching state that optimizes the cost function.
 Step 7. Apply the selected switching action to fire the inverter switches.

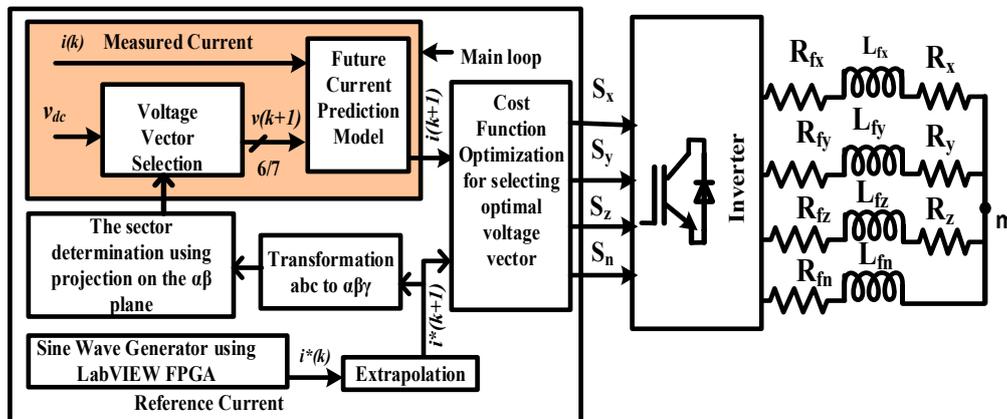


Figure 3. Proposed near state vector selection-based model predictive control (NSV-MPC) block diagram.

5. Simulation and Experimental Results

The proposed NSV-MPC has been validated in simulation by using Matlab/Simulink. Then, it is also validated through experimental implementation with a three-phase four-leg inverter laboratory prototype. The parameters of the inverter are as specified in Table 4. The experimental test was carried out using a field programmable gate array (FPGA)-based controller, and it can be used to implement the parallel processing technique of the model predictive controller to enhance the system dynamic response.

Table 4. Parameters of the experimental results.

Variable	Parameter	Value
v_{dc}	DC-link voltage	320 V
C	DC-link capacitance	2.2 mF
L_f	Filter inductance	15 mH
T_s	Sampling time	50 μ s
R	Load resistance	12 Ω
R_f	Filter resistance	0.1 Ω
f^*	Reference nominal frequency	50 Hz
i^*	Reference nominal peak current	10 A
L_{fn}	Neutral-leg inductance	8 mH
f_s	Sampling frequency	kHz

5.1. Experimental Setup

The current references were read by the NI LabVIEW FPGA 2015 module, which connected to a host computer. Figure 4 depicts the project setup in the laboratory. A National Instrument Single-Board RIO General Purpose Inverter Controller (GPIC) NI-sbRIO9606 with mezzanine card NI 9683 on-board was utilized to acquire the analogue input and generate the digital control signal output to the gate drive of the inverter. The prescaled current sensor LA25NP and voltage transducer LV25N were utilized to acquire appropriate analogue signals before sending them to the simultaneous analogue input from the GPIC board. The CMV was measured by using a Pintek DP-25 Differential Probe. The waveforms of the three-phase load currents and the CMV were measured with a LeCroy Wave Runner oscilloscope.

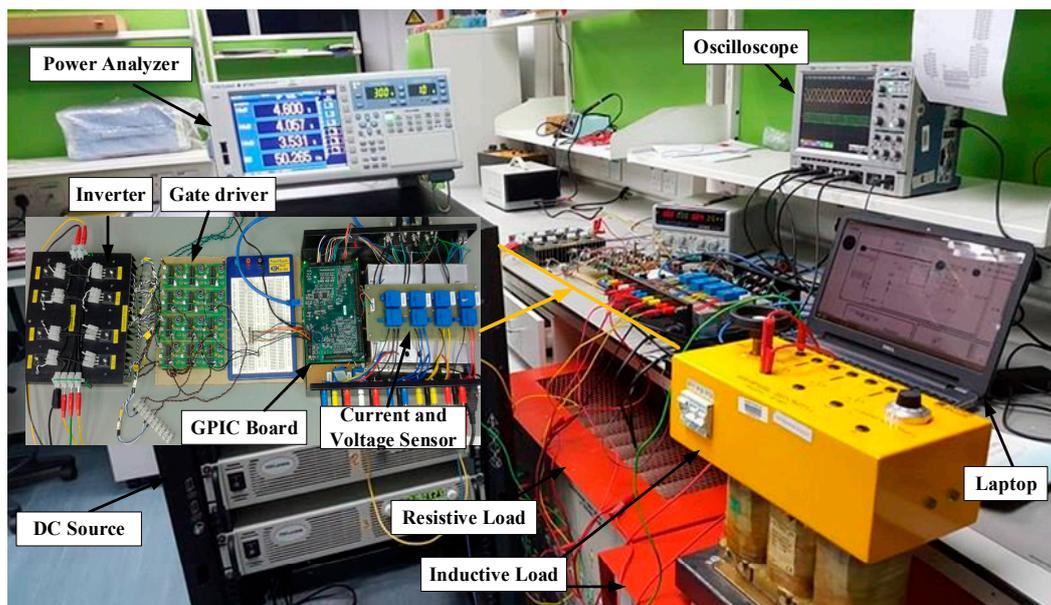


Figure 4. Experimental setup in the FPGA platform.

5.2. Results and Performance Analysis

All of the experimental results in this section were obtained by using the weighting factor $w_{swc} = 0.5$ and sampling time $T_s = 50 \mu s$. The same experimental validation was carried out for both conventional MPC and NSV-MPC. Ideally, the DC-link capacitors of a two-level four-leg inverter share equal voltages due to utilizing the full DC-link voltage by adopting the switching scheme. Three cases were considered in this work:

- Case 1. All available voltage vectors in conventional MPC at every sampling time.
- Case 2. One zero vector—either $PPPP$ or $NNNN$ —with six active vectors in proposed NSV-MPC at every sampling time.
- Case 3. Six active vectors in proposed NSV-MPC at every sampling time.

In the first case, a conventional MPC utilized 16 switching vectors to predict the future reference vector in each control cycle. Hence, the CMV was high, and required a large computational burden due to the high calculation time required to select the desire voltage vector. The peak value of CMV oscillated between $-\frac{v_{dc}}{2}$ and $+\frac{v_{dc}}{2}$ due to the alternating use of two zero vectors in the control algorithm, as illustrated in Figure 5.

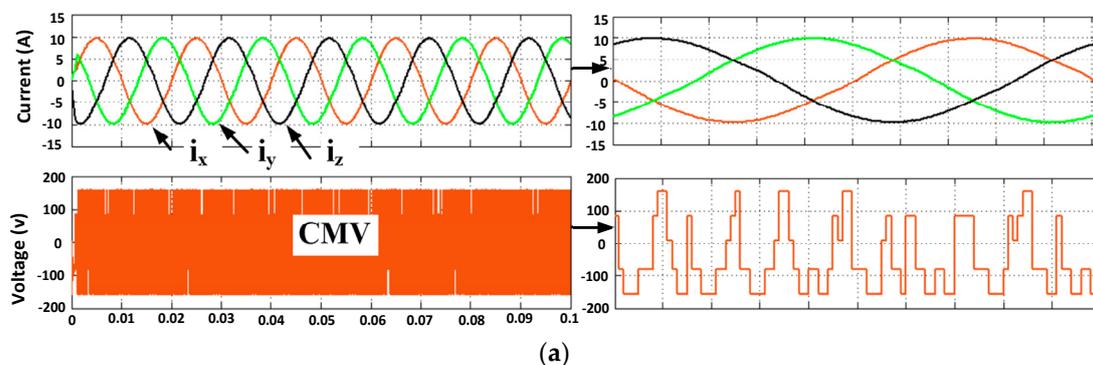


Figure 5. Cont.

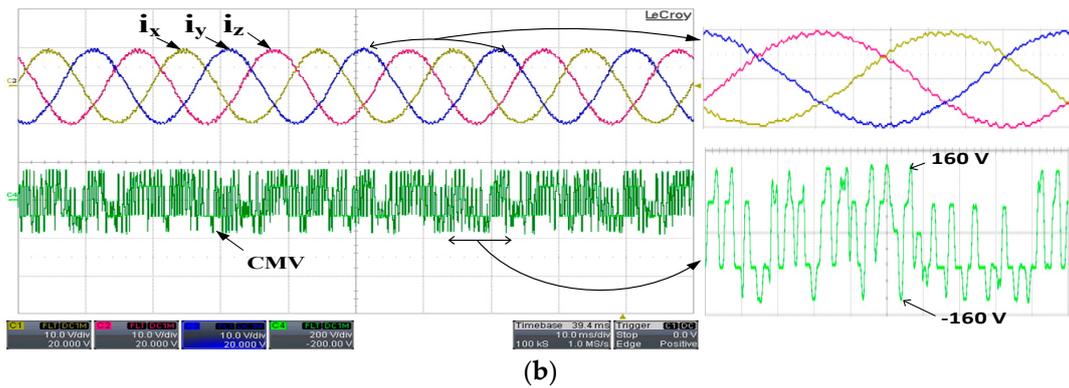


Figure 5. Each phase current and common mode voltage (CMV) for Case 1 (a) Simulation result, (b) Experimental result ($I = 10 \text{ A/div}$. $\text{CMV} = 200 \text{ V/div}$. and 10 ms/div).

In the second case, the NSV–MPC scheme utilized only one zero vector—either *PPPP* or *NNNN*—together with six active vectors at every sampling time. As shown in Figure 6, the one-sided peak value of CMV is large, and varies between $\frac{v_{dc}}{4}$ and $-\frac{v_{dc}}{2}$ or between $-\frac{v_{dc}}{4}$ and $\frac{v_{dc}}{2}$ respectively, due to the use of one zero vector. The computational burden is reduced since the number of switching voltage vectors is reduced.

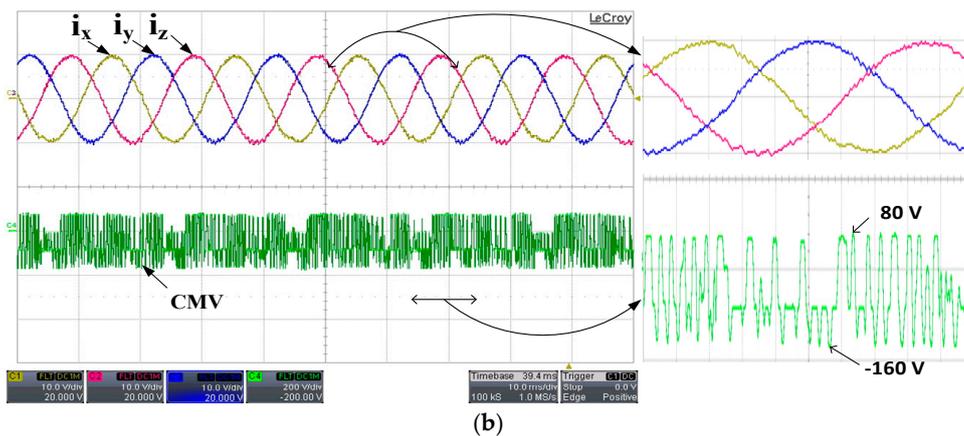
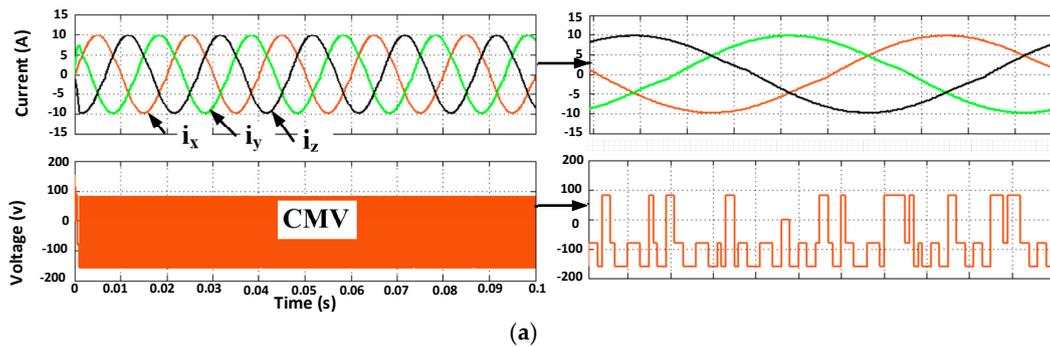
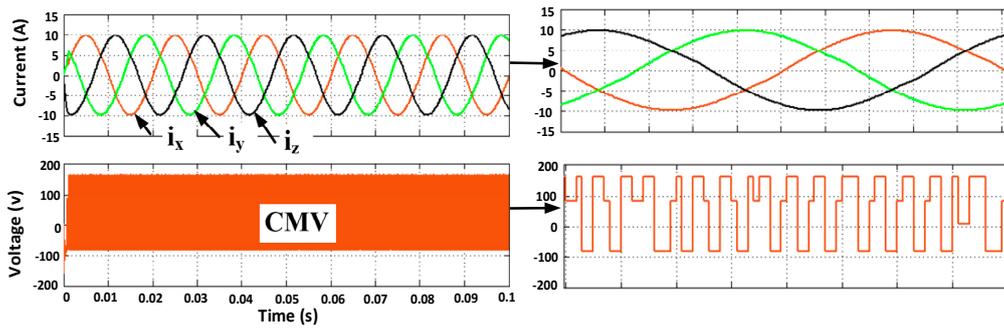
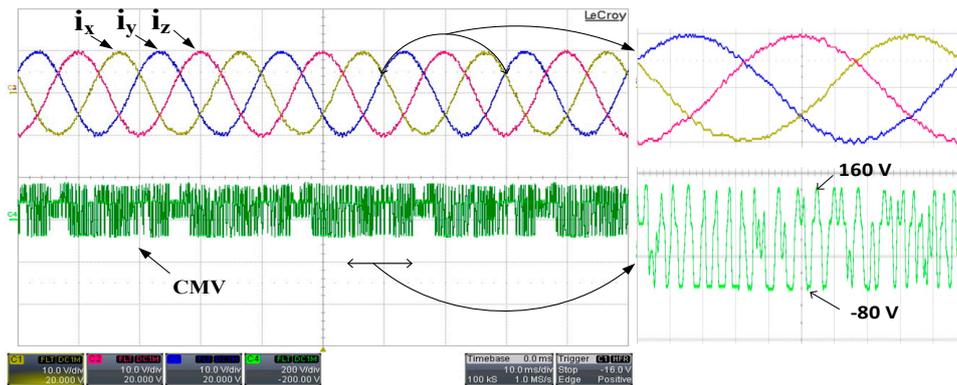


Figure 6. Cont.



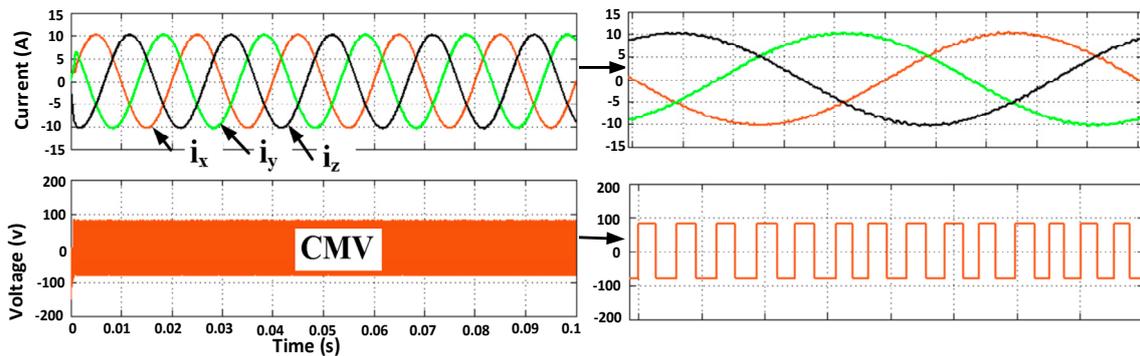
(c)



(d)

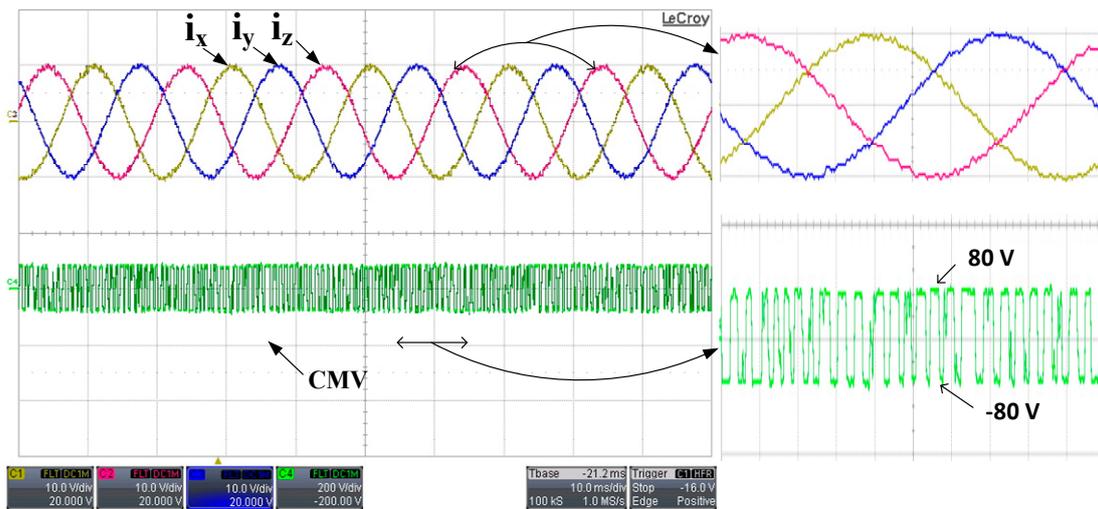
Figure 6. Each phase current and CMV for Case 2, first considering *PPPP* as the switching state: (a) Simulation result, (b) Experimental result; and considering *NNNN* as the switching state (c) Simulation result, (d) Experimental result ($I = 10 \text{ A/div.}$, $\text{CMV} = 200 \text{ V/div.}$ and 10 ms/div.).

In the third case, the proposed NSV-MPC was applied by using only six active vectors in each sampling instant to significantly reduce the peak-to-peak value of the CMV. Consequently, the calculation burden is also reduced through using a reduced number of switching vectors. Even though the ripple content in the load current is marginally higher than in Case 2, it is still in an allowable range. The CMV is confined within $\pm \frac{v_{dc}}{4}$, as shown in Figure 7.



(a)

Figure 7. Cont.



(b)

Figure 7. Each phase current and CMV for Case 3 (a) Simulation result, (b) Experimental result ($I = 10 \text{ A/div.}$, $\text{CMV} = 200 \text{ V/div.}$ and 10 ms/div.).

The Fast Fourier Transform (FFT) analysis of CMV was obtained using the powergui/FFT Analysis Toolbox of Matlab/Simulink software. The results of the mentioned cases are illustrated in Figure 8. As shown in the figures, the CMVs of the proposed NSV-MPC are significantly reduced as compared with the conventional MPC, which is due to the reduced number of voltage vectors in NSV-MPC.

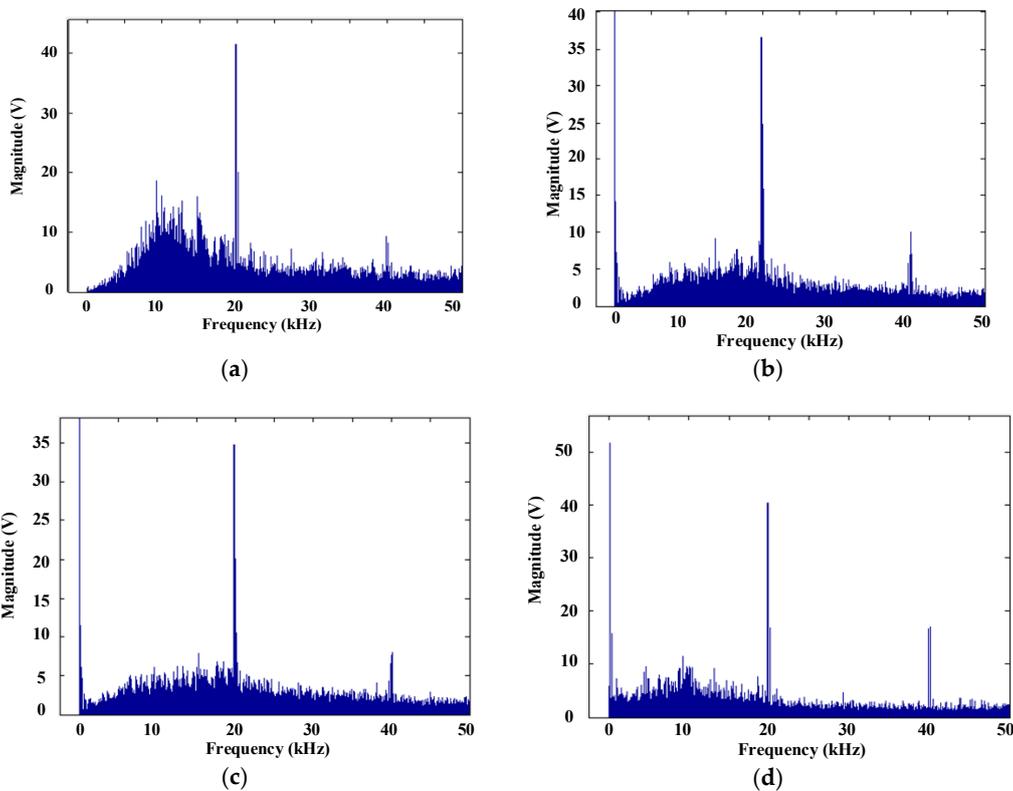
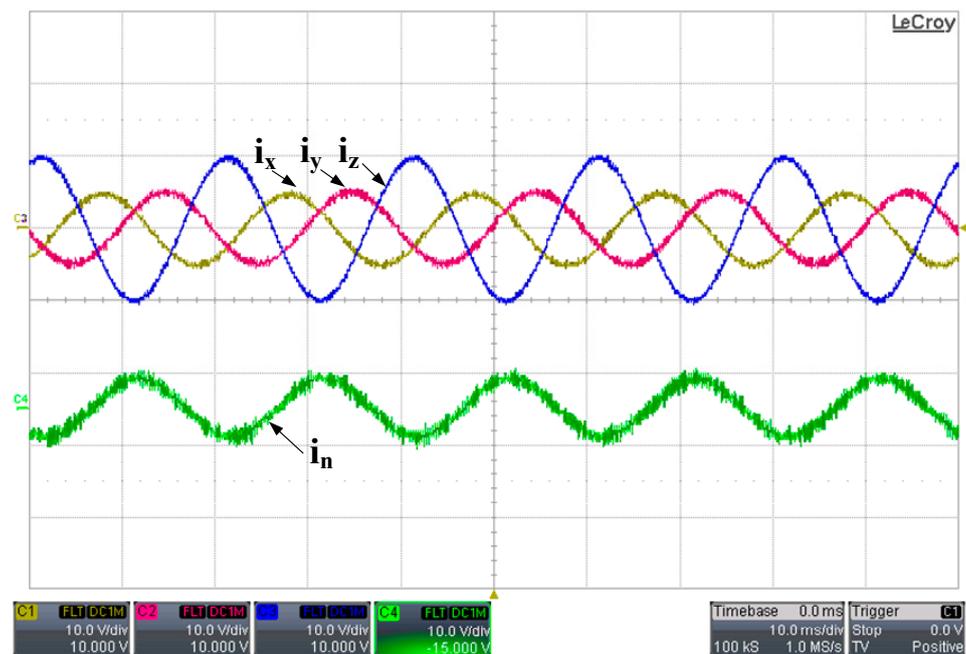
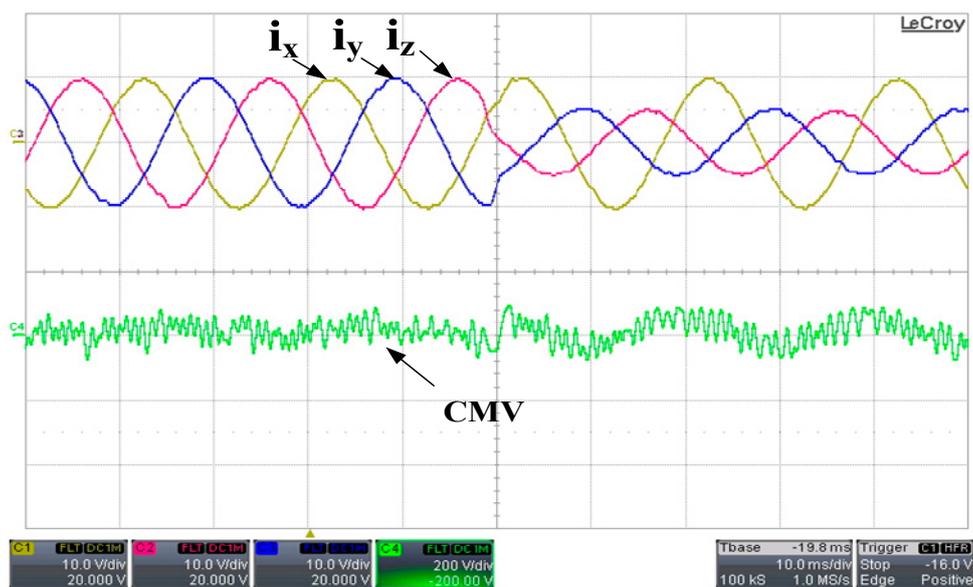


Figure 8. FFT analysis results of CMV (a) Conventional MPC, (b) Proposed NSV-MPC with *PPPP* vector, (c) Proposed NSV-MPC with *NNNN* vector, (d) Proposed NSV-MPC with active vectors only.

Figure 9 illustrates the unbalanced loading condition and the transient analysis of the proposed NSV-MPC method with balanced loads and filters. Figure 9a represents the unbalanced references connected to the balanced load and filter parameters. The unbalanced current flow in the fourth leg is known as the zero-sequence current, which is detected by adding the vectors of three phase currents. Figure 9b shows the response of a step change in phase $-y$ and $-z$ references from 10 A to 5 A. During the transient instant, the inverter load currents tracked their corresponding reference very well for the step change condition. In these cases, NSV-MPC showed the fast-dynamic response during the transient state.



(a)



(b)

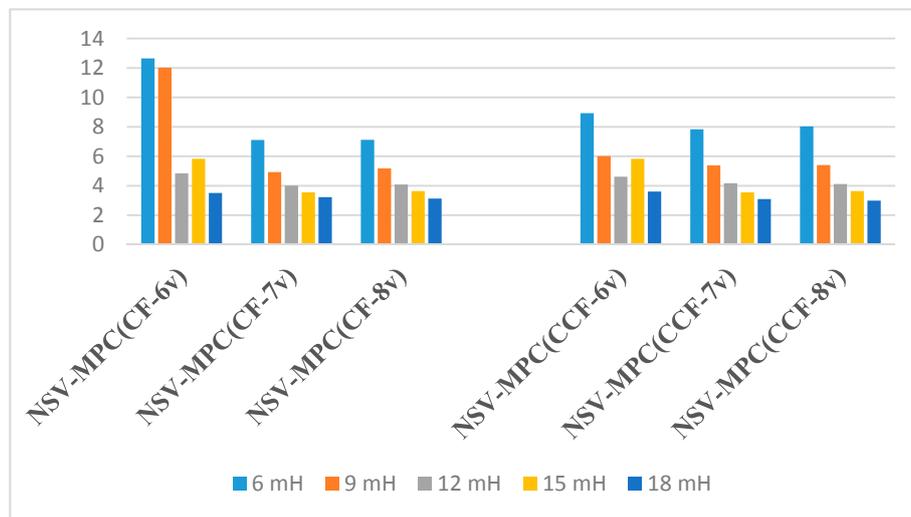
Figure 9. (a) Unbalanced references in phase $-y$ and $-z$ from 10 A to 5A with balanced resistive loads and filters, and (b) Step change in phase $-y$ and $-z$ references from 10 A to 5A with the proposed NSV-MPC technique.

6. Robustness Analysis and Performance Evaluation

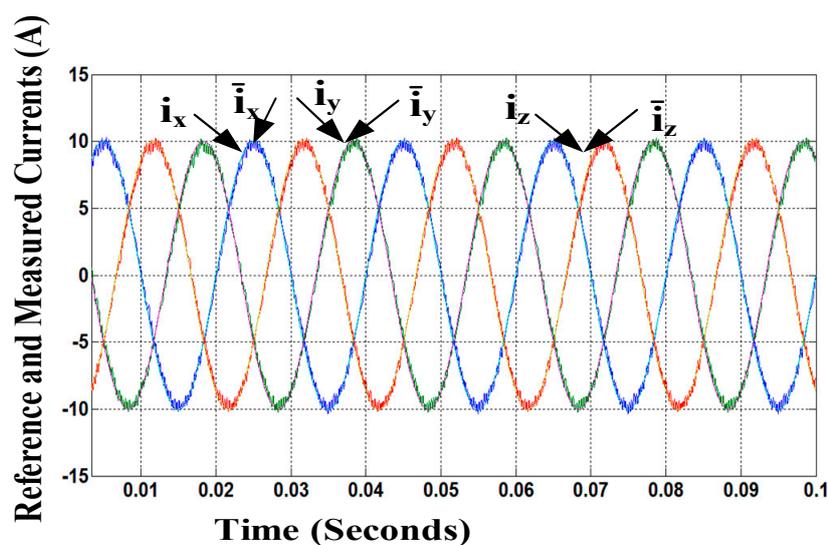
The performance and robustness analyses of the proposed control scheme are performed in the following section.

6.1. Robustness Analysis of Model Parameter Variations

The controller accuracy depends on the system parameters and the discrete predictive model. The effectiveness of the NSV-MPC was tested through robustness analysis by varying the system parameters. The response of the proposed system against the inductive filter variation was validated through both simulation and an experiment. Two cases were carried out: (a) CF: Change in inductive filter but no change in controller, where the filter's inductance changed from 6 mH to 18 mH without providing the information of the filter changes to the controller. (b) CCF: Changes to both the filter as well as to the controller, where the changed filter values are given to the controller to evaluate the effectiveness. In Figure 10a, the percentages of total harmonic distortion (THD) with respect to the variation of inductive value have been shown.



(a)



(b)

Figure 10. Cont.

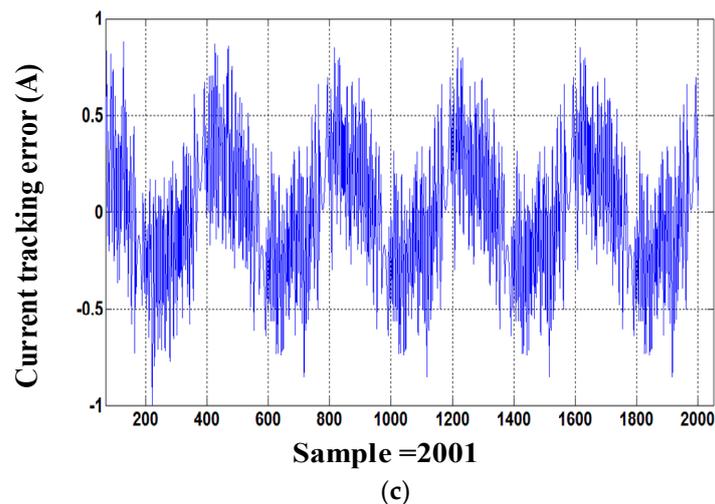


Figure 10. The results of proposed NSV-MPC: (a) The percentages of THD with respect to variation in inductive value, (b) Reference and measured currents, (c) Current tracking error of phase x .

6.2. Reference Current Tracking Error

Each leg of the three-phase four-leg inverter generated an independent voltage to control the zero-sequence voltage or current. The reference current tracking error of the proposed control scheme is very accurate. Figure 10b shows the reference and measured currents, and Figure 10c shows that the tracking error of current ($i_x^*(k) - i_x(k)$) in phase x is confined within ± 0.82 A. The percentage of reference tracking error with respect to the load current can be calculated from the reference and load current as follows:

$$i_{error_b}(\%) = \frac{\frac{1}{a} \sum_k^a |i_b^*(k) - i_b(k)|}{i_b(k)_{rms}} \quad (18)$$

where $b = x, y, z$ and $a = 2001$ is the number of samples used in simulation.

The peak-to-peak value of CMV, THD (%) of load current, and execution time of the proposed system were collected to assess the performance of the system. The proposed NSV-MPC technique improved the processing time by reducing the computational burden through using fewer numbers of voltage vectors in every control cycle. The number of ticks (1 tick = 25 ns) required by the proposed controller in completing each iteration of the control loop with a LabVIEW FPGA-based platform was less than the conventional controller. The comparisons of NSV-MPC and conventional MPC are illustrated in Tables 5 and 6.

Table 5. Execution time measurement.

Strategy	Conventional MPC	Execution Time (tick)	Proposed NSV-MPC	Execution Time (tick)	Improvement (%)
	(1 tick = 25 ns)		(1 tick = 25 ns)		
No. of Switching Vectors	16	336	6	187	44.34
			7	201	40.17

Table 6. CMV, percentage of THD, and current tracking error variation at different sampling times.

Strategy	CMV Variation	THD (%)	Current Tracking Error (%)	THD (%)	Current Tracking Error (%)	THD (%)	Current Tracking Error (%)
		Sampling Frequency		Sampling Frequency		Sampling Frequency	
		50 kHz		20 kHz		10 kHz	
Conventional MPC	−160 to 160	3.47%	3.58%	3.90%	4.68%	6.65%	6.59%
NSV-MPC with PPPP vector	−160 to 80	3.24%	3.36%	3.83%	4.26%	6.34%	6.11%

Table 6. Cont.

Strategy	CMV Variation	THD (%)	Current Tracking Error (%)	THD (%)	Current Tracking Error (%)	THD (%)	Current Tracking Error (%)
		Sampling Frequency		Sampling Frequency		Sampling Frequency	
		50 kHz		20 kHz		10 kHz	
NSV-MPC with NNNN vector	−80 to 160	3.24%	3.36%	3.83%	4.26%	6.33%	6.13%
NSV-MPC with active vectors	−80 to 80	3.62%	3.22%	4.37%	4.05%	6.58%	5.87%

7. Conclusions

In this paper, the NSV-MPC method was proposed to mitigate CMV as well as reduce computational burden. The proposed NSV-MPC method determined the active vectors based on the reference vector position, and was able to confine CMV within $\pm \frac{v_{dc}}{4}$. Moreover, this control technique reduced the computational burden by using a minimum number of usable voltage vectors in every sampling period. The experimental results for all of the possible combinations of switching vector selection were demonstrated to show the effectiveness of the proposed control method as compared with the conventional model predictive control. Besides, the load currents were able to track their references accurately. The steady state and transient state response showed the robustness and the effectiveness of the proposed control method.

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