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Characteristic Analysis and Fault-Tolerant Control of Circulating Current for Modular Multilevel Converters under Sub-Module Faults

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Abstract: A modular multilevel converter (MMC) is considered to be a promising topology for medium- or high-power applications. However, a significantly increased amount of sub-modules (SMs) in each arm also increase the risk of failures. Focusing on the fault-tolerant operation issue for the MMC under SM faults, the operation characteristics of MMC with different numbers of faulty SMs in the arms are analyzed and summarized in this paper. Based on the characteristics, a novel circulating current-suppressing (CCS) fault-tolerant control strategy comprised of a basic control unit (BCU) and virtual resistance compensation control unit (VRCCU) in two parts is proposed, which has three main features: (i) it can suppress the multi-different frequency components of the circulating current under different SM fault types simultaneously; (ii) it can help fast limiting of the transient fault current caused at the faulty SM bypassed moment; and (iii) it does not need extra communication systems to acquire the information of the number of faulty SMs. Moreover, by analyzing the stability performance of the proposed controller using the *Root-Locus* criterion, the election principle of the value of virtual resistance is revealed. Finally, the efficiency of the control strategy is confirmed with the simulation and experiment studies under different fault conditions.

Keywords: modular multilevel converter (MMC); circulating current; sub-module (SM) faults; characteristic analysis; fault-tolerant control

1. Introduction

The modular multilevel converter (MMC) was first introduced by R. Marquardt in 2001 [1]. Because of its modular design, it offers many advantages over the traditional 2-level converter such as having higher equivalent switching frequency; being easily redundant; having a common DC bus; and so on [2]. Thus, it attracts increasing attention nowadays, especially in the field of high-voltage direct current (HVDC) transmission systems [3].

In an actual project, the MMC always builds with a large number of sub-modules (SMs) per arm (e.g., Trans Bay Cable Project is reported to have 216 SMs per arm [4]) so that it can easily achieve higher voltage and power levels. However, the large number of SMs also increases the risk of failure, because each SM would become a potential failure point [5,6]. For enhancing the reliability of an MMC system, redundant SMs are often equipped in each arm [7]. Generally, there are two modes for configuring redundant SMs: (i) cold reserve, where the redundant SMs are bypassed under the normal operation state, replacing the same number of faulty SMs when SMs malfunction [8]; and (ii) hot

reserve, where the redundant SMs are operating in the same way as other SMs, but there are two options that can be adopted when SMs malfunction. One is bypassing the same number of faulty SMs in each arm to keep the system strictly symmetrical [9]; another way is just bypassing the faulty SMs [10,11]. We call them scheme "ii-a" and "ii-b" in this paper, respectively. Compared to the cold reserve mode, the hot reserve mode can make full use of all SMs under the normal operation state, and can avoid the long time needed for changing the redundant SM capacitors to rated values. In addition, as some extra healthy SMs need to be bypassed in scheme "ii-a", this not only causes the waste of healthy SMs, but also leads to a greater transient impact on the system when the large number of SMs are bypassed. Therefore, scheme "ii-b" is more preferable for the MMC since it is more economic and reliable. However, this scheme also has a potential problem, where the system will operate with asymmetric arms. For ensuring the subsequent stable operation, the corresponding fault-tolerant control approach should be considered, and this is also what this paper deals with.

Based on zero-sequence voltage injection technique, fault-tolerant control methods are proposed in [11,12]. They can ensure the converter line-to-line voltage balance output and retain the SM capacitor voltage unchanged after SM malfunction. However, the voltage injection methods will become increasingly complicated as the number of faulty SMs increases, and the main concern is only the modulation strategy. The mathematical model and fault characteristics analysis with faulty SMs are not yet involved. In [13], the zero-sequence voltage-injection technique is improved based on neutral-point shift control, and a circulating current-suppressing (CCS) control method based on *acb-dq* and *abc-dq* dual frames is also designed in this paper. It can achieve the suppression of unbalanced circulating current, but it needs positive-, negative-, and zero-sequence controllers simultaneously, and can only suppress the second-order frequency AC components of the circulating current. In [14], the energy-balancing fault-tolerant control mode is introduced. This method is easy to implement, which only needs to adjust the SM capacitor voltages on the faulty arms to ensure the energy equalization of each arm. In addition, the basic mathematical model of MMC with redundant SMs is developed in this paper; however, the specific fault characteristics with different numbers of faulty SMs in each arm are not detailed enough, so the CCS control method is not considered. For solving this problem under the energy-balancing control mode [14], the CCS control techniques are researched in varying degrees in [15,16]. The single-phase vector control method based on virtual rotating coordinate frames is proposed in [15]. However, it needs to extract the fundamental frequency component of the circulating current alone, which requires a higher accuracy of the filter, and the construction of the virtual rotating coordinate frame is complicated. In [16], the CCS control method based on proportion-resonant (PR) controller is proposed, which attaches the fundamental resonant controller to the traditional PR controller [17]. It can suppress the circulating current well under SM faults; however, the performance of the whole CCS system based on the PR control mode has not been analyzed regarding whether it can be optimized to be further studied. Moreover, a new CCS control system consisting of a phase energy controller (PEC) and dual current controller is proposed in [18]. It performs well under the SM fault conditions, but the structure of dual current control system is relatively complicated. In addition, the calculation and acquisition of SM capacitor energy will increase the burden on the control system. On the basis of the PEC, the CCS control scheme [18] is improved in [19], where the dual current control scheme is replaced by PIR controller. This method can simultaneously control the DC and AC components of the circulating current. However, it also needs an extra communication system to get the knowledge of SM capacitor energy.

In this paper, the redundant SMs are equipped with hot reserve mode and only bypass the faulty SMs when SMs malfunction. Focusing on the fault-tolerant operation issue for the MMC under SM faults, the operation characteristics of the MMC with different numbers of faulty SMs in the arms are analyzed and summarized. Based on the characteristics, a novel CCS fault-tolerant control strategy comprised of a basic control unit (BCU) and a virtual resistance compensation control unit (VRCCU) in two parts is proposed. It has three main features: (i) it can suppress the multi-different frequency components of the circulating current under different SM fault types simultaneously; (ii) it can help

fast limiting the transient fault current caused at the faulty SM bypassed moment; and (iii) it does not need extra communication systems to acquire the information of the number of faulty SMs. Moreover, the stability performance of the proposed controller is analyzed by using the *Root-Locus* criterion, and the election principle of the value of virtual resistance is revealed. In addition, the simulations in the MATLAB/SIMULINK environment and experiments with a 5-levles prototype are all studied with the proposed controller under different fault conditions. The results confirm the efficiency of the control strategy.

2. Basic Principles of MMC

The basic schematic diagram of MMC is shown in Figure 1a. It consists of six arms and connects to the grid through an isolation transformer. Each phase unit is comprised of the upper arm unit and the lower arm unit, where N identical SMs and an arm inductor L_m in the same arm comprise an arm unit. The resistance R_m in each arm represents inner inductor resistance and the arm power losses; L_s and R_s are the AC-side inductor and resistance, respectively [13]. U_{dc} is the total DC-link voltage.

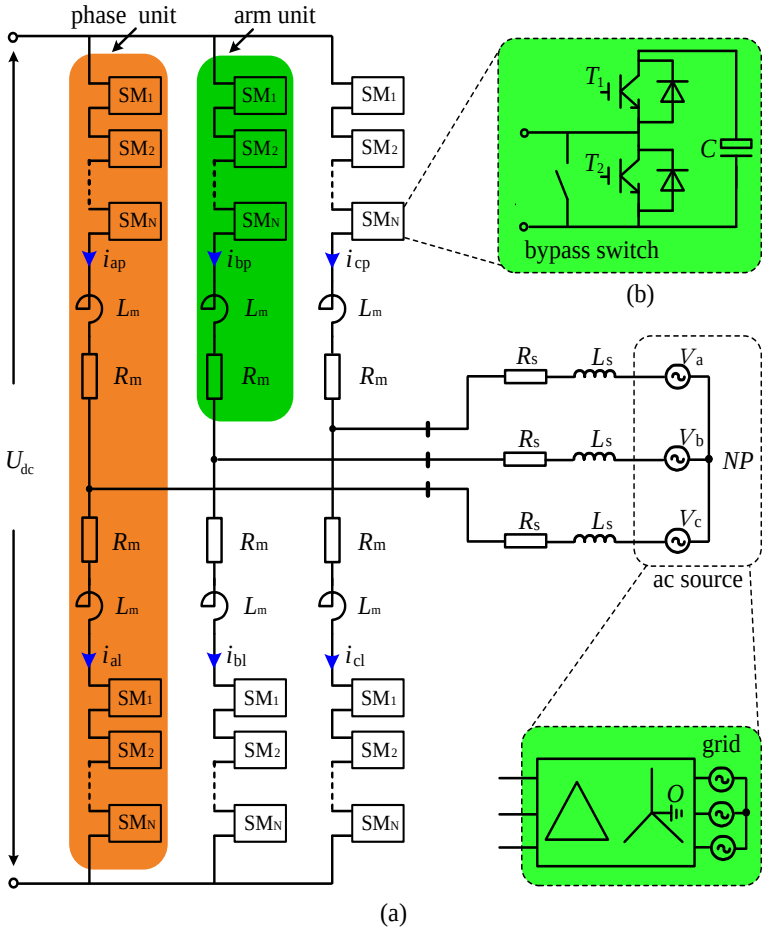

Figure 1. Basic structure of a grid-connected MMC: (**a**) circuit diagram of the MMC; (**b**) circuit diagram of SM.

Figure 1b shows the circuit diagram of the half-bridge SM. T_1 and T_2 are the insulated-gate bipolar transistor (IGBT) switches and C is the DC capacitor. Normally, the SM output voltage has only two states by the switches T_1 and T_2. When the T_1 is conducted and the T_2 is blocked, the SM is inserted, where the SM output voltage u_{sm} equals the capacitor voltage u_{cap}; when the T_1 is blocked and the T_2 is conducted, the SM is bypassed, where the SM output voltage u_{sm} equals 0.

3. Analysis of the Circulating Current Characteristic of MMC under SM Faults

3.1. Basic Matheatical Mode

During the subsequent studies of the circulating current characteristics, we assume the switches in SMs are ideal power devices, where the dead times and switching losses are ignored. The single-phase equivalent circuit of MMC is shown in Figure 2. By applying Kirchoff's voltage law (KVL) to the loop circled by the DC- and converter-sides, the basic equation of each phase can be obtained:

$$\begin{cases} \frac{U_{\mathrm{dc}}}{2} - u_{\mathrm{j}} = u_{\mathrm{jp}} \\ \frac{U_{\mathrm{dc}}}{2} + u_{\mathrm{j}} = u_{\mathrm{jl}} \end{cases} \tag{1}$$

where u_{j} is the converter-side AC voltage of phase j (j = a, b, and c). u_{jp} and u_{jl} are the upper arm and the lower arm voltages of phase j, respectively, which can be expressed as:

$$\begin{cases} u_{\mathrm{jp}} = {u_{\mathrm{jp\_cap}}}^{\Sigma} + L\frac{\mathrm{d}i_{\mathrm{jp}}}{\mathrm{d}t} + i_{\mathrm{jp}}R \\ u_{\mathrm{jl}} = {u_{\mathrm{jl\_cap}}}^{\Sigma} + L\frac{\mathrm{d}i_{\mathrm{jl}}}{\mathrm{d}t} + i_{\mathrm{jl}}R \end{cases} \tag{2}$$

where L denotes the equivalent arm inductor, which can be expressed as $L = L_{\mathrm{m}} + 2L_{\mathrm{s}}$. R denotes the equivalent arm resistance, which can be expressed as $R = R_{\mathrm{m}} + 2R_{\mathrm{s}}$. i_{jp} and i_{jl} are the upper arm and the lower arm currents of phase j, respectively. ${u_{\mathrm{jp\_cap}}}^{\Sigma}$ and ${u_{\mathrm{jl\_cap}}}^{\Sigma}$ are the output voltage of the total SMs in the upper arm the lower arm of phase j, respectively.

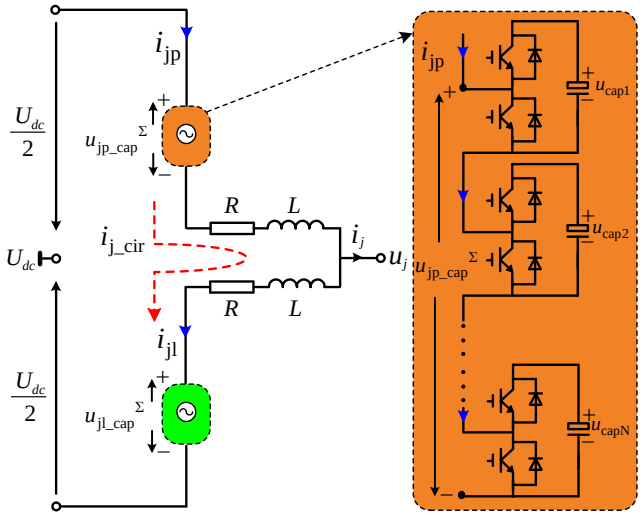

Figure 2. Single-phase equivalent circuit of the three-phase MMC.

Meanwhile, the upper arm the lower arm currents i_{jp}, i_{jl} can be expressed as [17]:

$$\begin{cases} i_{\mathrm{jp}} = \frac{1}{2}i_{\mathrm{j}} + i_{\mathrm{j\_cir}} \\ i_{\mathrm{jl}} = -\frac{1}{2}i_{\mathrm{j}} + i_{\mathrm{j\_cir}} \end{cases} \tag{3}$$

where i_{j} is the converter-side AC current of phase j. $i_{\mathrm{j\_cir}}$ is the inner unbalanced current of phase j, which is defined the circulating current. It consists of two parts as shown in Equation (4). One part is the AC component i_{jz}; and the other part is the DC component I_{jd}.

$$i_{\mathrm{j\_cir}} = i_{\mathrm{jz}} + I_{\mathrm{jd}} \tag{4}$$

Combining Equations (1) and (2) with Equations (3) and (4), the relationship of circulating current i_{j_cir} with the total SMs output voltage of the upper arm ${u_{jp\_cap}}^{\Sigma}$, the total SM output voltage of the lower arm ${u_{jl\_cap}}^{\Sigma}$ and the DC bus voltage U_{dc} of phase j can be obtained:

$$L\frac{di_{j\_cir}}{dt} = -\frac{1}{2}({u_{jp\_cap}}^{\Sigma} + {u_{jp\_cap}}^{\Sigma}) + \frac{1}{2}U_{dc} - Ri_{j\_cir} \tag{5}$$

3.2. Mathematical Mode under SM Faults

With the hot reserve scheme "ii-b" redundant mode, the faulty SMs are only bypassed when SMs malfunction. Though the reduced number of healthy SMs would cause the capacitor voltage be changed in the faulty arms, the SMs in the same arm also can operate with the same capacitor voltage with the voltage balancing control [14]. They can be expressed as:

$$\begin{cases} u_{jp\_cap} = \frac{1}{C}\int i_{jp}\frac{1-S_j}{2}dt \\ u_{jl\_cap} = \frac{1}{C}\int i_{jl}\frac{1+S_j}{2}dt \end{cases} \tag{6}$$

where u_{jp_cap} and u_{jl_cap} are the capacitor voltage in the upper arm and the lower arm of phase j, respectively. S_j denotes the modulation function of phase j.

Assuming the converter-side AC voltage u_j and the converter-side AC current i_j are purely sinusoidal and only considering the second harmonic component in the circulating current i_{jz} in the initial, the following equations can be obtained:

$$S_j = m\sin(\omega t + \varphi_j) \tag{7}$$

$$\begin{cases} i_{jp} = \frac{1}{2}I_j\sin(\omega t + \theta_j) + I_{jd} + I_{jz}\sin(2\omega t + \theta_{jz}) \\ i_{jn} = -\frac{1}{2}I_j\sin(\omega t + \theta_j) + I_{jd} + I_{jz}\sin(2\omega t + \theta_{jz}) \end{cases} \tag{8}$$

where m and ω are the modulation index and fundamental angle frequency, respectively. I_j and I_{jz} are the amplitude of i_j and i_{jz}, respectively. φ_j, θ_j, and θ_{jz} are the phase angle of S_j, i_j and i_{jz}, respectively.

For easy to analysis, it is assumed that the number of the faulty SMs in the upper arm and in the lower arm of phase j are n_{jp_fault} and n_{jl_fault}, respectively. When the faulty SMs are bypassed, the total SMs output voltage in the upper arm ${u_{jp\_cap}}^{\Sigma}$ and the lower arm ${u_{jl\_cap}}^{\Sigma}$, as shown in Figure 2, can be expressed as:

$$\begin{cases} {u_{jp\_cap}}^{\Sigma} = \frac{1-S_j}{2}(n + n_m - n_{jp\_fault})u_{jp\_cap} \\ {u_{jl\_cap}}^{\Sigma} = \frac{1+S_j}{2}(n + n_m - n_{jl\_fault})u_{jl\_cap} \end{cases} \tag{9}$$

Substituting Equations (6)–(8) into Equation (9) and summating the AC components in the ${u_{jp\_cap}}^{\Sigma}$ and ${u_{jl\_cap}}^{\Sigma}$, then the follow equations can be obtained:

$$\begin{cases} \Delta{u_{jp\_cap}}^{\Sigma} = \frac{C}{2(n+n_m-n_{jp\_fault})}(f_1 + f_2 + f_3 + f_4) \\ \Delta{u_{jl\_cap}}^{\Sigma} = \frac{C}{2(n+n_m-n_{jl\_fault})}(g_1 + g_2 + g_3 + g_4) \end{cases} \tag{10}$$

with

$$\begin{cases} f_1 = \frac{m}{2\omega}I_{jd}\cos(\omega t + \varphi_j) - \frac{8+m^2}{32\omega}I_j\cos(\omega t + \theta_j) + \frac{3m}{8\omega}I_{jz}\cos(\omega t + \theta_{jz} - \varphi_j) \\ f_2 = -\frac{m^2}{4\omega}I_{jd}\sin(2\omega t + \varphi_j + \theta_j) + \frac{3m}{16\omega}I_j\sin(2\omega t + \varphi_j + \theta_j) - \frac{3-m^2}{12\omega}I_{jz}\cos(2\omega t + \theta_{jz}) \\ f_3 = \frac{m^2}{32\omega}I_j\cos(3\omega t + 2\varphi_j + \theta_j) + \frac{5m}{24\omega}I_{jz}\sin(3\omega t + \varphi_j + \theta_{jz}) \\ f_4 = \frac{m^2}{24\omega}I_{jz}\cos(4\omega t + 2\varphi_j + +\theta_{jz}) \end{cases} \tag{11}$$

$$\begin{cases} g_1 = -\frac{m}{2\omega} I_{\mathrm{jd}} \cos(\omega t + \varphi_{\mathrm{j}}) + \frac{8+m^2}{32\omega} I_{\mathrm{j}} \cos(\omega t + \theta_{\mathrm{j}}) - \frac{3m}{8\omega} I_{\mathrm{jz}} \cos(\omega t + \theta_{\mathrm{jz}} - \varphi_{\mathrm{j}}) \\ g_2 = -\frac{m^2}{4\omega} I_{\mathrm{jd}} \sin(2\omega t + \varphi_{\mathrm{j}} + \theta_{\mathrm{j}}) + \frac{3m}{16\omega} I_{\mathrm{j}} \sin(2\omega t + \varphi_{\mathrm{j}} + \theta_{\mathrm{j}}) - \frac{3-m^2}{12\omega} I_{\mathrm{jz}} \cos(2\omega t + \theta_{\mathrm{jz}}) \\ g_3 = -\frac{m^2}{32\omega} I_{\mathrm{j}} \cos(3\omega t + 2\varphi_{\mathrm{j}} + \theta_{\mathrm{j}}) - \frac{5m}{24\omega} I_{\mathrm{jz}} \sin(3\omega t + \varphi_{\mathrm{j}} + \theta_{\mathrm{jz}}) \\ g_4 = \frac{m^2}{24\omega} I_{\mathrm{jz}} \cos(4\omega t + 2\varphi_{\mathrm{j}} + +\theta_{\mathrm{jz}}) \end{cases} \tag{12}$$

where $\Delta u_{\mathrm{jp\_cap}}{}^{\Sigma}$ and $\Delta u_{\mathrm{jl\_cap}}{}^{\Sigma}$ are the AC components of the total SMs output voltage in the upper arm and the lower arm, respectively. To facilitate the writing and expression, $f_1 - f_4$ are defined to replace the different components in $\Delta u_{\mathrm{jp\_cap}}{}^{\Sigma}$ and $g_1 - g_4$ are defined to represent the different components in $\Delta u_{\mathrm{jl\_cap}}{}^{\Sigma}$.

Contrasting Equations (11) and (12), it can be seen that $f_1 = -g_1$; $f_2 = g_2$; $f_3 = -g_3$; $f_4 = g_4$. Therefore, the total AC components of the total SMs output voltage in the phase j can be written as:

$$\Delta u_{\mathrm{j}}{}^{\Sigma} = (\Delta u_{\mathrm{jp\_cap}}{}^{\Sigma} + \Delta u_{\mathrm{jl\_cap}}{}^{\Sigma}) = \kappa_{\mathrm{j}}(f_1 + f_3) + \mu_{\mathrm{j}}(f_2 + f_4) \tag{13}$$

with

$$\begin{cases} \kappa_{\mathrm{j}} = \frac{C}{2}\left(\frac{1}{n+n_{\mathrm{m}}-n_{\mathrm{jp\_fault}}} - \frac{1}{n+n_{\mathrm{m}}-n_{\mathrm{jl\_fault}}}\right) \\ \mu_{\mathrm{j}} = \frac{C}{2}\left(\frac{1}{n+n_{\mathrm{m}}-n_{\mathrm{jp\_fault}}} + \frac{1}{n+n_{\mathrm{m}}-n_{\mathrm{jl\_fault}}}\right) \end{cases} \tag{14}$$

where κ_{j} and μ_{j} are defined as the coefficients about the fault SM numbers in the upper arm and the lower arm of phase j, respectively.

3.3. Summarizing of the Circulting Current Characteristic under SM Faults

Substituting Equations (13) and (14) into Equation (5), it can be observed that total AC components $\Delta u_{\mathrm{j}}{}^{\Sigma}$ of the total SMs output voltage in phase j would generate fluctuating current through the arm inductor L_{m}, which is the main reason for the circulating current's generation. Thus, the harmonic components of the circulating current under SM faults can be indirectly analyzed by the fluctuating voltage $\Delta u_{\mathrm{j}}{}^{\Sigma}$. Based on Equations (13) and (14), the following conclusions can be obtained:

1. Three-phase with symmetrical fault, which means: Condition 1a, $\kappa_{\mathrm{a}} = \kappa_{\mathrm{b}} = \kappa_{\mathrm{c}} = 0$; and Condition 1b, $\mu_{\mathrm{a}} = \mu_{\mathrm{b}} = \mu_{\mathrm{c}} \neq 0$. The harmonic components of the circulating current in this fault situation are actually the same as the normal operation situation. It only consists of even-order frequency components, which are negative-sequence symmetrical. As the higher-order contents are very small, the twice frequency component is the mainly. This conclusion also can explain the main characteristics of the circulating current of MMC under the normal operation state, which is consistent with the conclusion in [17].
2. Single-phase with symmetrical fault, which means: Condition 2a, the $\kappa_{\mathrm{a}} = \kappa_{\mathrm{b}} = \kappa_{\mathrm{c}} = 0$; and Condition 2b, μ_{a}, μ_{b}, μ_{c} are not exactly equal (because the fault SMs cause the factor μ of the fault phase not equaling to the normal phase). In this fault situation, the harmonics of the circulating current are also only included by even-orders restricted by the Condition 2a, and the twice frequency component is the main part. However, owing to Condition 2b, the even-order frequency components will no longer be negative-sequenced symmetrically.
3. Single-phase with asymmetrical fault, which means: Condition 3a, the κ_{a}, κ_{b}, κ_{c} are not exactly equal to 0 (because the different number of faulty SMs in the upper arm and the lower arm cause the factor κ of the fault phase not equaling 0); and Condition 3b, μ_{a}, μ_{b}, μ_{c} are not exactly equal. The odd-order harmonics will appear in the circulating current besides the even-order harmonics during this fault situation as the Condition 3a. In addition, the even-order frequency components will also no longer be negative-sequenced symmetrically owing to the Condition 3b. Similarly, the fundamental and twice frequency components are the main parts of the even- and odd-order frequency components, respectively.

4. Multi-phase with symmetrical/asymmetrical fault. As analyzed previously, the conditions about κ_a, κ_b, κ_c and μ_a, μ_b, μ_c can be obtained in the same way at first. Then, the harmonic characteristics of the circulating current can be concluded based on the conditions. They are basically the same as the single-phase symmetrical/asymmetrical faults, which are not repeated here.

Concluding the analysis of the above, it can be observed that if the healthy SM numbers are not equal in each arm after SM malfunction, the total SM output voltage's AC components in the upper arm $\Delta u_{jp\_cap}{}^{\Sigma}$ and the lower arm $\Delta u_{jl\_cap}{}^{\Sigma}$ will not be balanced anymore. It will induce asymmetrical circulating current, which will be included by the odd- and even-order frequency components. The fundamental and twice frequency components are respectively the main parts. These changes in the circulating current would affect the performance of the MMC. Therefore, in order to enhance the fault-tolerant ability for the MMC, the circulating current-suppressing controller, except for the consideration of the suppression of the inherent the negative-sequence twice frequency component, should have the ability to suppress the asymmetric twice frequency. The fundamental frequency components may be generated by the SM faults.

4. Fault-Tolerant Control of Circulating Current Suppressing Strategy for MMC

4.1. Anysis of the Nonideal PR Control Mode

Combining the analysis in Section 3.3, it can be observed that in order to ensure the suppressing effect for the circulating current continuously when SM faults occur, the fault-tolerant controller should consider the suppression of the symmetrical twice frequency component, the asymmetrical twice frequency component and the fundamental frequency component synchronously, based on the following considerations:

1. During normal situations, a PR-based control strategy is often adopted in the traditional CCS control method [17,20,21]. It mainly has two modes, ideal PR and non-ideal PR. However, the ideal PR controller only tends to infinite magnitude at the resonant frequency, which will result in its performance being greatly reduced when the grid frequency fluctuates. Therefore, most PR controllers consider adopting a non-ideal PR control mode since it can reduce the sensibility to the frequency deviation. The transfer function of a non-ideal PR controller can be expressed as:
$$G(s) = k_p + k_r \frac{s}{s^2 + 2\omega_c s + \omega_0^2} \tag{15}$$
where k_p, k_r, ω_c, and ω_0 are the proportional gain, resonant gain, cutoff frequency, and resonant frequency, respectively.
2. Compared to the fault-tolerant control method based on a PI controller [13], the suppressing strategy based on a PR controller can achieve the independent control of each phase. In addition, it can avoid the *acb-dq* decoupling control. This would ensure the control effect when the three-phase alternative circulating currents appear asymmetrical. Meanwhile, it reduces the positive-, negative-, and zero-sequence controllers, which is more concise.
3. Furthermore, in order to achieve the suppression for the fundamental frequency component, it only needs to introduce a fundamental frequency resonant controller into the traditional PR control system, which can reduce the design burden of the whole control system.

It can be seen that non-ideal PR control mode shows obvious advantages in the circulating current suppressing fault-tolerant control fields under SM faults. It can simultaneously achieve the suppression of multi-different frequency components of the circulating current under different SM fault types and is easy to realize.

4.2. Fault-Tolerant Controller Design

According to the analysis in previous section, the basic control unit (BCU) based on non-ideal PR mode of the CCS fault-tolerant controller is designed in the first step, which is used for suppressing the fundamental frequency component, symmetrical twice frequency component, and asymmetrical twice frequency component. As shown in Figure 3a, in the BCU, a fundamental frequency non-ideal resonant controller, is introduced into the traditional non-ideal PR-based CCS control system [21] to suppress the fundamental frequency component, and a filter link based on low-pass filter (LPF) is used to extract the multi-different harmonic components of the circulating current. However, it should be noticed that when the SM incurred faults and bypassed the arm, it would result in a transient impact on the system. This causes a large fault circulating current and it may result in more serious failures if it cannot be limited quickly. Therefore, accelerating the response speed of the fault-tolerant controller at the sub-module faulting time will help fast limiting of the fault current and reduction of its harm to the system. Figure 3b shows the equivalent closed-loop control model of BCU of the fault-tolerant controller. From it, the closed-loop transfer function of the BCU can be obtained as:

$$G_{\mathrm{B}}(s) = \frac{\beta_1 s^4 + \beta_2 s^3 + \beta_3 s^2 + \beta_4 s + \beta_5}{\alpha_1 s^5 + \alpha_2 s^4 + \alpha_3 s^3 + \alpha_4 s^2 + \alpha_5 s + \alpha_6} \tag{16}$$

with

$$\begin{cases} \beta_1 = k_{\mathrm{p}} \\ \beta_2 = 4\omega_{\mathrm{c}} k_{\mathrm{p}} \\ \beta_3 = k_{\mathrm{r1}} + k_{\mathrm{r2}} + (4\omega_{\mathrm{c}}^2 + 5\omega_0^2) k_{\mathrm{p}} \\ \beta_4 = 2\omega_{\mathrm{c}}(k_{\mathrm{r1}} + k_{\mathrm{r2}}) + 10\omega_{\mathrm{c}}\omega_0^2 k_{\mathrm{p}} \\ \beta_5 = 4\omega_0^2 k_{\mathrm{r1}} + \omega_0^2 k_{\mathrm{r2}} + 4\omega_0^4 k_{\mathrm{p}} \end{cases} \tag{17}$$

$$\begin{cases} \alpha_1 = L \\ \alpha_2 = k_{\mathrm{p}} + R + 4\omega_{\mathrm{c}} L \\ \alpha_3 = 4\omega_{\mathrm{c}}(k_{\mathrm{p}} + R) + (4\omega_{\mathrm{c}}^2 + 5\omega_0^2) L \\ \alpha_4 = k_{\mathrm{r1}} + k_{\mathrm{r2}} + (4\omega_{\mathrm{c}}^2 + 5\omega_0^2)(k_{\mathrm{p}} + R) + 10\omega_{\mathrm{c}}\omega_0^2 L \\ \alpha_5 = 2\omega_{\mathrm{c}}(k_{\mathrm{r1}} + k_{\mathrm{r2}}) + 10\omega_{\mathrm{c}}\omega^2(k_{\mathrm{p}} + R) + 4\omega_0^4 L \\ \alpha_6 = 4\omega_0^2 k_{\mathrm{r1}} + \omega_0^2 k_{\mathrm{r2}} + 4\omega_0^4 (k_{\mathrm{p}} + R) \end{cases} \tag{18}$$

where k_{r1}, k_{r2} are the resonant gain of the fundamental and twice frequency resonant controller, respectively.

Owing to the response time of the control system primarily depending on the position of the closed-loop poles, in order to fast limit the fault circulating current we can consider improving the performance of the controller by adjusting the nature of the closed-loop poles without affecting the closed-loop zeros of the system. Combining Equation (16), this can be achieved through adjusting the value of R or L in the denominator. However, in the actual event, R is often limited to a small number for reducing the system losses, and L is also often selected with the determination of system parameters. Therefore, in order to essentially improve the performance of the fault-tolerant controller, it should be realized through other additional control methods.

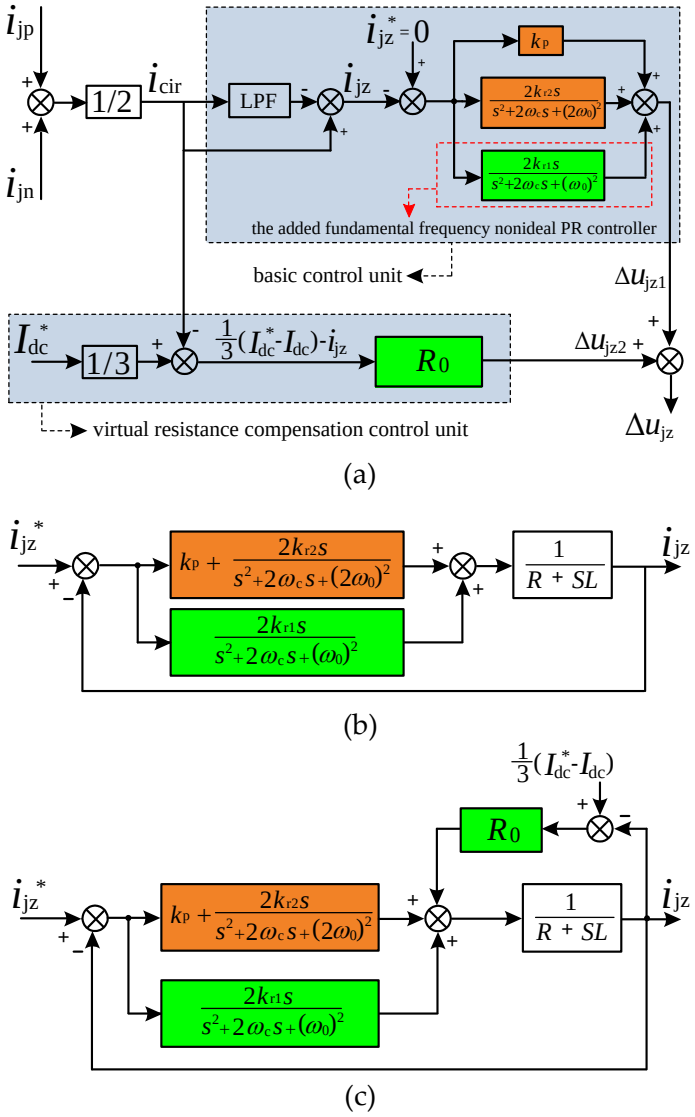

Figure 3. Schematic diagram of the circulating current suppressing fault-tolerant controller for the MMC under SM faults: (**a**) diagram of fault-tolerant control system; (**b**) equivalent closed-loop control model of the BCU; (**c**) equivalent closed-loop control model of the overall fault-tolerant controller.

To solve this problem, a virtual resistance compensation control unit (VRCCU) is designed and introduced into the BCU, and finally the proposed circulating current suppressing fault-tolerant controller for the MMC under SM faults is obtained, which is shown in Figure 3a. The VRCCU is only composed of a proportional controller, whose proportional gain R_0 is defined as the value of the virtual resistance. In addition, the DC-link current reference value $I_{dc}{}^*$ can be obtained from $I_{dc}{}^* = (P_{ref} + Q_{ref})/U_{dc}$, where P_{ref}, Q_{ref} are the active power and reactive power reference values, respectively. In the same way, the equivalent closed-loop control model of the whole fault-tolerant controller can be obtained as Figure 3c. From it, the closed-loop transfer function of it can be expressed as Equation (19). By contrasting Equations (16)–(18) with Equations (19)–(21), it can be seen that β_i is equal to γ_i (i = 1, 2, 3, 4, 5); but α_i compared to λ_i, R in α_i is changed to $(R + R_0)$ in the λ_i. Figure 4 shows the step response

of the closed-loop transfer function $G_{BF}(s)$ by controlling R_0 as a variable. It can be observed that with the increase of R_0, the response speed of the system is accelerated.

$$G_{BF}(s) = \frac{\gamma_1 s^4 + \gamma_2 s^3 + \gamma_3 s^2 + \gamma_4 s + \gamma_5}{\lambda_1 s^5 + \lambda_2 s^4 + \lambda_3 s^3 + \lambda_4 s^2 + \lambda_5 s + \lambda_6} \tag{19}$$

with

$$\begin{cases} \gamma_1 = k_p \\ \gamma_2 = 4\omega_c k_p \\ \gamma_3 = k_{r1} + k_{r2} + (4\omega_c^2 + 5\omega_0^2)k_p \\ \gamma_4 = 2\omega_c(k_{r1} + k_{r2}) + 10\omega_c\omega_0^2 k_p \\ \gamma_5 = 4\omega_0^2 k_{r1} + \omega_0^2 k_{r2} + 4\omega_0^4 k_p \end{cases} \tag{20}$$

$$\begin{cases} \lambda_1 = L \\ \lambda_2 = k_p + (R_0 + R) + 4\omega_c L \\ \lambda_3 = 4\omega_c(k_p + R_0 + R) + (4\omega_c^2 + 5\omega^2)L \\ \lambda_4 = k_{r1} + k_{r2} + (4\omega_c^2 + 5\omega^2)(k_p + R_0 + R) + 10\omega_c\omega^2 L \\ \lambda_5 = 2\omega_c(k_{r1} + k_{r2}) + 10\omega_c\omega^2(k_p + R_0 + R) + 4\omega^4 L \\ \lambda_6 = 4\omega^2 k_{r1} + \omega^2 k_{r2} + 4\omega^4(k_p + R_0 + R) \end{cases} \tag{21}$$

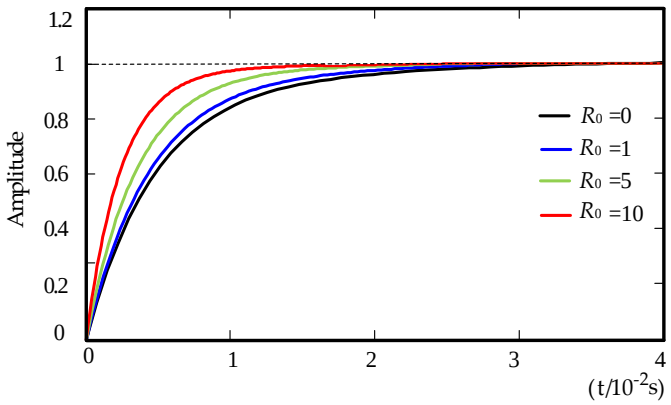

Figure 4. Step response of the closed-loop transfer function G_{BF} (s).

In addition, under the premise of the other parameters of the system being determined, the root locus of the system with different virtual resistance R_0 and different resonant gain k_{r1}, k_{r2} can be obtained by the control variable method, respectively, where Figure 5a shows the root locus of the system with different R_0, Figure 5b shows the root locus of the system with different k_{r1} and k_{r2}. From Figure 5a, it can be seen that with the increase of R_0, the system-dominated poles gradually close in on the imaginary axis, which indicates that the dynamic response speed of the system is accelerated. From Figure 5b, it can be seen that when the resonant gain increases, the system-dominated poles also gradually close in on the imaginary axis, but at the same time the stability of the system would be worse. Based on these conclusions, it can be concluded that with the introduction of the VRCCU, the response speed of the whole fault-tolerant controller can be accelerated by appropriately increasing the R_0 value; and then appropriately reducing the resonant gain k_{r1}, k_{r2} to ensure the stability of the control system.

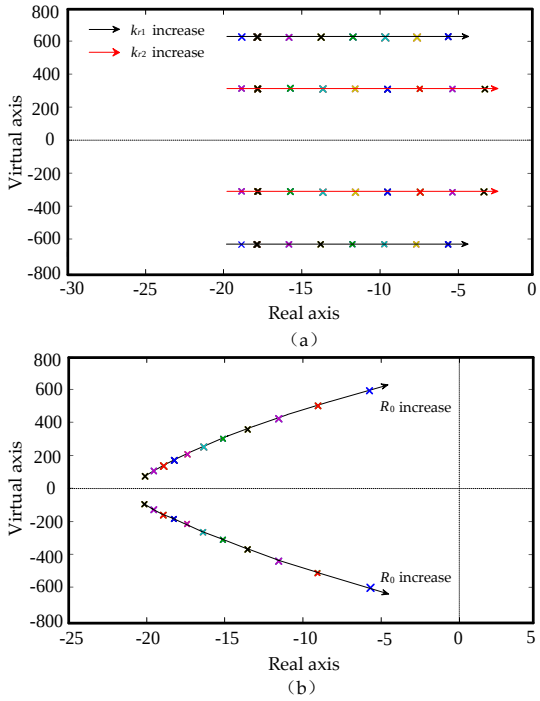

Figure 5. The root locus of the system: (**a**) Root locus with different R_0; (**b**) Root locus with different k_{r1} and k_{r2}.

4.3. System Control Structure

The overall control system of MMC with the fault-tolerant controller is shown in Figure 6. The three-phase reference voltage v_j^* (j = a, b, c) is produced by adopting the traditional vector control method [13]. For realizing fault-tolerant control of the MMC, the correction amount Δu_{jz} generated by the proposed CCS fault-tolerant controller, can be added to the modulation waves for the upper and lower arms of phase j in the opposite direction.

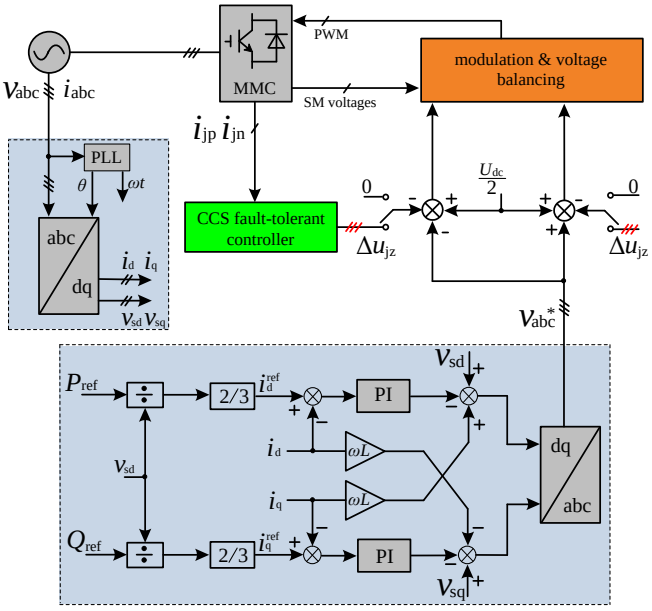

Figure 6. Schematic diagram of the overall control system with the fault-tolerant controller.

5. Simulation Results

To confirm the proposed fault-tolerant control strategy, the MMC system as shown in Figure 1 is established in MATLAB/SIMULINK. The system parameters are shown in Table 1. In the simulation model, the modulation is based on nearest level control [22], and SM capacitor voltages balancing control is based on sorting algorithm [14].

Table 1. Main parameters of the simulation system.

Parameters	Value
Ac system nominal voltage	10 kV
Ac System inductance L_s	5 mH
Fundamental frequency	50 Hz
Ac system power losses R_s	0.03 Ω
Arm inductance L_m	5 mH
Series arm resistance R_m	0.01 Ω
Dc bus voltage U_{dc}	20 kV
Number of SMs per arm N	20
Number of redundant SMs per arm n_m	5
Sub-module capacitor C	2000 μF
Transformer ratio	1:1 (Y/Δ)

5.1. Case 1

In this case, the simulation conditions are as follows: the traditional non-ideal PR-based CCS controller is initially applied in the normal operation state; at 0.2 s, five SMs in the upper and the lower arms of phase a are respectively bypassed.

The performance of the MMC in this case is shown in Figure 7. It can be seen that the MMC is operating with a good performance during the normal operation state. When the SM occurring faults are bypassed from the fault arm at 0.2 s, the capacitor voltage of the rest of the healthy SMs in the upper arm and lower arm of phase a are increased by 33%, as shown in Figure 7a. By contrast, the capacitor voltages in phase b and c are continuously operating with the initial value because of no faulty SMs, as shown in Figure 7b,c. The arm current and circulating current of phase a are shown in Figure 7d,e, respectively. It can be observed that except for a transient fault current caused in the fault arm at SM faulting time, the circulating current can be continuously suppressed by the traditional circulating current controller during the fault operation state. This result also can illustrate that the twice frequency component is always the only and main component of the circulating current under this fault case, which is consistent with the conclusions in Section 3.3. Compared to the fault phase (phase a), the circulating currents of phases b and c with no faulty SMs are affected slightly, as shown in Figure 7f,g. In addition, the AC current and DC-link current of the system are shown in Figure 7h,i, respectively. They all can maintain a stable output, except for a transient performance at the faulting time.

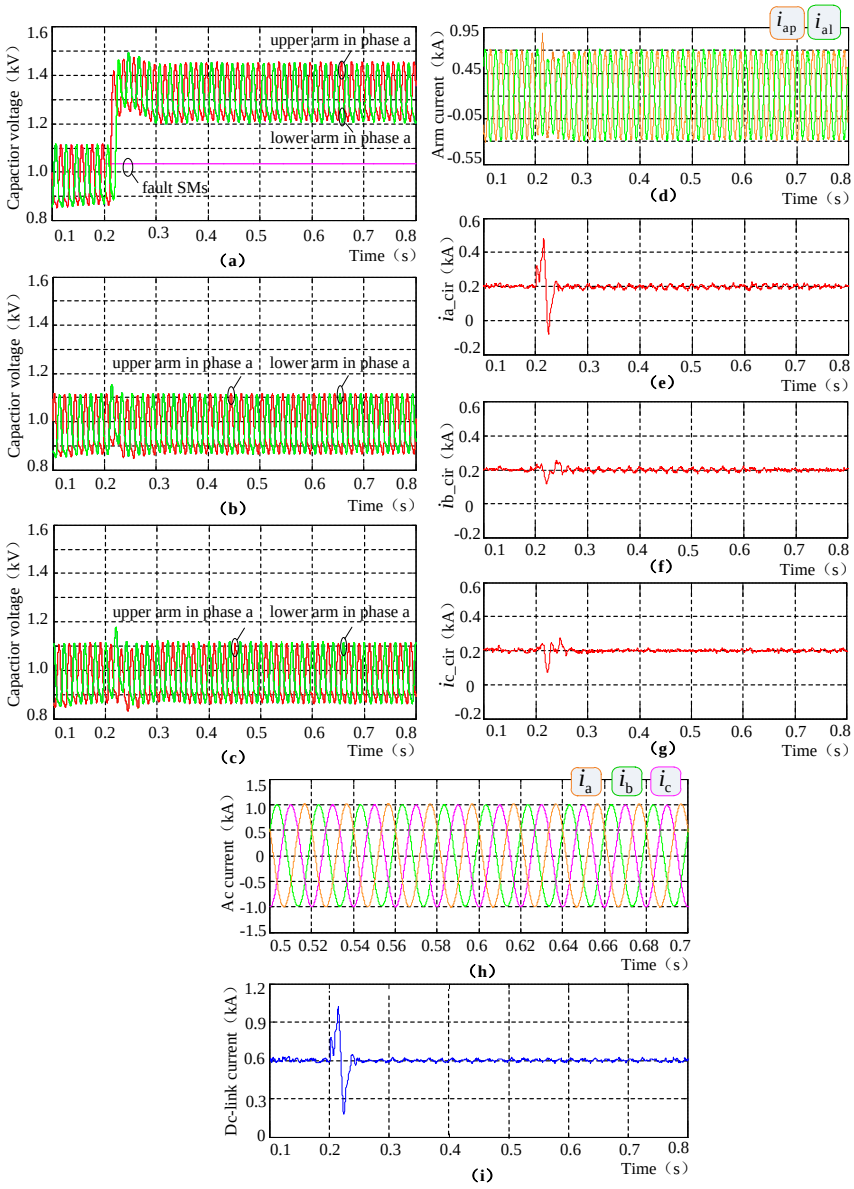

Figure 7. Simulation results under single-phase symmetrical fault: (**a**) capacitor voltage of phase a; (**b**) capacitor voltage of phase b; (**c**) capacitor voltage of phase c; (**d**) arm current of phase a; (**e**) circulating current of phase a; (**f**) circulating current of phase b; (**g**) circulating current of phase c; (**h**) AC current; (**i**) DC-link current.

5.2. Case 2

In this case, the simulation conditions are as follows: the traditional non-ideal PR-based CCS controller is initially applied in the normal operation state; at 0.2 s, only five SMs in the upper arm of phase a are bypassed; at 0.6 s, the whole BCU control part is enabled.

The performance of the MMC in this case is shown in Figure 8. Similarly, the MMC is operating with good performance during the normal operation state. When the SM incurs faults and is bypassed from the fault arm at 0.2 s, only the upper arm capacitor voltage of phase a is increased by 33%, as shown in Figure 8a–c. There is also a transient fault current caused in the fault arm at the faulting time. However, unlike the single-phase asymmetrical fault case, if there is only a traditional circulating current controller under this case, a fundamental component is additionally caused in the circulating current of fault phase (phase a), owing to the different number of healthy SMs in the upper arm and

the lower arm, as shown in Figure 8d,e. Furthermore, the caused fundamental component of the circulating current in the fault phase would result in the fluctuation of the DC-link current, as shown in Figure 8i. However, when the whole BCU part is enabled at 0.6 s, the ripple of the circulating current and DC-link current are all eliminated immediately, as shown in Figure 8e,i. Besides, combining all the simulation results shown in Figure 8 shows that the MMC system can still maintain stable operation after the BCU part is adopted.

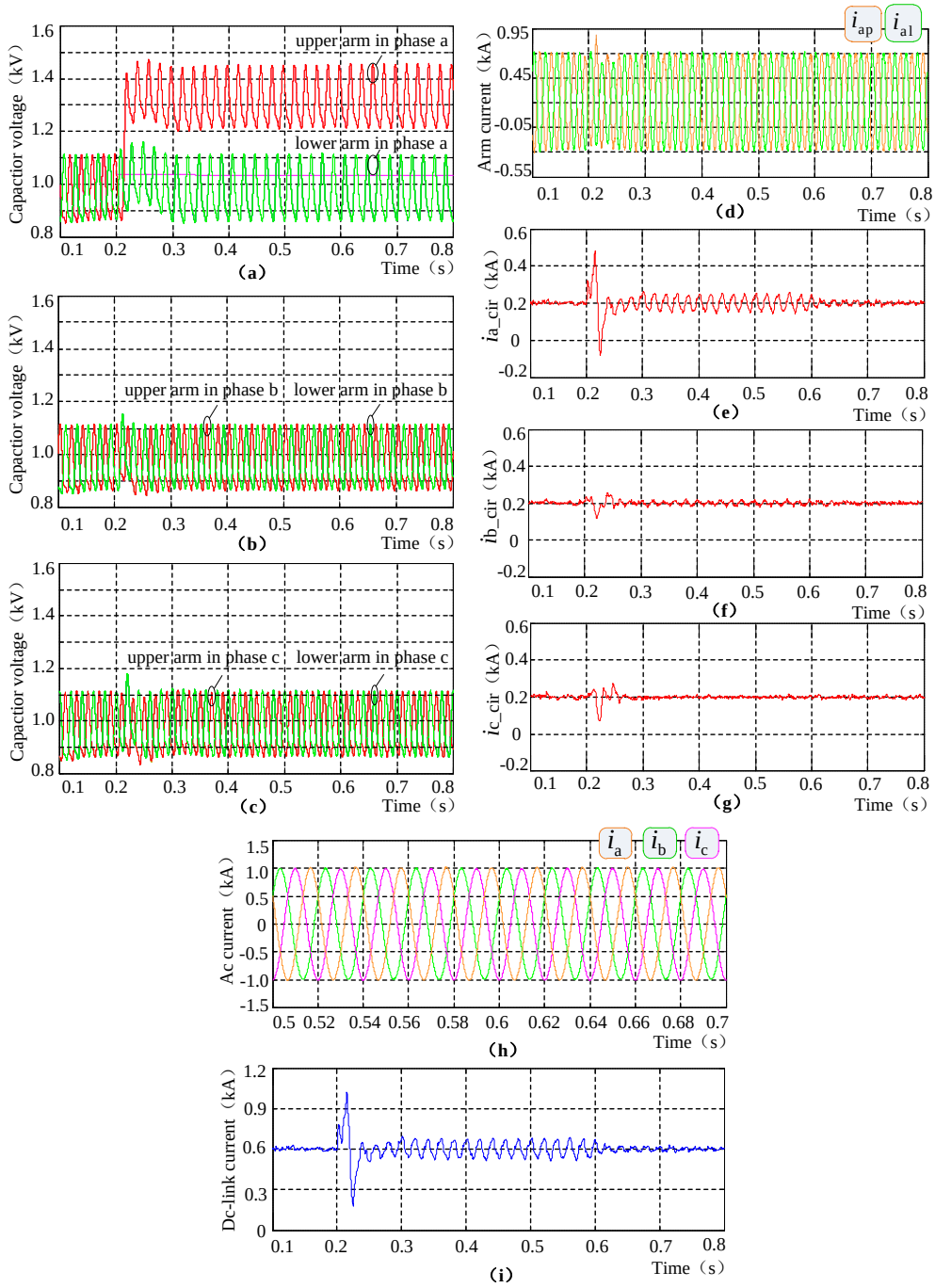

Figure 8. Simulation results under single-phase asymmetrical fault: (**a**) capacitor voltage of phase a; (**b**) capacitor voltage of phase b; (**c**) capacitor voltage of phase c; (**d**) arm current of phase a; (**e**) circulating current of phase a; (**f**) circulating current of phase b; (**g**) circulating current of phase c; (**h**) AC current; (**i**) DC-link current.

5.3. Case 3

In this case, the simulation conditions are as follows: the traditional non-ideal PR-based CCS controller is initially applied in the normal operation state; at 0.2 s, five SMs in the lower arm of phase b and in the upper arm of phase a, c are respectively bypassed; at 0.6 s, the whole BCU control part is enabled.

The performance of the MMC in this case is shown in Figure 9. The capacitor voltage of phase a, b, and c are shown in Figure 9a–c, respectively. They are fluctuating smoothly during the normal operation state. When the faulty SMs bypassed at 0.2 s, capacitor voltage in the faulty arms are increased by 33%. Figure 9d,e show the circulating current in phases a, b, and c. Similarly, the transient fault currents and fundamental frequency fluctuations are caused in every fault phase after SMs malfunction. However, the fluctuations are all suppressed when the BCU control part is enabled at 0.6 s. In addition, the AC current and DC-link current of the system also maintain a stable output after the BCU control part is enabled, as shown in Figure 9g,h, respectively.

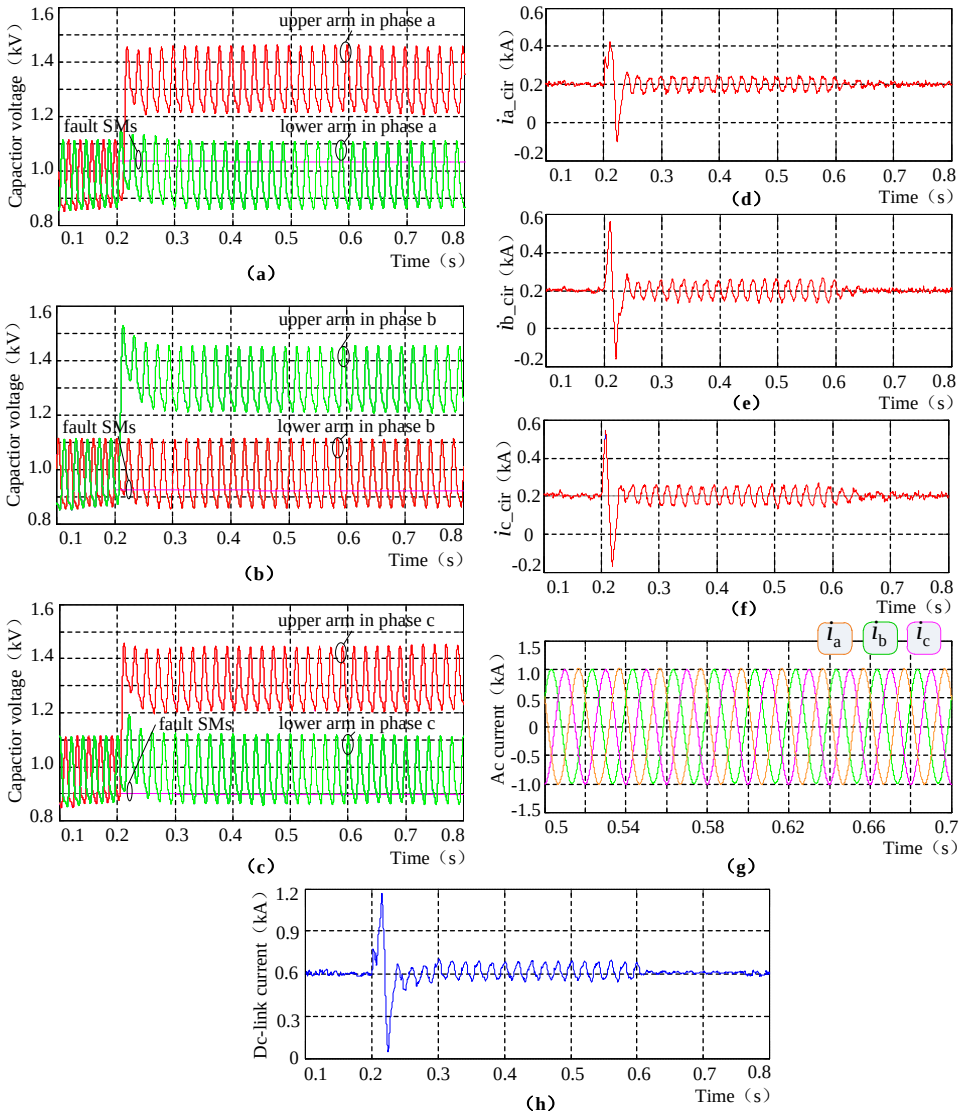

Figure 9. Simulation results under three-phase asymmetrical fault: (**a**) capacitor voltage of phase a; (**b**) capacitor voltage of phase b; (**c**) capacitor voltage of phase c; (**d**) circulating current of phase a; (**e**) circulating current of phase b; (**f**) circulating current of phase c; (**g**) AC current; (**h**) DC-link current.

5.4. Case 4

Combining the simulation results in Sections 5.1–5.3 shows that the fundamental frequency fluctuation will be caused in the circulating current if the upper arm and the lower arm are operating asymmetrically. It will affect the stable operation of MMC system. This phenomenon is consistent with the conclusions in Section 3.3. However, with the control of BCU, the fundamental component is effectively suppressed and the performance of the MMC is improved. Furthermore, in order to verify the efficiency of the VRCCU and the whole circulating current-suppressing fault-tolerant controller, single-phase asymmetrical fault case as the example is further simulated in this section. The simulation conditions are as follows: the fault-tolerant controller is applied in the system at 0.26 s; five SMs in the upper arm of phase a are bypassed at 0.3 s.

The performance of the MMC in this case is shown in Figure 10. The circulating current of phase a with different virtual resistance values are shown in Figure 10a–d, respectively, where Figure 10a is the waveform with R_0 = 0, Figure 10b is the waveform with R_0 = 1, Figure 10c is the waveform with R_0 = 5, Figure 10d is the waveform with R_0 = 10. It can be seen that the twice frequency component in the circulating current during the normal operation state disappears when the circulating current-suppressing fault-tolerant controller is enabled at 0.26 s and the circulating current can be continuously suppressed well after SMs are faulting and bypassed at 0.3 s. In addition, by contrasting the excessive ratio η (where η is defined as $\eta = (i_{\text{cirm}} - i_{\text{cirb}})/i_{\text{cirb}}$, i_{cirm} and i_{cirb} are the peak value of the circulating current at the SMs faulting time and the normal operation state, respectively). Regarding the circulating current at the SMs faulting time, it can be seen that the η keeps decreasing as R_0 grows. In particular, the transient fault current of the circulating current can be almost fully suppressed when R_0 = 10. Under the virtual resistance value R_0 = 10, the arm currents of the fault phase, the DC-link current and the AC current of the system are measured and shown in Figure 10e–g, respectively. They can all maintain a stable output, and the transient fault current in the DC-link current is also effectively suppressed with the fault-tolerant controller.

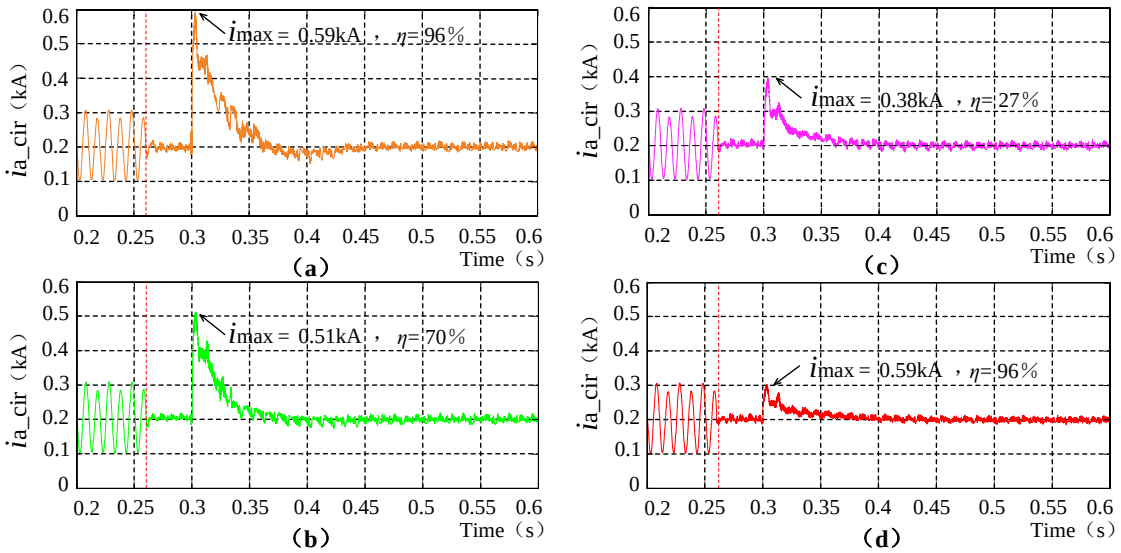

Figure 10. *Cont.*

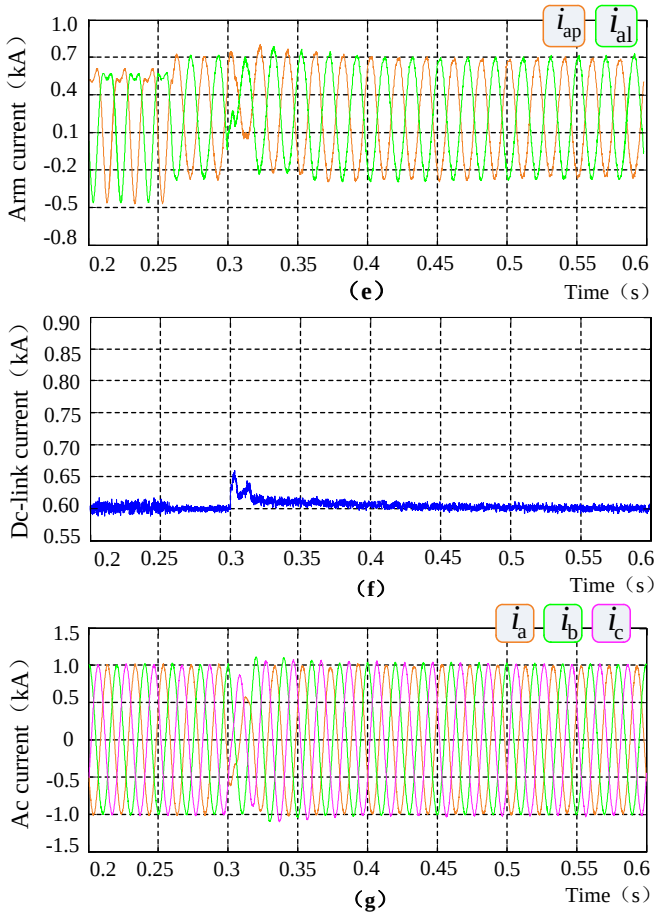

Figure 10. Simulation results about the virtual resistance compensation control: (**a**) circulating current of phase a under R_0 = 0; (**b**) circulating current of phase a under R_0 = 1; (**c**) circulating current of phase a under R_0 = 5; (**d**) circulating current of phase a under R_0 = 10; (**e**) arm current of phase a; (**f**) DC-link current; (**g**) AC current.

6. Experiments

To verify the proposed fault-tolerant control strategy, a MMC prototype as shown in Figure 1 is built. Figure 11 shows the photograph of the prototype. The Mitsubishi PS21765 is used as the switch/diode in each SM, the core unit of the control system is the digital signal processor (DSP) chip 28335, and the pulse signals from the DSP are transferred to each SM by the optical fiber. In addition, the DC bus voltage is provided by the programmable source Chorma61511. The main circuit parameters of the experiment system are shown in Table 2.

Table 2. Main parameters of the experiment system.

Parameters	Value
Dc bus voltage U_{dc}	240 V
Ac System inductance L_s	5 mH
Fundamental frequency	50 Hz
Arm inductance L_m	5 mH
Number of SMs per arm N	4
Number of redundant SMs per arm n_m	1
Sub-module capacitor C	2000 μF
Transformer ratio	1:1 (Y/Δ)

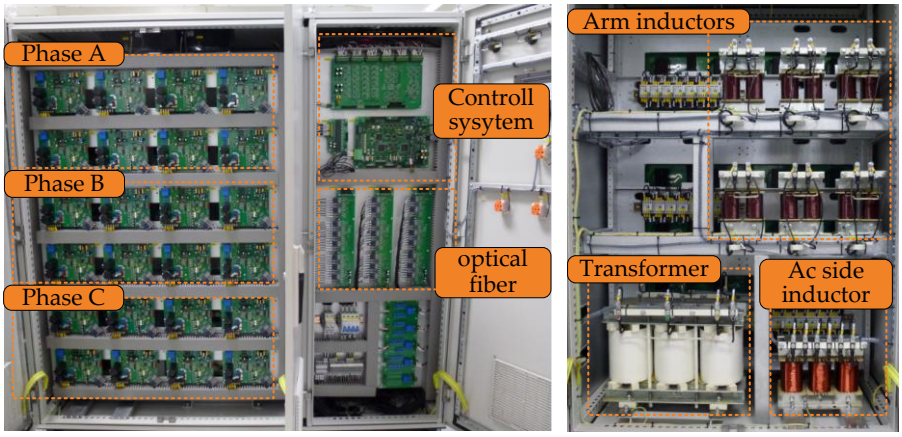

Figure 11. Photograph of the MMC prototype: (**a**) front side of the prototype; (**b**) rear side of the prototype.

6.1. Case 1

In the course of the experiment, single-phase asymmetric fault is taken as an example. The experimental conditions are as follows: the traditional non-ideal PR-based CCS controller is initially applied in the normal operation state; at time t_0, SM_4 in the upper arm of phase a is bypassed; and the whole BCU control part is enabled at time t_1.

The performance of the MMC in this case is shown in Figure 12. It can be seen that the MMC is operating with a good performance before the SM faulting at t_0 moment. When the SM_4 occurring faults and bypassed at t_0 moment, the upper arm capacitor voltage of phase a is increased by 33% (from 60 V to 80 V), as shown in Figure 12e. The arm and circulating currents (the M-channel of the oscilloscope measures the sum of the upper and lower arm currents, then can obtain the twice value of the circulating current) of the fault phase (phase a) and the normal phase (take phase b as an example) are shown in Figure 12a–d, respectively. A transient fault current is caused in the fault arm at the faulting time, and a fundamental frequency fluctuation is additional caused in the circulating current of fault phase, as shown in Figure 12a. However, the arm and circulating current in the normal phase are affected slightly, as shown in Figure 12b. Furthermore, the caused fundamental component of the circulating current in the fault phase would result in the fluctuation of DC-link current, as shown in Figure 12f. However, when the whole BCU control part is enabled at t_1 moment, the ripple of the circulating current and DC-link current are all eliminated immediately, as shown in Figure 12b,g. Besides, it can be seen that the MMC system still maintains stable operation after the BCU control part is enabled.

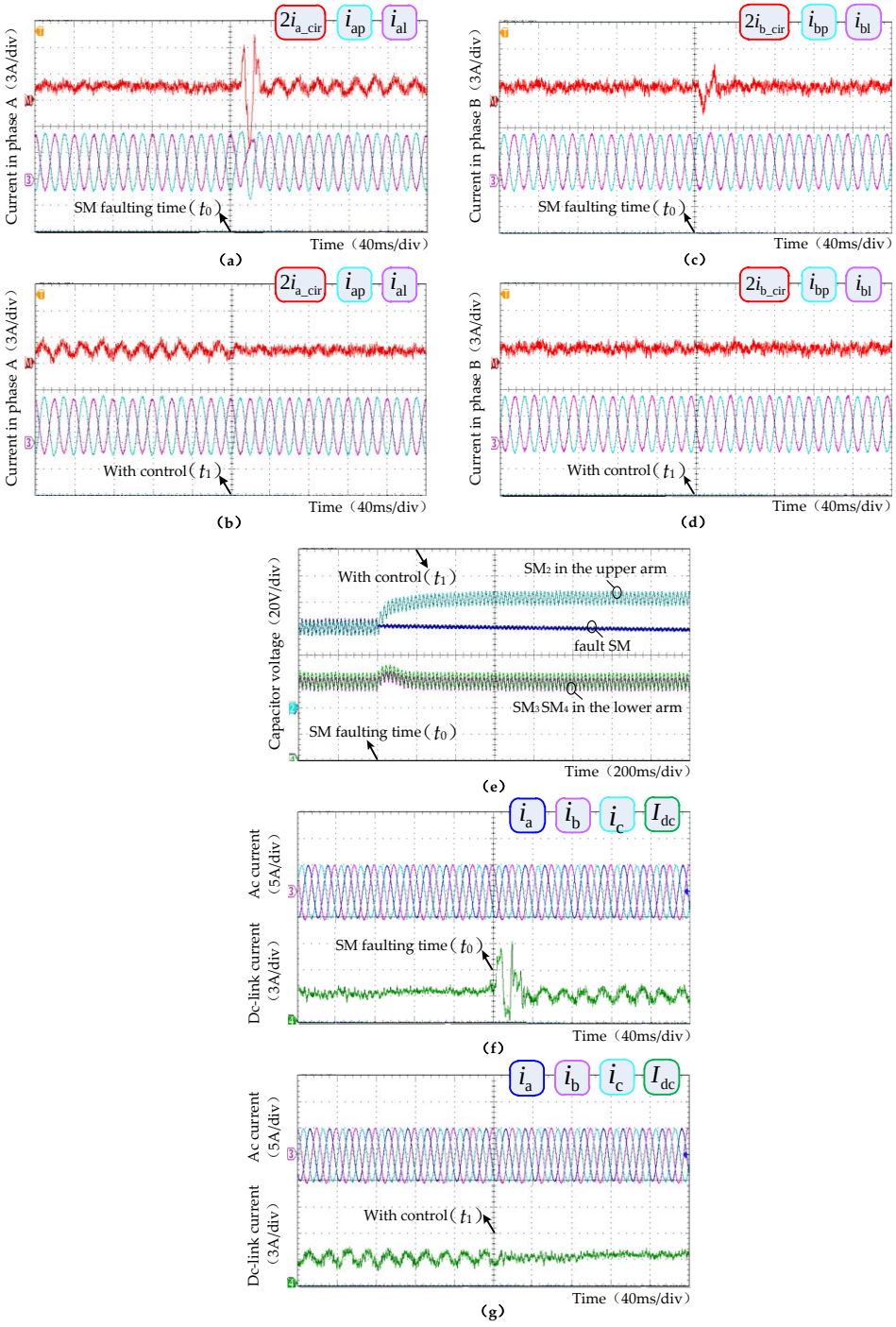

Figure 12. Experiment results about the basic unit control: (**a**) arm and circulating current of phase a under faults; (**b**) arm and circulating current of phase a with control; (**c**) arm and circulating current of phase b under faults; (**d**) arm and circulating current of phase b with control; (**e**) capacitor voltage of phase a; (**f**) AC and DC-link current under faults; (**g**) AC and DC-link current with control.

6.2. Case 2

From Section 6.1, it can be seen that the performance of the MMC with the BCU under prototype environment is basically consistent with the simulation results. Similarly, in order to confirm the efficiency of the VRCCU and the whole circulating current-suppressing fault-tolerant controller under the prototype environment, the single-phase asymmetric fault as an example is further analyzed in

this section. The experimental conditions are as follows: the fault-tolerant controller is applied in the system at time t_2; and SM_4 in the upper arm of phase a is bypassed at time t_3.

The performance of the MMC in this case is shown in Figure 13. The arm operation states of the fault phase with virtual resistance value $R_0 = 0$, $R_0 = 5$ and $R_0 = 10$ are shown in Figure 13a–c, respectively. It can be seen that the twice frequency component in the circulating current during the normal operation state disappears when the circulating current-suppressing fault-tolerant controller is enabled at t_2 moment and the circulating current can be continuously suppressed well after the SM_4 is faulting and bypassed at t_3 moment. In the same way, calculating the excessive ratio η under different virtual resistance value, the results are shown in Table 3. The η keeps decreasing as R_0 grows, and the transient fault current of the circulating current is almost reduced by 119 percent when $R_0 = 10$ compared to when $R_0 = 0$. In addition, the AC and DC-link current of the system are measured and shown in Figure 13d. They can all maintain a stable output, and the transient fault current in the DC-link current is also effectively suppressed with the fault-tolerant controller.

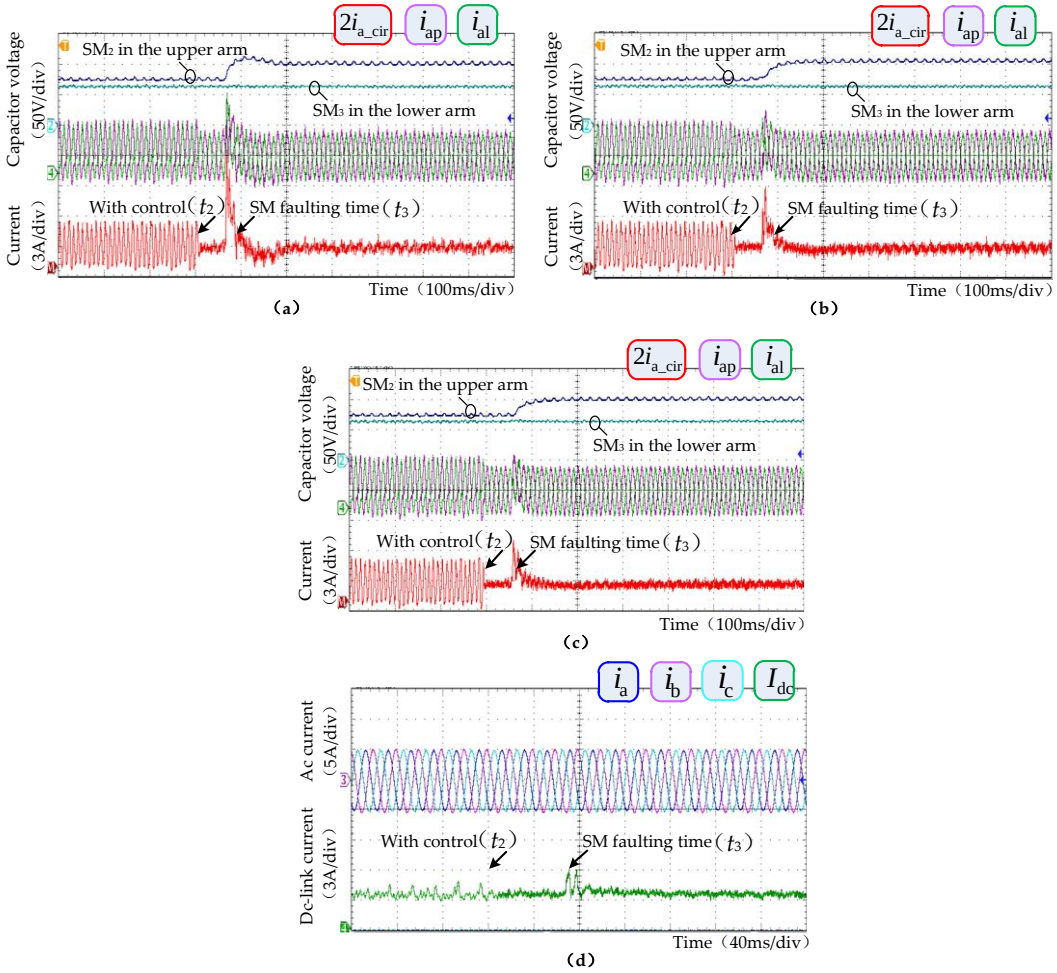

Figure 13. Experiment results about the virtual resistance compensation control: (**a**) arm operating state of phase a under $R_0 = 0$; (**b**) arm operating state of phase a under $R_0 = 5$; (**c**) arm operating state of phase a under $R_0 = 10$; (**d**) AC and DC-link current.

Table 3. Calculating results of the excessive ratio η.

The value of virtual resistance R_0	$R_0 = 0$	$R_0 = 5$	$R_0 = 10$
Twice peak value of the circulating current at t_3 moment $2i_{cirm}$	11.40 A	7.88 A	6.17 A
Excessive ratio of the circulating current η	1.59	0.79	0.40

According to the simulation and experiment results, it can be seen that this proposed fault-tolerant controller could effectively solve the problems generated by SM faults in the arm.

7. Conclusions

The fault-tolerant operation issue of MMC under SM faults is studied in this paper. The main works and contributions can be summarized as:

(1) The operation characteristics of the MMC with different number of faulty SMs in arms are analyzed and summarized. It reveals that unequal faulty SM numbers in each arm will generate asymmetrical circulating current included by the odd- and even-order frequency components, and its fluctuation mainly consists of fundamental and twice frequency components.

(2) A novel CCS fault-tolerant control strategy comprised by BCU and VRCCU in two parts is proposed. It can suppress the multi-different frequency components of the circulating current under different SM fault types simultaneously; and can help fast-limiting of the transient fault current caused at the faulty SM bypassed moment. Moreover, it does not need extra communication systems to acquire the information of the number of faulty SMs.

(3) The stability performance of the proposed controller is analyzed by using the *Root-Locus* criterion. It reveals that the response speed of the whole fault-tolerant controller can be accelerated by appropriately increasing the R_0 value, and then appropriately reducing the resonant gain to ensure the stability of the control system.

(4) The simulations in the MATLAB/SIMULINK environment and experiments with a 5-level prototype are all studied with the proposed controller under different fault conditions. The results confirm the efficiency of the control strategy.

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References

1. Marquardt, R. Stromrichterschaltungen mit Verteilten Energiespeichern. German Patent DE10103031A1, 24 January 2001.
2. Saeedifard, M.; Iravani, R. Dynamic performance of a modular multilevel back-to-back HVDC system. *IEEE Trans. Power Deliv.* **2010**, *25*, 2903–2912. [CrossRef]
3. Bergna, G.; Berne, E.; Egrot, P. An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2360–2371. [CrossRef]
4. Simon, P.T. Modeling the Trans Bay Cable project as voltage-sourced converter with modular multilevel converter design. In Proceedings of the IEEE Power and Energy Society General Meeting, Detroit, MI, USA, 24–29 July 2011; pp. 1–8.

5. Abdelsalam, M.; Tennakoon, S.; Griffiths, A.L.; Marei, M. Investigation of sub-module fault types of modular multi-level converters in HVDC networks. In Proceedings of the International Universities Power Engineering Conference (UPEC), Stoke, UK, 1–4 September 2015; pp. 1–6.
6. Jiang, W.; Wang, C.; Wang, M. Fault detection and remedy of multilevel inverter based on BP neural network. In Proceedings of the Asia-Pacific Power and Energy Engineering Conference (APPEEC), Shanghai, China, 27–29 March 2012; pp. 1–4.
7. Moon, J.W.; Kim, C.S.; Park, J.W. Circulating current control in MMC under the unbalanced voltage. *IEEE Trans. Power Deliv.* **2013**, *28*, 1952–1959. [CrossRef]
8. Son, G.; Lee, H.J.; Nam, T. Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer. *IEEE Trans. Power Deliv.* **2012**, *27*, 1611–1619.
9. Konstantinou, G.; Pou, J.; Ceballos, S. Active redundant sub-module configuration in modular multilevel converters. *IEEE Trans. Power Deliv.* **2013**, *28*, 2333–2341. [CrossRef]
10. Liu, G.; Xu, Z.; Xue, Y. Optimized control strategy based on dynamic redundancy for the modular multilevel converter. *IEEE Trans. Power Electron.* **2015**, *30*, 339–348. [CrossRef]
11. Li, S.; Wang, Z.; Wang, G. Fluctuation volt age control and fault-tolerant operation of modular multilevel converters with zero-sequence injection. *Int. Trans. Electr. Energy Syst.* **2014**, *24*, 944–959. [CrossRef]
12. Shen, K.; Xiao, B.; Mei, J. A modulation reconfiguration based fault-tolerant control scheme for modular multilevel converters. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–31 March 2013; pp. 3251–3255.
13. Yang, Q.; Qin, J. A post-fault strategy to control the modular multilevel converter under submodule failure. *IEEE Trans. Power Deliv.* **2012**, *27*, 1538–1547.
14. Hu, P.; Jiang, D.; Zhou, Y. Energy-balancing control strategy for modular multilevel converters under submodule Fault Conditions. *IEEE Trans. Power Electron.* **2014**, *29*, 5021–5029. [CrossRef]
15. Deng, F.; Tian, Y.; Zhu, R. Fault-tolerant approach for modular multilevel converters under submodule faults. *IEEE Trans. Power Electron.* **2016**, *63*, 7253–7263. [CrossRef]
16. Lu, Z.; Chen, Z.; Gong, Y. Sub-module fault analysis and fault-tolerant control strategy for modular multilevel converter. In Proceedings of the International Conference on AC and DC Power Transmission (ACDC 2016), Beijing, China, 28–29 March 2016; pp. 1–5.
17. Zhou, Y.; Jiang, D.; Guo, J. Control of modular multilevel converter based on stationary frame under unbalanced AC system. In Proceedings of the International Conference on Digital Manufacturing and Automation (ICDMA), Guilin, China, 31 July–2 August 2012; pp. 293–296.
18. Wang, Z.; Zhang, A.; Zhang, H. Control strategy for modular multilevel converters in sub-module fault state. In Proceedings of the IEEE Conference on Industrial Electronics and Applications (ICIEA), Auckland, New Zealand, 15–17 June 2015; pp. 369–374.
19. Wang, Z.; Zhang, A.; Zhang, H. Control strategy for modular multilevel converters with redundant sub-modules using energy reallocation. *IEEE Trans. Power Electron.* **2015**, *30*, 339–348. [CrossRef]
20. She, X.; Huang, A.; Ni, X. AC circulating currents suppression in modular multilevel converter. In Proceedings of the IEEE Industrial Electronics Society, Annual Conference (IECON), Montreal, QC, Canada, 25–28 October 2012; pp. 191–196.
21. Li, S.; Wang, X.; Li, T. Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions. *IEEE Trans. Power Electron.* **2015**, *30*, 387–397. [CrossRef]
22. Guan, M.; Xu, Z. Control and modulation strategies for modular multilevel converter based HVDC system. In Proceedings of the IEEE Industrial Electronics Society, Annual Conference (IECON), Melbourne, Australia, 7–10 November 2011; pp. 849–854.