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Energy Balance Control of a Cascaded Multilevel Inverter for Standalone Solar Photovoltaic Applications

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Abstract: This paper presents a clock phase-shifting (CPS) energy balance control (EBC) method for cascaded half-bridge multilevel inverters in standalone solar photovoltaic (PV) systems. It is based on the conservation of energy in each cascaded unit. By shifting the phase of the clock pulse of each cascaded unit, a staircase-like output voltage is obtained. The CPS EBC not only regulates the staircase-like output voltage of the cascaded multilevel inverters accurately under static conditions, but also suppresses the fluctuations of DC sources and improves its dynamic responses to load steps. Thus, the problems existing in solar PV systems using the cascaded multilevel inverters are avoided. Results obtained from simulations and experiments are presented to verify the feasibility and advantages of the proposed control method.

Keywords: solar photovoltaic systems; cascaded multilevel inverter; energy balance control

1. Introduction

Renewable energy sources are becoming increasingly important for electricity generation, since non-renewable energy sources such as fossil fuels are facing serious problems, e.g., pollutions, uncertain future of fossil-fuel prices, being unsustainable and CO_2 emissions [1]. Among these alternative energy sources, solar energy has been identified as being clean and easily available [2]. However, DC power produced by PV modules is not compatible with standard electrical appliances operating with AC power. In order to be compatible with the standard AC electrical appliances, various inverter topologies are proposed and employed to convert the DC electricity to the AC form [1]. Among these topologies, multilevel inverters have been receiving much attention, the most popular of them being cascaded multilevel inverter topologies [3,4], diode-clamped multilevel inverter topologies [5,6] and flying-capacitor multilevel inverter topologies [7,8]. A comparative analysis of the three topologies demonstrates that the cascaded topology is simple and uses the least components. Also, the cascaded topology is ideally suited for solar PV systems, where isolated input DC sources are available. Therefore, the cascaded topology is considered as the most suitable for solar PV systems in all multilevel topologies. Figure 1 displays the block diagram of a standalone solar PV system using a cascaded half-bridge multilevel inverter [9]. Compared with the typical cascaded H-bridge (CHB) multilevel topology, the cascaded half-bridge multilevel topology reduces nearly half the number of required switches. Recently, a cascaded switched-diode topology has been proposed [10,11]. The comparison with cascaded half-bridge multilevel topology illustrates that more voltage levels are produced with fewer required switches. However, under a case of resistance-inductance (R-L) loads, high voltage spikes occur at the base of the stepped output voltage due to the lack of a path for reverse load currents, which tend to deteriorate power quality [12].

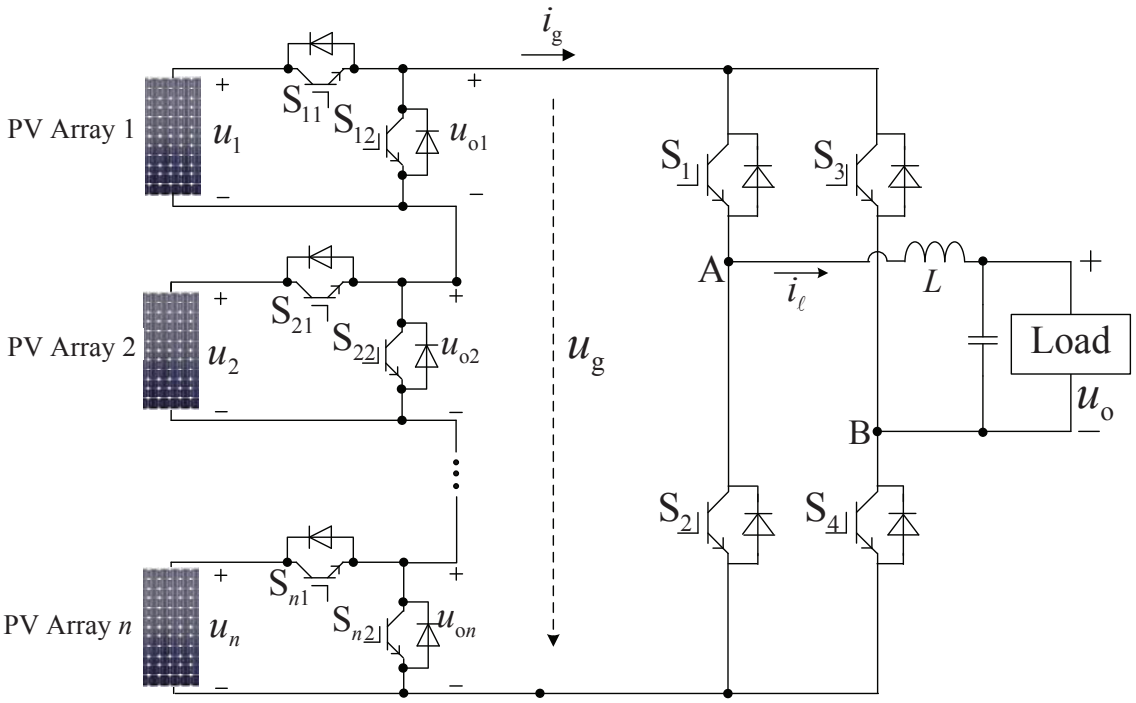

Figure 1. Standalone solar PV system with a cascaded half-bridge multilevel inverter.

Basic modulations techniques for cascaded multilevel topologies are rooted on the fundamental frequency switching [9], sinusoidal pulse width modulation (PWM) [13,14], and space vector PWM (SV-PWM) [15]. However, in solar PV systems, DC sources of a multilevel inverter topology are supplied by PV modules, as shown in Figure 1, which brings about a series of problems:

- Power imbalance: the power of a PV array supplied to each cascaded unit of the multilevel inverter may be different, introduced by cloud shading, different irradiance levels and ambient temperatures.
- DC supply with fluctuations: the DC supply from a PV array is always with fluctuation caused by variety of external factors, such as illumination change, shadow, ambient temperature and etc. More specifically, following variations in a certain range of irradiance level will lead to the instability of the voltage, which manifests as low frequency pulsation.
- Load variations: with the constant expansion of application fields, loads of an inverter are becoming more and more diversified. Abrupt load variations happen regularly.

The existence of these problems cause distortions or bring lots of low harmonics to the output voltages of the cascaded multilevel inverters using basic modulation techniques, which leads great hazards to electrical equipment. In recent years, some nonlinear control methods, e.g., hysteresis control, sliding mode control, fuzzy logic control and so on, have been attempted in multilevel inverters. As presented in [16], the advantages of using various accessible DC voltage levels have been fully exploited by using the hysteresis control. Sliding-mode control (SMC), as presented in [17], provides fast dynamic responses. However, the variable switching frequency and nonzero steady-state error are the drawbacks of these methods. Then in [18], a fuzzy logic control has been proposed. The dynamic behaviours are improved by considering moving cloud obfuscating the PV arrays.

Among the problems in solar PV systems, the power imbalance can be classified into two categories: (1) the inter-phase power imbalance, which occurs when each phase generates different amount of power; and (2) the inter-bridge power imbalance, which happens when each bridge in the same phase generates different amounts of power [19]. A three-phase system focus

more on the interphase power imbalance because three-phase unbalanced currents result in wasted power. New control methods [19,20] or converter topology [21] have been proposed to deal with the interphase power imbalance problem of CHB converters in PV systems. In contrast, the interbridge power imbalance gets more attention in single-phase systems. A continuous time-domain power balancing control algorithm was presented to solve the interbridge imbalance of a single-phase CHB converter [22]. However, this method can improve but not completely suppress fluctuations of the DC supply of the multilevel inverter. Thus, the problem of DC supply with fluctuations in PV application has not been solved. A CPS one-cycle control method was proposed for multilevel inverters. While its inhibitory capability to the interbridge power imbalance and variations of input voltage is satisfactory, the inhibitory capability to load changes is still poor [12].

The objective of this paper is to verify the ability of the proposed CPS EBC method to deal with the problems of a multilevel inverter in standalone solar PV applications. The basic structure of this paper is as follows. Section 2 introduces the cascaded half-bridge topology. The derivation of the control equation, the design and implementation of the proposed CPS EBC method are illustrated in Section 3. Section 4 presents the simulation and experimental results. Final conclusions are given in Section 5.

2. Topology of the Cascaded Half-Bridge Multilevel Topology

Figure 1 displays the cascaded half-bridge topology for standalone solar PV applications. The topology is divided into two stages. The first stage is cascaded by n half-bridge converters. The cascaded unit, e.g., unit 1, as shown in Figure 1, contains a DC source supplied from a PV array, the DC voltage of which is equal to u_1, switches S_{11} and S_{12}. The output of the unit 1 u_{o1} have two values, which are u_1 when switch S_{11} conducts and S_{12} is off, and when switch S_{11} is off and S_{12} is turned on, the value of u_{o1} is 0. For states of switches S_{11}, S_{12}, S_{21}, S_{22}, $\cdots$, $S_{(n-1)1}$, $S_{(n-1)2}$, S_{n1} S_{n2}, the output voltage of the first stage u_g obtains 2^n different values, as listed in Table 1, the maximum of them is given as follows:

$$u_g = u_{o1} + u_{o2} + \cdots + u_{on}. \tag{1}$$

From Table 1, it can be observed that the first stage generates a positive output voltage. For generating both positive and negative values, the second stage, which is a full-bridge inverter, is required. Table 2 lists the obtained output voltage u_o under different switch states. Through the judgement of the positive or the negative sign of a reference voltage u_{ref}, both the positive and negative halves of u_o are achieved.

Table 1. Values of u_g under different switch states of the first stage.

State	Switches States									u_g
	S_{11}	S_{12}	S_{21}	S_{22}	$\cdots$	$S_{(n-1)1}$	$S_{(n-1)2}$	S_{n1}	S_{n2}	
1	off	on	off	on	$\cdots$	off	on	off	on	0
2	on	off	off	on	$\cdots$	off	on	off	on	u_1
3	off	on	on	off	$\cdots$	off	on	off	on	u_2
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
n	off	on	off	on	$\cdots$	off	on	on	off	u_n
$n+1$	on	off	on	off	$\cdots$	off	on	off	on	$u_1 + u_2$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
2^n	on	off	on	off	$\cdots$	on	off	on	off	$\sum_{i=1}^{n} u_i$

Table 2. Values of u_o under different switch states of the second stage.

State	Switches States				u_o	Condition
	S_1	S_2	S_3	S_4		
1	on	off	off	on	u_g	$u_{ref} > 0$
2	off	on	on	off	$-u_g$	$u_{ref} < 0$

Under the symmetric case, that is, all the DC sources are equal to u_{dc}, the total number of required switches N_{IGBT} against the output voltage levels N_{level} are shown as follows,

$$N_{IGBT} = N_{level} + 3. \tag{2}$$

Compared with the CHB multilevel topology ($N_{IGBT} = 2(N_{level} - 1)$), the cascaded half-bridge multilevel topology reduces nearly half the number of required switches. However, in designing such a multilevel topology, it should be noted that the switches of the full-bridge converter S_1, $\cdots$, S_4 have to withstand the total voltage of all cascaded units, while the switches of the first stage S_{11}, S_{12}, $\cdots$, S_{n1}, S_{n2} only withstand a fraction of the total voltage of all cascaded units. This indicates that the four switches in the full-bridge cell of the second stage are with a high capability of the voltage rating, which makes the total voltage rating increase and leads to the limitation of the high voltage applications. Thus, the cascaded half-bridge multilevel topology is more suitable for medium voltage (2.3, 3.3, 4.16 or 6.9 kV) applications [23].

3. The CPS EBC Method for Cascaded Half-Bridge Multilevel Topology

3.1. The Design of the CPS EBC

According to the topology analysis in Section 2, the second stage implements the generation of the positive and negative halves of output voltage by comparing the reference voltage u_{ref} with zero. Thus, the second stage in Figure 1 can be omitted. Then a topology is constructed for the design of the CPS EBC, as shown in Figure 2. Compared with Figure 1, it can be seen that the second stage is omitted.

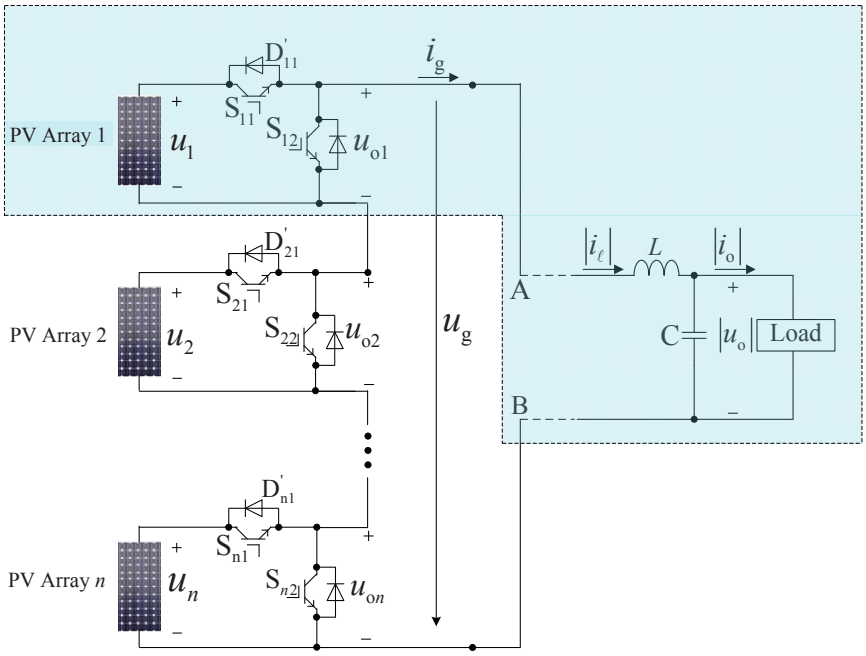

Figure 2. The structure of the topology leaving out the details of the second stage.

Figure 3 shows the structure of the proposed CPS EBC method to control the topology shown in Figure 2. The structure displays that a CPS EBC contains n independent EBC controllers. Each independent EBC controller corresponds to a cascaded unit, for instance, the EBC controller 1 in Figure 3 is used for controlling cascaded unit 1, which is the part of the dotted box in Figure 2. The n independent EBC controller are similar but with a T_s/n phase-shift of the clock pulse, where T_s denotes the switching cycle of the multilevel inverter. For an example of cascaded unit 1, the control equation of the EBC controller 1 is derived as follows. From Figure 2, it can be seen that the part of the dotted box can be regarded as a buck circuits: the circuit, constructed by u_1, S_{11}, S_{12}, L, C. Then similar to that of [24], the control principle of the EBC controller 1 is that, by keeping the balance between the energy injected into the circuit from DC sources $W_{in1}(k)$ and the sum of the output energy $W_{out1}(k)$ and the energy the inductor L stores $\Delta W_\ell(k)$ in a switch cycle, e.g., the k^{th} switching cycle $[(k-1)T_s, kT_s)$ [24], the EBC controller forces the output voltage to be a desired value , as

$$W_{in1}(k) = W_{out1}(k) + \Delta W_\ell(k) \quad (k = 1, 2, \cdots) \tag{3}$$

During the k^{th} switching cycle, the part of the dotted box in Figure 2 operates as a buck converter in two states. In state 1, S_{11} is on for the duration $t_{on1}(k)$. In this switching state, DC sources injects energy into the circuit and $i_g = |i_\ell|$ flows through the loop ($u_1 \rightarrow S_{11} \rightarrow L \rightarrow C \parallel R \rightarrow S_{n2} \rightarrow S_{(n-1)2} \rightarrow \cdots \rightarrow S_{22} \rightarrow u_1$). L is charged, and R consumes energy, then u_{o1} is obtained using

$$u_{o1}(t) = u_1 \quad (t \in [(k-1)T_s, (k-1)T_s + t_{on1}(k)) \tag{4}$$

In state 2, S_{11} is turned off and S_{12} is on for the duration $t_{off1}(k)$. In this switching state, no energy is fed into the circuit, and $i_g = |i_\ell|$ flows through the loop ($S_{12} \rightarrow L \rightarrow C \parallel R \rightarrow S_{n2} \rightarrow S_{(n-1)2} \rightarrow \cdots \rightarrow S_{12}$). L is discharged, and R consumes energy. Then u_{o1} is obtained using

$$u_{o1}(t) = 0 \quad (t \in [(k-1)T_s + t_{on1}(k), kT_s) \tag{5}$$

The above analysis of the operation states illustrates that the DC source u_1 of the cascaded unit 1 works in the time interval $[(k-1)T_s, (k-1)T_s + t_{on1}(k))$, while L and R operate in the entire switching cycle. The energy values of $W_{in1}(k)$, $W_{out1}(k)$ and $\Delta W_{\ell 1}(k)$ during the k^{th} switching cycle are calculated as follows:

$$W_{in1}(k) = \int_{(k-1)T_s}^{(k-1)T_s + t_{on1}(k)} u_1(t) i_g(t) dt \tag{6}$$

as $i_g = |i_\ell(t)|$, then $W_{in1}(k)$ is derived as below:

$$W_{in1}(k) = \int_{(k-1)T_s}^{(k-1)T_s + t_{on1}(k)} u_1(t) |i_\ell(t)| dt \tag{7}$$

$$W_{out1}(k) = \int_{(k-1)T_s}^{(k-1)T_s + T_s} |u_{ref1}(t)||i_o(t)| dt \tag{8}$$

$\Delta W_{\ell 1}(k)$ is calculated as the following:

$$\Delta W_{\ell 1}(k) = \int_{(k-1)T_s}^{(k-1)T_s + T_s} |u_\ell(t)||i_\ell(t)| dt \tag{9}$$

Substituting the values of $W_{in1}(k)$, $W_{out1}(k)$ and $\Delta W_\ell(k)$ into (3) derives:

$$\int_{(k-1)T_s}^{(k-1)T_s + t_{on1}(k)} u_1(t) |i_\ell(t)| dt = |u_{ref1}||i_o(t)| T_s + \int_{(k-1)T_s}^{kT_s} |u_\ell(t)||i_\ell(t)| dt \quad (k = 1, 2, \cdots) \tag{10}$$

Combining the aforementioned state analysis, (10) can be realized by controlling u_{o1}, which is expressed in

$$\int_{(k-1)T_s}^{kT_s} u_{o1}(t)|i_\ell(t)|dt = |u_{ref1}||i_o(t)|T_s + \int_{(k-1)T_s}^{kT_s} |u_\ell(t)||i_\ell(t)|dt \quad (k = 1, 2, \cdots) \tag{11}$$

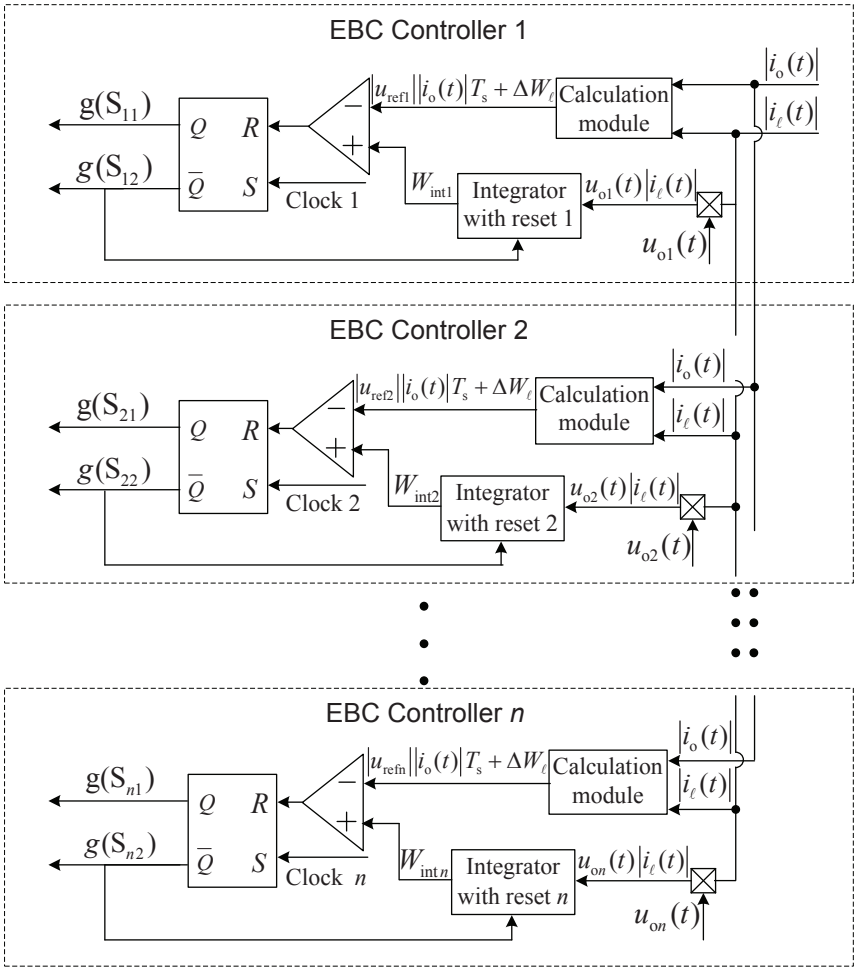

Figure 3. The structure of the CPS EBC method for the topology leaving out the details of the second stage.

3.2. The Implementation of CPS EBC

As a part of the control reference, $|u_{ref1}||i_o(t)|T_s$ is calculated instantaneously. The other part $\int_{(k-1)T_s}^{kT_s} |u_\ell(t)||i_\ell(t)|dt$ is calculated in the instant of the beginning of the k^{th} switching cycle and kept the same during the entire switching cycle. Note here, the value of $\int_{(k-1)T_s}^{kT_s} |u_\ell(t)||i_\ell(t)|dt$ is collected only in the time point k^{th} T_s, thus there is a switching cycle lag. The errors due to this switching cycle lag are ignored here, since the duration of the switching cycle is short. This means that the value used in the k^{th} switching cycle is actually the value obtained in the $(k-1)^{th}$ switching cycle.

After the computation of the control reference, the CPS EBC method is implemented with comparison and integration as shown in Figure 3. Here, the implementation of the EBC controller 1 is described as follows. When S_{11} is turned on by a clock pulse with fixed frequency, the integral operation starts and $u_{o1}(t) = u_1$. Thus the output of the integrator $W_{int1}(t)$ is calculated as follows:

$$W_{int1}(t) = \int_{(n-1)T_s}^{t} u_{o1}(t)|i_\ell(t)|dt = \int_{(n-1)T_s}^{t} u_1|i_\ell(t)|dt \tag{12}$$

as time goes on, $W_{\text{int1}}(t)$ increases from its initial value and is compared with the control reference instantaneously. At the instant when $W_{\text{int1}}(t)$ reaches $W_{\text{out1}}(k) + \Delta W_{\ell 1}(k)$, a reset pulse is generated by the comparator to reset the RS flip-flop to be ($Q = 0$). Then S_{11} is turned off, while S_{12} is turned on. At the same time, $W_{\text{int1}}(t)$ is reset to zero. The switching state is kept until the arrival of the next clock pulse, which starts the $(k+1)^{\text{th}}$ switching cycle.

As the design and implementation for other EBC controllers are similar to that of the EBC controller 1, the details are not presented here.

4. Simulation and Experimental Results

When designing solar PV fed inverters, the estimation of PV characteristics and maximum power point tracking (MPPT) control are one focus for solar PV modelling, meanwhile another way to simulate PV arrays employs a DC power supply with variable output voltage. Concerning stand-alone PV systems, the extraction of energy from PV arrays depends on the load demand [18,25]. In this research, on the premise of guaranteeing the installed output power of PV arrays, each PV array is only simulated by a *V*-*I* characteristic with an open-circuit voltage that is equal to 80 V. It should be noticed that the PV modelling method employed in this research cannot represent the PV arrays controlled by a MPPT algorithm. At first, a five-level and nine-level two-stage half-bridge multilevel inverter with a switching frequency of 2,500 Hz are set up. The parameters are $u_1 = u_2 = \cdots = u_n = 80$ V, $R = 50\ \Omega$, $L = 16$ mH, $C = 10\ \mu F$, $u_{\text{ref1}} = u_{\text{ref2}} = \cdots = u_{\text{ref}n} = 60$ V. Then a five-level experimental prototype, the parameters of which are identical with that of the simulation model, is built. In the experimental prototype shown in Figure 4, the voltage and current are sampled by the measurement, which is made up of HALL voltage sensors CHV-25P/100 (Measurement range: 0–±150 V; Measurement accuracy: ±0.1%) and HALL current sensors CHB-25NP/6 A (Measurement range: 0–±9 A; Measurement accuracy: ±0.8%), respectively. The gate drivers of the IGBT are configured on SKYPER 32R (SEMIKRON, Nuremberg, Germany), which are powered with the DC power source (0/15 V). In the experiment, PV arrays are emulated by DC power with variable output voltage and a function generators. The function generator TFG1900B (Suin Instuments, Nanjing, China) is connected in series with the DC power, which generate fluctuations (here is the low frequency ripples) to simulate the variations in irradiance and temperature of PV array outputs. The overall control strategy is implemented on a DS1104 (dSPACE company, Padbourne, Germany) system, where the proposed CPS EBC controller was programmed for the five-level half-bridge cascaded multilevel inverter.

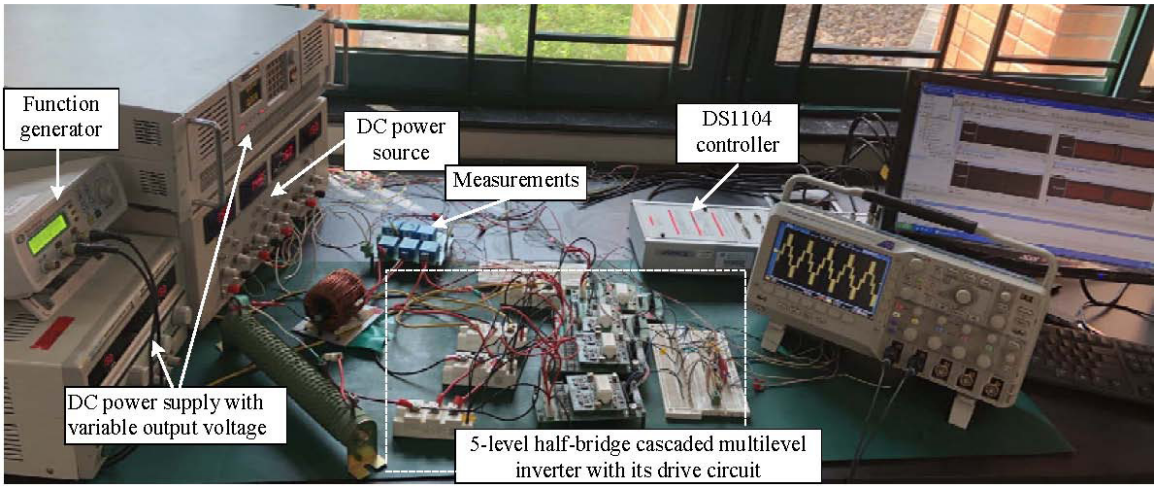

Figure 4. The hardware and interface of the experimental prototype.

To reveal the limitations of the conventional controller for solar PV applications, a carrier phase-shifted sinusoidal pulse width modulation (CPS SPWM) controller is configured. Although in recent years some nonlinear control methods have been attempted for controlling multilevel inverters, the CPS SPWM controller based on the sinusoidal PWM is still the most typical modulation strategy in cascade multilevel converter applications, as the CPS SPWM has the advantages of low-switching technique, balancing switching loads and good harmonic characteristics. The comparative studies demonstrate the ability to suppress DC source fluctuations and the improved dynamic responses to load variations using the CPS EBC. A comparison is made with the CPS SPWM because it is most frequently used for controlling cascaded multilevel inverters.

4.1. The Operation of CPS EBC

Figure 5 shows the gate signals of the cascaded half-bridge multilevel inverter. From Figure 5a, it can be seen that when S_{11} is on, S_{21} is off; When S_{11} is turned off, S_{21} is on. The gate signals of the second stage are shown in Figure 5b. S_1 and S_4 are on-state when $u_{ref} \geq 0$. In this switching state, $u_o = u_g$. When $u_{ref} < 0$, S_1 and S_4 are turned off and S_2 and S_3 are turned on. In this switching state, $u_o = -u_g$ for the negative half cycle. By judging the sign of u_{ref}, both the positive and negative halves of output voltage are obtained.

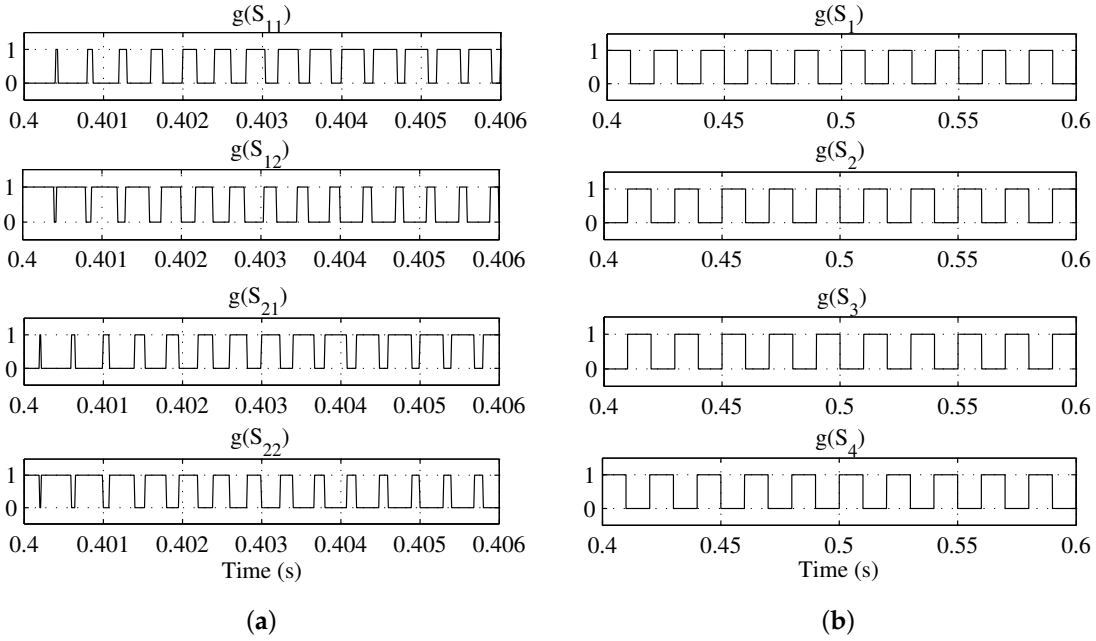

Figure 5. Gate signals of the five-level simulation prototype. (**a**) The gates of the first stage; and (**b**) The gates of the second stage.

As shown in Figure 6a, the output of the first stage u_g, which is the sum of the output voltage of all the cascaded units, has positive and zero values. The output current i_g of the first stage is also positive. The voltage between points A and B u_{AB}, the output voltage u_o and the inductor current i_ℓ of the multilevel inverter are shown in Figure 6b. From the waveforms in the figure, it can be seen that u_{AB} is a staircase waveform with a frequency of 50 Hz and an amplitude of 160 V. After the $(L-C)$ filter, u_o and i_ℓ are almost sinusoidal waveforms. Figure 7a demonstrates that the total harmonic distortion (THD) of u_{AB} of the five-level simulation prototype is 35.65% and the frequencies that the main harmonics focus on is multiples of 5000 Hz (5000 Hz, 10,000 Hz, 15,000 Hz, ...), where 5,000 Hz is twice of the switching frequency (2500 Hz).

Figure 8 illustrates the simulation results of the operation of a nine-level multilevel topology. It is observed from Figure 8a that u_g and i_g have zero and positive values. Figure 8b shows the waveforms of u_{AB}, u_o and i_ℓ of the nine-level multilevel topology. The waveforms in the figure demonstrate

that u_{AB} is a staircase waveform with a frequency of 50 Hz and an amplitude of 320 V. After the $(L-C)$ filter, u_o and i_ℓ are almost sinusoidal waveforms. The THD of u_{AB} of the nine-level multilevel inverter is 16.96%, as shown in Figure 7b. The frequencies that the main harmonics focus on is multiples of 10,000 Hz (10,000 Hz, 20,000 Hz, 30,000 Hz, ...), where 10,000 Hz is four times of the switching frequency 2500 Hz. The comparison with THD of u_{AB} of the five-level prototype, the THD is reduced and the frequencies that the main harmonics focus on move backward, which reduces the designing standards of the output filter.

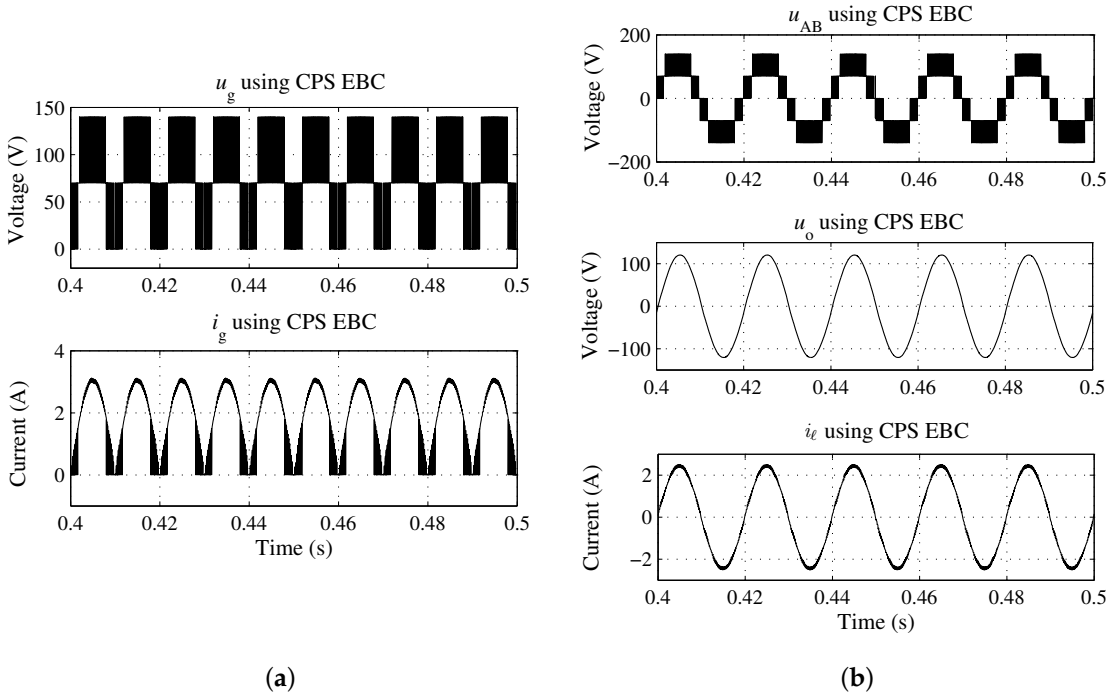

Figure 6. The simulation results of the five-level prototype. (**a**) The output voltage u_g and current i_g of the first stage; (**b**) The output voltage u_o and current i_o of the second stage.

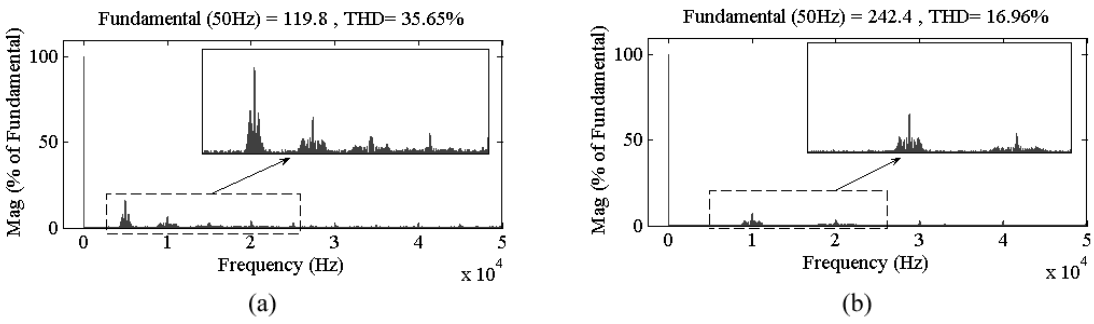

Figure 7. The fast fourier transform (FFT) analysis result of u_{AB}. (**a**) The five-level simulation prototype; and (**b**) The nine-level simulation prototype.

The experimental results of the five-level prototype using the CPS EBC are shown in Figures 9 and 10. The figures illustrate that the results are consistent with the simulation results in Figure 6. u_g and i_g of the first stage are positive. u_{AB} is a five-level staircase waveform. The THD of u_{AB} is 42.18% and the frequencies that the main harmonics focus on is (5000 Hz, 10,000 Hz, 15,000 Hz, ...) , as shown in Figure 10a. After the $(L-C)$ filter, u_o and i_ℓ are sinusoidal waveforms. The THD of u_o is 2.40%, as shown in Figure 10b.

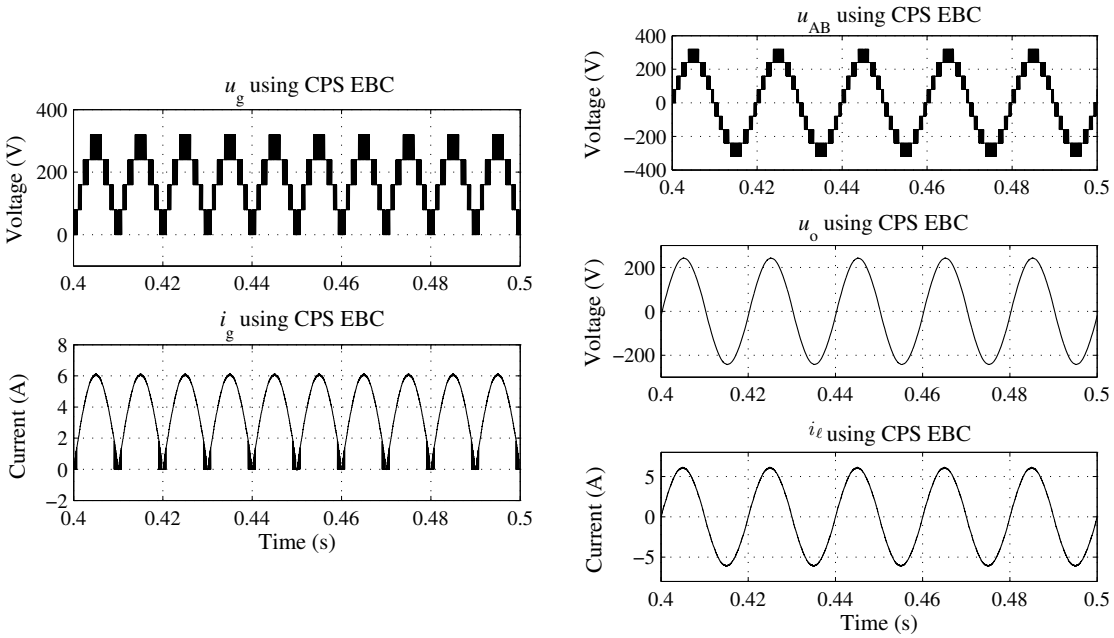

Figure 8. The simulation results of the nine-level prototype. (**a**) The output voltage u_g and current i_g of the first stage; and (**b**) The output voltage u_o and current i_o of the second stage.

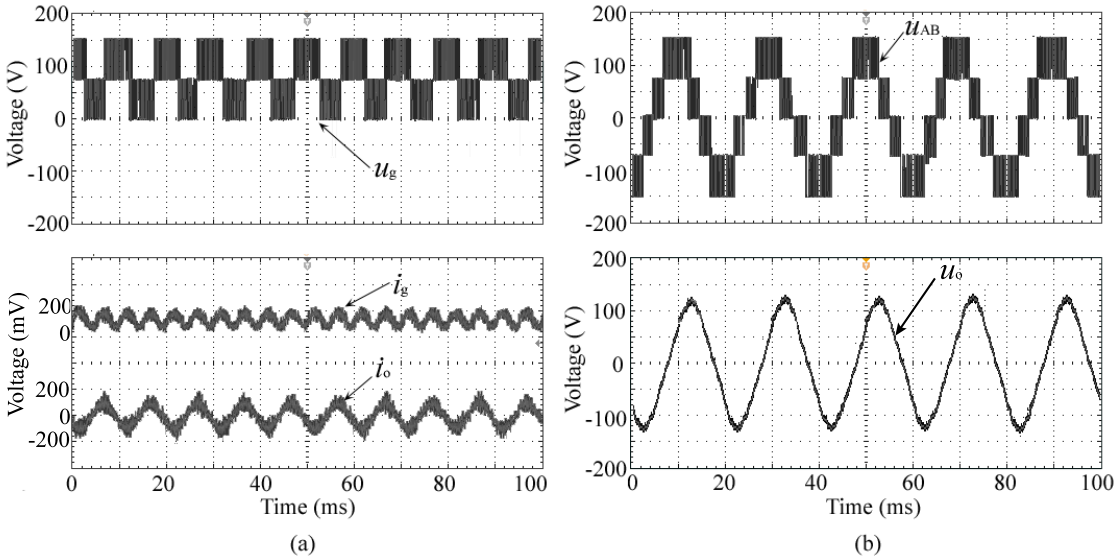

Figure 9. The experimental results of the operation of the five-level prototype using CPS EBC. (**a**) The output voltage u_g of the first stage (figure top); The current i_g and i_o (figure bottom); and (**b**) The stepped voltage u_{AB} (figure top); The output voltage u_o (figure bottom).

The above simulation and experimental results verify the feasibility of the CPS EBC method for the cascaded half-bridge multilevel inverter in standalone solar PV applications.

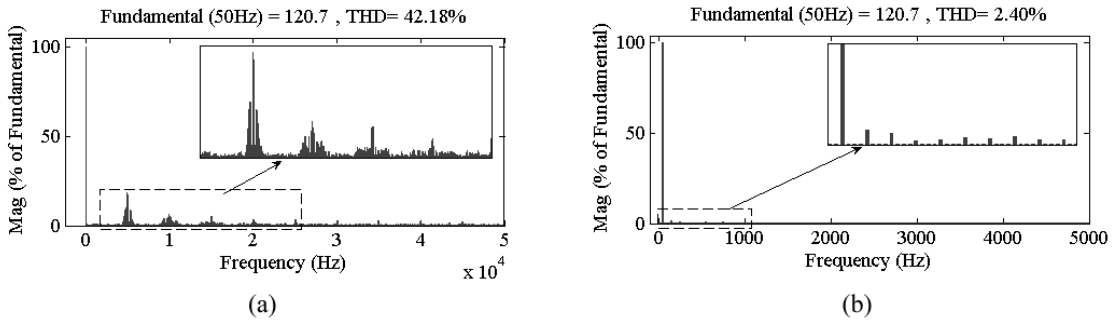

Figure 10. The FFT analysis result of the experimental prototype. (**a**) The stepped voltage u_{AB}; and (**b**) The output voltage u_o.

4.2. The Suppression Ability of the CPS EBC against Interbridge Power Imbalance in DC Sources

To evaluate the ability of the CPS EBC to suppress the power imbalance of the PV arrays, DC sources ($u_1, u_2, \cdots, u_n$) are designed by different DC voltages. The simulation and experimental results are demonstrated in Figure 11.

Figure 11a shows the simulation results under power imbalance (under the obfuscation of cloud shadowing, the PV unit 1 (u_1) is with a voltage drop 15 V). The comparison results demonstrate that u_o using CPS SPWM tracks its reference 120 V with a drop 18 V. In contrast, u_o using CPS EBC tracks its reference with no voltage drop. Figure 11b display the experimental results using the CPS EBC and the CPS SPWM under the cases of power imbalance. From the comparisons, it can be observed that the experimental results are consistent with the simulation results in Figure 11a. Thus the ability of the proposed CPS EBC against the interbridge power imbalance is verified.

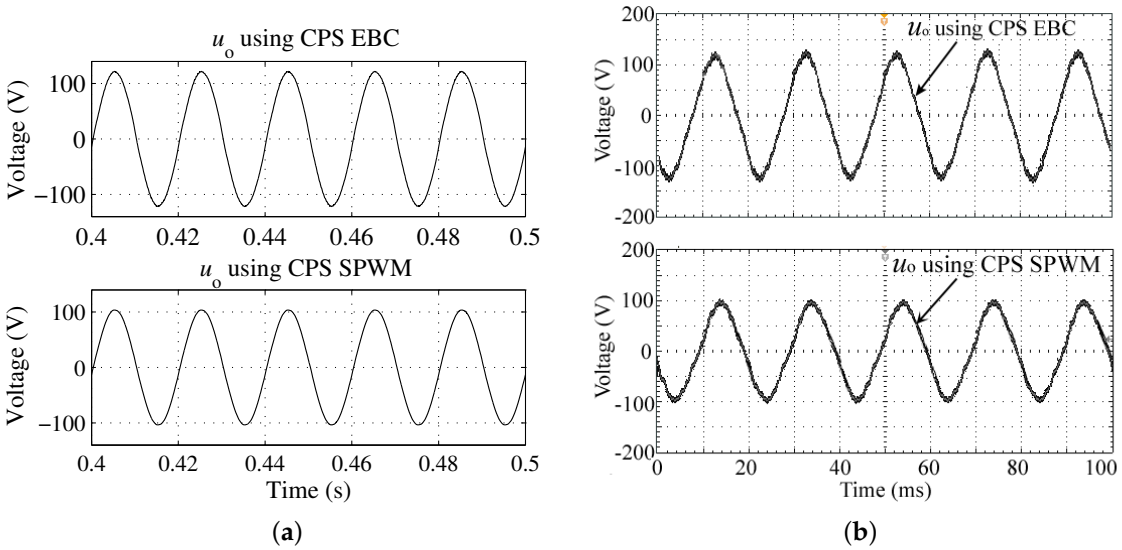

Figure 11. The results of the five-level prototype under the case of power imbalance ($u_1 = 65$ V and $u_2 = 80$ V). (**a**) Simulation results; and (**b**) Experimental results.

4.3. The Suppression Ability of the CPS EBC against Interferences in DC Sources

To evaluate the ability of the CPS EBC to suppress the fluctuations of DC sources, DC sources ($u_1, u_2, \cdots, u_n$) are designed by DC voltage mixed with low frequency interferences. The simulation and experimental results are demonstrated in Figures 12–15.

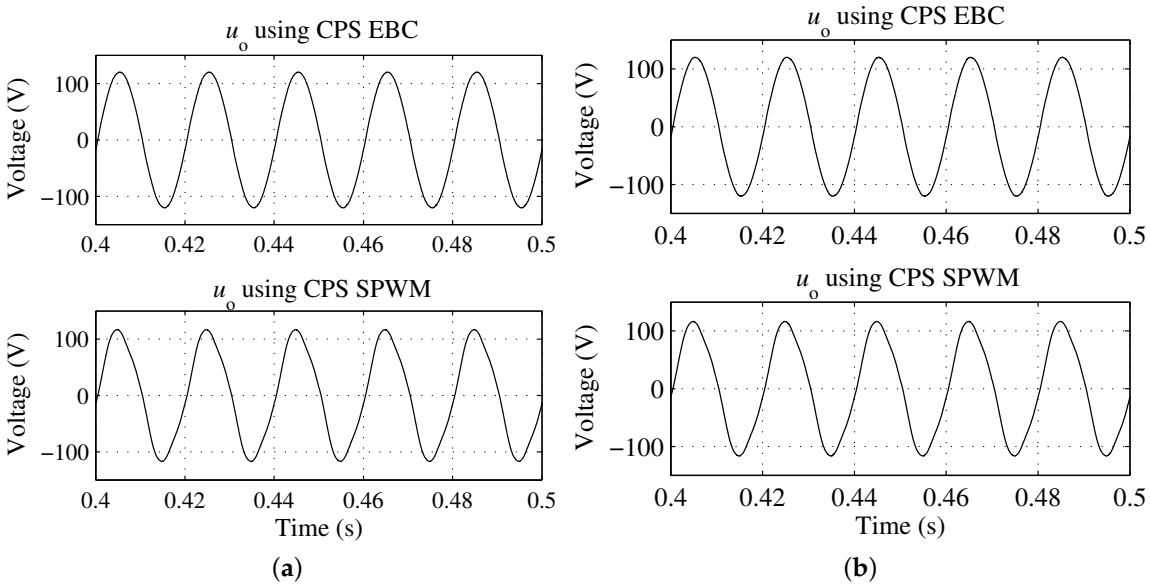

Figure 12. The simulation results of the five-level prototype under the case of unbalance DC voltages and DC voltages with fluctuations. (**a**) DC voltage u_1 contains a ripple with a frequency of 100 Hz and an amplitude of 16 V; and (**b**) DC voltage of each cascaded unit contains a frequency of 100 Hz and an amplitude of 8 V.

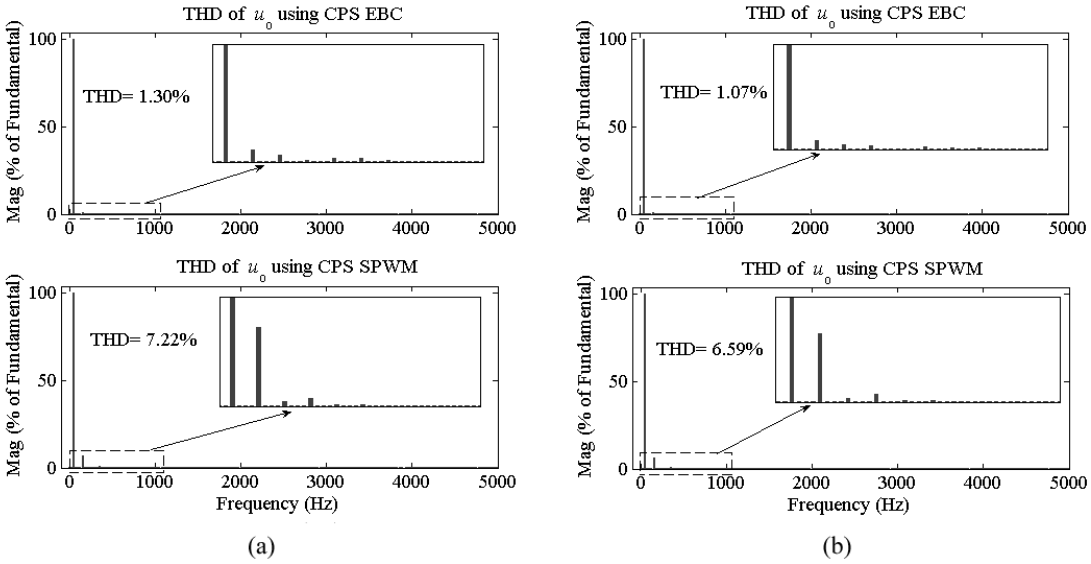

Figure 13. The comparison of the THD of the five-level simulation prototype under the case of DC voltages with fluctuations. (**a**) DC voltage u_1 contains a ripple with a frequency of 100 Hz and an amplitude of 16 V; and (**b**) DC voltage of each cascaded unit contains a frequency of 100 Hz and an amplitude of 8 V.

Table 3. Simulation and Experimental results under DC voltages with fluctuation.

	Cases	Simulation		Experiment	
		CPS EBC	**CPS SPWM**	**CPS EBC**	**CPS SPWM**
THD (%)	Unbalance DC sources	1.30	7.22	2.90	9.11
	DC sources with fluctuation	1.07	6.59	2.74	8.89

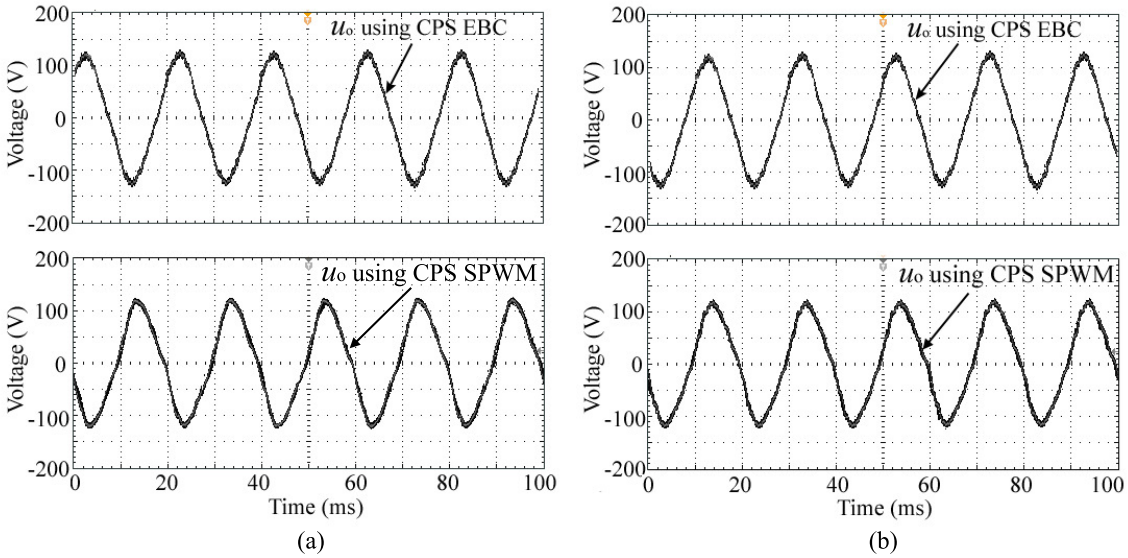

Figure 14. The experimental results of the five-level prototype under the case of DC voltages with fluctuations. (**a**) DC voltage u_1 contains a ripple with a frequency of 100 Hz and an amplitude of 16 V; and (**b**) DC voltage of each cascaded unit contains a frequency of 100 Hz and an amplitude of 8 V.

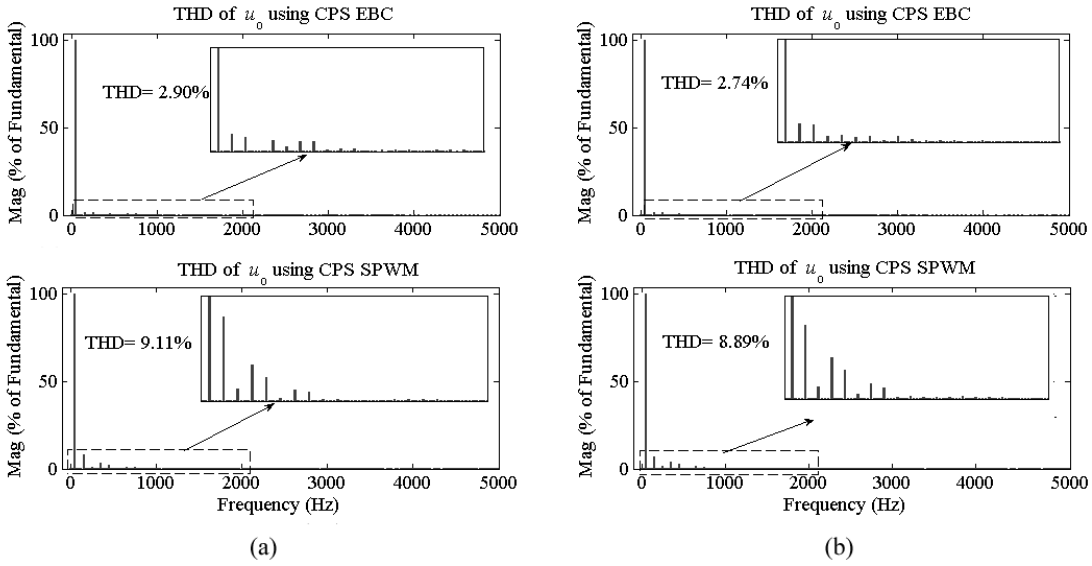

Figure 15. The comparison of the THD of the five-level experimental prototype under the case of DC voltages with fluctuations. (**a**) DC voltage u_1 contains a ripple with a frequency of 100 Hz and an amplitude of 16 V; and (**b**) DC voltage of each cascaded unit contains a frequency of 100 Hz and an amplitude of 8 V.

Figure 12a shows the simulation results under unbalance DC voltages (a ripple with a frequency 100 Hz and an amplitude 16 V is added in u_1). The comparison results demonstrate that u_o using CPS SPWM is not a ideal sine wave but with distortions. The FFT analysis in Figure 13a shows low order harmonic voltages are contained in u_o. In comparison, u_o using the CPS EBC is kept as a ideal sine wave. No low order harmonic voltages are brought into u_o, as shown in Figure 13a. Similarly, under the DC voltages mixed with low frequency ripples (100 Hz ripples with an amplitude 8 V are added in u_1 and u_2, respectively). The comparison results in Figure 12b illustrate that u_o using the CPS SPWM distorts due to the low order harmonic voltages. However, u_o using the CPS EBC, is kept

as a ideal sine wave. This can also be observed from the comparison of the FFT analysis in Figure 13b. Figures 14 and 15 display the experimental results using the CPS EBC and the CPS SPWM under the cases of unbalanced DC voltage and DC voltage with fluctuations. From the comparisons, it can be observed that the experimental results are consistent with the simulation results in Figure 12. All the comparison results of the THD of u_o under the cases of unbalance DC voltages and DC voltages containing low frequency ripples are summarized in Table 3. The figures and tables verify that the CPS EBC has strong inhibitions against fluctuations of DC sources.

4.4. The Dynamic Responses of CPS EBC to Load Variations

To evaluate the dynamic performances of the proposed CPS EBC, the responses to variations in the load of the converter using the CPS EBC is compared with that of the CPS SPWM. Figures 16 and 17 demonstrate the comparison results.

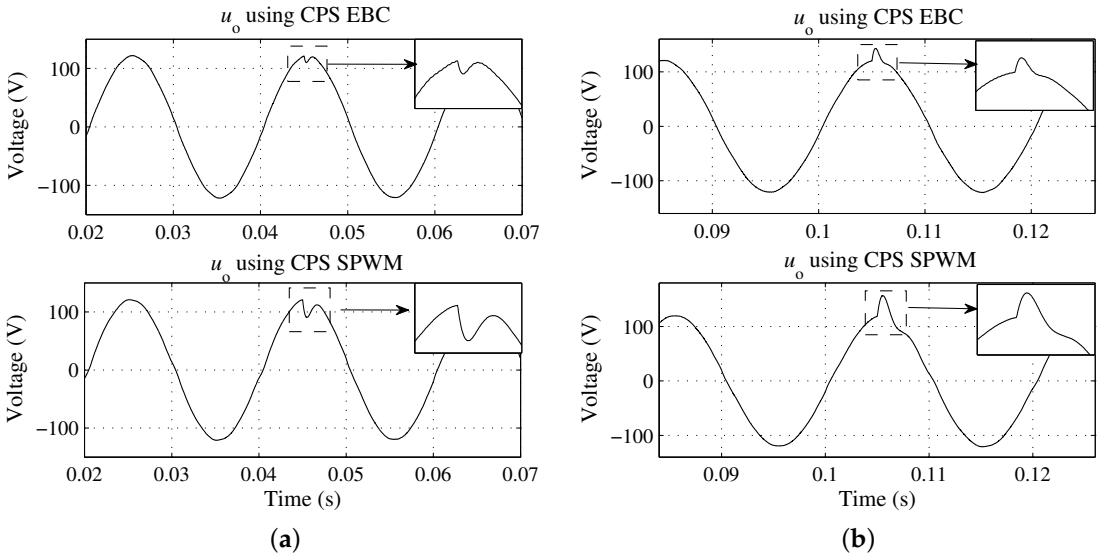

Figure 16. The simulation results of the five-level prototype under cases of load steps. (**a**) load steps as 50 Ω → 25 Ω; and (**b**) load steps as 25 Ω → 50 Ω.

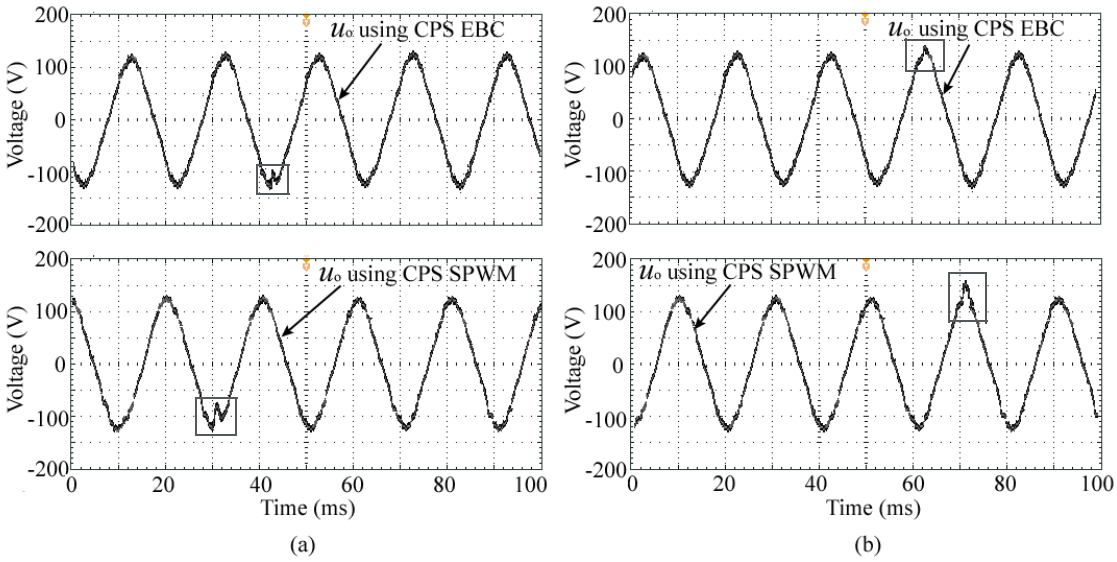

Figure 17. The experiment results of the five-level prototype under cases of load steps. (**a**) load steps as 50 Ω → 25 Ω; and (**b**) load steps as 25 Ω → 50 Ω.

In the simulation and experiment, the load steps from 50 Ω → 25 Ω at $t = 0.045$ s and 25 Ω → 50 Ω at $t = 0.105$ s. The comparison results of the voltage shoot Δu_o and the settling time $t_{settling}$ of the dynamic responses to the load variations are summarized in Table 4. From the figures and table, it can be observed that, under the load variation, Δu_o and $t_{settling}$ are significantly reduced by using the proposed CPS EBC. For instance, under the load variation from 50 Ω to 25 Ω, the simulation results of Δu_o is reduced from −26 V (using CPS SPWM) to −10 V (using CPS EBC) and $t_{settling}$ is reduced from 1.9 ms (using CPS SPWM) to 0.9 ms (using CPS EBC).

Table 4. Simulation and Experimental results under load variations.

	R (Ω)	CPS EBC		CPS SPWM	
		Δu_o (V)	$t_{settling}$ (ms)	Δu_o (V)	$t_{settling}$ (ms)
Simulation	50 → 25	−10	0.9	−26	1.9
	25 → 50	18	1.2	32	2
Experiment	50 → 25	−16	1.2	−32	2.2
	25→ 50	18	1.4	36	2.3

Thus, the improved dynamic responses to load variations of the CPS EBC method are verified from the above simulation and experimental results.

5. Conclusions

The CPS EBC method has been proposed and implemented for controlling the cascaded half-bridge multilevel inverters for standalone solar PV applications. It is composed by n similar but independent EBC controllers. DC sources mixed with fluctuations are designed to simulate the DC voltage supplied by the solar PV arrays. Simulation and experimental results demonstrate that, by shifting the phase of the clock pulse of each cascaded half-bridge, staircase-like voltage waveforms are obtained. Under the cases of unbalance DC voltage, DC voltages with low frequency ripples and load variations, the comparison results between the CPS EBC and the CPS SPWM method reveal that the CPS EBC produces a superior ability in suppressing the fluctuations in DC voltages and improved dynamic performances under load variations, in terms of shorter settling time and smaller voltage shoots. Thus, the distortions of the output voltage of the solar PV systems, due to the power imbalance, the DC supply with fluctuations are avoided. Meanwhile the dynamic responses to load variations are improved. These results illustrate that the CPS EBC method is more suitable than the CPS SPWM to control multilevel inverters for standalone solar PV applications.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CPS	Clock phase-shifting
EBC	Energy balance control
PV	Photovoltaic
CHB	Cascaded H-bridge
R-L	Resistance-inductance
PWM	Pulse-width Modulation
SV-PWM	Space vector PWM
SMC	Sliding-mode control

CPS SPWM	Carrier phase shifted-sinusoidal pulse width modulation
MPPT	Maximum power point tracking
THD	Total harmonic distortion
FFT	Fast fourier transform

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