

Full Research Paper

A Dynamic Range Expansion Technique for CMOS Image Sensors with Dual Charge Storage in a Pixel and Multiple Sampling

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Abstract: A dynamic range expansion technique for CMOS image sensors with dual charge storage in a pixel and multiple sampling technique is presented. Each pixel contains a photodiode and a storage diode which is connected to the photodiode via a separation gate. The sensitivity of the signal charge in the storage diode can be controlled either by a separation gate which limits the charge to flow into the storage diode or by controlling the accumulation time in the storage diode. The operation of the sensitivity control with separation gate techniques is simulated and it is found that a blocking layer to the storage diode plays an important role for high controllability of sensitivity of the storage diode. A prototype chip for testing multiple short time accumulations is fabricated and measured.

Keywords: Image sensor, wide dynamic range, multiple sampling, motion blur.

1. Introduction

Wide dynamic range image sensors are required for many applications such as digital cameras, security systems, automobiles and industrial cameras. However, there exists a difficulty to meet all the requirements of high sensitivity, low noise, sufficient wide dynamic range, and small motion blur.

Many methods to enhance the dynamic range of CMOS image sensors have been reported. The non-linear responses such as the logarithmic response [1] and well capacity adjustment [2] are useful for dynamic range expansion with a relatively simple structure and processing. However, these techniques are not compatible with a pinned photodiode technology, which is a key technology for low noise image sensors. Another group of dynamic expansion methods uses multiple exposure-time signals in one frame [3-5] and the pinned photodiodes can be used. However, the use of multiple different exposure-time signals has the problem of the motion blur. A technique using an in-pixel overflow integration capacitor [6,7] has excellent properties from the viewpoints of low noise by using pinned photodiodes and small motion blur. However, in this method, the dynamic range is determined by the capacitor size in the pixel.

In this paper, wide dynamic range expansion techniques for the flexible control of dynamic range and reduced motion blur are proposed. The pixel contains two charge storages, a photodiode and a storage diode. The storage diode is connected to the photodiode via a separation gate, SP. To expand the dynamic range of the sensor, the SP gate for short period of time is repeatedly opened during accumulation period in the photodiode to allow charge generated on the photo-detector between SP gate and photodiode, flowing into the storage diode.

Since the charge in storage diode can also be controlled by the accumulation time in the storage diode, the dynamic range can be expanded by the combination of the SP gate control and short accumulation time in the storage diode. The signal charge for short accumulation time in the storage diode is read out for multiple times in one frame. On the other hand, the charge in the photodiode is accumulated for long time, maximally frame period to achieve high sensitivity. The read multiple short-accumulation time signals of the storage diode and the long-accumulation time signal of the photodiode are synthesized in an external system.

The proposed techniques enable the flexible control of the dynamic range for most of applications. Furthermore, the duration of the signal accumulation in the storage diode can be approximately equalized to that of the photodiode, and the problem of unnatural motion blur can be reduced. The operation of the sensitivity control with the separation gate is confirmed by device simulations. The function of the multiple short-time accumulations has been confirmed by implemented in a prototyped chip. In the following, the pixel structure, the dynamic range expansion methods, the enhancement of SP gate controllability and the implementation of a prototype sensor chip are described.

2. Pixel Structure

The simplified structure (top view) of the proposed pixel and its cross-section at line aa' is shown in Figures 1(a) and 1(b), respectively. The pixel consists of two pinned diodes, PD and SD, which are for a photodiode and a storage diode, respectively. The SD region is connected to the PD region via a separation gate, SP and two kinds of n-type layer are formed under p⁺ layer in the PD region. A relatively lightly-doped n-type layer between the PD and SP gates is a photo-detector for both the SD and PD signals. Electrons flow into the SD region when the SP gate is opened. The transfer gates, TX1 and TX2 are used for reading out the signal charges in the PD and SD, respectively. The charges are transferred to the common floating diffusion (n⁺) and the voltage signals are read out through a source follower buffer in the pixel.

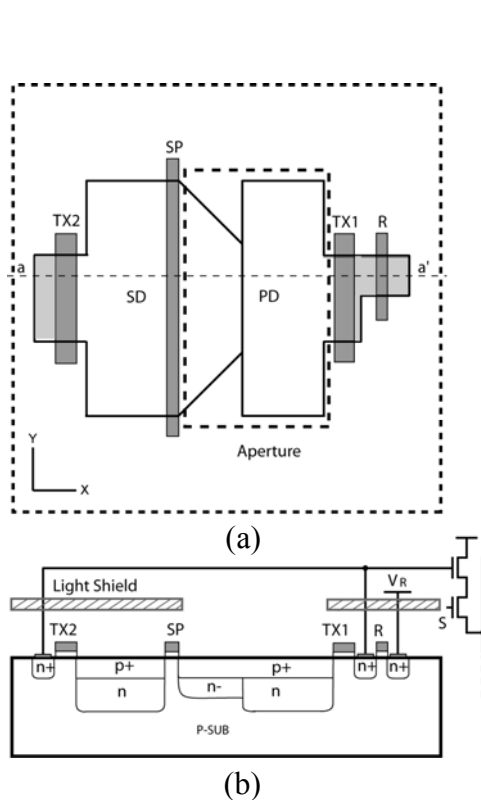


Figure 1. (a) Simplified structure and (b) Cross section at line aa' of the proposed pixel.

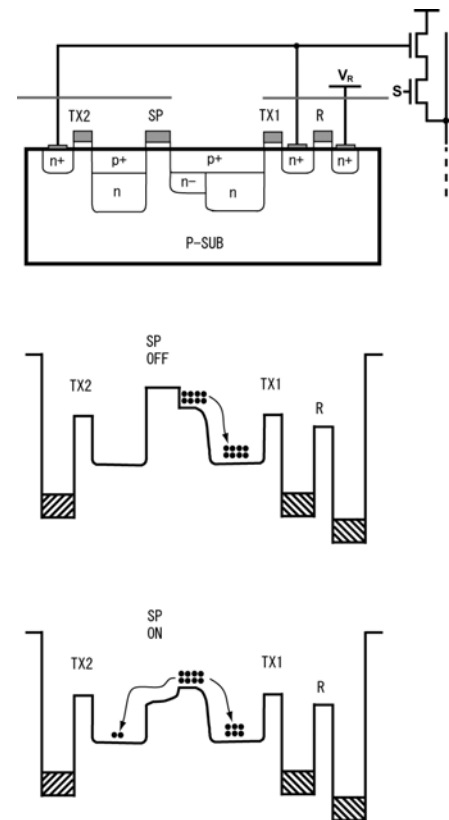


Figure 2. Direction of charge flows when the SP gate is opened and closed.

3. Dynamic Range Expansion

The most important task in operating this sensor is the sensitivity control of the signal charge in the SD. Two techniques can be used for controlling the sensitivity of the signal charge in the SD. One is by controlling the SP gate and the other is by controlling the accumulation time in the SD.

3.1. Sensitivity control with SP gate

Figure 2 shows the principle of the sensitivity control of the SD signal by the SP gate. If the SP gate perfectly controls the sensitivity in the SD, wide dynamic range imaging with small motion blur is possible with only controlling the SP gate. Figure 3 shows the timing diagram of the wide dynamic range imaging with controlling the SP gate. The accumulation time in the PD can be maximally set to the frame period, T_F , which is 33 ms at 30 fps. The SP gate is repeatedly opened for short period of time, T_{SP} at every cycle of the signal readout of one row, whose period is denoted by T_H . The dynamic range expansion ratio R_{DE} is defined as

$$R_{DE} = \frac{Q_{PD}}{Q_{SD}} \quad (1)$$

where Q_{PD} and Q_{SD} are photo-induced charges in the PD and SD, respectively. The Q_{PD} is expressed as

$$Q_{PD} = S_{PD} T_F \quad (2)$$

where S_{PD} is the sensitivity of the PD. The Q_{SD} is expressed as

$$Q_{SD} = S_{SD} T_F \left(\frac{T_{SP}}{T_H} \right) + S_{SDC} T_F \quad (3)$$

where S_{SD} is the sensitivity of the SD, and S_{SDC} is the sensitivity of the SD when the SP gate is closed. The S_{SDC} is due to carriers generated by light penetrated into the SD and diffused from deep inside the pixel. The R_{DE} is given by

$$R_{DE} = \frac{S_{PD}}{S_{SD} \left(\frac{T_{SP}}{T_H} \right) + S_{SDC}} \quad (4)$$

For efficient control, the S_{SDC} has to be minimized. If $S_{SDC}=0$, the R_{DE} can be controlled effectively by the ratio T_{SP}/T_H .

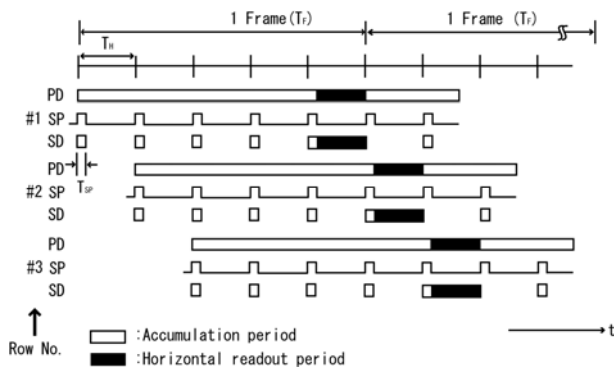


Figure 3. Accumulation and readout timing of proposed sensitivity control with SP gate.

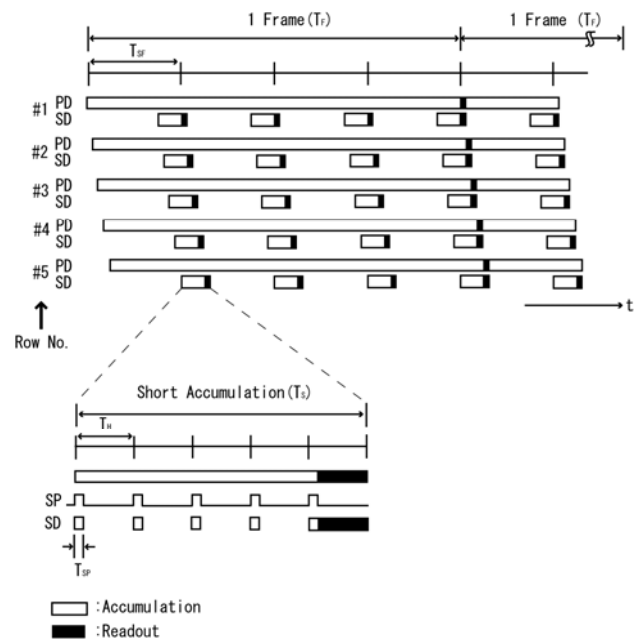


Figure 4. Accumulation and readout timing of proposed multiples short accumulation and gated charge storage in SD.

3.2. Multiple short accumulation and gated charge storage in SD

Figure 4 shows the accumulation and readout timing for the combination of multiple short accumulations and the gated charge storage in the SD. In this technique, charge accumulation time in the PD region is set to full frame period, T_F , to achieve high sensitivity, while the charge accumulation time in the SD is set to a shorter time, T_S . The short time accumulation in the SD and the readout are repeated M times. During T_S , the SP gate is repeatedly opened for short period of time, T_{SP} .

The dynamic range expansion ratio in this method is given by

$$R_{DE} = \frac{Q_{PD}}{Q_{SD}} \quad (5)$$

where, the Q_{PD} is expressed as

$$Q_{PD} = S_{PD} T_F \quad (6)$$

and the Q_{SD} is given by

$$Q_{SD} = S_{SD} T_S \left(\frac{T_{SP}}{T_H} \right) + S_{SDC} T_S \quad (7)$$

Therefore, the dynamic range expansion ratio can be expressed as

$$R_{DE} = \frac{T_F}{T_S} \times \frac{S_{PD} T_H}{(S_{SD} T_{SP} + S_{SDC} T_H)} \quad (8)$$

Using the short accumulation, the R_{DE} can be set to a large ratio, even if the S_{SDC} is not small enough.

There are two merits in the multiple sampling for short accumulation signals in the SD. One is the reduction of motion blur in the synthesized wide dynamic range image, because by adding multiple accumulation signals, the duration of image capturing in the PD and SD can be similar.

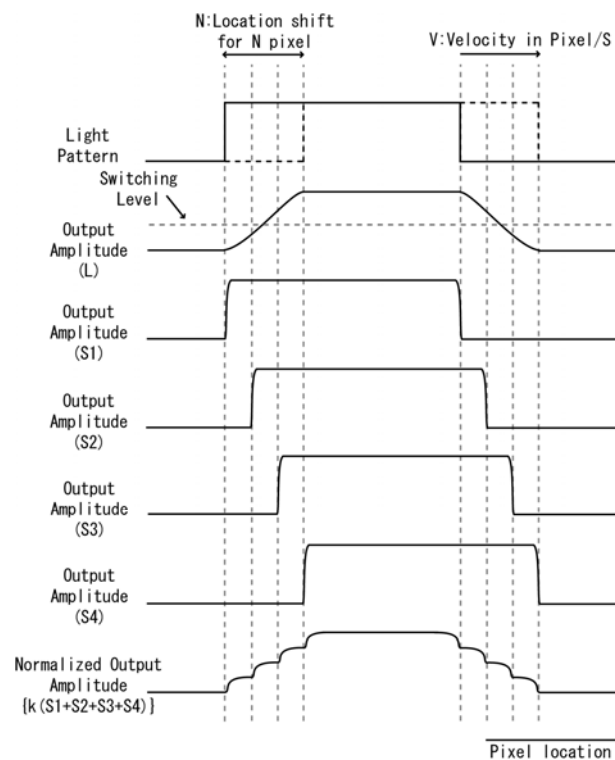


Figure 5. Moving light pattern captured by a line sensor.

Figure 5 explains the effect of multiple sampling in the reduction of the motion blur effect in the synthesized wide dynamic range image. When a moving light pattern is captured by a line sensor, the long accumulation signal, L , shows a trapezoidal shape. On the other hand, short accumulation signals, $S1 \sim S4$, show a rectangular shape. However, the addition of short accumulation signals shown at the bottom of Figure 5 has a shape similar to that of L .

In contrast, the implementation of dual and multiple sampling methods [3,5], the difference of image capturing duration between the longest accumulation signal and the shortest accumulation signal causes motion blur appears in the synthesized images.

Another merit of the multiple sampling technique is the reduction of SNR dip [8] at the boundary of the high and the low illumination regions when accumulation time is switched from T_F to T_S . If the noise is dominated by photon shot noise, it is given by

$$SNR_{dip} = 10 \log_{10} \left(\frac{T_F}{T_S} \times \frac{S_{PD}}{(S_{SD} + S_{SDC})} \times \frac{1}{M} \right) \quad (9)$$

where T_F and S_{PD} are the accumulation time and sensitivity of the PD, and T_S and S_{SD} are those of the SD, respectively. Therefore, the SNR dip is improved by $10 \log_{10} M$ dB using the M-time sampling.

4. Enhancement of SP gate controllability

To enhance the SP gate controllability, or to increase the sensitivity ratio S_{SD}/S_{SDC} , the formation of a blocking layer under the SD which blocks the diffused photo-electrons from deep inside the pixel as shown in Figure 6(a), is useful. Relatively highly doped p-layer, p-type well region, is formed under the SD region. The difference of doping concentration between p-type well and p-type substrate creates a potential barrier to electrons generated at deep inside, preventing the electrons from flowing into the SD region.

The effect of the blocking layer is confirmed by device simulations. In Table 1, the size parameters used in the simulations are shown. Figure 6 shows a simulation result to show the effectiveness of the blocking layer. It shows movement of a photo-electron diffused from deep inside the pixel to the surface in case of a pixel with [Figure 6(a)] and without [Figure 6(b)] the blocking layer formed under the SD, respectively. Using the blocking layer, the photo-electron diffused from deep inside the pixel reaches to the PD region, while it comes to the SD region if the blocking layer is not used.

Table 1

Size parameters in the simulations

Pixel size	$7.5 \mu\text{m} \times 7.5 \mu\text{m}$
PD size	$3.8 \mu\text{m}^2$
SD size	$2.6 \mu\text{m}^2$
Aperture ratio	12 %

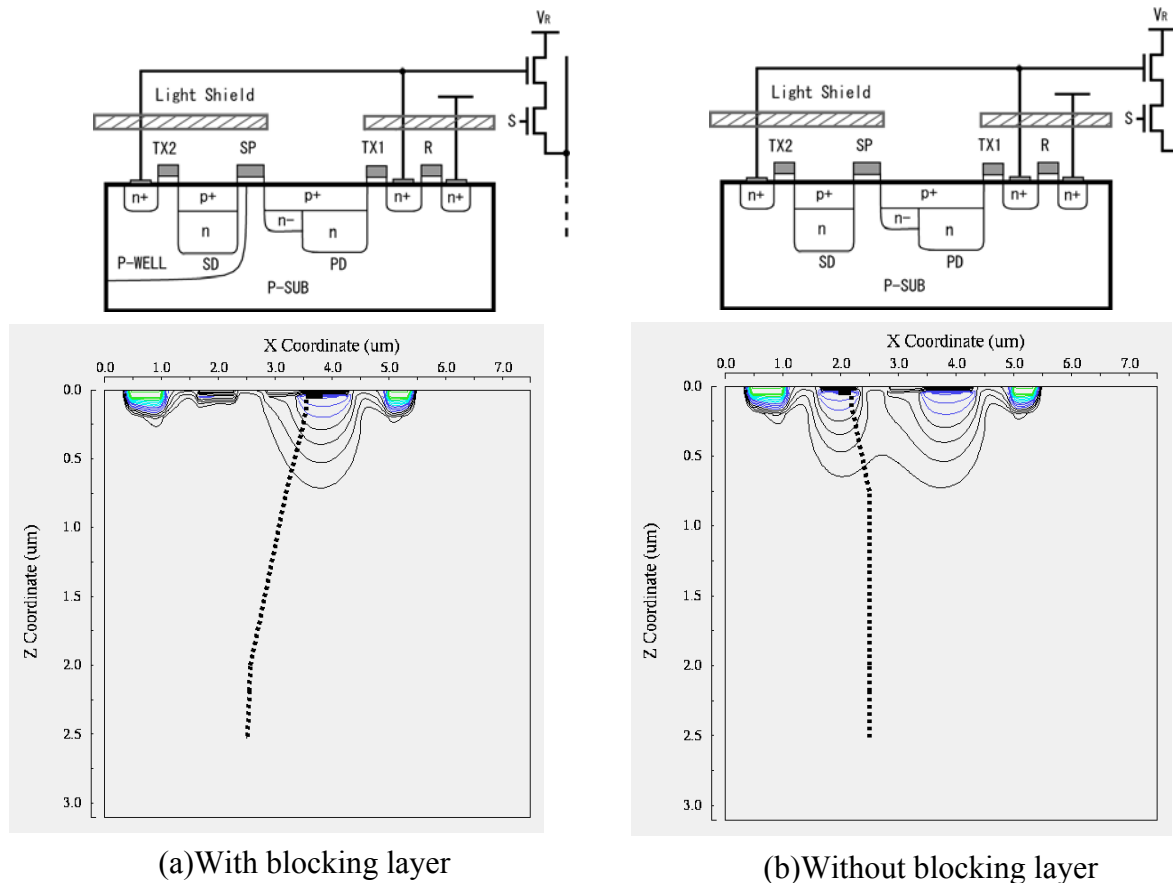


Figure 6. The movement of photo-electron diffused from deep inside the pixel to the surface.

Fig. 7 shows the sensitivity ratio, S_{SDC}/S_{PD} as a function of the wavelength of light for the pixel with and without the blocking layer under the SD. Without the blocking layer, the sensitivity ratio has a large dependency to the light wavelength. With the blocking layer, the sensitivity when the SP gate is closed has relatively low sensitivity and less dependent to the incident light wavelength.

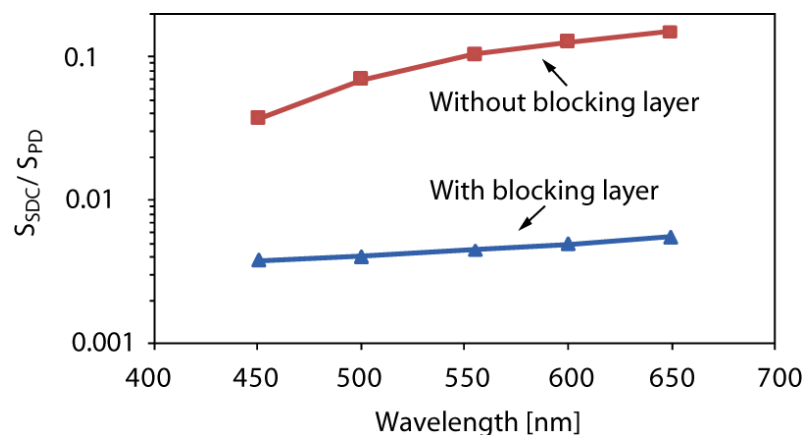


Figure 7. Sensitivity when the SP gate is closed.

The sensitivity control in the SD with the SP gate is simulated. In the simulation, the blocking layer under the SD is used. Figure 8 shows the sensitivity ratio as a function of the wavelength of incident light when the SP gate is closed (S_{SDC}/S_{PD}) and opened (S_{SD}/S_{PD}). In the simulation, the SP gate open period, T_{SP} is set to full period in every cycle of the signal readout of one row, T_H , and the full frame period, T_F , is set to 33 ms. The simulation result shows the sensitivity ratio, S_{SD}/S_{PD} can be controlled efficiently by the SP gate. The sensitivity ratio S_{SD}/S_{SDC} given by

$$\frac{S_{SD}}{S_{SDC}} = \frac{S_{SD}/S_{PD}}{S_{SDC}/S_{PD}} \quad (10)$$

is calculated to be 5 to 14 depending on the incident light wavelength. For meeting the requirements of both the wide dynamic range and small motion blur, the controllability of the SD sensitivity with the SP gate is very important. Using the blocking layer, the controllability of the SD sensitivity with SP gate can be sufficiently increased.

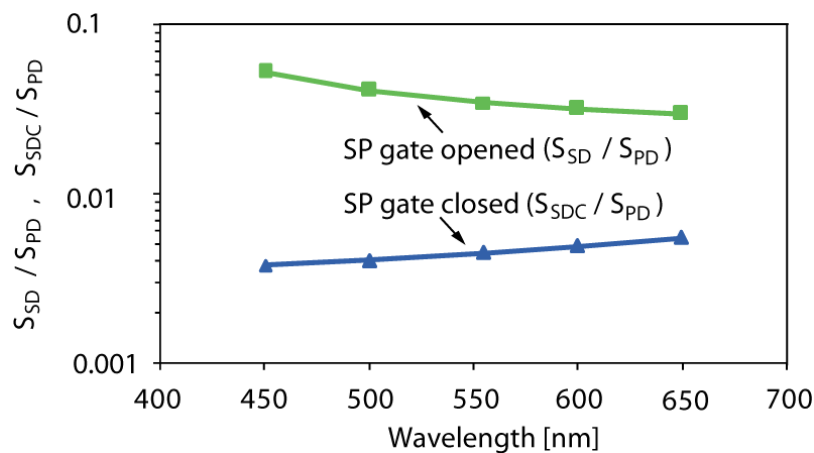


Figure 8. Sensitivity when the SP gate is opened and closed.

5. Implementation for testing wide dynamic range imaging with multiple short accumulations

The proposed pixel structure requires additional process steps for the SP gate control of sensitivity. As a preliminary study to this final goal, a prototype CMOS image sensor using standard CMOS image sensor process is implemented. In the standard CMOS image sensor technology, the lightly doped n-type region in the PD and p-type region under the SD cannot be created. Therefore, in the prototype chip, the sensitivity control with the accumulation time and the number of the readout times only in the SD is tested.

The equivalent pixel structure is shown in Figure 9. The light is mainly irradiated to the PD region, and the SD region receives leakage light flux only. Figure 10 shows the chip micrograph of the prototype wide dynamic range CMOS image sensor with $0.18 \mu\text{m}$ technology. The pixel pitch is $7.5 \mu\text{m}$. The aperture ratio is 17.5 % and a microlens is used at the top of the structure.

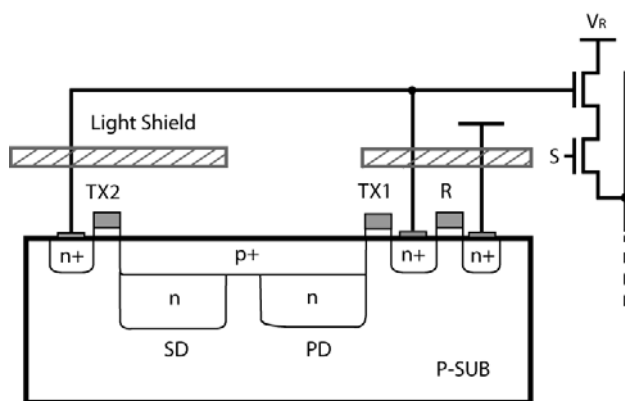


Figure 9. Equivalent pixel structure implemented.

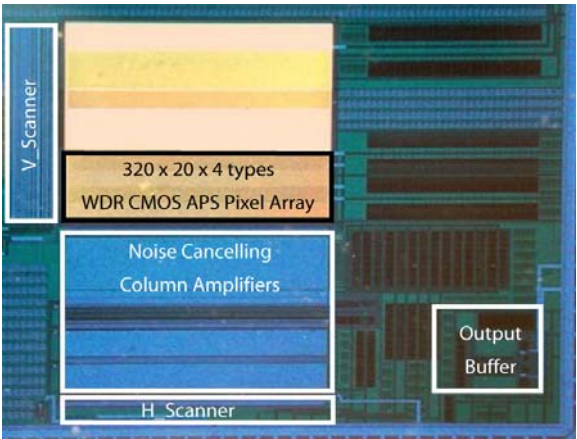


Figure 10. Fabricated wide dynamic range CMOS image sensor chip

The sensor contains a vertical and horizontal shift registers, noise canceling column amplifiers and output buffers. The pixel array is connected to noise canceling column amplifiers where the reset noise and the fixed pattern noise are cancelled using correlated double sampling (CDS) technique. The analog sensor outputs are connected to a 12bits AD converter on a camera board for testing.

Control pulses for the chip are generated by an off-chip FPGA board, so that the accumulation and readout timing can be manipulated by an appropriate verilog HDL program.

Figure 11 shows the accumulation and readout timing of the actually implemented sensor. In the implemented pixel structure, the charge accumulation time in the PD is set to full frame period, T_F , which is 33 ms at 30 fps and the output is read out once per frame, while the charge accumulation time in the SD is set to shorter time, T_S , which is 100 μ s per sub-frame. Therefore, the ratio of T_F to T_S is 330. The short accumulation in the SD and the readout are repeated multiple times per frame, e.g. four times in Figure 11.

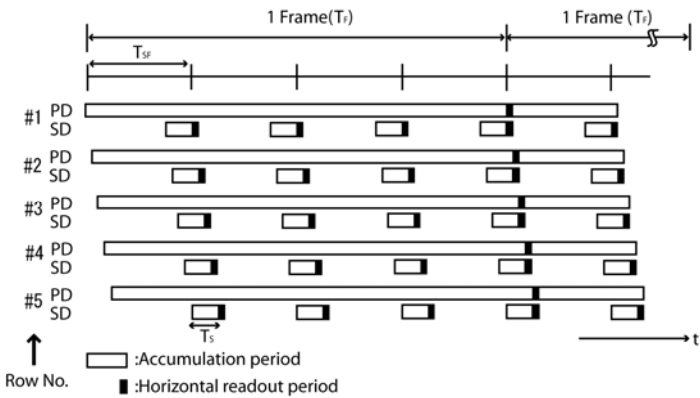


Figure 11. Accumulation and readout timing of the implemented sensor.

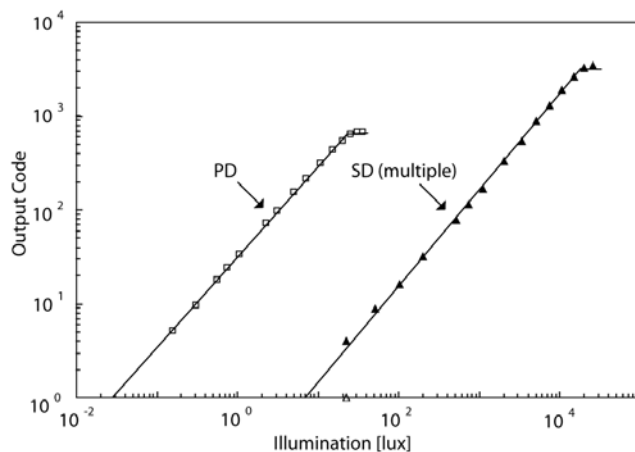


Figure 12. Measured PD and SD outputs with four time sampling.

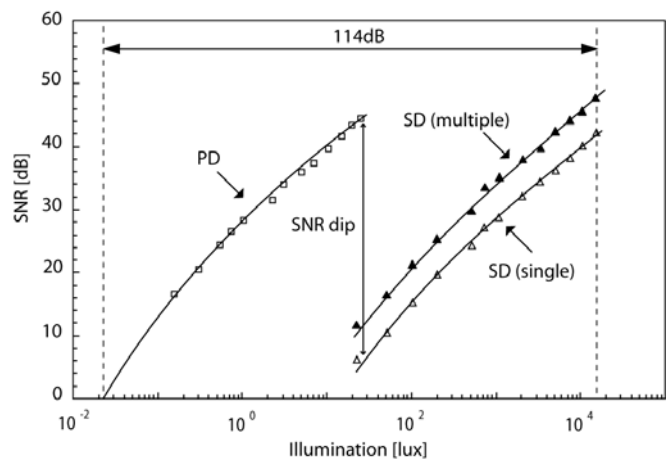


Figure 13. Measured SNR of the prototype image sensor.

The linearity of the PD and SD outputs of the image sensor is measured as shown in Figure 12. The light intensity is controlled by ND filters and an iris in a filter box. Measurement results show that the image sensor has a sufficient linear response. The linearity up to 22 lx and 15,000 lx is obtained in the PD and SD output signals, respectively. The SNR characteristic of the proposed image sensor is shown in Figure 13. The minimum illumination level when the SNR equals to 0 dB is 0.03 lx and the maximum illumination level is 15,000 lx. The combined dynamic range with the PD and SD signals is 114 dB.

From Figure 13, the SNR dip without multiple sampling is 38 dB. Using the sampling of four times in the SD signal, the SNR dip is reduced to 32 dB. Thus, the SNR dip is improved by 6 dB and it is explained by the calculation with Eq. (9). The SNR dip depends on the choice of T_F/T_S , and if the application of the wide dynamic range sensor does not allow a large SNR dip, the ratio T_F/T_S has to be reduced and the resulting dynamic range is also reduced. By using the multiples sampling, the dynamic range can be increased compared with the single sampling case under the condition of the same SNR at the switching point. From Eq. (9), the dynamic range enhancement using the multiple sampling of M times is a factor of M if the noise is dominated by photon shot noise. On the other hand, if the readout random noise dominates, the dynamic range enhancement factor using the M samplings is $\sqrt{M}$. Figure 14 shows the measured dynamic range enhancement factor to the T_F/T_S . In the measurement result of Figure 14, the factor is 2.75 to 3.45, depending to the choice of T_F/T_S .

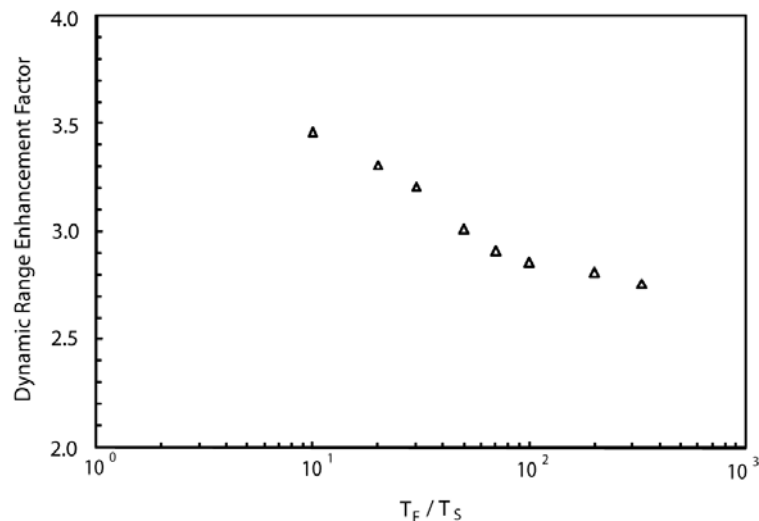


Figure 14 Measured dynamic range enhancement factor using 4 samplings.

6. Conclusions

Dynamic range expansion techniques for CMOS image sensors with dual charge storage in a pixel and multiple sampling have been described. Two types of dynamic range expansion techniques have been discussed; the sensitivity control with separation gate and the multiple short accumulations in a storage diode. The sensitivity control with the separation gate technique has been simulated and the simulation result shows that the sensitivity ratio of the storage diode signal to the photodiode signal can be controlled by the separation gate. The formation of a blocking layer under the storage diode is necessary to increase the controllability by the separation gate. A prototype chip is implemented for testing the dynamic range expansion with the multiple short accumulation signals. The experimental results show that the implemented sensor has a linear response with the illumination level and the multiple sampling technique for short accumulation signals allows flexible control of dynamic range and reduces the signal-to-noise ratio dip at the switching point of the long accumulation signal to the short accumulation signal in the synthesized wide dynamic range image.

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References and Notes

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