

Article

The Design and Characterization of a Prototype Wideband Voltage Sensor Based on a Resistive Divider

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Abstract: The most important advantage of voltage dividers over traditional voltage transformers is that voltage dividers do not have an iron core with non-linear hysteresis characteristics. The voltage dividers have a linear behavior with respect to over-voltages and a flat frequency response larger frequency range. The weak point of a voltage divider is the influence of external high-voltage (HV) and earth parts in its vicinity. Electrical fields arising from high voltages in neighboring phases and from ground conductors and structures are one of their main sources for systematic measurement errors. This paper describes a shielding voltage divider for a 24 kV medium voltage network insulated in SF6 composed of two resistive-capacitive dividers, one integrated within the other, achieving a flat frequency response up to 10 kHz for ratio error and up to 5 kHz for phase displacement error. The metal shielding improves its immunity against electric and magnetic fields. The characterization performed on the built-in voltage sensor shows an accuracy class of 0.2 for a frequency range from 20 Hz to 5 kHz and a class of 0.5 for 1 Hz up to 20 Hz. A low temperature effect is also achieved for operation conditions of MV power grids.

Keywords: resistive divider; voltage sensor; high-voltage calibration; electric field; frequency response; capacitive effect

1. Introduction

High-voltage (HV) dividers are a good alternative to traditional voltage transformers for power frequency measurements on medium- and high-voltage power lines [1,2]. An HV divider connected to a digital recorder is an appropriate measuring system for both continuous operation voltages (50 or 60 Hz, harmonics and subharmonics) and temporal or transient over-voltages (such as ferroresonances, switching, and lightning over-voltages) [3]. However, at present, the traceability for the measurement of harmonics and over-voltages is missing in most of the electrical grids because conventional voltage transformers are used.

Distributed generation of electric power, a common feature of smart grids, involves increasing levels of power electronics integration, such as power converters, electronic controllers, and loads with a greater number of semiconductor components. Consequently, the voltage wave of smart grids contains an increasing amount of harmonics. The international standards [4,5] evolved in recent years require measurements in frequency ranges up to 5 kHz. However, it is known that conventional measuring transformers [6–9] have a cut-off frequency no higher than 1 kHz. Furthermore, saturation phenomena appear for frequencies below grid frequency (50/60 Hz). For these reasons, new HV measuring systems have to be developed with metrological capabilities from a few hertz to several kilohertz for smart grids that are characterized in accordance with present international standards [10].

To date, high voltage resistive dividers [11,12] have not been used in electrical networks as voltage transfer devices. At first, this was due to the power supply requirements of voltmeters, energy meters and relays; at present, this is due to the different technical challenges to be solved, such as the capacitive influence of nearby metal parts connected to earth or high voltage that causes significant ratio and angle errors. Influence of overvoltages and high temperature changes are other challenges that must be solved. However, classical technology of HV dividers has been developed to design a double resistive-capacitive divider, one integrated inside the other, insulated in SF₆, and with a flat frequency response ($\pm 0.2\%$) from 20 Hz to 5 kHz, for use in 20 kV power grids. The divider design and the electrical magnitudes of each component have been carefully chosen to achieve an industrial solution to be used in power grids. The prototype has passed the insulation coordination tests (125 kV for lightning impulses and 50 kV for power frequency voltage) maintaining its technical performances (a class of 0.2 from 20 Hz up to 5 kHz). This prototype opens a practical industrial approach to the on-line monitoring of power quality and to knowledge of grid overvoltages (temporary, switching, and lightning) to be supported by the grid components (power transformers, surge arresters, cables, etc.).

2. Voltage Sensor

2.1. Physical Design

The voltage divider consists of a 50 M Ω HV resistive branch, composed of two HV film resistors, R_1 and R_2 , of 25 M Ω , each one connected in series (Figure 1). The low-voltage (LV) resistive branch of the divider, r , of 50 k Ω is composed of four 200 k Ω resistors arranged in parallel in a coaxial configuration. Two blocks of four capacitors, with a rated capacitance of 202 pF each form two capacitances, C_p , of 808 pF, connected in series. The HV resistor is placed on the axis of the set of capacitors (Figure 1). The first block of capacitors is connected in parallel with the first resistor of the HV branch through an upper electrode and a central electrode. The second block of capacitors is connected between the central electrode and the metallic enclosure (see Figure 1). The central electrode serves as mechanical support for the two capacitor blocks and the two resistors of the HV branch. The configuration is designed to achieve a voltage distribution along each HV resistor for higher frequencies as close as possible to the voltage distribution obtained for 50 Hz. The voltage distribution along the HV resistors was determined by FEM simulation for the frequency range from 50 Hz to 5 kHz (see Figure 2a). The central electrode is connected to joint point of both HV resistances. The set is in a steel–aluminum casing to achieve a good shielding. The LV branch is also arranged in an aluminum compartment, different to the HV branch, although sharing the same gas insulation. The SF₆ gas at 0.2 MPa is used as an internal insulation to pass dielectric tests corresponding to the insulation level of 24 kV. A plug-in connector is used to be connected to the cable entry of the enclosed metal box.

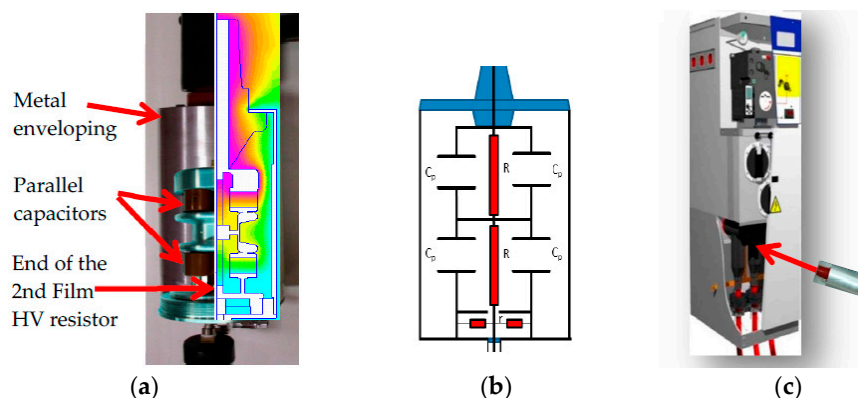


Figure 1. Voltage divider for MV switchgear under metal enclosure: (a) The cut-away view of the voltage divider enclosed in a metallic enveloping; (b) schematic electrical circuit; (c) general view of the HV divider sensor to be connected in a MV cabin.

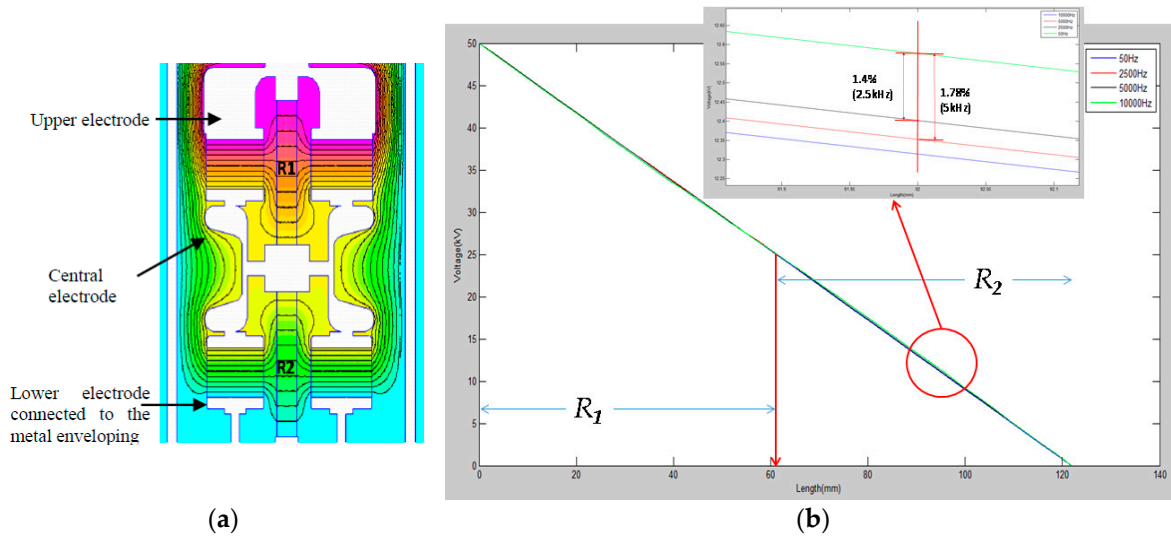


Figure 2. Voltage distribution: (a) Cut-away view of equipotential lines in the voltage divider; (b) voltage distribution along the two resistors of the HV branch for frequency range 50 Hz–5 kHz.

2.2. Simplified Electrical Model

The simplified electric circuit of the double RC voltage divider is shown in Figure 3a. No inductance effect is considered because the cylindrical configuration of the divider and its size lead to an inductance less than 1 μH , which does not affect the frequency operation range of the divider. Each resistor of the HV branch, R_1 and R_2 , is modeled through an ideal resistance, R , in parallel with a capacitance: C_s for the first resistor R_1 and C_s' for the second one R_2 . The parallel capacitance C_s and C_s' includes not only the stray capacitance of the resistor but also the capacitance between the end electrodes of each HV resistor, R_1 and R_2 . Consequently, a different value of these capacitances C_s and C_s' associated to each HV resistor is expected. The LV branch is represented by an ideal resistor r and a parallel capacitance C_c' (see Figure 3a) in which two additional capacitive effects are included: the coaxial cable C_c and of the digital recorder C_r (20 pF). In practice, the impedance of the recorder is considered a resistance of 1 M Ω , r^* , that must be added to the value of the LV resistance. The capacitances, C_{e1} , C_{e2p} , and C_e' , represent the earth capacitive effect between the metallic enveloping and the upper electrode, the central electrode, and the LV resistor respectively. The C_{e2p} also includes any small difference between the first and the second capacitor blocks.

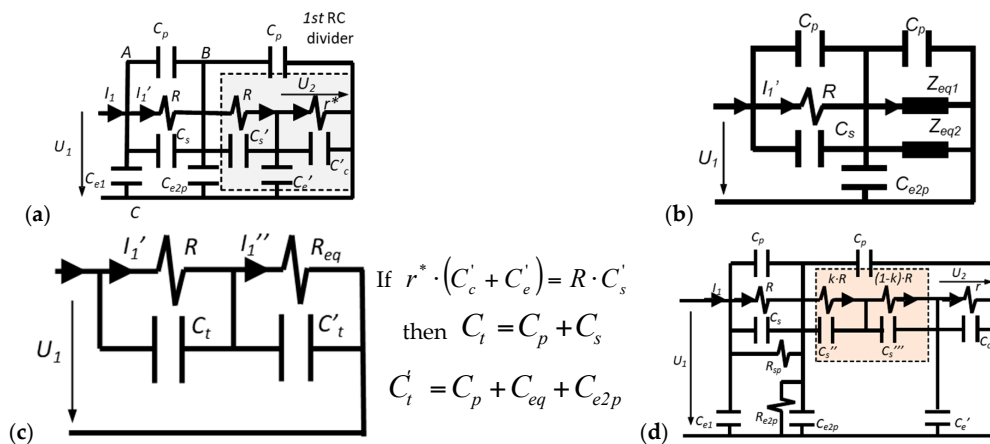


Figure 3. Equivalent electric schemes: (a) simplified divider model; (b) equivalent circuit replacing the 1st RC divider by two impedances in parallel Z_{eq1} and Z_{eq2} ; (c) equivalent model 2nd RC divider; (d) improved divider model analyzed in Section 4.

The circuit of Figure 3a is a simplified circuit for a specific frequency range to be determined. In this circuit, the LV branch ($r^*/C_c' + C_e'$) with the second block (R/C_s') of the HV branch form the first RC divider, whose equivalent circuit is composed of two parallel impedances Z_{eq1} and Z_{eq2} shown in Figure 3b.

$$Z_{eq1} = \left(\frac{1 - (s \cdot c)^2}{1 - (s \cdot a)^2} \right) \cdot R + \left(\frac{1 - (s \cdot c)^2}{1 - (s \cdot b)^2} \right) \cdot r^* \quad (1)$$

$$Z_{eq2} = \left(\frac{1 - (s \cdot c)^2}{1 - (s \cdot a)^2} \right) \cdot \left(\frac{R}{R_{eq}} \right)^2 \cdot C_s' + \left(\frac{1 - (s \cdot c)^2}{1 - (s \cdot b)^2} \right) \cdot \left(\frac{r^*}{R_{eq}} \right)^2 \cdot (C_c' + C_e') \quad (2)$$

where

$$a = R \cdot C_s', b = r^* \cdot (C_c' + C_e'), c = R_{eq} \cdot C_{eq} \quad (3)$$

if the following condition is met:

$$r^* \cdot (C_c' + C_e') = R \cdot C_s' \quad (4)$$

Thus, both impedances Z_{eq1} and Z_{eq2} become R_{eq} and C_{eq} :

$$R_{eq1} = R + r^* \quad (5)$$

$$C_{eq} = \left(\frac{R}{R_{eq}} \right)^2 \cdot C_s' + \left(\frac{r^*}{R_{eq}} \right)^2 \cdot (C_c' + C_e') \quad (6)$$

Consequently, the circuit of Figure 3b leads to the circuit of Figure 3c in the second RC divider, in which the first RC divider is therein. It justifies the name “double RC divider” that the authors have given to this voltage sensor. Using this design, the earth capacitances C_{e2} and C_e' became a part of the total parallel capacitances of the circuit shown in Figure 3c. An appropriate selection of the capacities C_{e2p} , C_e' , C_s , C_s' , and C_c is required to compensate the ratio and phase displacement errors of the divider. An improved model is shown in Figure 3d, in which the main difference from the simplified one is that the second resistor R of the HV branch is split into two parts and a stray capacitance is associated with each one. In addition, a parallel leakage resistance is introduced in each capacitor block to represent its insulation resistance. The behavior of this improved model is explained in detail by simulation in Section 4.

The transfer function of the divider is given by the following formula:

$$G_d(s) = \frac{U_2}{U_1} = r \cdot \frac{1 + s \cdot R_{eq} \cdot C_{eq}}{1 + s \cdot r^* \cdot C_c'} \cdot \frac{1}{\left[R_{eq} + R \cdot \left(\frac{1 + s \cdot R_{eq} \cdot C_t'}{1 + s \cdot R \cdot C_t} \right) \right]} \quad (7)$$

For direct voltage ($s = 0$) the transfer function is transformed in the following:

$$G_d(s = 0) = \frac{r^*}{R_{eq} + R} \quad (8)$$

and the normalized Laplace transfer function ($G_{nd}^*(s = 0) = 1$) by the following one:

$$G_{nd}^*(s) = \frac{G_d(s)}{G_d(s = 0)} = \frac{R + R_{eq}}{R_{eq}} \cdot \frac{1 + s \cdot R_{eq} \cdot C_{eq}}{1 + s \cdot r^* \cdot C_c'} \cdot \frac{1}{\left[1 + \frac{R}{R_{eq}} \cdot \left(\frac{1 + s \cdot R_{eq} \cdot C_t'}{1 + s \cdot R \cdot C_t} \right) \right]} \quad (9)$$

Each RC divider should be designed to meet the following requirements:

Requirement of the 1st RC divider:

$$R \cdot C_s' = r^* \cdot (C_c' + C_e') = r^* \cdot C_c'' \quad (10)$$

Requirement of the 2nd RC divider:

$$R_{eq} \cdot C'_t = R \cdot C_t \quad (11)$$

where

$$C_t = C_p + C_s, C'_t = C_p + C_{eq} + C_{e2p} \quad (12)$$

If both RC dividers meet these requirements, the normalized transfer function will be 1 p.u. The capacitances, C_s and C'_s , must be designed to comply with Equation (13), taking into account Equation (6):

$$C_s = \frac{R_{eq}}{R} \cdot C_{eq} + \frac{R_{eq}}{R} \cdot C_e + \frac{(R_{eq} - R)}{R} \cdot C_p \quad (13)$$

and the length of the coaxial cable must be chosen to comply the following condition:

$$\text{Length coaxial cable} = \frac{C'_c - C_r}{c_c} \quad (14)$$

where c_c is the capacitance per length unit of the coaxial cable of 66 pF/m, and C_r is the capacitance of the digital recorder.

3. Frequency Response Analysis

3.1. Frequency Response Analysis Using the Simplified Model

In general, Equations (10) and (11) are not fully complied. One of the most common causes is the cable length of the coaxial cable used to connect with the digital recorder that modifies the C_c value. It can be slightly different from the theoretical value that satisfies Equations (10) and (11). The theoretical ratio error and the phase displacement error caused by the length of the coaxial cable can be determined using the transfer function, i.e., Equation (9), derived from the simplified circuit. In this simplified circuit, the theoretical maximum ratio error caused by the cable length of the coaxial cable can be determined through that equation for $s \rightarrow \infty$:

$$\lim_{s \rightarrow \infty} G_{nd}(s) = \frac{R_{eq} + R}{r^*} \cdot \frac{C_{eq}}{C'_c} \cdot \frac{C_t}{(C_t + C'_t)} \quad (15)$$

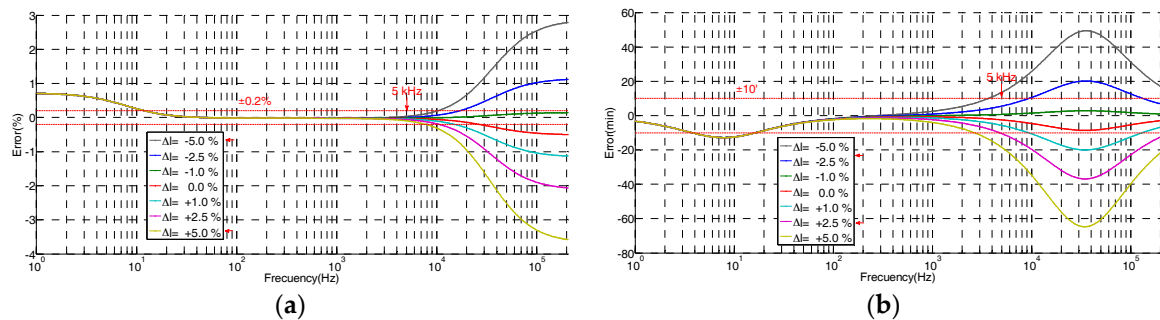
To apply Equation (9) to the designed sensor, its electrical parameters must be determined. Most of them are determined by measurements. The electrical data of the digital recorder (Z_r and C_r) are collected from the manufacturer's data sheet. Other parameters were estimated by modeling in order to achieve the best fitting to the actual measured in the laboratory. All parameter values of the built HV sensor are shown in Table 1.

The theoretical frequency response derived from Equation (9) of the built HV sensor is shown in Figure 4 for different coaxial cable lengths. The difference between the real length of the coaxial cable and the reference length value given by Equation (10) provokes a clear ratio and angle errors for frequencies higher than 2 kHz. When the cable length is larger than the reference value, a negative ratio error is expected (see Figure 4). Length variations around $\pm 5\%$ (around ± 5 cm of the coaxial cable) are acceptably to keep ratio error within an accuracy class of 0.2, but length variations lower than $\pm 2.5\%$ are recommended if the phase displacement error is to be kept within the admissible limits for a maximum frequency of 5 kHz. This length requirement for the coaxial cable can be easily fulfilled if the global measuring set, composed of the HV divider, a coaxial cable, and a digital recorder, is supplied by the same manufacturer.

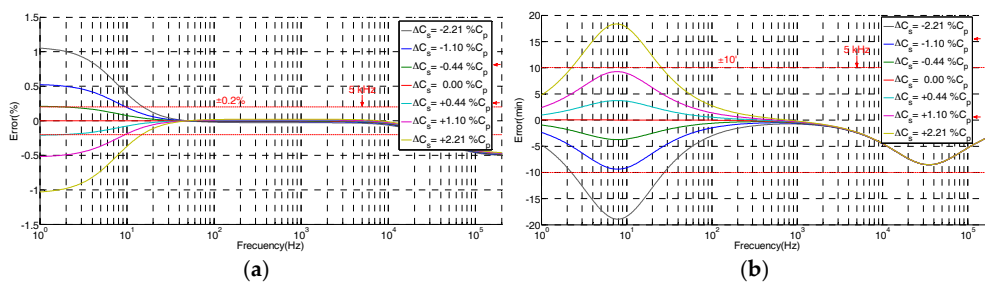
Table 1. Electrical parameters of the built high-voltage (HV) sensor.

Parameter	Primary Value	Determined By	Simplified Model Figure 3b	Simplified Model Figure 3b	Improved Model Figure 3d
R	25 M Ω	Measurements	25 M Ω	25 M Ω	25 M Ω
r	50 k Ω	Measurements	-	-	-
Z_r	1 M Ω	Data Sheet	-	-	-
$r^* = r \cdot Z_r / (r + Z_r)$	-	Derived	47.6 k Ω	47.6 k Ω	47.6 k Ω
C_p	809.2 pF	Measurements	809.2 pF	809.2 pF	809.2 pF
$C_c^{(1)}$	63.8 pF	Measurements	-	-	-
C_r	20.0 pF	Data sheet	-	-	-
$C_c' = C_c + C_r$	83.8 pF	Derived	-	-	-
C_e'	12.1 pF	Measurements	12.1 pF	12.1 pF	12.1 pF
$C_c'' = C_c' + C_e'$	-	Derived	95.9 pF	95.9 pF	95.9 pF
$C_{e1}^{(3)}$	29.5 pF	Measurements	-	-	29.5 pF
C_{e2p}	12.5 pF	Measurements	12.5 pF	12.5 pF	12.5 pF
C_s	2.2 pF	Measurements	2.2 pF ⁽²⁾	2.2 pF ⁽²⁾	2.2 pF ⁽²⁾
C_s'	0.18 pF	Modeling	0.18 pF	0.18 pF	-
C_s''/C_s'''	-	Modeling	-	-	0.20/0.87 pF
R_{equ}	-	Derived (5)	25 048 k Ω	25 048 k Ω	-
C_{equ}	-	Derived (6)	0.15 pF	-	-
C_t	-	Derived (12)	-	811.4 pF	-
C_t'	-	Derived (12)	-	821.9 pF	-
R_s	-	Modeling	-	-	865 M Ω
R_{e2}	-	Modeling	-	-	658 M Ω
k	-	Modeling	-	-	0.96

⁽¹⁾ This capacitance corresponds to a length of the coaxial cable 97 cm (66 pF/m). ⁽²⁾ The measured value is different to the reference value 14.3 pF given by Equations (11) and (12). ⁽³⁾ The capacitance difference between the magnitudes of the 2nd capacitor block C_p and the 1st one is included in the C_{e2p} value.

**Figure 4.** Errors due to difference of length of coaxial cable C_c regarding to the theoretical value regarding the simplified model of Figure 3: (a) ratio error; (b) phase displacement error.

The theoretical frequency response derived from the simplified model (Equation (9)) is shown in Figure 5 for different C_s values referred to a percentage of C_p . It justifies the change of the ratio error and angle error for lower frequencies due to changes of the C_s value regarding the reference value given by Equation (11).

**Figure 5.** Errors due to different C_s values using the simplified model of Figure 3: (a) ratio error; (b) phase displacement error.

3.2. Measuring the Response Frequency of the Built Sensor

Taking into account the data of Table 1, the two restrictions referred in Equations (10) and (11) are checked for the built sensor (see Table 2). It can be observed that Equation (10), corresponding to the restriction of the 1st divider, is better complied (0.5%) with than the restriction given by Equation (11) associated with the 2nd divider (1.5%). The deviation due to the 2nd divider is caused by a real value of $C_s = 2.2$ pF (measured) when it should be 14.3 pF to satisfy Equation (11). An improved design of the upper electrode and the central electrode would permit a reduction in this discrepancy in order to obtain a class of 0.2 from 1 Hz to 5 kHz with the same divider ratio value, as is shown in Figure 5a.

Table 2. Checking restrictions of Equations (10) and (11) for the built voltage sensor.

Restriction of 1st RC Divisor	Equation (1) $R \cdot C_s' = r^* \cdot (C_c' + C_e')$	Restriction of 2nd RC Divisor	$R \cdot C_t = R_{eq} \cdot C_t'$
$R \cdot C_s'$ (k Ω ·pF)	4545	$R \cdot C_t$ (k Ω ·pF)	20,284
$r^* \cdot (C_c' + C_e')$ (k Ω ·pF)	4568	$R_{eq} \cdot C_t'$ (k Ω ·pF)	20,587

The frequency response of the built voltage sensor was measured (see Figure 6) for different C_c values (different cable lengths) in the LCOE calibration laboratory in order to check Equation (9) of the simplified model. It was also observed that, for lengths of the coaxial cable larger than the reference value (97 cm), the tendency of the ratio error and the angle error is negative for higher frequencies (>200 kHz) according to the simplified model, but a preliminary oscillation is observed in the interest frequency range (2–100 kHz). This effect is not detectable by the simplified model. For this reason, the improved model shown in Figure 3d is introduced in Section 4.

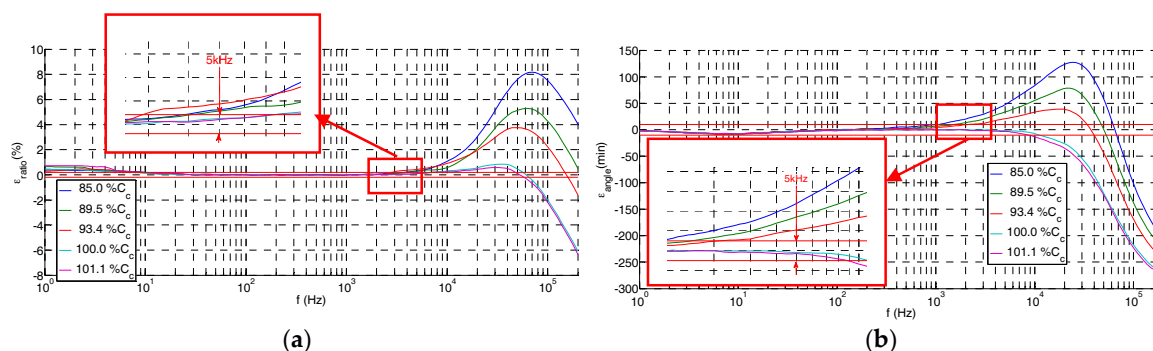


Figure 6. Measured errors in the real design of Figure 1 due to the difference in the length of coaxial cable C_c with respect to the theoretical value: (a) ratio error; (b) phase displacement error.

In the low frequency range (1–10 Hz), the rated ratio of the divider increases up to 0.7% (see Figure 7), while the angle error maintains lower than 10 min for the C_c values analyzed (85.0–101.1% C_c).

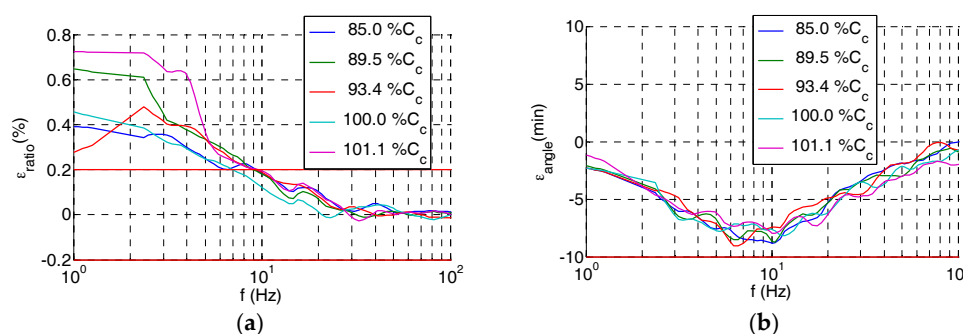


Figure 7. Measured errors of the built HV sensor in the low frequency range for difference lengths of the coaxial cable C_c : (a) ratio error; (b) phase displacement error.

Both frequency responses, of the simplified model derived from Equation (9) and of the built divider measured in the LCOE laboratory, are shown in Figure 8. It can be observed that the simplified model follows the real frequency behavior for a frequency range up to 3 kHz.

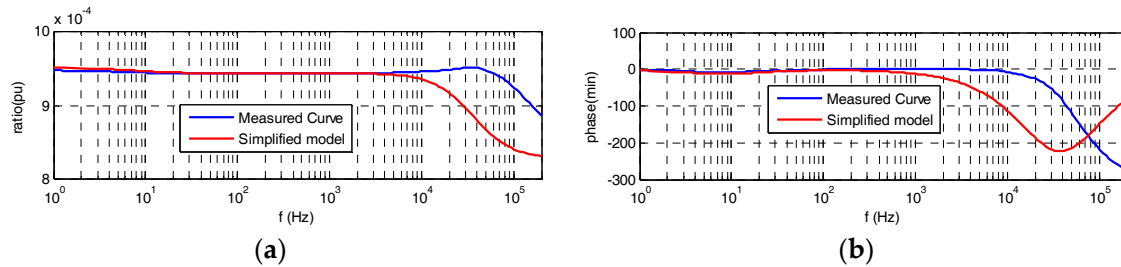


Figure 8. Frequency response curves: the red curve is obtained via Equation (9) and the blue curve was measured in the LCOE laboratory: (a) ratio error; (b) phase displacement error.

4. Improved Electrical Model

To improve the simplified model shown in Figure 3a, the 2nd resistor of the HV branch is split into two parts, as is shown in the circuit of Figure 3d. Each resistance part $k \cdot R$ and $(1 - k) \cdot R$ has a different stray capacitance C_s'' and C_s''' in parallel depending on the geometrical location between the resistance and the central electrode (see Figure 2a), which it is considered in the PSPICE circuit shown in Figure 9 by C_{sp1} (C_s'') and C_{sp2} (C_s'''), respectively. For the built sensor, an equivalent capacitance of C_s'' is in parallel with the first part of the resistance part $k \cdot R$ and another capacitance of C_s''' is in parallel with the other resistance part $(1 - k) \cdot R$. The values of the coefficient k (0.96) and of the capacitances C_s'' (0.20 pF) and C_s''' (0.87 pF) have been determined by an iterative process by means of circuit analysis and synthesis using PSPICE modeling and MATLAB in order to fit the theoretical curve of the frequency response to the real one measured in the laboratory. Furthermore, two additional resistors (R_{sp} and R_{e2p}) that mainly represent leakage resistances of both capacitor blocks are also added to simulate in a better way the real behavior of the built divider. The R_{sp} magnitude also includes any difference between the 1st and the 2nd HV resistances. The improved model achieves a good fitting to the measured frequency response (see Figure 10) for the set values of the parameters of Table 1, while the simplified model does not fit the high frequency range (Figure 8). The frequency response measured in the built divider with a small change in the emplacement of the 2nd resistance is also included in Figure 10. The emplacement change moved vertically 2 mm from the relative position of the 2nd resistance regarding the central electrode. A significant influence in the frequency response curve can be observed, which justifies the inclusion of stray capacitances C_s'' and C_s''' in the improved circuit model shown in Figure 3d and in its simulate PSPICE circuit shown in Figure 9.

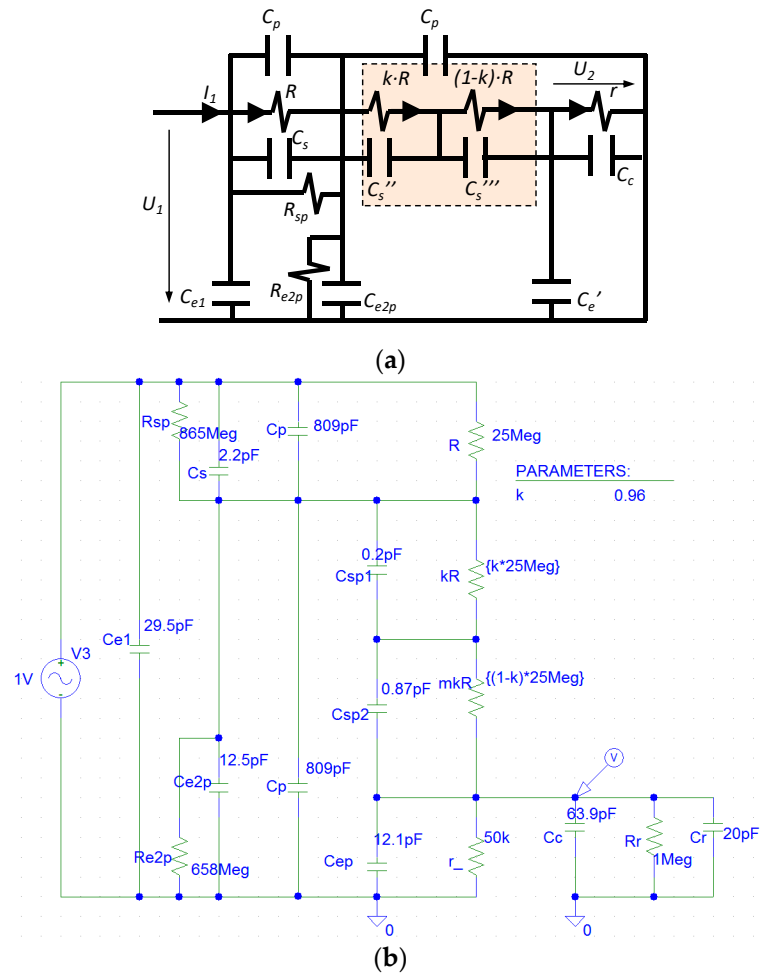


Figure 9. Improved model of the sensor: (a) equivalent electric circuit; (b) PSPICE model to fit the frequency response to the measured one.

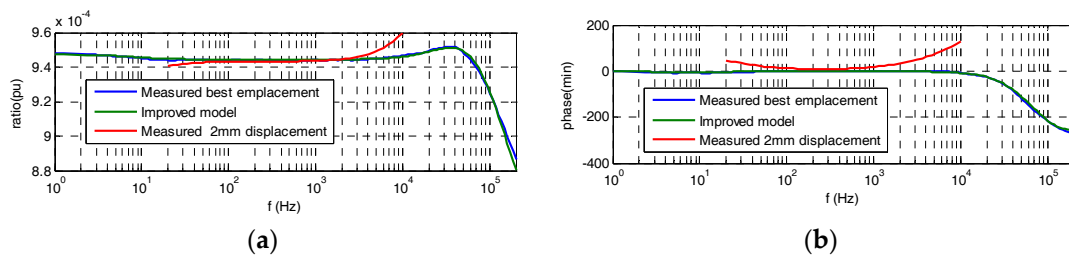


Figure 10. Frequency response curves measured with the best emplacement of the 2nd HV resistance (blue curve), with a vertical displacement of 2 mm (red curve), and obtained by PSPICE simulating the frequency response of best emplacement of the 2nd HV resistance (green curve) using the coefficient $k = 0.96$ to the frequency response measured: (a) ratio error; (b) phase displacement error.

5. High-Voltage Calibration and Insulation Testing

5.1. Ratio and Angle Errors

The voltage sensor was calibrated in a HV range from 1 to 14 kV ($24/\sqrt{3}$ kV) for a sinusoidal frequency of 50 Hz using voltage standard transformers. The calibration was complemented with a power frequency test of 60 Hz at 14 kV ($24/\sqrt{3}$ kV). An uncertainty of 0.08% for the HV calibration was achieved. The calibration was performed for two environment temperatures: 20 °C and 40 °C.

The ratio errors obtained are inside the admissible tolerances corresponding to an accuracy class of 0.2 (see Figure 11).

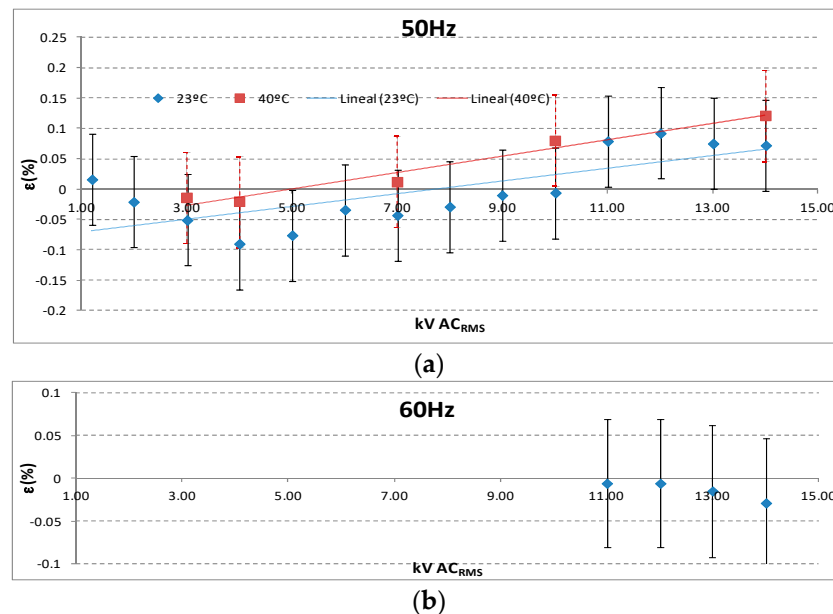


Figure 11. (a) Ratio errors for HV calibration from 1 to 14 kV, 50 Hz at 20 °C and 40 °C, (b) ratio errors for HV calibration from 11 to 14 kV, 60 Hz at 20 °C.

5.2. Insulation Tests

Insulation tests were usefully passed corresponding to the insulation level for material to be used in a power grid of 24 kV. Fifteen positive and negative lightning impulses 1.2/50 of 125 kV were applied without any breakdown and a power frequency voltage of 50 kV ($U_{peak}/\sqrt{2}$) for a minute was applied without any breakdown (see Figure 12).

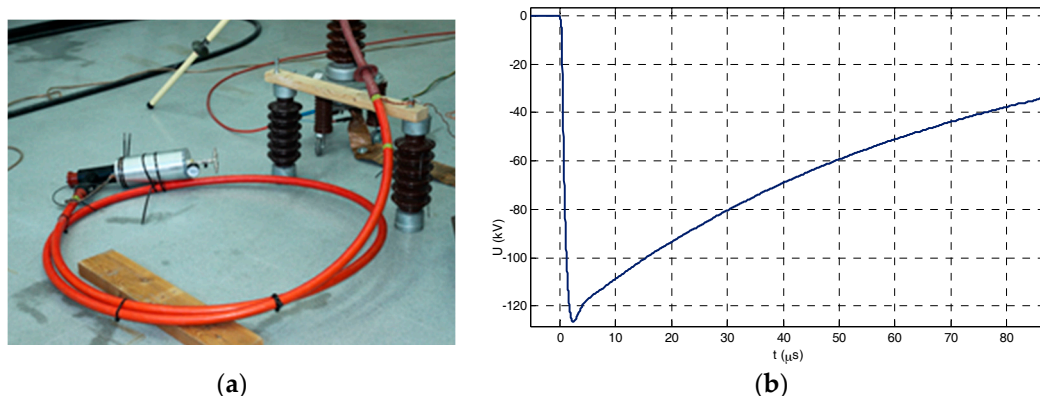


Figure 12. (a) Testing layout of the voltage divider prototype connected to a medium voltage cable, (b) negative lightning impulse (125 kV) applied during the withstand test.

6. Conclusions

A voltage sensor on the basis of a shielding double RC voltage divider has been designed, developed, built, and tested. The design is based in two RC dividers, one inside the other. This design permits to transform earth capacitances of the HV resistive branch to parallel capacitances. The frequency response of the built sensor shows a flat frequency response from 20 Hz to 5 kHz, with a ratio error and a phase displacement error inside the admissible errors of a class of 0.2. The class

increases to 0.5 if the sensor is used from 1 to 20 Hz. An optimized design to maintain the 0.2 class from DC to 5 kHz is attainable if the parallel capacitance C_s , of the first HV resistor, R , is increased. The insulation tests demonstrate that the built sensor can be used in power grids up to 24 kV.

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Conflicts of Interest: The authors declare no conflicts of interest.

References

1. International Electrotechnical Commission. *IEC 61869-1 Instrument Transformers—Part 1: General Requirements*; IEC: Geneva, Switzerland, 2007.
2. International Electrotechnical Commission. *IEC 61869-3 Additional Requirements for Inductive Voltage Transformers*; IEC: Geneva, Switzerland, 2011.
3. International Electrotechnical Commission. *IEC 60060-2 High Voltage Test Techniques—Part 2 Measuring Techniques*; IEC: Geneva, Switzerland, 2010.
4. International Electrotechnical Commission. *IEC 61000 Electromagnetic Compatibility (EMC)*; IEC: Geneva, Switzerland, 1992.
5. EN 50160 European Standard. *Voltage Characteristics in Public Distribution Systems-Voltage Disturbances*; CENELEC: Brussels, Belgium, 1999.
6. Klatt, M.; Meyer, J.; Elst, M.; Schegner, P. Frequency Responses of MV voltage transformers in the range of 50 Hz to 10 kHz. In Proceedings of the 14th International Conference on Harmonics and Quality of Power (ICHQP), Bergamo, Italy, 26–29 September 2010.
7. Seljeseth, H.; Saethre, E.A.; Ohnstad, T.; Lien, I. Voltage transformer frequency response. Measuring harmonics in Norwegian 300 kV and 132 kV power systems. In Proceedings of the 8th International Conference on Harmonics and Quality of Power, Athens, Greece, 14–16 October 1998; Volume 2, pp. 820–824.
8. Kunde, K.; Däumling, H.; Huth, R.; Schlierf, H.W.; Schmid, J. Frequency Response of Instrument Transformers in the kHz Range. Available online: <http://www.trench.at/content/download/1604/14169/file/Frequency%20Response%20of%20Instrument%20Transformers%20in%20the%20kHz%20range.pdf> (accessed on 17 November 2017).
9. Crotti, G.; Gallo, D.; Giordano, D.; Landi, C.; Luiso, M.; Modarres, M. Frequency response of MV voltage transformer under actual waveforms. *IEEE Trans. Instrum. Meas.* **2017**, *66*, 1146–1154. [CrossRef]
10. International Electrotechnical Commission. *IEC 60044-7 Instrument Transformers—Part 7: Electronic Voltage Transformers. Additional Requirements for Electronic Voltage Transformers*; IEC: Geneva, Switzerland, 1999.
11. Hlavacek, J.; Draxler, K.; Styblikova, R. 20 kV AC Divider with ratio correction. In Proceedings of the 19th International Symposium on High Voltage Engineering, Pilsen, Czech Republic, 23–28 August 2015.
12. Crotti, G.; Gallo, D.; Giordano, D.; Landi, C.; Luiso, M.; Modarres, M.; Zucca, M. Frequency compliance of MV voltage sensors for smart grid application. *IEEE Sens. J.* **2017**, *17*, 7621–7629. [CrossRef]



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