

Article

A Novel Offset Cancellation Based on Parasitic-Insensitive Switched-Capacitor Sensing Circuit for the Out-of-Plane Single-Gimbaled Decoupled CMOS-MEMS Gyroscope

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Abstract: This paper presents a novel parasitic-insensitive switched-capacitor (PISC) sensing circuit design in order to obtain high sensitivity and ultra linearity and reduce the parasitic effect for the out-of-plane single-gimbaled decoupled CMOS-MEMS gyroscope (SGDG). According to the simulation results, the proposed PISC circuit has better sensitivity and high linearity in a wide dynamic range. Experimental results also show a better performance. In addition, the PISC circuit can use signal processing to cancel the offset and noise. Thus, this circuit is very suitable for gyroscope measurement.

Keywords: out-of-plane gyroscope; parasitic-insensitive switched-capacitor (PISC); $\Sigma\Delta$ ADC

1. Introduction

Generally speaking, MEMS gyroscopes only have relatively small detection capacitances; therefore, the sensing circuit design is very important. The sensing mechanisms of MEMS gyroscopes are mainly categorized into piezoresistive [1–5] and capacitive [6–13] mechanisms. Capacitive gyroscopes have simpler structure and hence lower fabrication cost. In addition, they provide lower power consumption, higher sensitivity, and higher reliability as well as lower nonlinearity, lower temperature dependency, lower noise, and lower drift. Capacitance is also easily available in silicon technology because it does not require special materials and process steps. On the other hand, the piezoresistive sensing scheme is

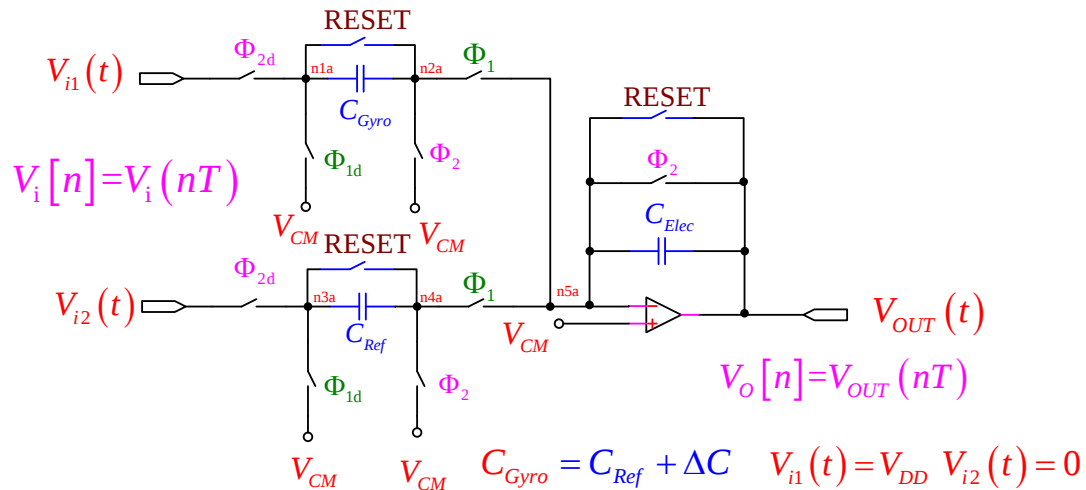
widely used in accelerometers. If the gyroscopes use piezoresistive materials, they should be driven in their primary modes with different mechanism because piezoresistive materials cannot induce passive nature by themselves [14]. In addition, its sensitivity is low, and its temperature dependency is high compared to the capacitive gyroscope. Hence, it is mainly used in low-end products.

Capacitive sensing circuits are categorized into synchronous [15], switched-capacitor [12,16–18], and fully differential circuits [8,11,19,20]. The transfer functions of the first two are independent of parasitic capacitance, and they can cancel the flicker noise and DC offset voltage to provide high accuracy. The synchronous sensing circuit requires bias control with either a large value off-chip or large-area integrated resistive circuit component [15]. In addition, in the frequency response, the transfer function of the synchronous sensing circuit has a zero point that increases the phase delay so that it cannot control feedback. The architecture of the fully differential sensing circuit is simple and contains no charge cancellation error, but its signals are attenuated by parasitic capacitance [19]. The switched-capacitor circuit technique is based on the realization that the capacitor and switch are equivalent to a resistor for reducing the layout area [16–18]. This technique can realize a variety of other signal-processing blocks, such as gain-stage, voltage-controlled oscillators (VCOs), and modulators. The switched-capacitor circuit can provide stability but it reduces the open-loop gain. In addition, the switched-capacitor circuit provides a virtual ground and robust DC biasing at the sensing node so that the sensed signal is insensitive to parasitic capacitance and undesirable charging. This circuit also offers a wide range of techniques to suppress offset and low-frequency noise, such as correlated double sampling (CDS) and programmable capacitor array (PCA). Thus, this circuit is very suitable for gyroscope measurement. A novel parasitic-insensitive switched-capacitor (PISC) sensing circuit is designed in order to get high sensitivity and ultra linearity and reduce the parasitic effect for the out-of-plane single-gimbaled decoupled gyroscope (SGDG) in this study.

This paper is organized as follows: in Section 2, the PISC circuit design is briefly introduced. The simulation results are presented in Section 3. The experimental results are presented in Section 4. Finally, the conclusions are given in Section 5.

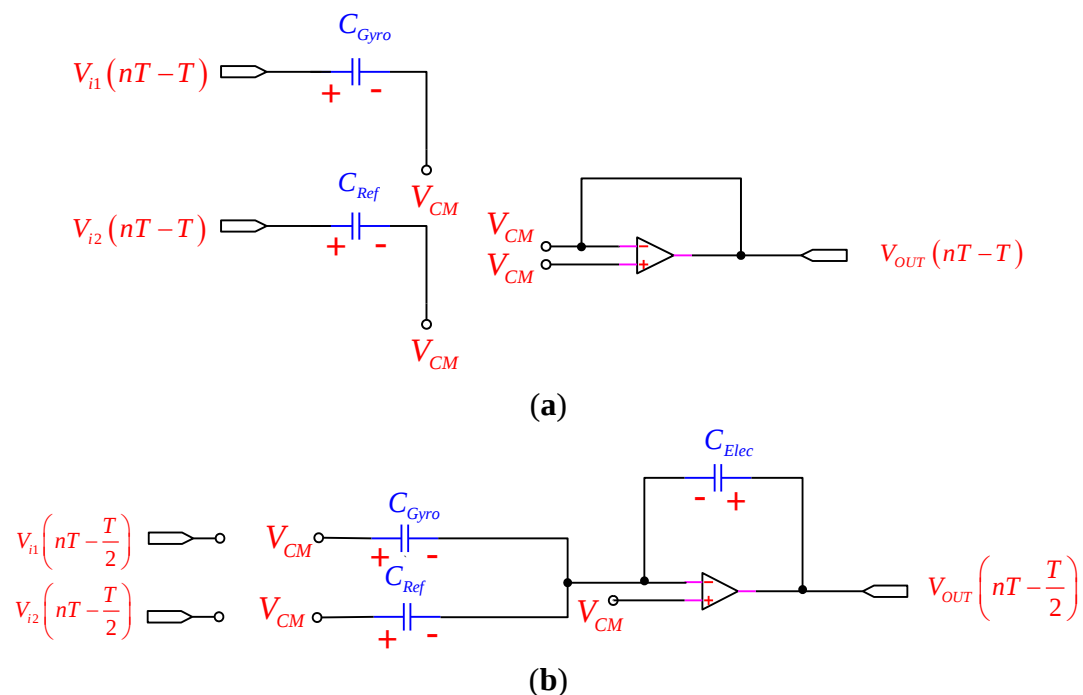
2. Circuit Design

The on-chip sensing circuit uses the switched-capacitor sensing circuit that detects the capacitance change due to the deflection of the proof mass. During the sampling phase of a traditional switched-capacitor amplifier, it only samples the input, sets the output to zero, and provides no amplification. This raises concern about its stability, and reduces the open-loop gain. The capacitors used are known as double-poly capacitors. There also exists a substantial parasitic capacitance. In order to reduce the parasitic effect, we propose the PISC sensing circuit, as shown in Figure 1 [16,17]. Here, the “RESET” switches are only utilized for discharging the capacitors initially. The C_{Gyro} is capacitance of detection of the gyroscope, the C_{Ref} is initial capacitance of detection of the gyroscope and the C_{Elec} is amplification capacitance. V_{CM} is common mode voltage, and its value is $V_{DD}/2$. In this study, the V_{CM} is set to 1.65 V.

Figure 1. The PISC sensing circuit.

At the beginning, the input signals voltages of the circuit are +1.65 V and −1.65 V. In order to maintain the cut-off condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit) [18]. Thus, we use the concept of voltage translation to change the input signal voltage. The input signal $V_{i1}(t)$ changes to V_{DD} , and the other $V_{i2}(t)$ changes to zero.

As shown in Figure 2(a), in the sampling mode, Φ_2 is on and Φ_1 is off, allowing the voltage across C_{Gyro} and C_{Ref} to track $V_{i1}(t)$ and $V_{i2}(t)$ while the operational amplifier (OP-amp) and C_{Elec} hold the previous value. In the transition to the amplification mode, the charge stored on C_{Gyro} and C_{Ref} are transferred to C_{Elec} through the virtual ground node, as shown in Figure 2(b).

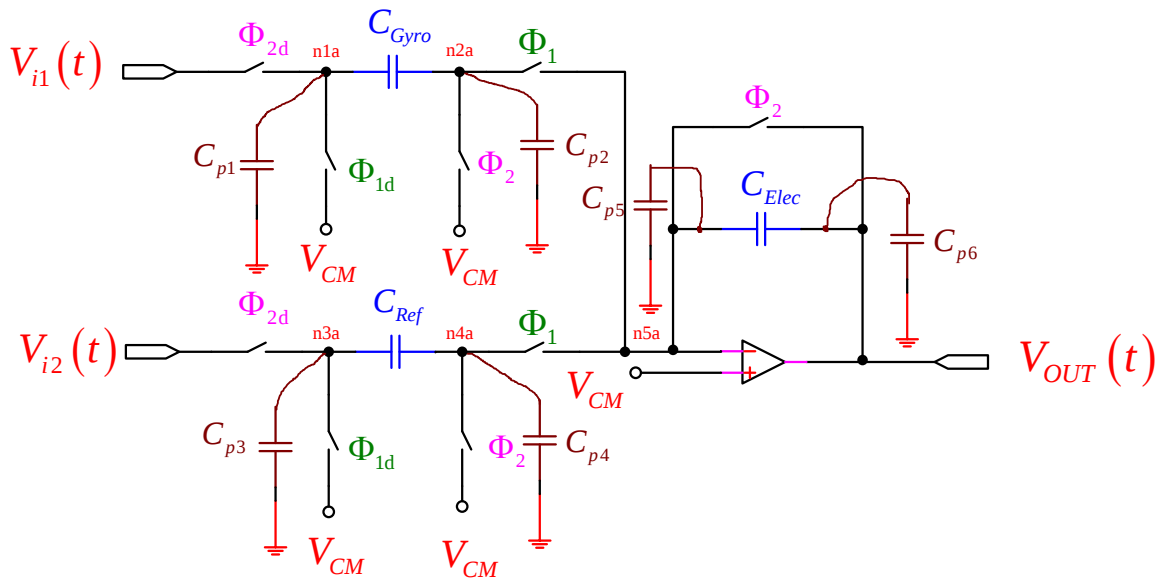
Figure 2. The PISC sensing circuit for the two operations: (a) sampling mode; (b) amplification mode.

The results in the transfer function for this switched-capacitor circuit are given by:

$$\frac{V_o(z)}{V_{i1}(z)} = \frac{1}{2} \left(\frac{-C_{Ref} + C_{Gyro}}{C_{Elec}} \right) z^{-\frac{1}{2}} = \frac{1}{2} \left(\frac{\Delta C}{C_{Elec}} \right) z^{-\frac{1}{2}} \quad (1)$$

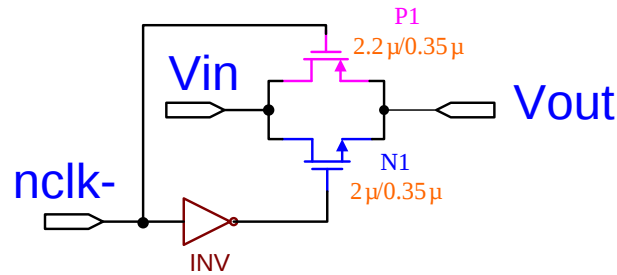
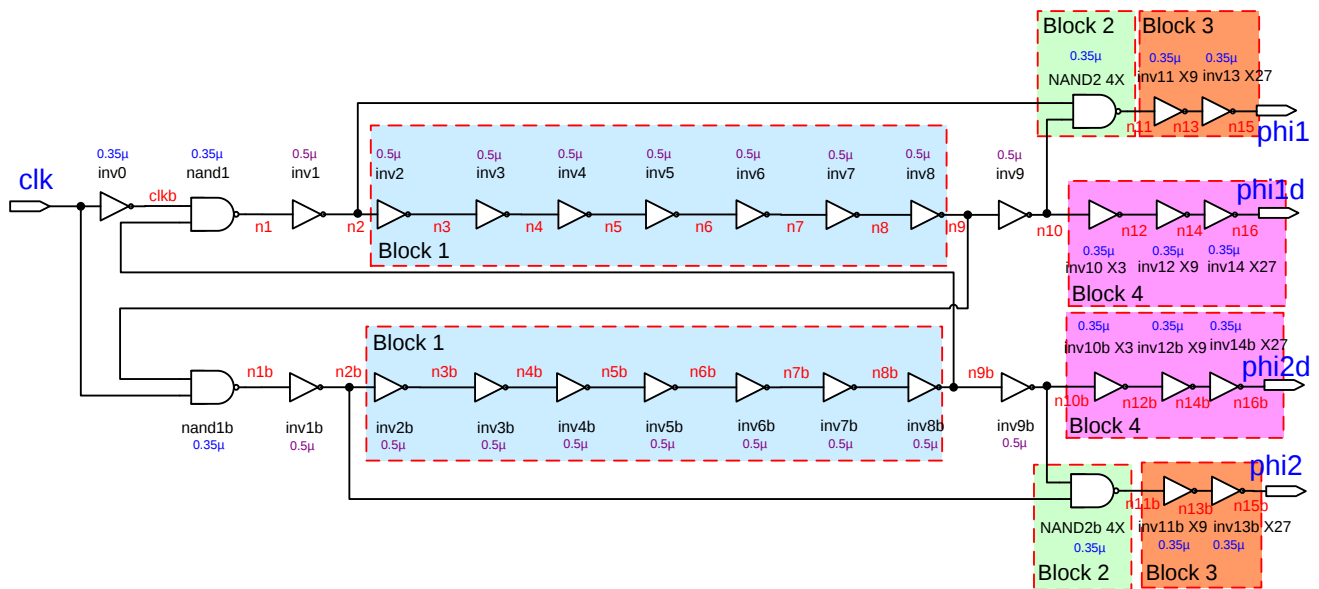
Note that Equation (1) represents its gain coefficient as the ratio of the difference capacitance and C_{Elec} . The $z^{-1/2}$ represents a period delay and can be ignored [16]. The behavior of the circuit with respect to parasitic capacitances is plotted in Figure 3 [16].

Figure 3. The PISC sensing circuit with parasitic capacitances shown.



Here, C_{p1} is continuously being charged to $V_{i1}(t)$ and discharged to the common mode (V_{CM}). However, when Φ_2 is turned on, the fact that C_{p1} is also charged to $V_{i1}(t-1)$ does not affect the charge that is placed on C_{Gyro} . When Φ_1 is turned on, C_{p1} is discharged through the Φ_1 switch attached to its node, and none of the discharging current passes through C_{Gyro} to affect the charge accumulating on C_{Elec} . Therefore, it does not affect the circuit operation. In addition, C_{p2} is either connected to V_{CM} through the Φ_2 switch or to the virtual ground through the Φ_1 switch. Since C_{p2} always remains discharged, it does not affect the operation of the circuit. Similarly, the operations of C_{p3} and C_{p4} do not effect as C_{p1} and C_{p2} . The effect of C_{p5} on the transfer function is small since it is always connected to the virtual ground of the OP-amp. Finally, C_{p6} is connected to the OP-amp output. Although it may affect the speed of the OP-amp, it would not affect the final settling point of the OP-amp output.

A switched-capacitor circuit is realized with basic building blocks such as the OP-amp, capacitors, switches, and non-overlapping clocks. The OP-amp circuit is shown in Figure 4. To improve the circuit stability, the OP-amp must provide a high enough stability margin. The folded-cascode OP-amp architecture is selected to provide the phase margin of 78.906°. The input differential pairs use large devices with a parallel symmetric layout for good matching, thereby reducing the input voltage offset and flicker (1/f) noise. To increase the phase margin of OP-amp, a large output compensation capacitor of up to 3.8 pF is used; it is made of double poly (poly1 and poly2). Table 1 provides a list of the device sizes.

Figure 5. Transmission gate.**Figure 6.** Schematic of the non-overlapping clock circuit.

A sensing circuit usually requires an ADC. In general, the output voltage for the sensing circuit is weak and small. A high resolution ADC is necessary for acquiring such a feeble signal. The $\Sigma\Delta$ ADC is the best choice for this application. It uses the over-sampling principle, noise shaping and decimation filtering to achieve the high resolution. It consists of a $\Sigma\Delta$ modulator and a decimation filter. In addition, the $\Sigma\Delta$ ADC operates in the discrete-time domain and is implemented using the switch-capacitor circuit technique. The switch-capacitor circuit can only be realized in MOS devices, not in bipolar transistors. In other words, the sensing circuit fabricated in the digital CMOS process is suitable for generating the digital output using $\Sigma\Delta$ ADCs. The behavior simulation model shown in Figure 7 is adopted for the $\Sigma\Delta$ modulator design to avoid the integrator overload and to satisfy the system requirements. The design is the second order $\Sigma\Delta$ modulator with a one-bit quantizer. The decimation digital filter is implemented by down-sampling and a comb filter. The discrete-time integrator parameters of K1 and K2 for the $\Sigma\Delta$ modulator are 0.1 and 0.5, respectively.

The circuit design for the $\Sigma\Delta$ modulator is shown in Figure 8. Here, “OTA1” and “OTA2” are folded-cascode OP-amps, as shown in Figure 4. The “COMP” indicates the comparator circuit, as shown in Figure 9. The “RESET” switches are only utilized for discharging the capacitors initially. The circuit is implemented using the switch-capacitor technique and controlled by a non-overlap clock circuit, as shown in Figure 6, which is used to eliminate the clock feed-through influence.

Figure 7. $\Sigma\Delta$ modulator behavior simulation.

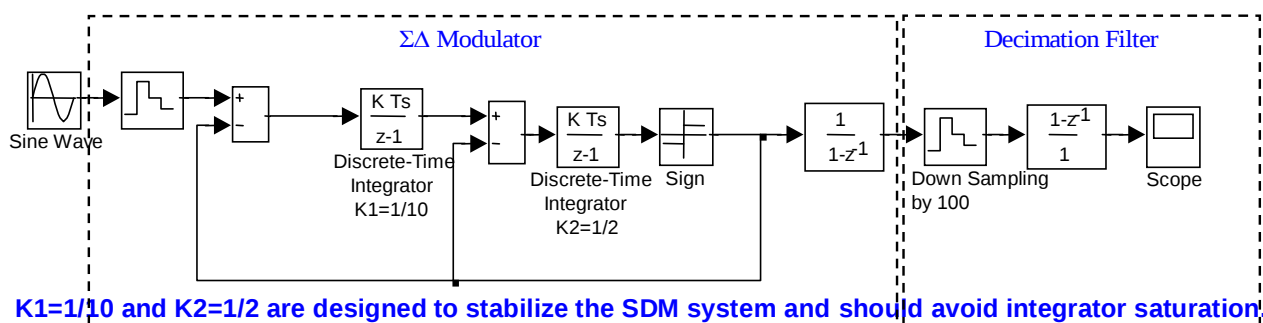


Figure 8. One-bit $\Sigma\Delta$ modulator circuit design.

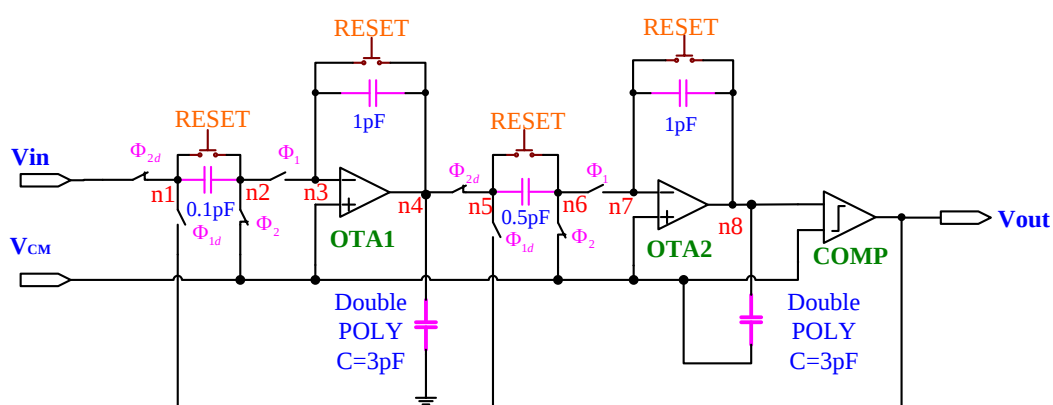
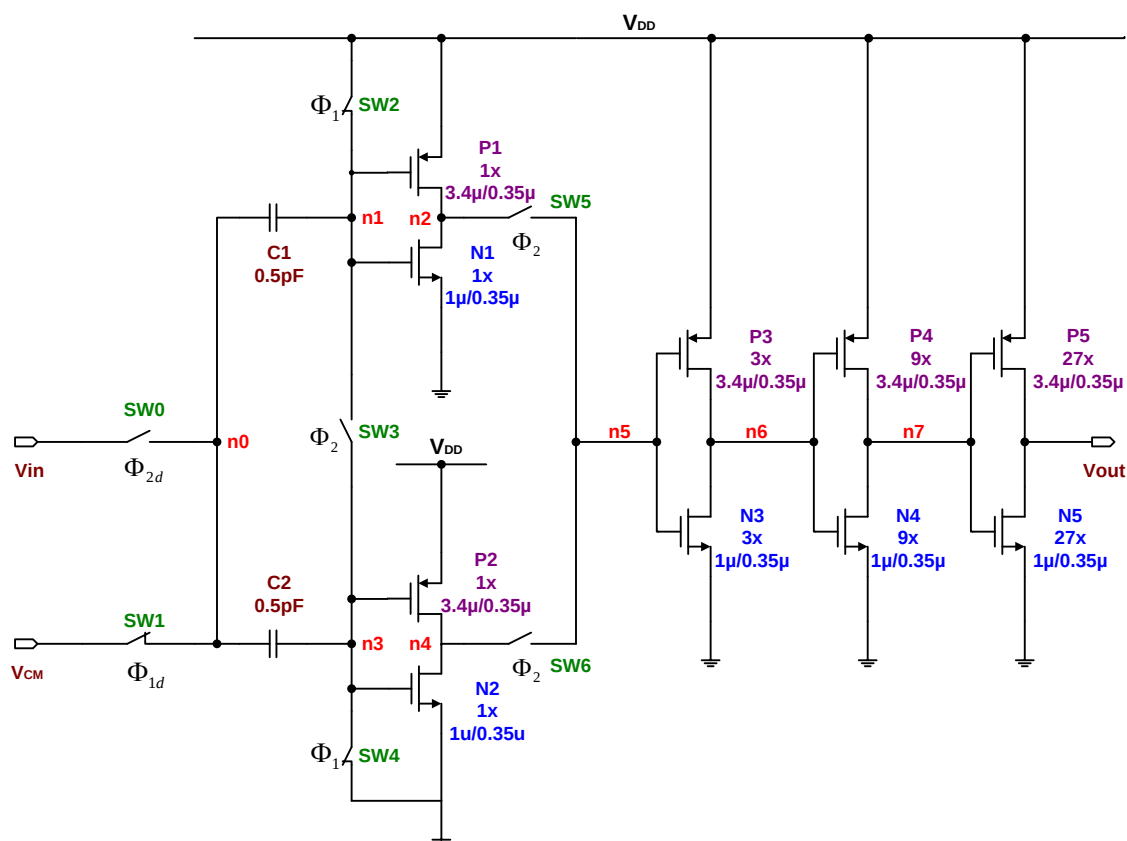


Figure 9. Comparator circuit design.



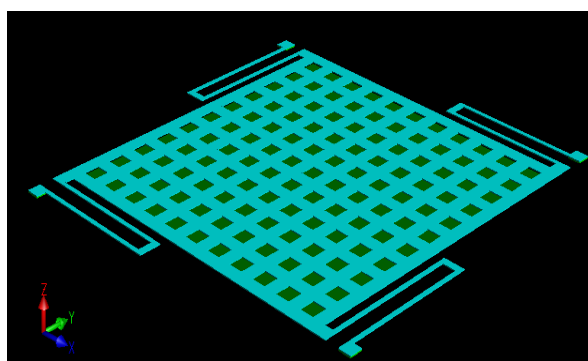
3. Simulation Results

In this paper, the simulation results for circuit design are the post-layout simulation results.

3.1. C_{Ref} Selection

The C_{Ref} is the initial capacitance of detection for the gyroscope. The capacitance value is simulated using the CoventorWare FEM simulator. The simulator uses the solid model of the gyroscope (see Figure 10(a)) and its capacitance value is about 516 fF, as shown in Figure 10(b). In addition, we also use the ARCHITECTTM simulator to estimate C_{Ref} . It models the mechanical and electrical effects of these rough environments on the out-of-plane SGD. In ARCHITECTTM, we work in a schematic-driven environment using symbols to represent individual components or elements of components, as seen in Figure 11. Typically, these component models are parameterized. The simulation result of electrode capacitance (c_{ap}) for the transient analysis is shown in Figure 12. It can be found that the initial capacitance, C_{Ref} is about 519 fF when the sensing signal (wyr) is 1 rad/s. The capacitance is calculated to be about 499 fF by the formula. After comparing the three methods, we choose this value of about 500 fF for a convenient layout.

Figure 10. Using the CoventorWare simulator to solve C_{Ref} (a) Solid model of the gyroscope. (b) Simulation results.



(a)

Capacitance (pF)		
	LowerPlate	UpperPlate
LowerPlate	5.163529E-01	-5.127232E-01
UpperPlate	-5.127326E-01	5.194461E-01

(b)

Figure 11. Schematic of out-of-plane SGD.

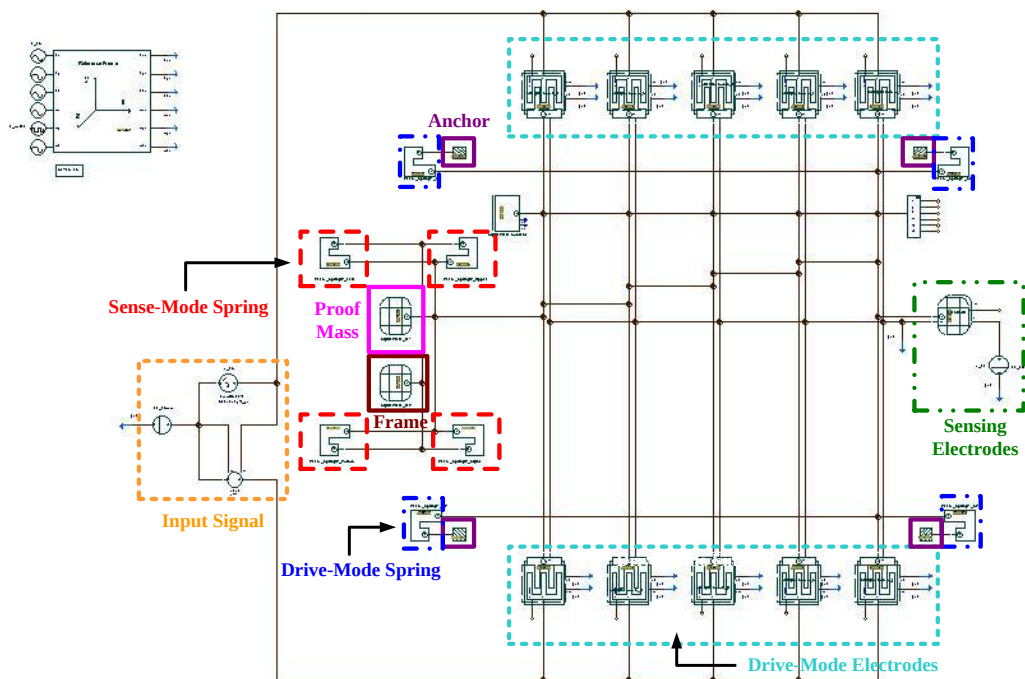
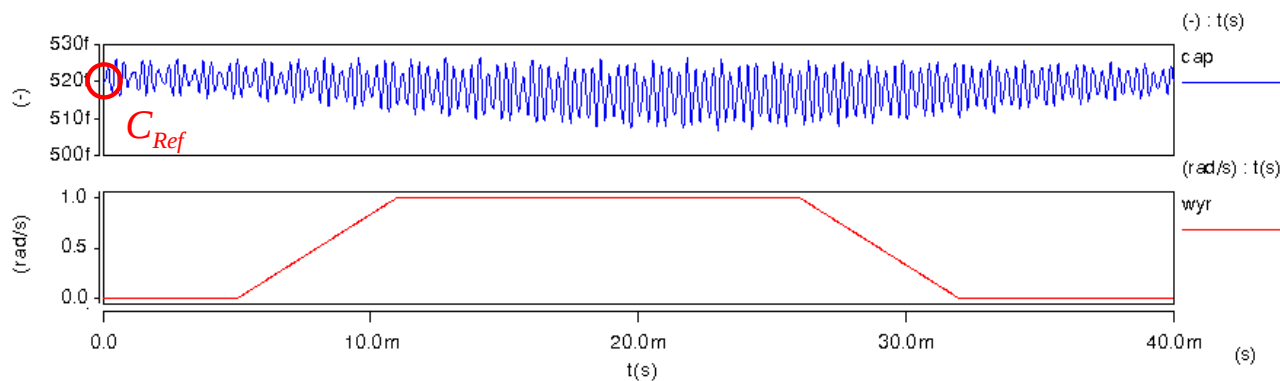


Figure 12. Using the ARCHITECT™ simulator to solve C_{Ref} .



3.2. C_{Elec} Selection

In Table 2, the output voltage of $C_{Gyro} = 500$ fF is close to $V_{CM} (= 1.65$ V) when C_{Elec} is 60 fF. Here, these output voltages are simulated by the HSPICE simulator. However, these values should be actually approached when C_{Elec} is 63 fF. But this time the layout is poor to achieve. Therefore, we choose C_{Elec} to be 60 fF.

Table 2. Output voltage (unit: V) under different C_{Gyro} (C_{Elec} swept from 10 fF to 100 fF).

C_{Gyro} (fF)	C_{Elec} (fF)									
	10	20	30	40	50	60	70	80	90	100
460	0.18	0.203	0.235	0.308	0.488	0.661	0.79	0.889	0.994	1.032
500	1.88	1.808	1.748	1.730	1.722	1.691	1.71	1.692	1.693	1.685
540	3.12	3.104	3.050	2.982	2.830	2.688	2.55	2.454	2.380	2.305

3.3. Parasitic-Insensitive Switched-Capacitor Circuit

Figure 13 shows the C-V curves of the two capacitive sensing circuits, including the PISC circuit and simple non-inverting amplifier. The proposed PISC circuit has the higher dynamic voltage output and sensing range than those of the simple non-inverting circuit. Figure 14 illustrates the enlarging parts of the PISC circuit of Figure 13 between 460 fF and 540 fF.

Figure 13. C-V curves of the two capacitive sensing circuits.

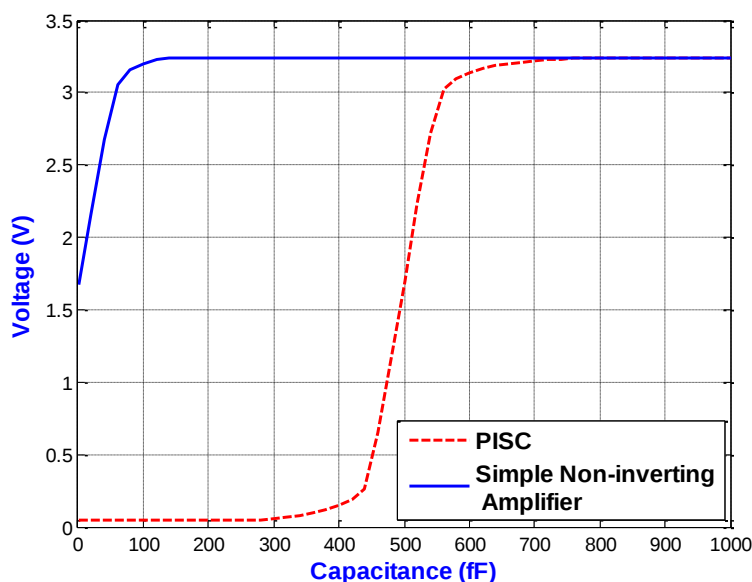
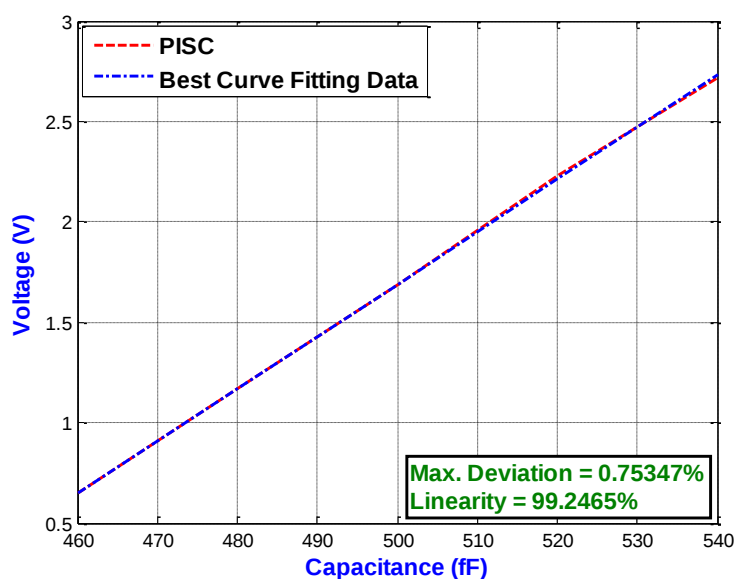


Figure 14. Enlarge picture of the PISC circuit of Figure 13 (460 fF–540 fF).



The proposed PISC circuit has an ultra linearity of 99.2465%. The detailed specifications and comparisons of the two circuits are summarized in Table 3. It can be noted that the proposed PISC circuit has the higher capacitance sensitivity, lower power dissipation, and smaller noise floor, but its resolution and voltage offset are less than those of the simple non-inverting circuit. The main reason is that it uses more components than the simple non-inverting circuit.

Table 3. Comparison of the two circuits ($C_{Gyro} = 540$ fF (25 °C), Frequency = 10 kHz).

Term	PISC	Simple Non-inverting Amplifier
Supply Voltage (V)	3.3	3.3
Power Dissipation (mW)	2.4108	2.4392
Dynamic Voltage Output (V)	0.0445–3.2427	1.6752–3.2434
ΔC Range (fF)	± 40	0–40
Sensing Range (fF)	440–540	0–40
Capacitance Sensitivity (mV/fF)	25.8938	24.9875
Linearity (%)	99.2465	98.5426
Ideal Resolution (fF)	0.01273	0.00962
Voltage Offset (mV)	1.9964	1.5534
Noise Floor ($\mu\text{V}/\text{Hz}^{1/2}$) (at 10 kHz)	0.1564	4.6716

Figure 15 shows the output results of the proposed PISC circuit under different C_{Gyro} . When the time reaches 100 μs , the clk in Figure 6 is turned on. From the simulation results, we can see that the proposed PISC circuit starts sampling after clk is turned on. In addition, the PISC circuit with $C_{Gyro} = 500$ fF is mainly for the noise and offset signals. Thus, we can use signal processing to cancel the noise and offset, as shown in Figure 16.

Table 4 shows that the PISC circuit using signal processing has significantly smaller voltage offset and noise floor than those without using signal processing. Their improvement factors are 24.6% and 29.3%, respectively, compared to without using signal processing.

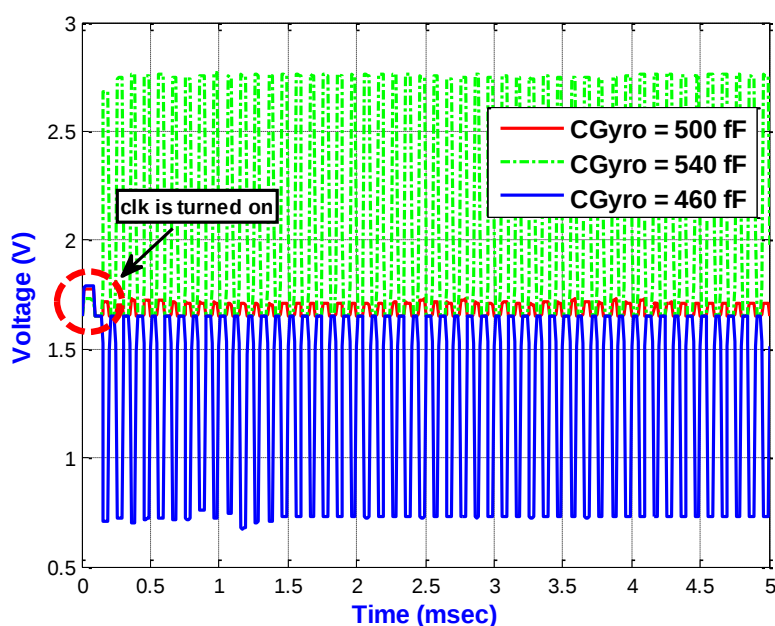
Figure 15. Output results of the proposed PISC circuit under different C_{Gyro} ($C_{Ref} = 500$ fF, $C_{Elec} = 60$ fF).

Figure 16. Output voltage using signal processing.

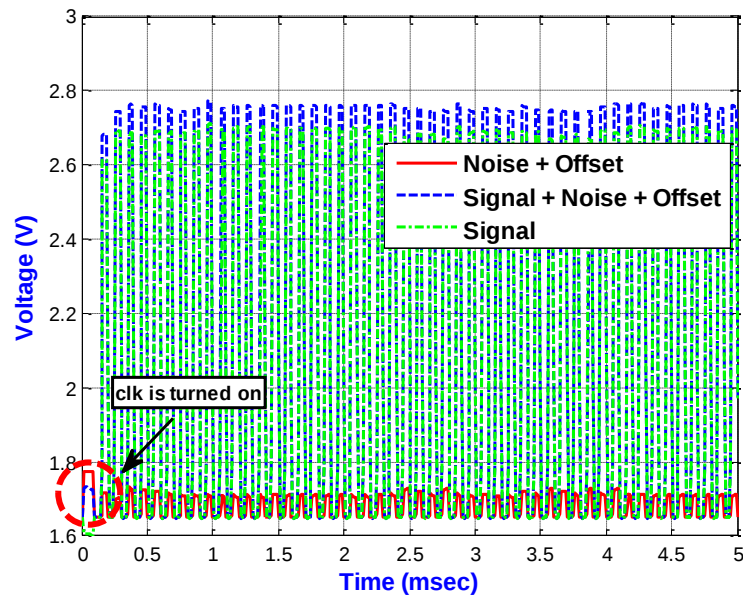


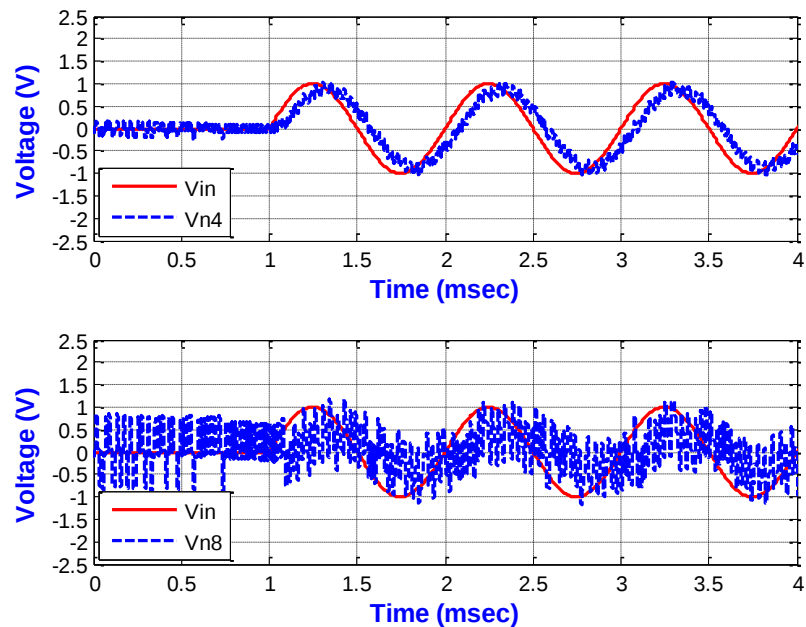
Table 4. Simulated demonstration of performance improvement with signal processing.

Term	Without Signal Processing	With Signal Processing	Improvement Factor (%)
Voltage Offset (mV)	1.9964	1.5053	24.6
Noise Floor ($\mu\text{V}/\text{Hz}^{1/2}$) (at 10 kHz)	0.1564	0.1106	29.3

3.4. SDM (Sigma-Delta Modulator)

The simulation results of the SDM circuit simulated by HSPICE simulator from nodes of n4 and n8 in Figure 8 are shown in Figure 17 with a sinusoidal input.

Figure 17. The simulation results of the SDM circuit from nodes n4 and n8 in Figure 8.

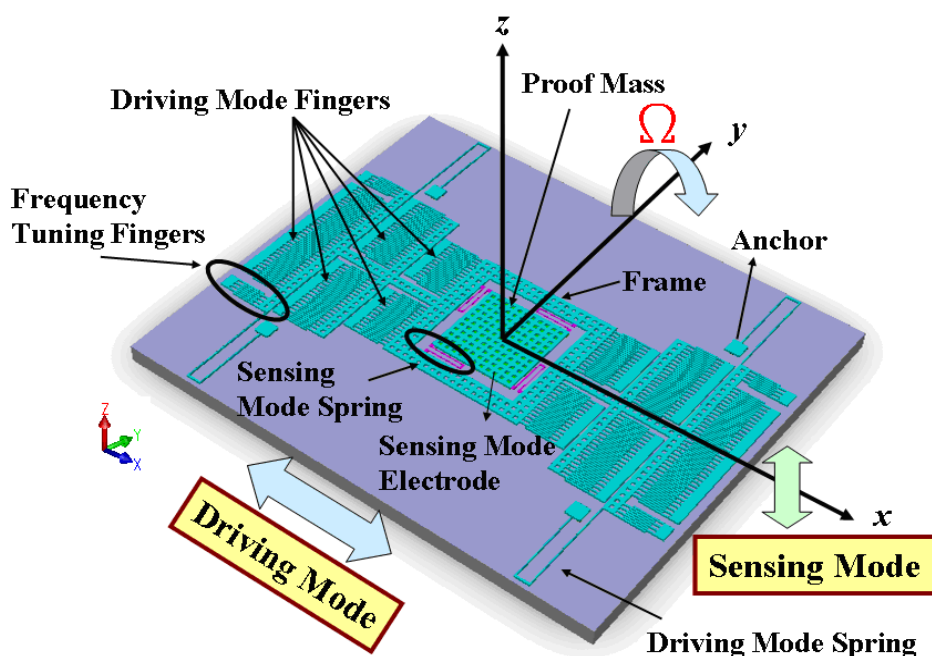


Compared with the behavior simulation shown in Figure 7, they are almost the same. The bit-stream output of the $\Sigma\Delta$ modulator from the one-bit quantizer will be sent to the decimation filter to obtain the digital output.

3.5. Application (Combined Out-of-Plane SGD in [21])

A single-gimbaled configuration is used to decouple the drive and sense modes of the gyroscope. Figure 18 shows the topology of the SGD, which is a y-axis sensitive out-of-plane gyroscope. The gyroscope is driven in the drive-mode with three rows of symmetrical comb fingers. The main purpose is to increase the number of fingers to 206 pairs (see Figure 18), and to provide greater driving force, the amplitude of the driving displacement, and less thermo-mechanical noise. As depicted in Figure 18, four translational springs outside the frame constrain the degree-of-freedom (DOF), and hence the frame can be driven only along the x-axis. Inside the frame, another set of linear springs allows the proof mass to move solely along the z-axis. When an external angular rate is applied to the proof mass along the y-axis, the proof mass vibrates due to Coriolis force along the z-axis. The Coriolis force is sensed by four inner springs.

Figure 18. Out-of-plane SGD.



The frame and the proof mass are actuated by the electrostatic comb drives at the resonant frequency. The sense electrode under the proof mass detects the capacitance difference using the parallel plates. The gyroscope is designed as a symmetrical and decoupled gyroscope in order to achieve a high sensitivity. The springs are all identical in shape in two modes, the drive and sense modes, and have different mass values. However, due to spring constant difference in the drive and sense modes, and in order to cancel process variations in the resonant frequencies, the drive-mode has two symmetrical frequency tuning fingers. These fingers create the force in the drive-mode and may reduce the frequency in some ranges relative to the applied DC voltage. The top view of the gyroscope chip, shown in Figure 19, is 1.725 mm $\times$ 1.515 mm and contains the SGD and PISC blocks. The

PISC circuit is located on the left of Figure 19. To avoid the damage caused by etching silicon dioxide in the wet etch, the PISC circuit is placed 50 μm away from the out-of-plane SGD. Except for the microstructure, the whole chip area is covered by the top metal layer, M4.

Figure 19. Top view of the out-of-plane SGD.

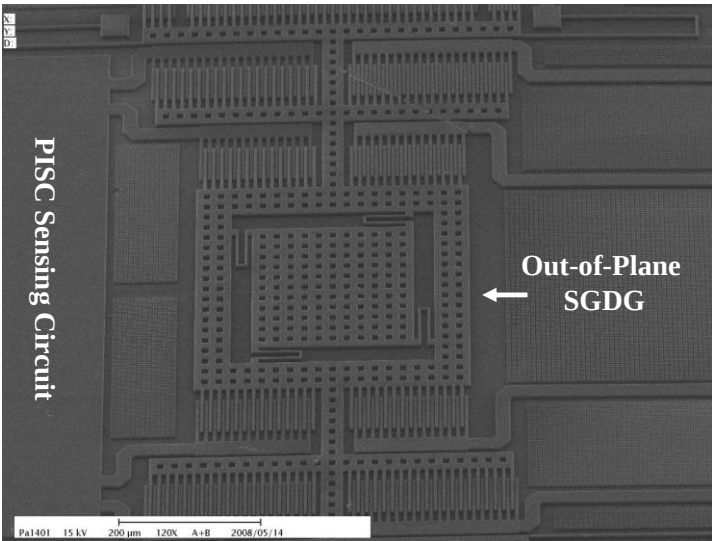


Figure 20 shows the output voltage of the gyroscope according to angular rate ($V_{Driving} = 3.3 \text{ V}$). Here, the $V_{Driving}$ means the driving voltage of the driving mode fingers. The sensitivity is 1.1866 mV/ %s and the linearity is 98.44% (with a full scale of 700 %s). Figure 21 shows the output voltage *versus* the angular rate under different $V_{Driving}$. For $V_{Driving} = 10 \text{ V}$, the sensitivity is 9.16 mV/ %s and the linearity is 99.16% (with a full scale of 300 %s). The results of the out-of-plane gyroscope are summarized in Table 5.

Figure 20. Output voltage of the gyroscope under different angular rates.

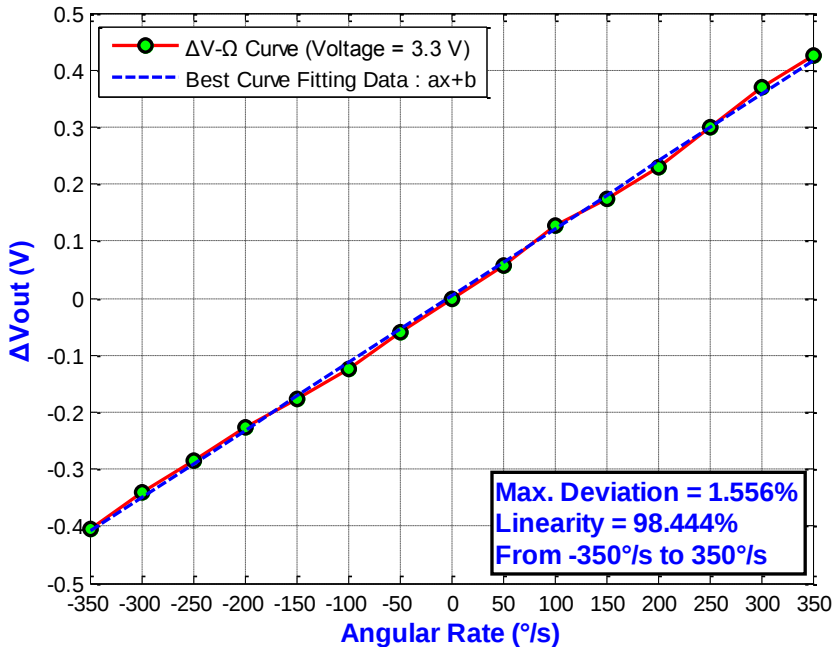
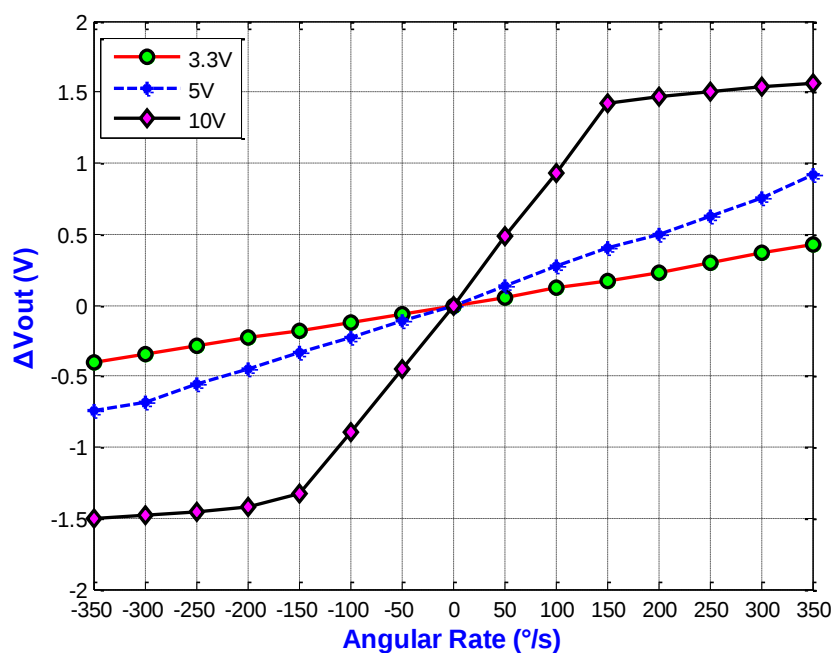
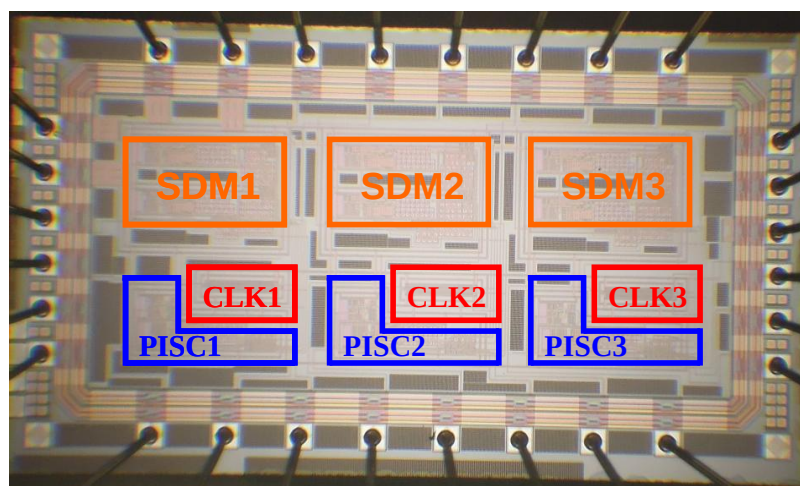


Figure 21. Output voltage *versus* the angular rate under different $V_{Driving}$.**Table 5.** Specification of the out-of-plane gyroscope.

Parameters	3.3 V	5 V	10 V
Sensitivity (mV/°s)	1.1866	2.3882	9.16
Dynamic Range (°s) (Full Scale)	700	600	300
Linearity (%)	98.44	98.28	99.16

4. Experimental Results

The proposed PISC circuit combined one-bit SDM circuit has been tested. The chip, shown in Figure 22, is 2.817 mm × 1.513 mm, and contains three PISCs, three CLKs, and three SDM blocks.

Figure 22. SEM of the proposed sensing circuit.

Here, the PISC1 means the PISC circuit has the $C_{Gyro} = 500$ fF, the PISC2 means the PISC circuit has the $C_{Gyro} = 540$ fF, and the PISC3 means the PISC circuit has the $C_{Gyro} = 460$ fF. CLK indicates the non-overlapping clock circuit. A photograph of the test PCB block is shown in Figure 23. The measured voltage result for the PISC2 circuit ($C_{Gyro} = 540$ fF) is 2.72 V, as shown in Figure 24. The pre- and post-layout simulation results are shown in the up-right corner in Figure 24. These results are very similar. Other results are summarized in Table 6. The experimental results of the PISC circuit using signal processing have significantly smaller voltage offset and noise floor than those without using signal processing, as shown in Figure 25.

Figure 23. Photograph of the test PCB.

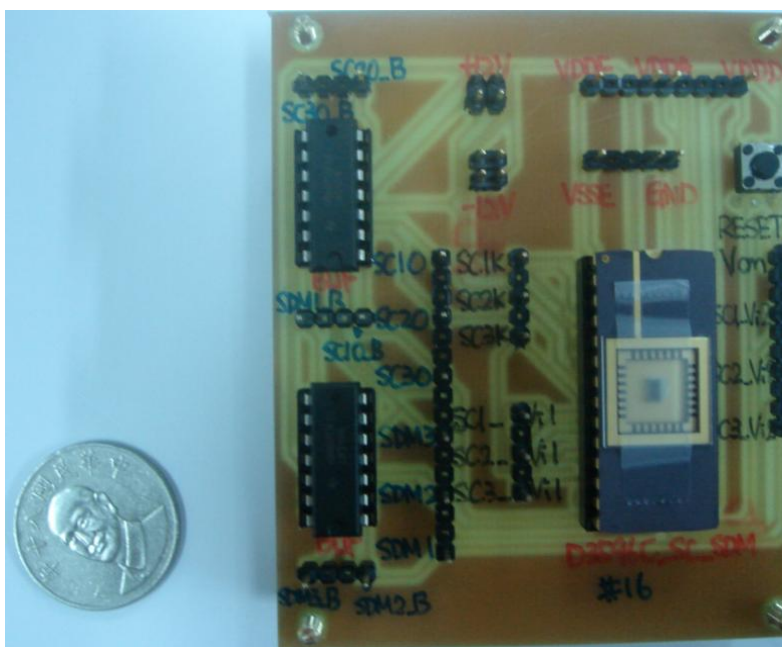


Figure 24. Measured results for PISC2 ($C_{Gyro} = 540$ fF).

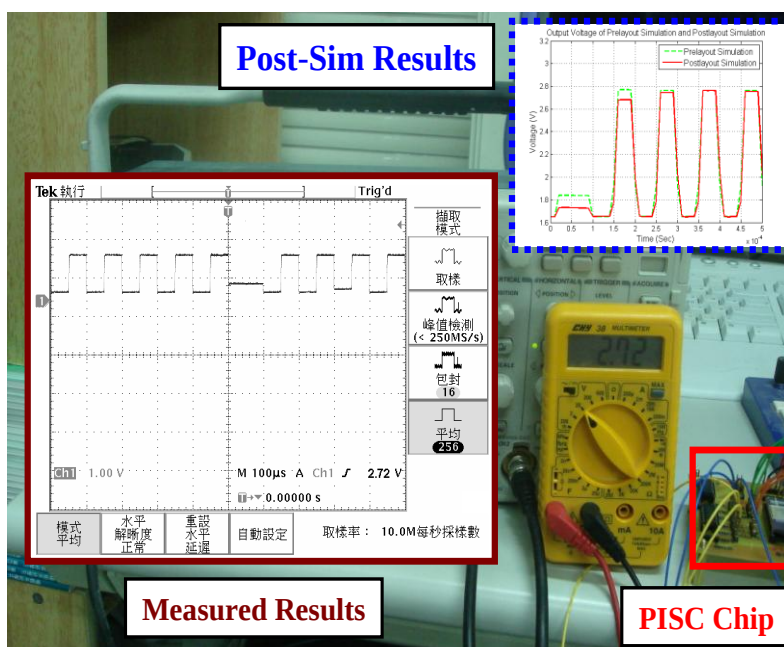


Table 6. Comparison of simulation and experimental results for PISC circuits.

Term	Simulation Results	Experimental Results
Supply Voltage (V)	3.3	3.3
PISC1 (V)	1.65–1.78	1.6–1.81
PISC2 (V)	1.65–2.78	1.6–2.8
PISC3 (V)	0.7–1.65	0.7–1.6

Figure 25. Experimental results using signal processing.

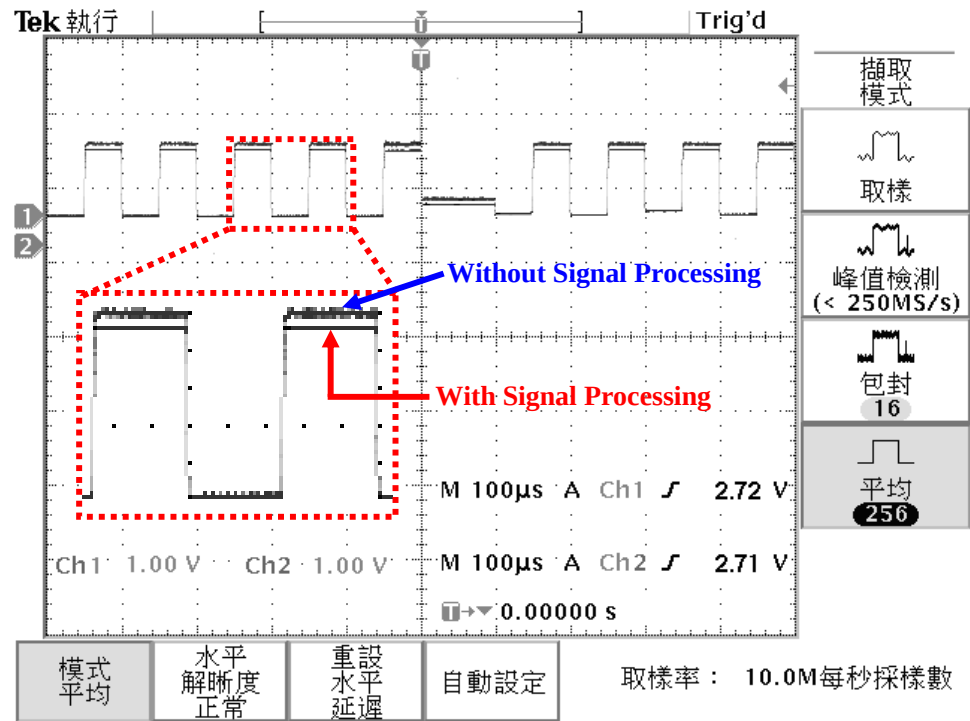


Table 7 summarizes a comparison on the results of the proposed PISC circuit and other capacitive sensing circuits reported in the literature. It can be noted that the proposed PISC circuit has the smallest noise floor and chip area. The voltage offset is comparable to [11] but smaller than the remaining solutions listed in Table 7. The capacitive sensing circuits in [11] is simulation result. The resolution is comparable to [12] but smaller than other capacitive sensing circuits already presented in the literature. For standalone applications, the device gives an analog output and provides digital output with embedded one-bit $\Sigma\Delta$ ADC.

5. Conclusions

In this study, we present a novel PISC sensing circuit design in order to obtain high sensitivity and ultra linearity for an out-of-plane gyroscope. From the simulation results, we can see that the proposed PISC circuit has a good sensitivity of 9.16 mV/%s and a high linearity of 99.16% in a wide dynamic range from -300 %s to 300 %s. The experimental results also show a good performance. In addition, the PISC circuit can use signal processing to cancel the offset and noise. Thus, this circuit is very suitable for gyroscope measurement.

Table 7. Comparison with CMOS capacitive sensing circuits in the literature.

	[7]	[10]	[11]	[12]	[13]	[19]	This Work
Process	0.35 μm , CMOS	0.8 μm , CMOS	0.35 μm , CMOS	2 μm , CMOS	0.35 μm , CMOS	0.8 μm , CMOS	0.35 μm , CMOS
Application	Gyroscope	Accelerometer	Accelerometer	Accelerometer	Gyroscope	Transducer	Gyroscope
Architecture	Fully Differential	Fully Differential	Fully Differential	Switched Capacitor	DC Sensing	Differential	PISC
ADC	7 bits SAR	None	1 bit $\Sigma\Delta$	None	None	None	1 bit $\Sigma\Delta$
Sensitivity	N.A.	4 fF/m/s ²	N.A.	0.122 V/m/s ²	N.A.	40 mV/fF	9.16 mV/ %s
Linearity (%)	N.A.	N.A.	N.A.	99.95	N.A.	N.A.	99.16
ΔC Range (fF)	~400	N.A.	0.13	~1,800	N.A.	0.2	± 40
Capacitance Sensitivity (mV/fF)	N.A.	N.A.	~10	10 ~ 50	N.A.	42	25.8938
Resolution (fF)	3.5	0.0255	N.A.	<0.01	0.195	10	0.01273
Voltage Offset (mV)	8	N.A.	1	N.A.	N.A.	200	1.9964
Noise Floor ($\mu\text{V}/\text{Hz}^{1/2}$)	N.A.	37 at 36 kHz	0.2 at 500 kHz	0.96 at 1 kHz	N.A.	N.A.	0.1564 at 10 kHz
Power Dissipation (mW)	N.A.	N.A.	5 at 3 V	N.A.	N.A.	N.A.	2.2973 at 3.3 V
Chip Area (mm ²)	3.625	5.76	N.A.	15.2	1.44	14.62	1.421
Simulation/Chip	C	C	S	C	C	C	C

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