Article

Ultra-Low Power High Temperature and Radiation Hard Complementary Metal-Oxide-Semiconductor (CMOS) Silicon-on-Insulator (SOI) Voltage Reference

El Hafed Boufouss *, Laurent A. Francis, Valeriya Kilchytska, Pierre Gérard, Pascal Simon and Denis Flandre

ICTEAM Institute—Electrical Engineering, Université catholique de Louvain, Maxwell Building, Place du Levant 3, B-1348 Louvain-la-Neuve, Belgium;
E-Mails: laurent.francis@uclouvain.be (L.A.F.); valeriya.kilchytska@uclouvain.be (V.K.); pierre.gerard@uclouvain.be (P.G.); pascal.simon@uclouvain.be (P.S.); denis.flandre@uclouvain.be (D.F.)

* Author to whom correspondence should be addressed; E-Mail: elhafed.boufouss@uclouvain.be; Tel.: +32-104-725-69; Fax: +32-104-725-98.

Abstract: This paper presents an ultra-low power CMOS voltage reference circuit which is robust under biomedical extreme conditions, such as high temperature and high total ionized dose (TID) radiation. To achieve such performances, the voltage reference is designed in a suitable 130 nm Silicon-on-Insulator (SOI) industrial technology and is optimized to work in the subthreshold regime of the transistors. The design simulations have been performed over the temperature range of -40–$200\,^\circ$C and for different process corners. Robustness to radiation was simulated using custom model parameters including TID effects, such as mobilities and threshold voltages degradation. The proposed circuit has been tested up to high total radiation dose, *i.e.*, 1 Mrad (Si) performed at three different temperatures (room temperature, $100\,^\circ$C and $200\,^\circ$C). The maximum drift of the reference voltage V_{REF} depends on the considered temperature and on radiation dose; however, it remains lower than 10% of the mean value of 1.5 V. The typical power dissipation at 2.5 V supply voltage is about 20 μW at room temperature and only 75 μW at a high temperature of $200\,^\circ$C. To understand the effects caused by the combination of high total ionizing dose and temperature on such voltage reference, the threshold voltages of the used SOI MOSFETs were extracted under different conditions. The evolution of V_{REF} and power consumption with temperature and radiation dose can then be explained in terms of the different balance between fixed oxide

charge and interface states build-up. The total occupied area including pad-ring is less than 0.09 mm^2.

1. Introduction

Silicon circuits are increasingly sought by biomedical applications, such as radiation detectors, breathing sensors and temperature sensors. These applications often require ultra-low power circuits, sometimes also robust to harsh environments. Figure 1 shows our previous development [1] of an ultra-low power microsystem, composed of a temperature sensor, a comparator and a voltage reference. This microsystem aims at temperature sensing in the harsh conditions used in medical sterilization such as high total ionized dose radiation (TID) or high temperature. It has three main functions: detecting a user-defined temperature threshold T_0, generating a wake-up signal that turns on a data-acquisition microprocessor above T_0, and measuring temperatures above T_0. The microsystem was developed using a suitable and robust technology, *i.e.*, 1 μm partially-depleted (PD) Silicon-on-Insulator (SOI). Such technology is often used in harsh environments applications because of its attractive features; extended range of working temperature (up to 300 °C), reduced parasitic effects, low-power, high speed and lower sensitivity to transient radiation effects comparing to other technologies [2]. However, during measurements, the voltage reference circuit was the weak point of the microsystem and showed a large shift in the measured reference voltage with radiation of up to 900 mV at 1 Mrad (Si) [3]. To overcome this limitation, a new design of an ultra-low power and harsh-environment immune voltage reference is performed. We firstly choose to port the design to a more suitable SOI industrial technology with Complementary Metal-Oxide-Semiconductor (CMOS) process node of 130 nm featuring a much reduced gate and buried oxides thickness and hence TID degradation [4]. Secondly, we improved the architecture by introducing a cascode bias stage for enhanced stability, and a new start-up design to avoid start deficiency at low temperature and extreme corners (resulting in high V_{th}). This proposed circuit is optimized to work in the subthreshold regime of the transistors in order to achieve ultra-low power dissipation (less than 100 μW) at high temperature (up to 200 °C).

In this paper, we firstly present the design of the voltage reference circuit. Then, we detail the experimental results of the voltage reference under large range of temperature and under combined high temperature and radiation influence. Lastly, we explain the impact of the combination of high total ionizing dose and high temperature on the proposed circuit and draw conclusions.

Figure 1. Biomedical microsystem adapted from [1].
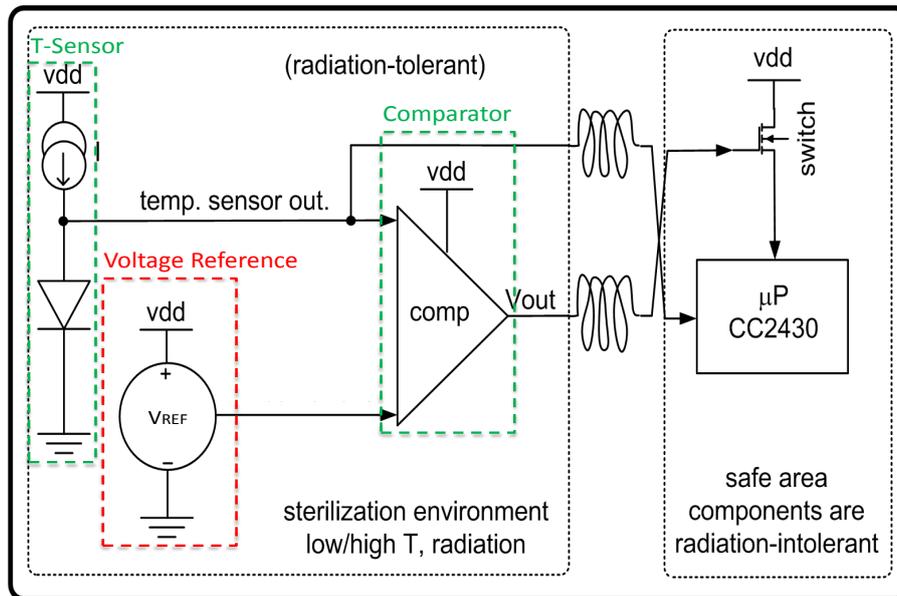
2. Basic Concepts

2.1. Voltage Reference Circuit Description

The voltage reference is a CMOS circuit (Figure 2) based on the gate-source voltage difference between a pair of P-type MOS (PMOS) and N-type (NMOS) transistors (M_p and M_n) biased by a proportional to absolute temperature (PTAT) current I_{REF} (Equation (8)). Differently to the initial work described in [5], our design was: (1) improved by introducing a cascode bias stage for enhanced stability and a new start-up design to avoid start deficiency at extreme temperature and process corners (resulting in high V_{th}); (2) extended to operate in a large temperature range from −40 to 200 °C; (3) conceived to limit the power dissipation in harsh environments, using transistors optimized to work in subthreshold regime.

Figure 2. Voltage reference circuit adapted from [3].
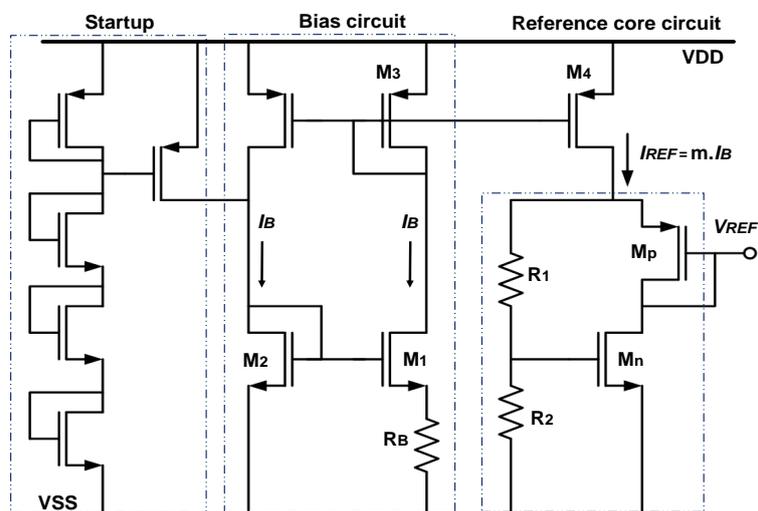
In the next paragraph, operation of our previous circuit [3] is reviewed, and in the next sections, an improved architecture is proposed.

2.2. Design Principles

From the analysis of the circuit described in Figure 2, the voltage reference value V_{REF} and the bias current I_B are obtained as:

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GSn} - |V_{GSp}| \tag{1}$$

$$I_B = \frac{V_{GS2} - V_{GS1}}{R_B} \tag{2}$$

where V_{GSn}, V_{GSp}, V_{GS1} and V_{GS2} are the gate-source voltages for transistors M_n, M_p, M_1 and M_2, respectively. For NMOS and PMOS transistors working in the subthreshold regime, the $I - V$ characteristics can be expressed by [6]:

$$I_{Dn} = \beta_n \cdot U_T^2 \cdot exp\left(\frac{V_{GS} - V_{thn}}{n \cdot U_T}\right) \cdot \left[1 - exp\left(\frac{V_{DS}}{U_T}\right)\right] \tag{3}$$

$$I_{Dp} = \beta_p \cdot U_T^2 \cdot exp\left(\frac{V_{SG} - |V_{thp}|}{n \cdot U_T}\right) \cdot \left[1 - exp\left(\frac{V_{SD}}{U_T}\right)\right] \tag{4}$$

where $\beta_n = \mu_n.C_{ox}.(W_n/L_n)$ and $\beta_p = \mu_p.C_{ox}.(W_p/L_p)$, $\mu_{n,p}$ is the electron and holes mobilities in the channel, C_{ox} is the oxide capacitance per unit area, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS respectively, W_n (W_p) and L_n (L_p) are the channel width and length for NMOS (PMOS), respectively. $U_T = k_B.T/q$ is the thermal voltage (k_B is the Boltzmann constant, q the elementary charge and T the absolute temperature), n is the subthreshold slope parameter, V_{GS} and V_{DS} (V_{SG} and V_{SD}) are the gate-to-source and drain-to-source voltages respectively for the NMOS (PMOS) transistor. For $|V_{DS}| > 4U_T$, the drain current I_D becomes almost independent of the drain-to-source voltage [7], so that from Equations (3) and (4) we can extract :

$$V_{GSn} = n \cdot U_T \cdot ln\left(\frac{I_{Dn}}{\beta_n \cdot U_T^2}\right) + V_{thn} \tag{5}$$

$$|V_{GSp}| = n \cdot U_T \cdot ln\left(\frac{I_{Dp}}{\beta_p \cdot U_T^2}\right) + |V_{thp}| \tag{6}$$

In Figure 2, if k is the size ratio $(W_1.L_2/(L_1.W_2))$ of transistors M_1 and M_2, m the current copy ratio in the output stage ($I_{REF} = m.I_B$) and using Equations (2) and (5), the bias current I_B is given by:

$$I_B = n \cdot U_T \cdot \left(\frac{ln(k)}{R_B}\right) \tag{7}$$

$$I_{REF} = m \cdot n \cdot U_T \cdot \left(\frac{ln(k)}{R_B} \right) \tag{8}$$

Assuming that the current through the resistances R_1 and R_2 is negligible and using Equations (1), (5) and (6) we obtain the following expression of V_{REF}:

$$V_{REF} = n \cdot U_T \cdot \left[ln \left(\frac{\beta_{Mp}}{\beta_{Mn}} \right) + M_r \cdot ln \left(\frac{n \cdot m \cdot ln(k)}{R_B \cdot \beta_{Mn} \cdot U_T} \right) \right] + (1 + M_r)V_{thn} - |V_{thp}| \tag{9}$$

with $\beta_{M_{n(p)}} = \mu_{n(p)} \cdot C_{ox} \cdot (W/L)_{n(p)}$ for the output transistors M_n and M_p respectively (Figure 2). These β parameters ($\propto T^{-\alpha}$ with $\alpha \geq 1.5$) together with the parameter n and the threshold voltage V_{thn} and V_{thp} have a temperature dependency [8,9]. M_r is the resistors ratio (R_1/R_2). R_B is a non-silicided polysilicon resistance, showing almost negligible temperature dependency in the simulations.

3. Circuit Realization

A new design of the voltage reference (Figure 3) was developed with a cascoded current source, to reduce the V_{REF} variations due to the process corners, supply voltage variation and mainly the radiation effects caused by single ionized particles [10]. As it is based on the same principle as the previous design [3], the voltage reference expression V_{REF} remains unchanged (Equation (9)).

Figure 3. Proposed voltage reference circuit.
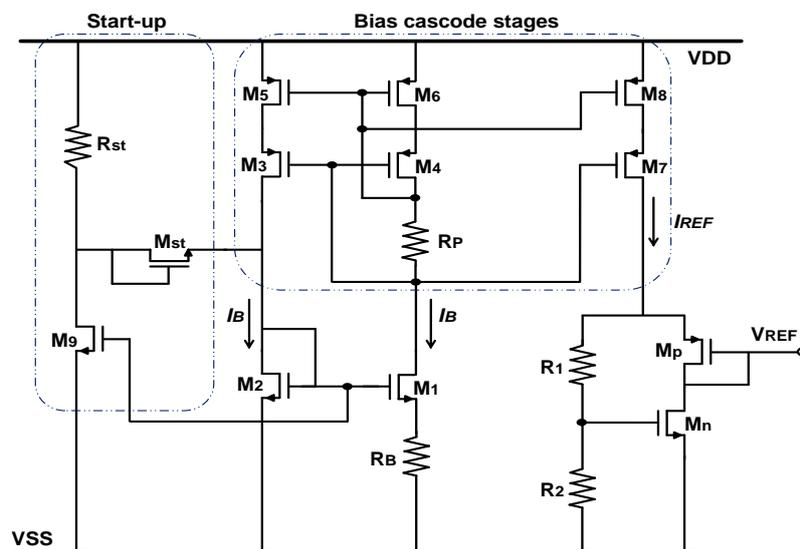
3.1. Design Phases

3.1.1. Technology Characterization at High Temperature

The voltage reference circuit was developed based on the analog MOSFETs of an industrial 130 nm PD SOI CMOS featuring a 5 nm gate oxide thickness and 280 nm minimum length. The SPICE

(BSIM3SOI) models available for this technology are commercially validated up to $150\,°C$. We checked the models validity up to $200\,°C$, by comparing the typical DC $I_D(V_{GS})$ characteristic of a MOSFET transistor extracted by simulations and from measurements for different temperatures (25, 150, 175 and $200\,°C$). Figures 4 and 5 show two examples of the good agreement between simulated and measured curves, for NMOS and PMOS transistors at $25\,°C$ and $200\,°C$, in the subthreshold region of interest. The slight discrepancies for the PMOS transistor can be neglected since the circuit design has to cope with much larger variations due to process, temperature and radiations.

Figure 4. Measured and simulated I_D versus V_{GS} curves at $25\,°C$, $V_{DS} = 1.5$ V, W $= 1\ \mu$m, L $= 0.28\ \mu$m.
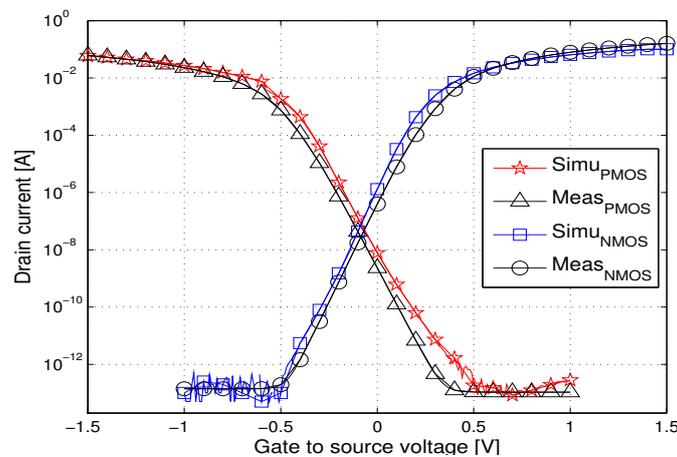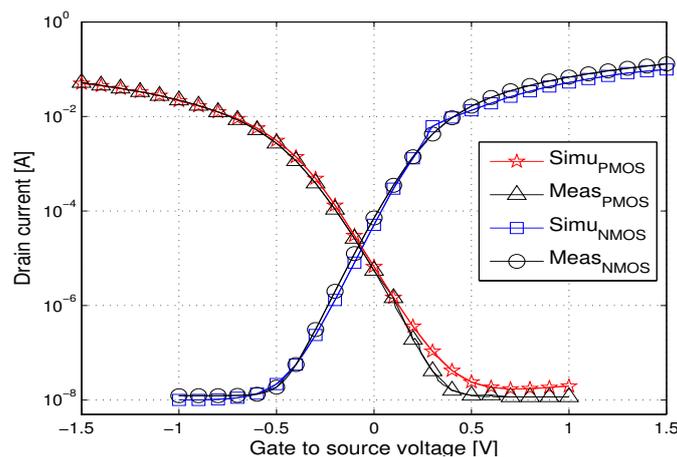

Figure 5. Measured and simulated I_D versus V_{GS} curves at $200\,°C$, $V_{DS} = 1.5$ V, W $= 1\ \mu$m, L $= 0.28\ \mu$m.

3.1.2. Design Optimization

The design optimization consists in determining the bias current I_B and the transistor and resistor sizes (in Figure 3) to minimize the V_{REF} variation with the device physical parameters as given by the previous equations and process corners. The temperature dependence of the voltage reference must be as

low as possible. The aforesaid dependence is expressed by evaluating the temperature coefficient (TC) defined by the following expression:

$$[TC] = \frac{1}{V_{REF}} \times \left[\frac{dV_{REF}}{dT} \right] \qquad (10)$$

In order to minimize the TC coefficient for our design, we have extracted temperature dependencies of the physical parameters, computed Equation (10) and searched the best design parameters (W_1, W_2, L_n, m, M_r, W_n, W_p and R_B). However this first guess does not take into account the process corners. Next, extensive ELDO (Mentor Graphics) simulations were performed for the different process corners in a temperature range of -40 to $200\,^{\circ}\mathrm{C}$.

3.2. Design Robustness Against Radiation Effects

To take into account the variations due to radiation effects, additional constraints were considered as follow:

- The designed circuit was checked with custom model parameters of transistors including TID effects on transistors [11] (up to 30% mobilities degradation and negative voltage threshold shifts of 100 mV).
- Using transistors with a body contact to limit the effect of the parasitic bipolar possibly created by radiation [10].
- Choosing relatively long transistor to assure lower leakage current and lower threshold voltages shift, which may appear as a result of TID and high-temperature effects [2,12,13].
- The circuit layout is further carried out by paying attention to critical components; thus all matched device pairs were realized by a centroid implementation, including the necessary dummies (Figure 6).

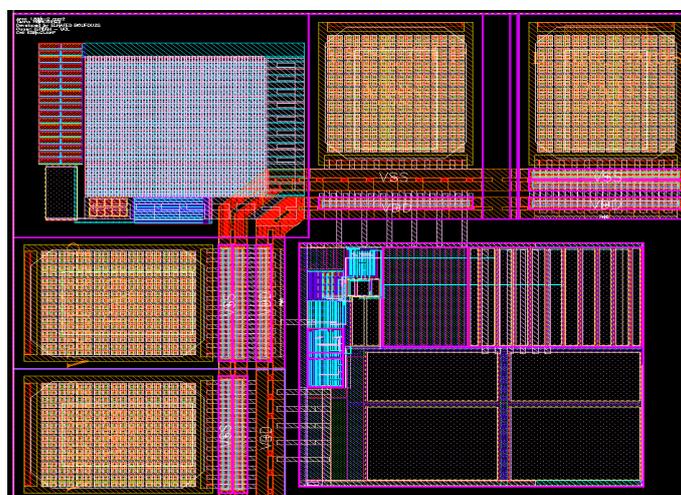**Figure 6.** Final layout of the voltage reference.

Table 1 gives the bias setting and different dimensions of transistors and resistors used in the proposed voltage reference circuit.

**Table 1.** Voltage references bias setting and devices dimensions.

Parameter	Description	Value
VDD	Power supply	2.5 V
I_B	Bias current@25 °C	2.5 μA
$(W/L)_1$	Size of NMOS M_1	40 μm/0.5 μm
$(W/L)_2$	Size of NMOS M_2	10 μm/0.5 μm
$(W/L)_{3-6}$	Size of PMOS M_3,M_4,M_5 and M_6	10 μm /0.5 μm
$(W/L)_{7-8}$	Size of PMOS M_7 and M_8	25 μm/0.5 μm
$(W/L)_p$	Size of PMOS M_p	200 μm/0.5 μm
$(W/L)_n$	Size of NMOS M_n	20 μm/1 μm
$(W/L)_9$	Size of NMOS M_9	5 μm/0.5 μm
$(W/L)_{st}$	Size of NMOS M_{st}	5 μm/1 μm
R_B	R_B resistor value	25 kΩ
R_1	R_1 resistor value	50 MΩ
R_2	R_2 resistor value	20 MΩ
R_{st}	R_{st} resistor value	1.5 MΩ

3.3. Simulations Results

Simulations are performed for five different process corners and a custom model parameters of transistors including TID effects, namely:

- Typ: typical corner (typical $|V_{th}|$ values)
- FFA: Fast PMOS and NMOS (min $|V_{th}|$ values) with minimum resistances values
- SSA: Slow PMOS and NMOS (max $|V_{th}|$ with maximum resistances values
- FSA and SFA: are the crossed cases (fast and slow)
- RAD: Custom model parameters of transistors including TID effects (30% degradation of the mobility and a threshold voltage shift of 100 mV).

As shown in Figure 7, the reference voltage V_{REF} versus temperature range of -40 to 200 °C gives an average voltage of 1.5 V for Typical corner, with a variation of $\pm 8\%$ over all process corners and temperature/radiation conditions. More specifically, lower $|V_{th}|$ values lead to a lower V_{REF} at a given temperature according to Equation (9), whereas the temperature dependence depends on the exact balance between the n, U_T and the V_{th} terms.

Figure 7. Simulated reference voltage V_{REF} versus temperature and process corners.
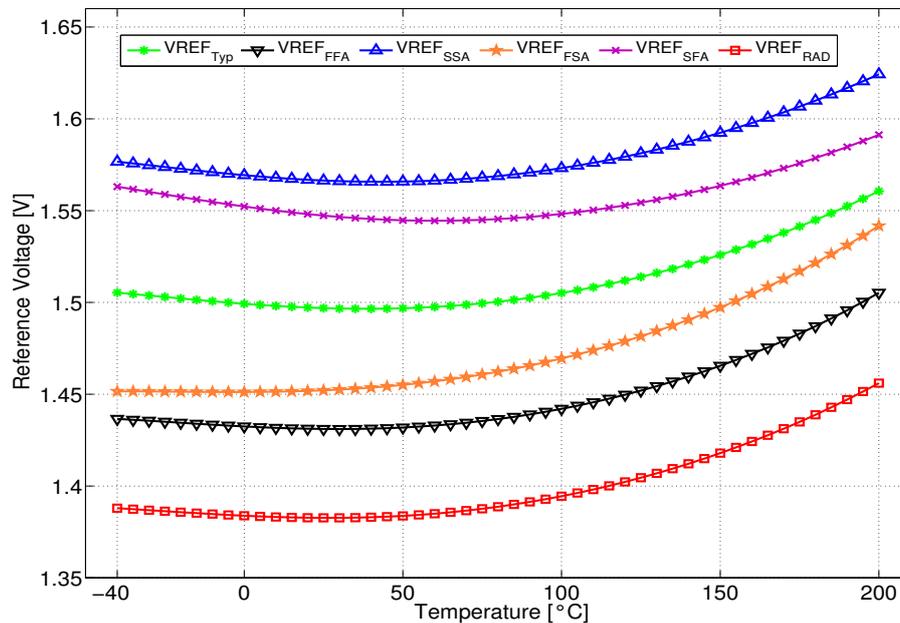

4. Experimental Results

The main purpose of our voltage reference is to be used in a harsh biomedical sterilization conditions. To validate this feature, first the voltage reference circuit was measured in a large range of temperatures from -40 to $200\,^\circ$C. Subsequently, other chips have been tested during irradiation at different temperatures, using a small ceramic heater resistor placed under chips. Irradiation was performed at the Cyclotron facility of UCL with Gamma-rays, using a Cobalt source (^{60}Co). The next sections present the measured results for a power supply of 2.5 V.

4.1. Temperature Measurements

The experimental voltage reference generates a mean reference voltage of about 1.5 V (Figure 8) with a variation of about 1%, for the temperature range of -40–$90\,^\circ$C with a temperature coefficient less than 133 $ppm/\,^\circ$C. This increases to 470 $ppm/\,^\circ$C for the large tested temperature range of -40–$200\,^\circ$C with a maximum variation of 10%. The maximum power dissipation is less than $42\,\mu W$ at the lower temperature of $-40\,^\circ$C, about $50\,\mu W$ at room temperature and only $75\,\mu W$ at a high temperature of $200\,^\circ$C (Figure 9).

The 10% increase of the reference voltage value V_{REF} textitversus temperature can be explained through the increase of the subthreshold current and parameters n, U_T and $(1/\beta_{Mn})$ shown in the Equation (9). The decrease of the absolute values of threshold voltages of transistors V_{thn} and $|V_{thp}|$ with temperature [8] helps (but not sufficiently) to limit the increase of V_{REF} value versus temperature. To first order, the power dissipation of the circuit is equal to "$V_{DD}.(m+2).I_B$" and according to Equation (8) is proportional to the term n.U_T ($\propto$ n.T). This explains the linear variation with temperature of the power dissipation of the reference voltage (Figure 9).

Figure 8. Measured voltage reference V_{REF} *versus* temperature.
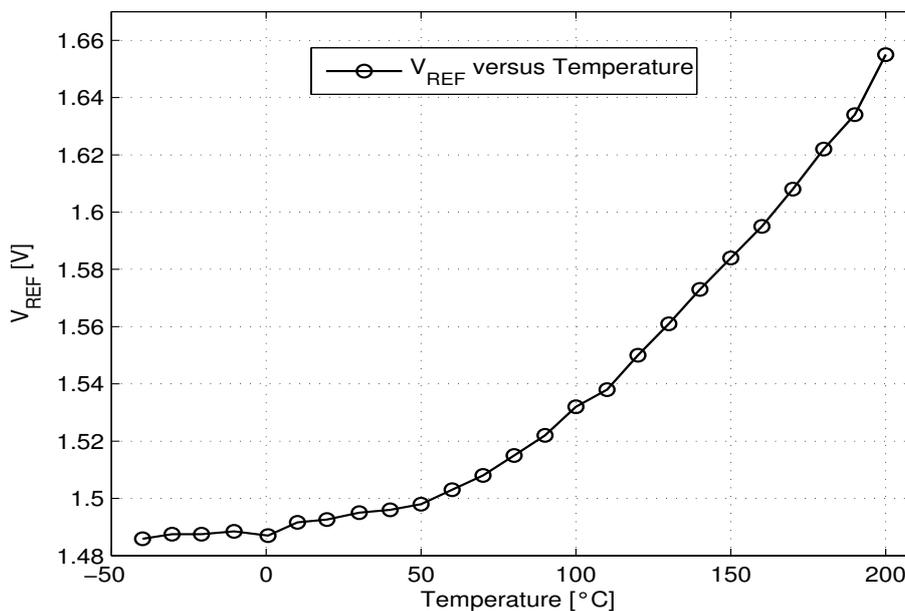
Figure 9. Measured current consumption *versus* temperature.
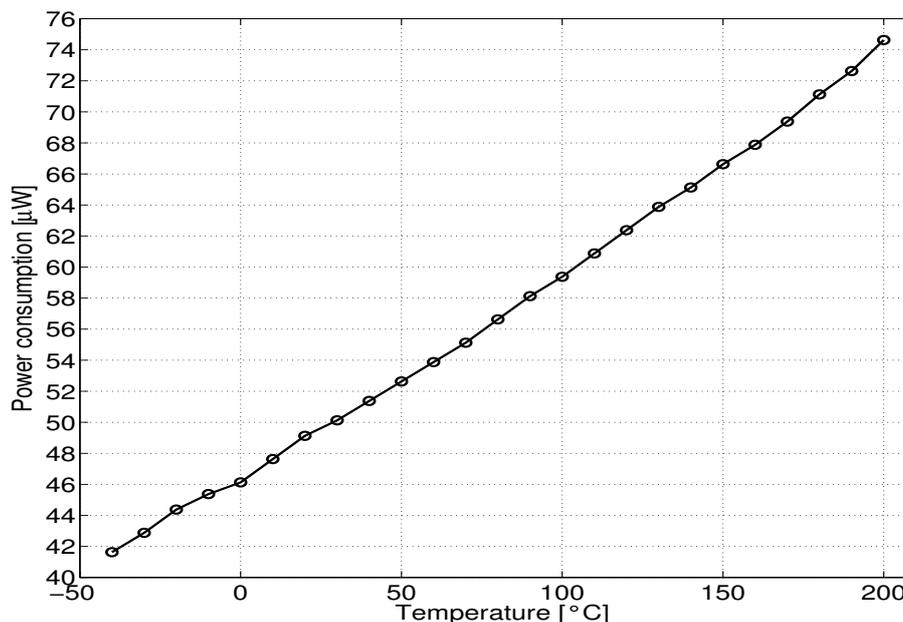
4.2. Measurements under Combined High Temperature and Radiation Exposure

Six chips were exposed to gamma-rays radiation during one week with a dose rate of 10 krad/h and regularly measured. Two chips were kept at room temperature, two heated at 100 °C during radiation and the last two chips at 200 °C. The voltage reference value remains about the expected voltage of 1.5 V with a maximum increase of $\pm 5\%$ shift for room and 200 °C temperature. At 100 °C the voltage reference value increases with total dose up to 400 krad (Si) and starts to decrease at higher dose (Figure 10). The power consumption of the voltage reference increases with radiation and temperature, except for the highest heating temperature during radiation for which the power remains stable at about 75 μW upon radiation (Figure 11). Similar trends are observed for all measured chips. Similarly to temperature case,

we can express the radiation dependencies of the voltage reference circuit. This is about 25 *ppm*/krad for room temperature up to 1 Mrad (Si).

Figure 10. Measured voltage reference V_{REF} *vs* TID at different temperatures.
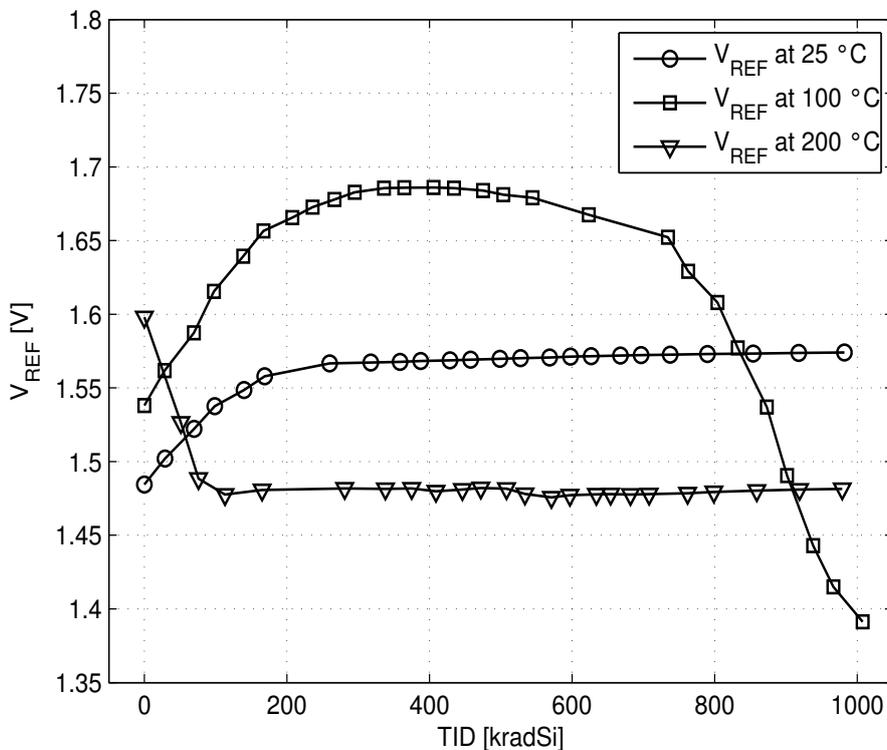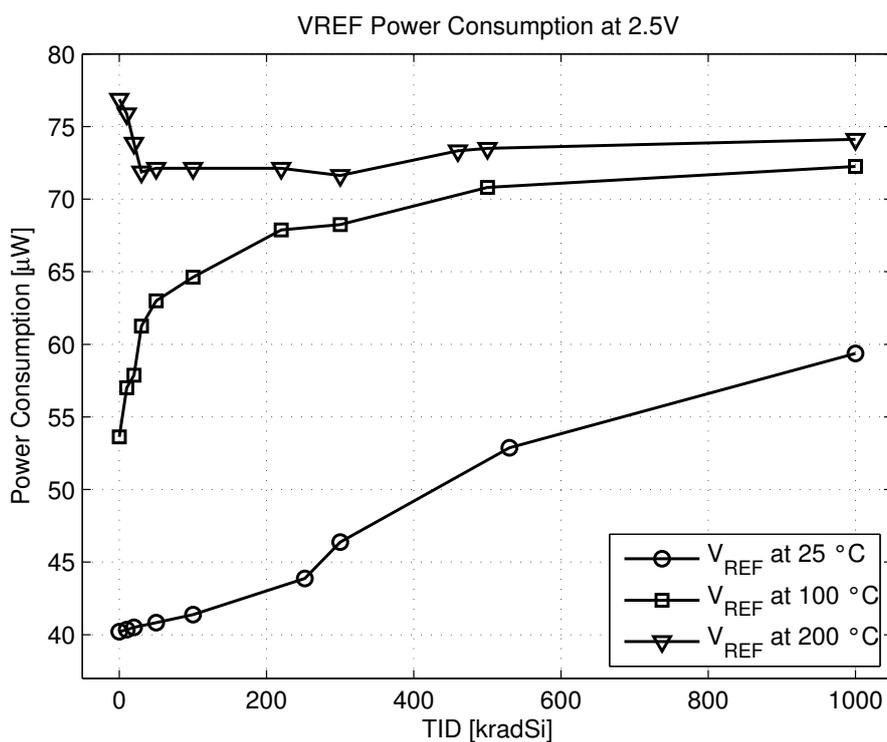

Figure 11. Measured voltage reference power consumption at 2.5 V power supply, in the same conditions as in Figure 10.

4.3. Discussion of Measurement Results

In order to understand the effect of the combination of radiation and high temperature on the designed voltage reference circuit, the threshold voltages $Vth_{n,p}$ for the used SOI transistors were extracted in the same conditions (irradiation + temperatures). Gamma-rays radiation is known to result in oxide and interface charges build-up (N_{ox} and N_{it}). They shift the threshold voltages as ($Vth_n \propto (N_{it} - N_{ox})$ and $|Vth_p| \propto (N_{it} + N_{ox})$) and degrade mobilities in transistors [11].

Thus, for PMOS (Figure 12) the absolute $|Vth_p|$ value increases with radiation. This effect is amplified at 200 °C due to higher N_{it} creation. For NMOS transistor (Figure 13), at room temperature, induced N_{ox} charges are dominant (versus N_{it}) and, therefore Vth_n value decreases slightly. At 100 °C a balance between N_{ox} and N_{it} occurs and keeps a relatively stable value for Vth_n versus radiation dose. N_{it} becomes dominant at 200 °C and leads to an increase of the NMOS threshold voltage with dose.

Figure 12. Measured PMOS voltage threshold *vs* TID at different temperatures.
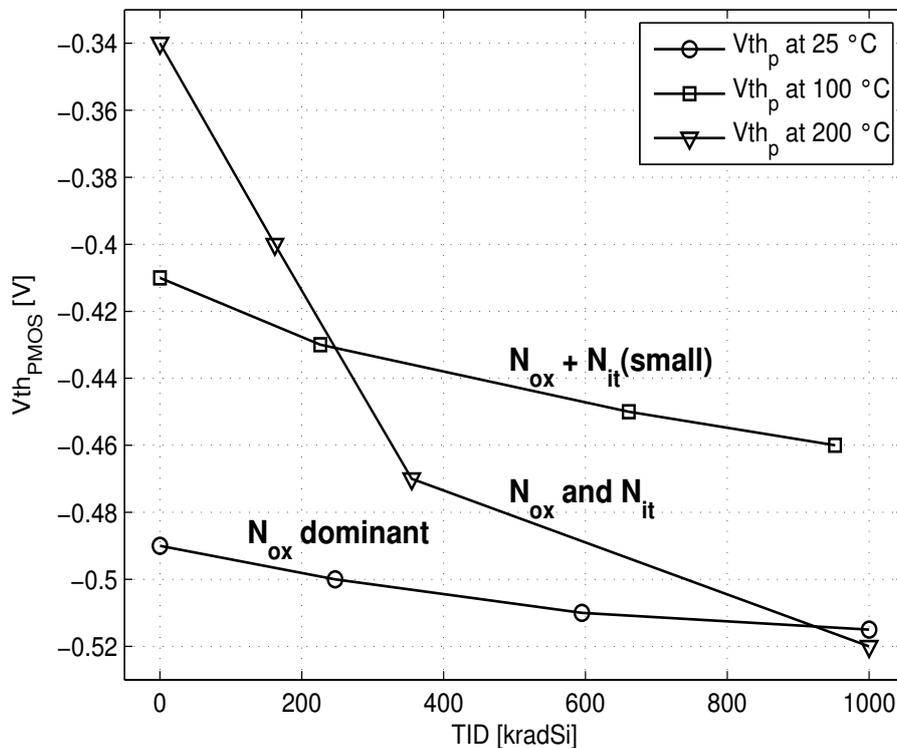
Then, based on the previous expression of V_{REF} (Equation (9)) and knowing that the parameter n is increased and the carrier mobilities $\mu_{n(p)}$ are degraded both by radiation and temperature [11,14], we can explain the combined effect of radiation and temperature on the circuit (Figures 10 and 11) as follows.

• At room temperature: As the shift of threshold voltages of PMOS and NMOS seems to be small, the increase of V_{REF} and the power dissipation can be explained by the increase of the parameter n and the decrease of the mobility μ_n ($\propto$ to $1/\beta_{Mn}$) under radiation.

• At 100 °C: At small dose (less than 400 krad) the same effects as for room temperature occur. For higher dose, the absolute value of the threshold voltage of PMOS increases while the NMOS one

remains quasi stable, thus leading to the decrease of the voltage value of V_{REF} and to stabilize the power dissipation.

• At 200 °C: After an initial decrease of Vth_n and increase of $|Vth_p|$ which is reflected in a decrease of V_{REF} and the power dissipation, both absolute values of Vth_n and Vth_p increase under radiation. Thus, they compensate each other in the Equation (9) leading to a stable value of V_{REF} and power consumption.

Figure 13. Measured NMOS voltage threshold *vs* TID at different temperatures.
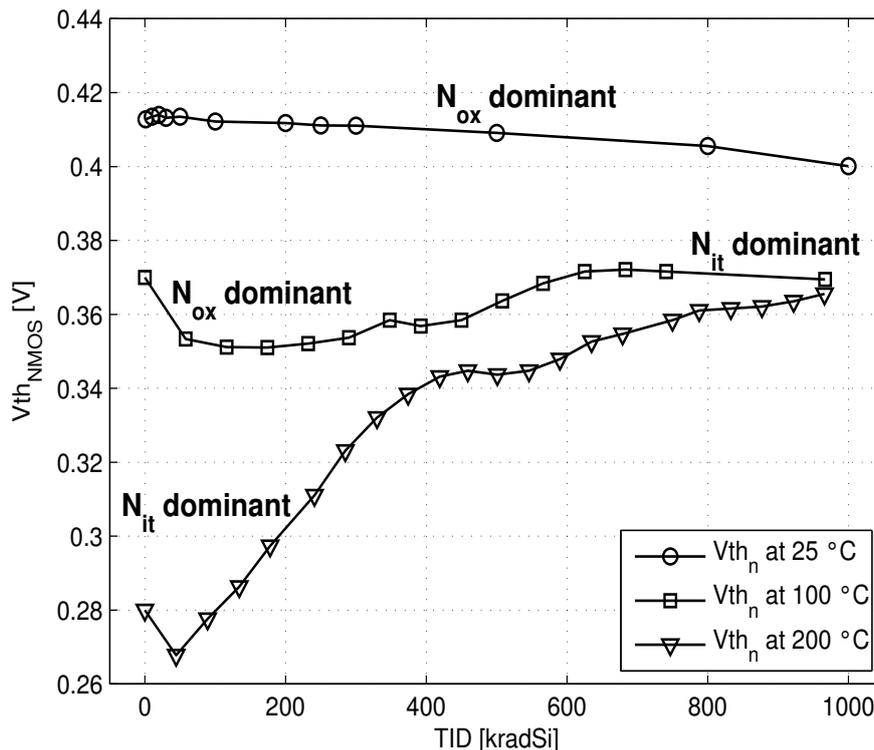
4.4. Comparison with the State of the Art

Table 2 summarizes the performance of the proposed voltage reference circuit and compares it with results of the literature. When compared to our previous work [3], the new circuit is twice less sensitive to temperature variation and the sensitivity to radiation is divided by more than one order of magnitude thanks to: (1) the suitable SOI technology featuring a reduced oxide thickness (5 nm in this work versus 25 nm in the previous work) which limits oxide charge build-up and hence TID degradation; (2) to the new design circuit performed with reasonable margin for the current consumption.

When compared to literature, the proposed circuit operates in a wider range of temperature −40 to 200 °C and radiation (up to 1 Mrad (Si)) than other solutions. Our circuit proposes a high reference voltage value of 1.5 V with a small current consumption (less than 20 μA at room temperature) and achieves a low temperature coefficient for a similar range of temperature.

Table 2. Performance comparison with similar voltage references described in the literature.

Parameter	This Work	Previous work [3]	Leung [5]	Malcovati [15]	Ivanovic [16]	Gromov [17]
Technology	0.13 μm SOI	1 μm SOI	0.6 μm Bulk	0.35 μm BiCMOS	–	0.13 μm Bulk
Supply voltage	2.5 V	5 V	1.4 to 3 V	1 V	–	1.4 V
Reference voltage (V)	1.5	1.8	0.333	0.54	1.6	0.405
Temperature range ($^\circ$C)	−40–200	−40–300	0–100	0–80	−40–120	0–80
TC (ppm/$^\circ$C)	133 [−40, 90 $^\circ$C] 470 [−40, 200 $^\circ$C]	375 [−40, 90 $^\circ$C] 825 [−40, 200 $^\circ$C]	94	212	90	200
Consumption @ 25 $^\circ$C	20 μA	2 μA	9.7 μA	92 μA	-	-
V_{REF} shift due to radiation ($ppm/krad$)	25	426	–	–	140	0.68
Irradiation particles	Gamma-rays	Gamma-rays	–	–	Neutron	X-rays
Maximum V_{REF} shift due to Combined effect of temperature and radiation up to 1 Mrad (Si)	+10%	–	–	–	–	–
Dose Mrad (Si)	1	1	–	–	1	44

5. Conclusions

In this work we demonstrated an ultra-low power voltage reference circuit, designed in the subthreshold regime of transistors, developed to be used in harsh environment such as biomedical sterilization. This circuit was simulated up to 200 °C using our extended MOS models and was shown to consume about 75 μW only at higher temperature. The design was verified to be robust against radiation effects (using custom model parameters) and the voltage reference value very fairly stable over a large range of process corners and temperature variations. To enhance immunity to total dose effects, the layout has been implemented using specific guidelines and a suitable SOI CMOS technology with thin gate and buried oxides. Measurements have shown a fairly correct operation of such ultra-low power circuit for a large temperature range (from -40 °C up to 200 °C) and under a combination of total ionizing dose (up to 1 Mrad (Si)) and high temperature. The threshold voltages $Vth_{n,p}$ for the used SOI transistors were extracted under radiation and temperature. They show a significant increase of the absolute value of PMOS threshold voltage with radiation at high temperature, while for NMOS the threshold voltage value Vth_n decreases slightly at room temperature, keeps a relative stable value versus radiation dose at 100 °C and increases at higher temperature 200 °C, depending on the balance between N_{ox} and N_{it} build-up. The results fairly support the observed V_{REF} and power consumption dependences on temperature and total dose radiation.

Conflict of Interest

The authors declare no conflict of interest.

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