

Article

A Digitalized Silicon Microgyroscope Based on Embedded FPGA

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Received: 16 July 2012; in revised form: 28 August 2012 / Accepted: 9 September 2012 / Published: 27 September 2012

Abstract: This paper presents a novel digital miniaturization method for a prototype silicon micro-gyroscope (SMG) with the symmetrical and decoupled structure. The schematic blocks of the overall system consist of high precision analog front-end interface, high-speed 18-bit analog to digital convertor, a high-performance core Field Programmable Gate Array (FPGA) chip and other peripherals such as high-speed serial ports for transmitting data. In drive mode, the closed-loop drive circuit are implemented by automatic gain control (AGC) loop and software phase-locked loop (SPLL) based on the Coordinated Rotation Digital Computer (CORDIC) algorithm. Meanwhile, the sense demodulation module based on varying step least mean square demodulation (LMSD) are addressed in detail. All kinds of algorithms are simulated by Simulink and DSPbuilder tools, which is in good agreement with the theoretical design. The experimental results have fully demonstrated the stability and flexibility of the system.

Keywords: digital miniaturization; silicon microgyroscope (SMG); automatic gain control (AGC) loop; software phase-locked loop (SPLL); adaptive step least mean square demodulation (AS-LMSD)

1. Introduction

The silicon Micro-electromechanical Systems (MEMS) microgyroscope has been developed recently in the automotive industry as a kind of miniaturized angular rate sensor for several applications like rollover detection, inertial navigation, and the electronic stability programs. As is known, it has the merits of small volume, light weight, high reliability and low cost, thus it is easy to digitize and intellectualize and suitable for mass production.

Apart from the micro structure design and vacuum packaging, the readout electronics for this inertial sensors have usually been realized using analog circuit technology by either PCB or ASIC. Considering the investigation on the signal detection and control technology applied in the SMG has significant meaning since it is crucial to improve gyro's accuracy and back-end system integration. Most traditional SMG control and signal detection tasks are implemented only with analog circuits, which are easily susceptible to outer electromagnetic interference with poor device temperature characterization. On the other hand, some intelligent control and signal processing methods can be realized to enhance the stability and flexibility.

Compared with other embedded devices such as Micro-programmed Control Unit (MCU) and Digital Signal Processing (DSP), FPGA is a high performance device integrated with millions of digital logic elements, which can perform more complex numerical computing, logic decision and measuring-control functions even with low power consumption and fast parallel processing. Nowadays, It has been developed into a System on Chip (SoC) integrated device based on a FPGA/DSP hybrid system.

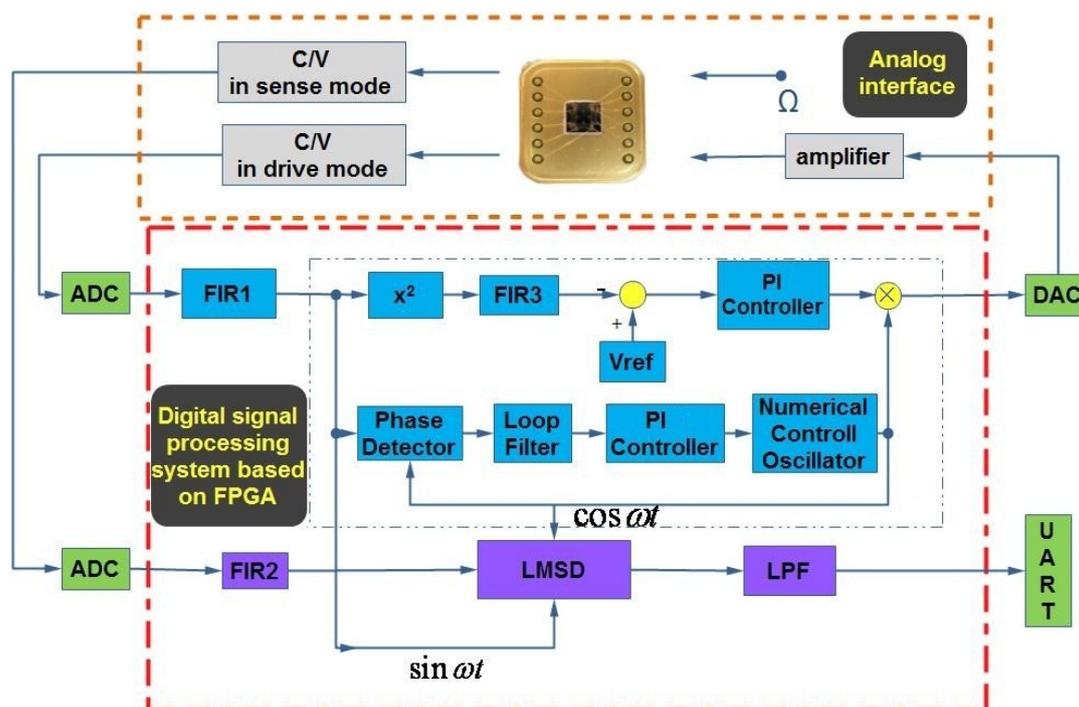
Some mature prototype microgyroscopes have been realized by analog circuit technology [1–3]. However, compared with other digital systems, they obviously lack enough flexibility and compatibility to satisfy different types of gyroscope structures and a variety of applications. Especially, the updated advanced algorithms by changing many circuit parameters cannot be easily performed in a relatively simple analog circuit. In order to further improve the overall system performance, many kinds of digital control circuits have been investigated to date. Though some novel digital systems based on DSP (digital signal processor) have been achieved [4,5], there are some great advantages in using FPGA instead, especially considering its faster parallel speed and lower power consumption, which will greatly better its whole performance eventually. Though a typical digital system based on FPGA was presented in [6], the conversion accuracy was only 12-bit that will inevitably cause much quantization noise and make the signal accuracy poor. In [7,8], a hardware platform for intelligent tuning, model identification and closed-loop operation was developed and tested over a generation two JPL/Boeing pyrex post resonator MEMS gyroscope. The real-time filtering and control of this device was successfully implemented through a digital design based on both a main digital ASIC and a monitoring-function FPGA chip. A software interface allows the user to configure, calibrate, and tune the bias voltages on the microgyroscope. Later on, a more advanced evolutionary computation algorithm for mode-matching tuning was further developed, and also another novel compact Disc Resonator Gyroscope was easily embedded in this compatible digital platform [9,10], which demonstrates the merits of adopting FPGA. Certainly, the JPL gyroscope based on FPGA and 24-bit sigma-delta A/D attained good performance, however, compared with a relatively high resonant frequency, the nearly 50 kHz sampling rate is so low that it may sometimes cause time

and phase delay effects. In [11,12], the double closed-loop and force-feedback digital control architectures are implemented with a certain noise and stability performance by using the sigma-delta modulation in both drive and sense modes. In [13,14], with the similar sigma-delta technology, the combination of ASIC and FPGA is implemented to achieve low noise and high Signal Noise Ratio (SNR) capability. Even though the performance is obviously updated by FPGA, for some special applications, we still need to achieve its miniaturization. Based on the previous investigations, here we will offer a digital system based on FPGA with 16-bit accuracy and high processing speeds of up to 300 kHz after miniaturization, which can assure both the system resolution and avoiding processing delays. Meanwhile, all the detailed components, including algorithm simulation and verification in FPGA, will be presented to show the characteristics of our digital system in this work.

2. Design of the Hybrid System

As can be seen in Figure 1, a hybrid detection and control circuitry commonly includes an analog interface circuit and a digital processing system based on FPGA in the drive and sense modes.

Figure 1. Design scheme of the digital system.



The gyroscope structure adopted here is that the drive mode and sense mode are completely symmetric because they are both varying-area style. First, the proof mass is electrostatically driven to single harmonic vibration in drive mode. Then, if the rotation occurs, another single harmonic vibration in sense mode will happen in the perpendicular direction. All the motions can be actuated and sensed through an interdigital combo structure. A detailed schematic has been introduced in our previous work [2]. The whole digital system consists of an analog part and a digital part. For the analog part, there are two capacitance to voltage (C/V) convertors for the output ports of the gyroscope in two modes. One is to detect the varying capacitance in drive mode and the other is specially designed for sense mode. The amplified adjustable feedback AC voltage and constant DC voltage is applied on the input

port for driving the proof mass of the gyroscope. For the digital part, there are two off-chip 18-bit A/D converters and one 16-bit D/A convertor together with their signal conditioning circuits, the Universal Asynchronous Receiver/Transmitter (UART) for transmitting the final demodulated signal, and a high performance core FPGA chip. In FPGA, the automatic gain control (AGC) loop and the software phase-locked loop (SPLL) are realized by an algorithm in drive mode. The automatic gain control (AGC) loop is comprised of an x^2 type amplitude detector, a low pass filter FIR3, a reference voltage V_{ref} to set the vibrating amplitude of the gyroscope and PI controller. The software phase-locked loop (SPLL) is comprised of phase detector, loop filter, a PI controller and numerical control oscillator (NCO). Meanwhile, the varying step least mean square demodulation (LMSD) is implemented by algorithm in sense mode. The detailed operation mechanism will be discussed in the following sections.

As for the key analog interface, there have been a lot of papers discussing it extensively. By experimental comparison, the front end with the ring diode detection is adopted to improve the SNR ratio. The minor signal can be picked up by demodulating the Coriolis effect induced aF magnitude of change in the vibrating capacitance using a high frequency carrier up to 10 MHz and precision integrated ring diode HSM2829 (HP company). Almost all the discrete devices like capacitances and resistances with fine temperature coefficients are adopted by the industrial standard.

Different from the full analog circuit design, apart from the necessary front-end, almost other parts are realized in FPGA. Actually, the analog front-end are similarly adopted in drive and sense modes, and the subsequent digital parts include AGC, SPLL and LMSD are all realized using specific Verilog language in FPGA. Here all the 128 order filter FIR and LPF filters are selected from the Megacore IP library embedded in the software development tools. Besides, to save limited hardware resources, 16-bit fixed-point numbers and algorithms are implemented without decreasing the system precision.

2.1. AGC Loop in Drive Mode

In the traditional analog electrostatically actuated microgyroscope, the 90 degrees phase difference between driving force and vibrating displacement cannot be ensured in the case of the temperature variation. Therefore, there always exists a certain drift for the natural frequency of microgyroscope even though the self-oscillation is working. To solve this problem, in FPGA a closed-loop self-oscillating driving scheme is utilized. Most discrete device parameters are represented as the numerical values stored in FPGA that can be made immune to outer interferences including temperature drift.

Essentially, the microgyroscope should be a linear sensor only responsive to the input angular rate around the input axis. Hence, the driving status must be stable in both amplitude and frequency. To satisfy these two requirements, closed-loop control must be achieved in the actuation of the microgyroscope. One is that the phase angle of the whole closed-loop $\theta = 2n\pi$; the other is that the gain of the whole loop $A > 1$ at first. The closed-loop actuation of a microgyroscope commonly adopts AGC, which can implement the closed-loop driving with a nonlinear dynamics characteristic, gradually reducing the closed-loop gain of the entire closed-loop to 1 within 100 ms.

The principle of the digital AGC module is shown in Figure 2. One 10 MHz carrier signal is directly applied on the proof mass and the ring diode demodulation method is adopted. Here the AGC loop consists of an amplitude extractor and PI controller. In the amplitude extractor, followed by an

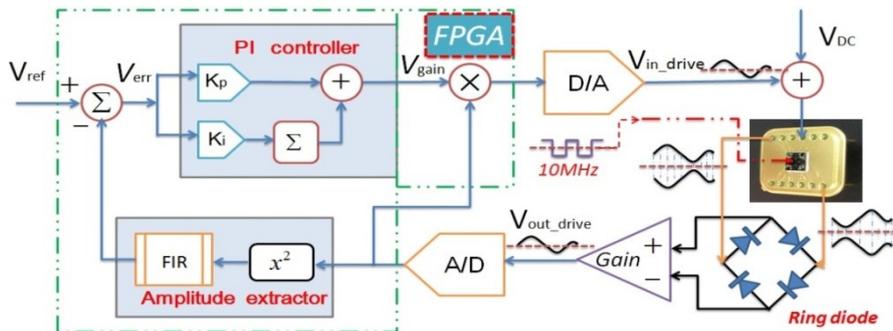
A/D convertor, the filtered drive detection signal V_{out_drive} will be multiplied by itself through an x^2 type amplitude detector to get square term and the DC term. Through another high-order low pass FIR its effective amplitude will then be derived. The error between the actual signal amplitude and expected reference amplitude V_{ref} will be calculated. In the PI controller, the error value V_{err} will be sent to two branches. One is to calculate the proportional term by multiplying K_p (proportional coefficient) and the other is to calculate the integral term by multiplying K_i (integral coefficient) and accumulating the previous results. Next, the key variable gain will be generated using superposition of the proportional term and the integral term. Last, prior to a D/A convertor, the changing drive detection signal V_{out_drive} will be real-time multiplied by the variable gain V_{gain} to get an adjustable driving signal V_{in_drive} to push the proof mass of the gyroscope steadily. Once the proportional coefficient and integral coefficient are set properly, the P part will realize the fast tracking and the I part will attain an unbiased effect. Finally, the input signal will always keep constant, *i.e.*, the vibrating amplitude of the gyroscope is forced to be stable even in harsh environment. The PI controller after digitalization can be correspondingly expressed as

$$u(k) = K_p \left[e(k) + \frac{T_o}{T_i} \sum_{i=0}^k e(i) \right] \quad (1)$$

$$D(z) = \frac{U(z)}{E(z)} = K_p + K_i \frac{1}{1-z^{-1}} \quad (2)$$

where $e(k)$ is the error value at k step, K_p and K_i are proportional and integral coefficients respectively. $U(z)$ and $E(z)$ are functions of controller output and error input in z domain. T_o and T_i are sampling and integral time constant respectively.

Figure 2. Schematic diagram of digital AGC module.

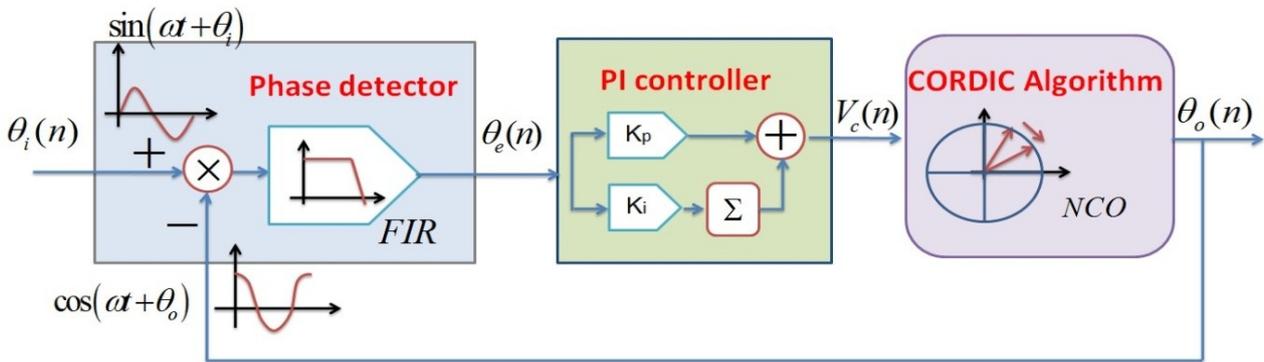


2.2. SPLL Module Based on CORDIC Algorithm

In drive mode, the driving signal and the displacement detection signal in drive mode are always perpendicular, even though the resonant frequency has a certain drift over temperature. Almost most analog or digital gyroscope circuit systems adopt the PLL technique to sustain the phase difference stability and resonant frequency tracking [15]. In order to realize such self-oscillating in drive mode, software phase-locked loop (SPLL) can achieve this function via software, which makes an output signal track the input signal by the phase difference of 90° . This special algorithm aims to synchronize the output signal with its input signal in frequency as well as in phase. As shown in Figure 3, this adopted SPLL consists of phase detector (PD), loop filter (LF) and numerical controlled oscillator (NCO), which is totally a closed-loop. First, PD is a phase comparator to catch the equivalent phase

difference between the output feedback signal $\theta_o(n)$ and the input signal $\theta_i(n)$ by multiplication, and then it is filtered by FIR to appropriately generate an error signal $\theta_e(n)$ for the PI controller input. In the PI controller, $\theta_e(n)$ is both amplified by the coefficient K_p and integrated after being multiplied by the coefficient K_i , which is followed by summation. Especially, adjusting here the loop parameter can improve the overall system performance. The output signal $V_c(n)$ of PI controller is used to control the frequency and phase of NCO. In fact, NCO is actually a numeric-frequency converter and its output frequency $\omega(n)$ varies with the digital value of control voltage $V_c(n)$. In this design, a CORDIC algorithm-based NCO module is adopted, which will simultaneously compute the trigonometric functions such as sine and cosine. Additionally, compared with the traditional look-up table method, this method can save a load of resources and greatly lower the power dissipation in FPGA.

Figure 3. Schematic of the SPLL module.



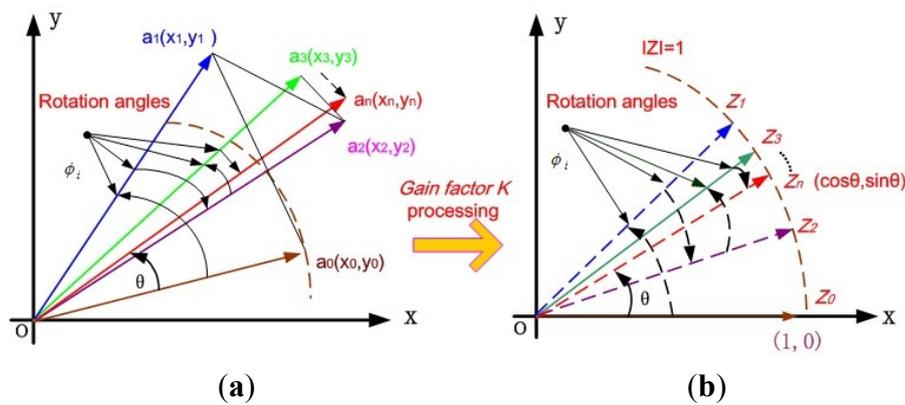
Normally in SPLL module, the NCO can be realized by DDS generator [16]. However, it will consume a lot of hardware resources in FPGA due to its non-flexible look-up table method. The Coordinate Rotate Digital Computer (CORDIC) algorithm was first proposed by Volder and Walther in 1959 and has been implemented in fiber optic gyroscopes to lock the laser resonant frequency [17]. Based on the coordinate transformation of the minor angle rotation, the basic idea is to realize the computation of the trigonometric function. Through this algorithm, the final result can be timely calculated after n iterations even over a period of several clocks using addition, subtraction and shift operations, combined with the advanced pipeline technology in FPGA. In Figure 4(a), if an unit vector $\mathbf{a}_0(x_0, y_0)$ in rectangular coordinate system is rotated to the desired vector $\mathbf{a}_n(x_n, y_n)$ through n times successive regular rotation operations. After n iterations, $\sin\theta$ and $\cos\theta$ can be obtained, where θ is the final total rotation angle. In the case of one time iteration, this vector transformation can be written as:

$$\begin{cases} x_{i+1} = \cos(\phi_i)[x_i - y_i \tan(\phi_i)] \\ y_{i+1} = \cos(\phi_i)[y_i + x_i \tan(\phi_i)] \end{cases} \quad (3)$$

where ϕ_i is the one-step rotation angle. If we divide a desired rotation θ into many steps angles ϕ_i ($i=0,1,2,\dots,n$), i.e., let the limited $\tan(\phi_i) = \pm 2^{-i}$, the rotation-induced production terms $\tan(\phi_i)$ can be simplified to the convenient digital shift operation in FPGA. Here each step rotation direction can be marked by d_i , then the final rotated angle can be described as

$$\theta = \sum_{i=0}^{n-1} d_i \phi_i, \quad d_i \in \{-1, 1\} \quad (4)$$

Figure 4. Sketch of the CORDIC algorithm. (a) Rotation mode without K processing. (b) Rotation mode with K processing.



Considering each step rotation angle is a primitive set value, *i.e.*, $\cos(\phi_i)$ must be a constant. Thus, each step iteration calculation for any rotation angle θ can be expressed as

$$\begin{cases} x_{i+1} = K_i[x_i - y_i \cdot d_i \cdot 2^{-i}] \\ y_{i+1} = K_i[y_i + x_i \cdot d_i \cdot 2^{-i}] \end{cases} \quad d_i = \pm 1 \quad (5)$$

where each step gain factor K_i and general gain factor K are given by

$$\begin{cases} K_i = \cos(\arctan(2^{-i})) = 1 / \sqrt{1 + 2^{-2i}} \\ K = \prod_{i=0}^n K_i \end{cases} \quad (6)$$

In order to realize the shift-add operation, the general gain factor constant K can first be extracted from the iteration equations alone, and finally processed as the system uniform gain after all the iterations. Theoretically, when i approximates to infinite, K will almost equal 0.6037, and conversely the whole system gain approximately equals 1.647. Obviously, the real value of A_n can be calculated by:

$$A_n = \prod_n \sqrt{1 + 2^{-2i}} \quad (7)$$

Another auxiliary variable z_i can be used to primitively determine the accumulated angle value and the next step rotation direction by the sign:

$$z_{i+1} = z_i - d_i \cdot \arctan(2^{-i}) \quad (8)$$

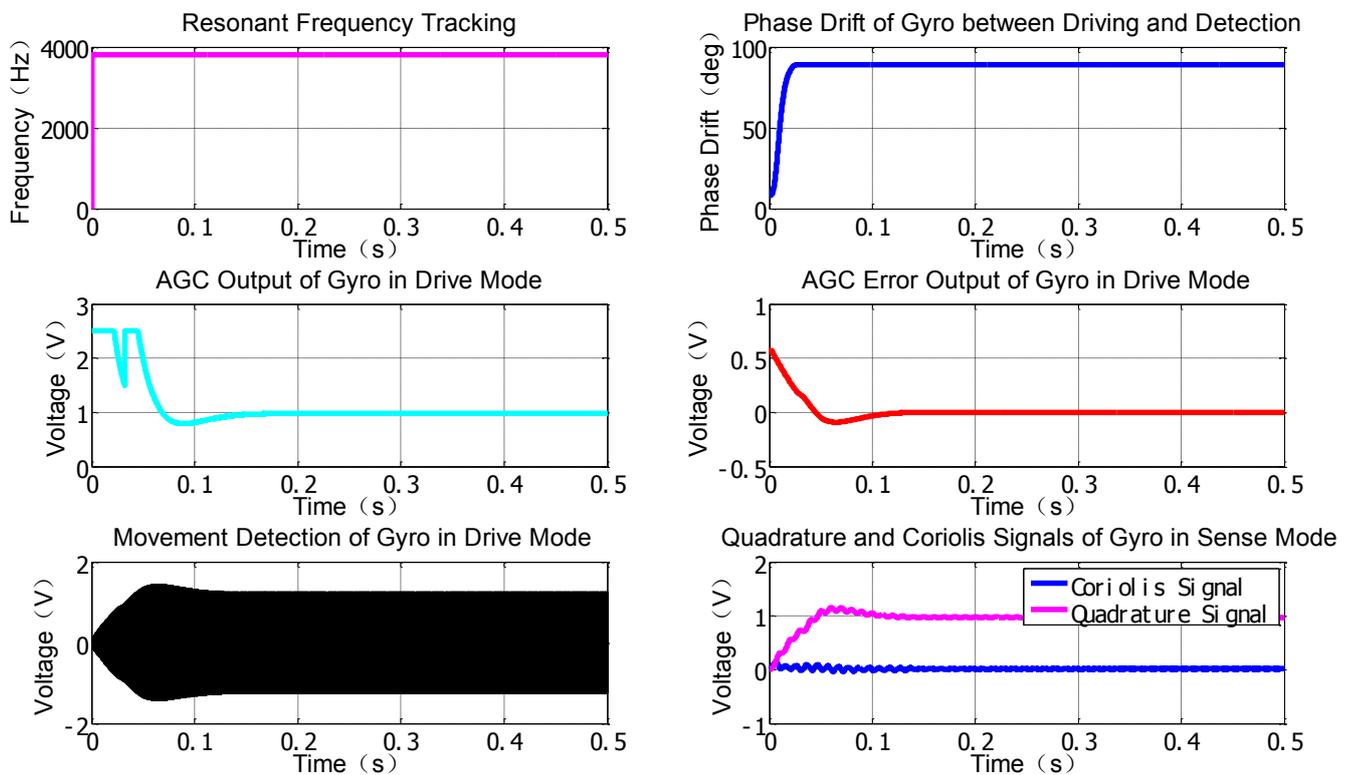
In the rotation mode, the final angle accumulator value z_n is just the expected rotation angle θ . During the whole iteration process, the rotation direction will be used to decrease the remaining angle value in the angle accumulator. Thus, the final z_n is will infinitely approach to the expected angle value θ . By the CORDIC algorithm in rotation mode, the difference function can be simply generalized from Equations (5) and (8) as

$$\begin{cases} x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} = z_i - d_i \cdot \arctan(2^{-i}) \end{cases} \quad (9)$$

where

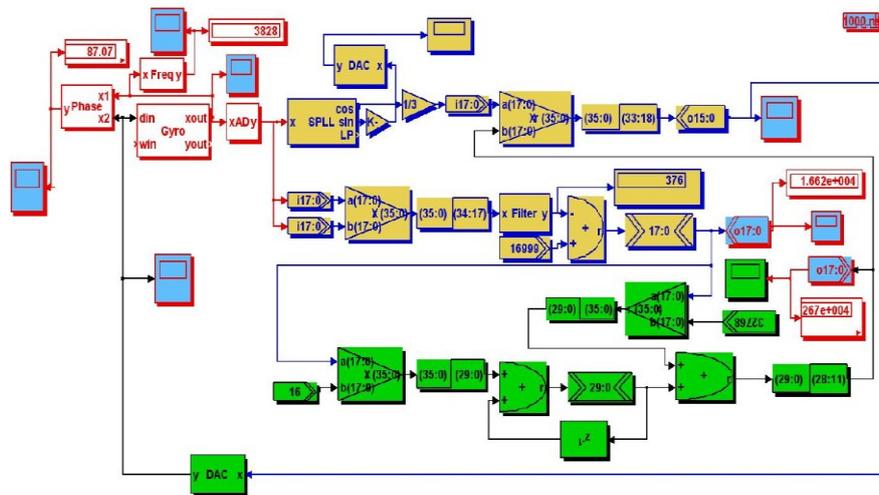
Other important modules like AGC will be implemented using the discrete multiplier, digital filter and PI modules. Besides, some instruments in gray and specific variables in blue for monitoring the real-time key signal nodes are employed to record some useful curves as shown in Figure 6. From the simulation results in drive mode, the resonant frequency is tracked fast and the phase drift is avoided when the SPLL starts to work. Only after less than 100 ms, the stable AGC control output can perform well and the AGC error rapidly converges to zero. The envelope curves of the resonant movement detection clearly prove that the AGC and SPLL are completely effective. Moreover, the demodulation results of the LSMD are in good agreement with the preset Coriolis and quadrature signals.

Figure 6. Matlab simulation results.

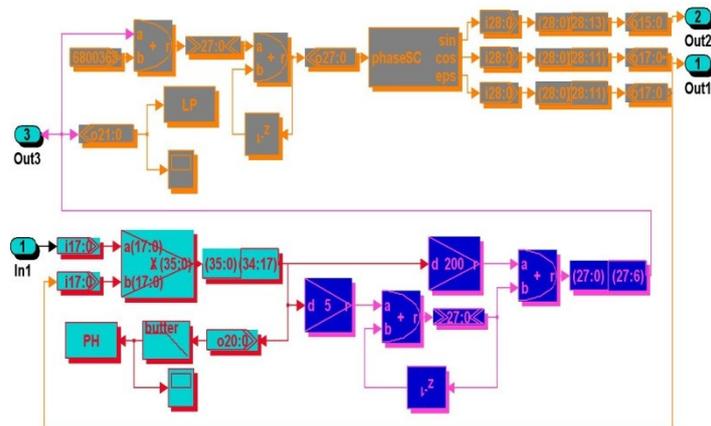


Similarly, the corresponding simulation blocks created by DSPbuilder tools can be seen in Figure 7, and the simulation results with certain fixed point algorithm in digital domain are given in Figure 8, which are also in good accordance with the former simulation in the analog domain by Matlab. Actually, these two simulation methods are essentially different, the former one is based on the continuous signal expressed by floating numbers for some key nodes' parameters in block diagram, and the latter one is based on the discrete numerical signals expressed by fixed numbers in complement form. It is clearly shown in Figure 7(a,b) that all the effective numerical values in drive mode are expressed in 16-bit binary complement formats, and a lot of binary numbers can be reasonably truncated according to the corresponding precision requirement.

Figure 7. DSPbuilder simulation block diagram based on FPGA. (a) The whole system in drive mode. (b) Expanded SPLL internal elements.

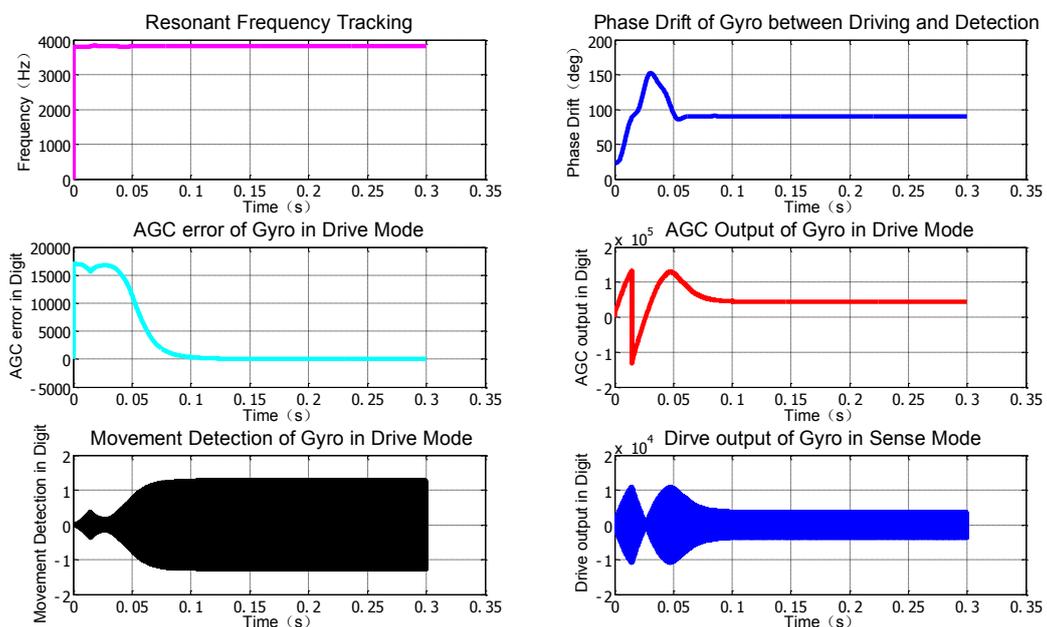


(a)



(b)

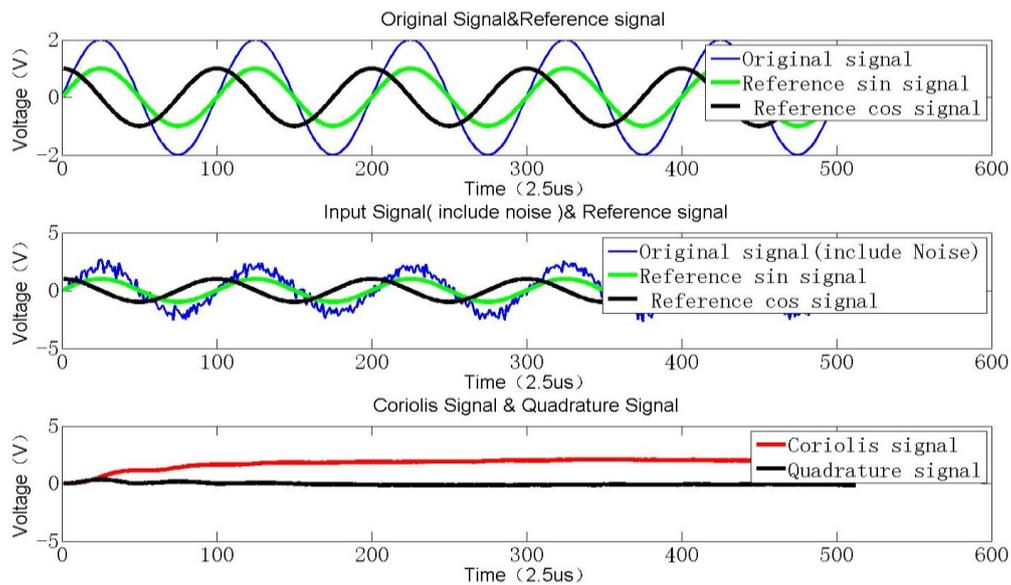
Figure 8. DSPbuilder simulation results with fixed point algorithm.



2.3. Adaptive Varying Step LMSD Algorithm

Due to fabrication error induced by the stiffness coupling term between the drive and sense modes, apart from the inevitable noise $n(k)$, the output signal $S(k)$ of the SMG essentially can be decomposed into two perpendicular parts. One is Coriolis signal $S_{cori}(k)$ which represents the input rotation angular rate around the input axis, and the other is the quadrature signal $S_{qua}(k)$ which denotes the initial structure-induced error. These two signals are both orthogonal to each other in theory. For an angular rate sensor, the Coriolis signal is utilized to detect the angular rate by synchronous demodulation. However there always exists a slightly vicious double-frequency signal produced by the multiplication operation. Besides, the following high-order LP filter is required especially if the resonant frequency of SMG is rather low, which not only causes a problem of calculation divergence but also consumes more hardware resources. A special demodulation technique using sigma-delta convertor is simulated to evaluate the system performance [18]. Here, to save the limited resources and attain an excellent demodulation effect, a better approach varying step LMSD can be realized to minimize the mean square error between the input signal and the output signal [19]. As shown in Figure 9, a Coriolis signal, *i.e.*, a sinusoidal function, added with an equivalent quadrature signal and some certain noise is simulated as a hybrid input signal. After the adaptive varying step LMSD processing, an expected value of the input signal amplitude can be derived. By comparing this expected signal amplitude $d(k)$ with the generated input signal $W^T \cdot r(k)$, an estimation error $e(k)$ can be recorded. Through continuously minimizing the variance error, an optimum vector W will be derived in the end.

Figure 9. Schematic simulation of LMSD algorithm.



$$\min \{E[d(k) - W^T \cdot r(k)]\} \quad (14)$$

$$S(k) = S_{cori}(k) + S_{qua}(k) + n(k) \quad (15)$$

$$r(k) = [r_1(k), r_2(k)] \quad (16)$$

$$e(k) = d(k) - W^T \cdot r(k) \quad (17)$$

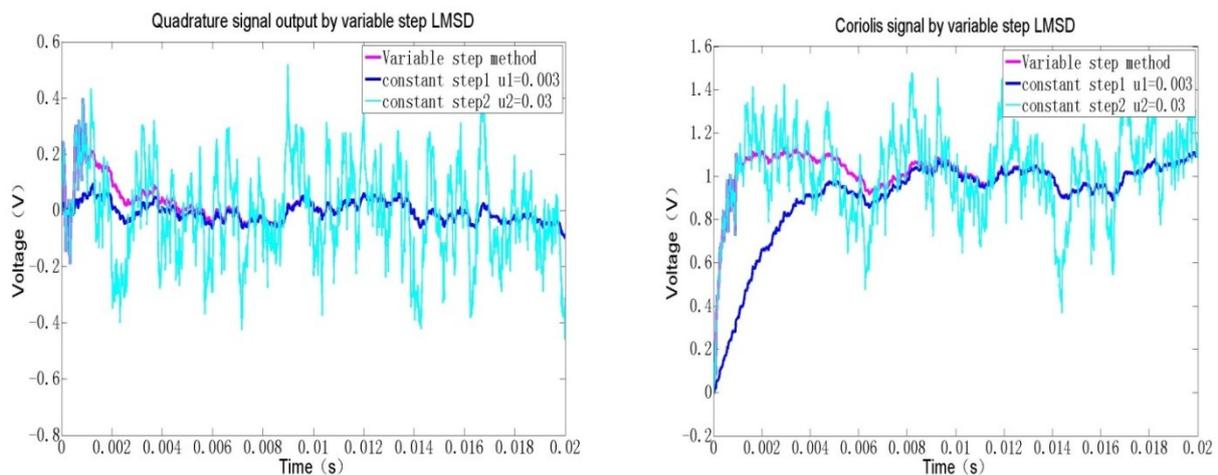
$$\mathbf{W}(k) = \mathbf{W}(k-1) + 2u \cdot e(k) \cdot \mathbf{r}(k) \quad (18)$$

$$A_{cori}(k) = W_1(k), A_{qua}(k) = W_2(k) \quad (19)$$

In Equations (14–19), the varying step LMSD algorithm flow is shown in detail. In Equation (16), $\mathbf{r}(k)$ is actually the reference signal vector with $\sin(k)$ and $\cos(k)$ components. In Equation (17), the evaluated \mathbf{W}^T will converge to a stable vector to make the difference $e(k)$ between the actual angular rate and the evaluated value $\mathbf{W}^T \cdot \mathbf{r}(k)$ as small as possible. $S(k)$ denotes the hybrid signals of the coriolis and quadrature signals including the white noise. From Equations (16) to (19), the 4-step iteration will be operated to track the effective amplitudes $A_{cori}(k)$ and $A_{qua}(k)$ of two signals. Especially, u is the step length here first set 0.003 and then 0.03 after the error attains a certain range, which can improve the convergence rate.

As can be seen from Figure 9, the two direct current terms, which reflect both the Coriolis and quadrature components, can be obtained through a concise iteration algorithm. Obviously, the demodulation results can be rapidly converged to two constant values after 200 loops. The sample rate is high up to 300 kHz, so the interval time is about 33 μ s. In actual system, a high-resolution 18-bit A/D converter is selected, therefore, the quantification error in the full range of ± 2.5 V is about 0.019 mV, which exceeds far beyond the equivalent angular rate noise. In the FPGA realization, some digital 18-bit multipliers are used to ensure the computation resolution after C/V conversion. Especially the fixed point processing method is adopted to save the limited resources and lower the power consumption. In Figure 10, the Coriolis signal and quadrature signal are calculated by basic LMSD and varying step LMSD methods.

Figure 10. Varying step LMSD effects.

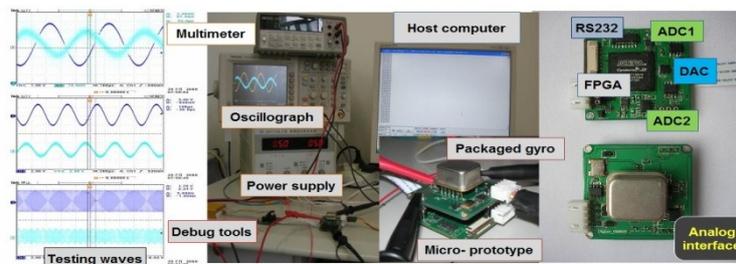


When the step length u is only set to 0.03, the approaching time is short and the divergence magnitude is poor, which demonstrates a strong noise. Whereas if the step length u is only changed to 0.003, the approaching time is longer, but the convergence error becomes smaller than the former. Thus, if we first set u equal 0.03 to improve the approaching rate. After the output signal error approaches a certain range, then we adjust u equal 0.003 to make the divergence error as small as possible. By this intelligent varying step method, we can realize both high-speed and low-noise LMSD method.

3. Experimental Results

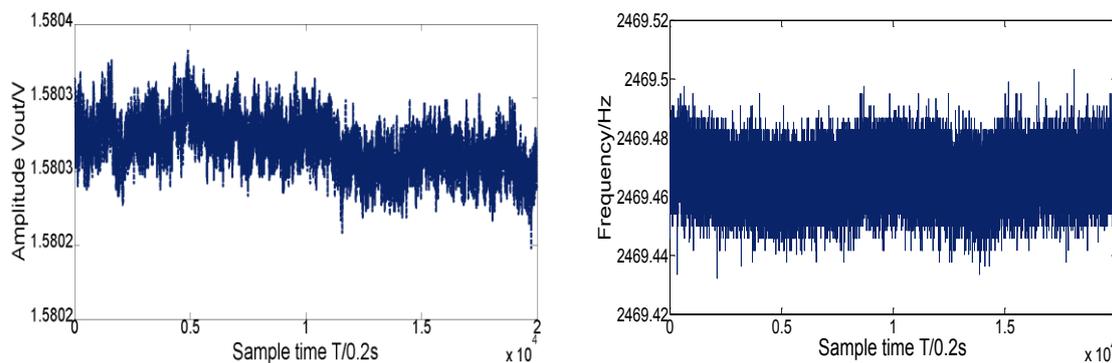
As can be seen from Figure 11, the digitalized silicon microgyroscope based on an embedded FPGA is implemented with two four-layer circuit boards of 4 cm × 4 cm size. One board is designed for a precision analog interface with demodulated gyroscope signals and the other is for the data converters and FPGA processing. In the specific electronics, two 18-bit resolution ADCs AD7690 (Analog Device) are used to ensure little quantization noises for drive and sense modes. Meanwhile, a 16-bit resolution DAC DAC8832 (Texas Instruments Company) is adopted to ensure the faster sampling rate up to 300 kHz. A high performance FPGA chip EP3C16 (Altera Company) is preferred to satisfy the requirements of the small BGA (Ball Grid Array) package and low power consumption. To facilitate debugging, a special switched JTAG or AS port with 10 pins is attached at the edge of the digital board. Last, the demodulated angular rate signal can be transmitted to the host computer through UART. These components are all low power with high performance.

Figure 11. Experimental setup for drive and sense modes.



Nearly one hour of detection results of vibrating frequency and amplitude in drive mode are shown in Figure 12. The mean value of the vibrating frequency in drive mode is near 2,469.47 Hz, and its variance is below 0.01 Hz.

Figure 12. Results of amplitude and frequency outputs in drive mode.



Similarly, the mean detection voltage value of vibrating amplitude in drive mode is near 1.5803 V, and its variance is 1.45×10^{-5} V, thus the stability of both vibrating frequency and amplitude in drive mode have achieved a high precision (the relative error is lower than 1×10^{-5}). The testing results demonstrate the stability in drive mode and the high precision detection ability of minor signal in sense mode. With the scale factor of 8.775 mV/°/s in full measurement range of ± 300 °/s, the nonlinearity is less than 400 ppm and ZRO (Zero Rate output) is very stable at room temperature. Through the overall

temperature range from $-40\text{ }^{\circ}\text{C}$ to $60\text{ }^{\circ}\text{C}$, the maximum scale factor deviates by about 10 percent from the room temperature value, which to some extent verifies the temperature stability in harsh environment. All the experimental results can be seen from Figures 12–14.

Figure 13. ZRO and scale factor of the microgyroscope at room temperature.

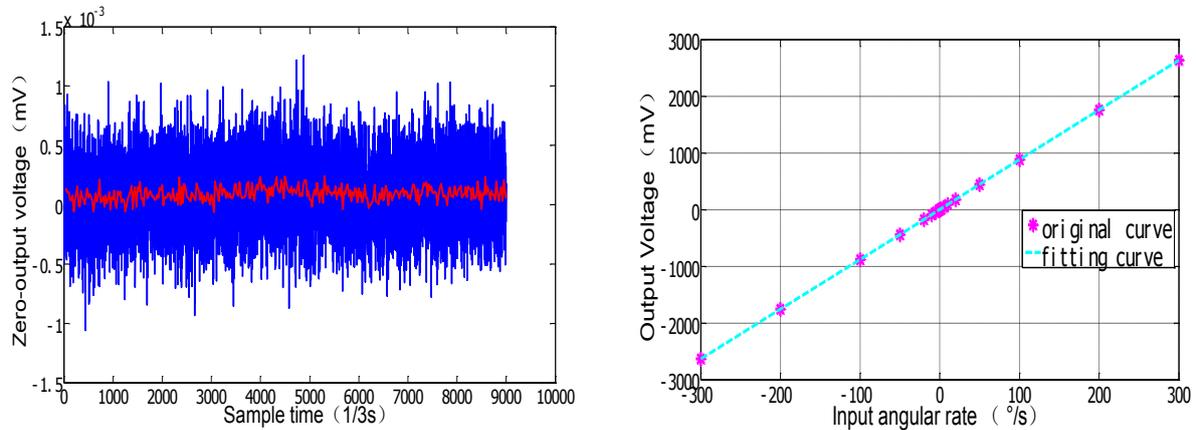
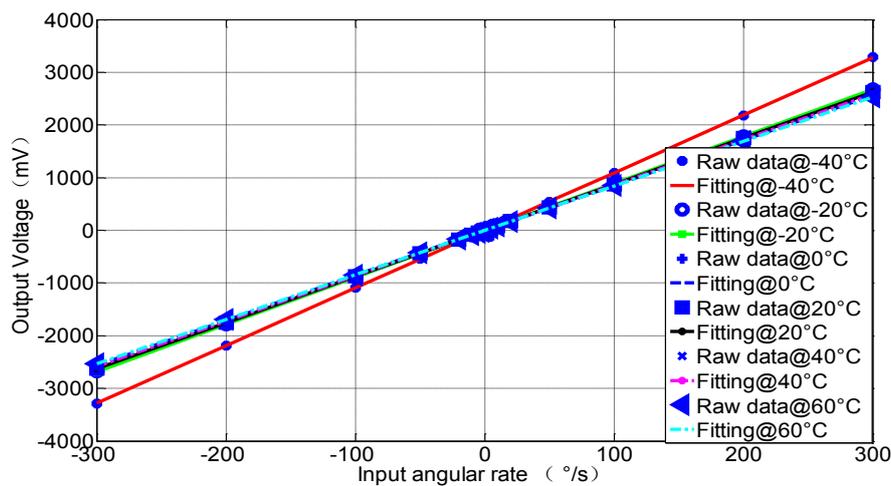


Figure 14. Scale factor of the SMG over temperature.

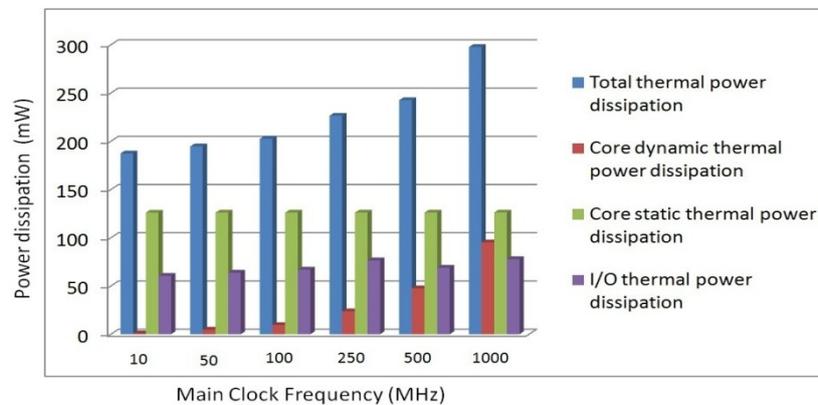


In Table 1, some key specifications in the experimental results can be compared with that of the previous analog design, where bias stability and linearity are obviously improved in room temperature, noise and the minimum measurable angular rate are decreased by digital filter function, bias stability in full temperature range is improved. According to signal processing theory, the higher the sampling rate is, the better the recovered original signal is. Besides, after we adopt the 300 kHz sampling rate, the phase delay of digitalized signals in each digital modules will be so small that the processing speed can catch up the fast response of the resonant frequency, amplitude and phase of the gyroscope's resonance and the responding Coriolis effect. Thus the gyroscope will work in a fine state and the key specifications shown in Table 1 will naturally be better. If we continue to increase the sampling rate, the specifications will not be improved much, but make the core dynamic thermal power dissipation as high as possible. Regarding these facts, we should select a proper sampling rate as a trade-off.

Table 1. Performance index comparison of analog with digital microgyro prototype.

Technical Data		Value (Analog)	Value (Digital)
Performance (+25 °C)	Scale factor	9.6 mV/°/s	8.775 mV/°/s
	Bias stability	15 °/h	12.45 °/h
	Noise	0.024 °/s/√Hz	0.01 °/s/√Hz
	Dynamic range	±300 °/s	±300 °/s
	The minimum measurable angular rate	0.02 °/s	0.01 °/s
	Linearity	≤400 ppm	≤200 ppm
Power Supply	Supply voltage	±5 V	±5 V
	Current dissipation	≤20 mA	≤30 mA
Environment (−40 °C~+60 °C)	Bias stability	3 °/s	1 °/s
	Temperature drift	<0.03 °/s/°C	<0.01 °/s/°C

Though the FPGA chip has introduced some more current dissipation than that of the analog design, we still think that it is a good method to realize miniaturization. Along with the analog-digital mixed integrated circuit techniques update, the overall power consumption will be greatly decreased using the new developing low power FPGA chip substitute of 28 nm technology with the compatible package. In Figure 15, the total thermal power dissipation including core dynamic thermal power dissipation, core static thermal power dissipation and I/O dissipation over main clock frequency is illustrated.

Figure 15. Power dissipation analysis over main clock frequency.

When the main clock frequency of more than 100 MHz is adopted, the core dynamic dissipation is increased dramatically, while other thermal power dissipations will not be changed too much. Thus, in order to make the core dynamic thermal power dissipation smaller, only 50 MHz main frequency is adopted in our system. For a lot of clock signals and 300 KHz sampling rate in the digital system, actually it is easy to deploy them by dividing the main frequency.

4. Conclusions

The performance of the microgyroscope is greatly decided by the measure and control electronics. From many previous researches, there is a general tendency to select digital technology to replace the traditional analog circuit. Considering the faster parallel speed and low power consumption, a digital microgyroscope based on an embedded FPGA is developed. Different from other FPGA system, the

fast sampling rate AD converter with enough 18-bit precision is utilized, and advanced algorithms include SPLL and LSMD are successfully simulated and implemented by hardware programming.

In drive mode, the AGC and SPLL modules work in parallel to ensure the real-time self-exciting and phase locking. The AGC module can make the oscillating amplitude of the proof mass stable in a set constant value. Meanwhile, the SPLL module can track the natural frequency over temperature drift by keeping the 90 degree phase difference between the input driving signal and displacement detection signal. Both the Matlab and DSPbuilder simulations based on FPGA are implemented to validate the algorithm function by adjusting the key parameters, which could provide a reference for the following hardware debugging. In sense mode, to avoid the traditional multiplication method, a varying step LMSD is adopted to realize faster and accurate demodulation. All used algorithms are programmed by fixed point numerical computing, which could save a lot of hardware resources of FPGA and greatly lower the power consumption.

A vacuum packaged microgyroscope is inserted in two pieces of printed circuit boards. The final testing results show that the digital microgyroscope based on embedded FPGA has good performance. Especially, this prototype can be further developed to form a Micro Inertial Measure Unit (MIMU) system by only adding another front-end for another sensing structure without changing the digital parts. Besides, the most previous analog devices are replaced by a digital algorithm, thus our FPGA-based digital gyroscope can have better temperature performance in many harsh applications.

Acknowledgements

The authors gratefully acknowledge the financial supports from Chinese National Science Foundation (Contract No. 61001048), Key Laboratory of Micro-Inertial Instrument and Advanced Navigation Technology, Ministry of Education, China (Project No. KL201102), Major Project Guidance Foundation of Basic Scientific Research Operation Expenses, Southeast University (No. 3222002107), and Natural Science Fund project in Jiangsu Province (BK2012739).

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