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Constant-Voltage and Constant-Current Controls of the Inductive Power Transfer System for Electric Vehicles Based on Full-Bridge Synchronous Rectification

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Abstract: When an inductive power transfer (IPT) system conducts wireless charging for electric cars, the coupling coefficient between the coils is easily affected by fluctuations in the external environment. With frequent changes in the battery load impedance, it is difficult for the IPT system to achieve constant-voltage and constant-current (CVCC) controls. A CVCC control method is proposed for the IPT system that has a double-sided LCC compensation structure based on full-bridge synchronous rectification. The proposed method achieved good dynamic stability and was able to effectively switch between the output current and voltage of the system by adjusting only the duty cycle of the switch on the secondary side of the rectification bridge. As a result, the system efficiency was improved. The output characteristics of the double-sided LCC compensation structure was derived and the conduction condition with zero voltage was analyzed by using four switches through two conduction time series of the rectifier circuit. Then, the output voltage of the synchronized rectifier was derived. The hardware implementation of the full-bridge controllable rectifier was described in detail. Finally, a MATLAB/Simulink 2018a simulation model was developed and applied to an 11 kW prototype to analyze and validate the design. The results showed that the designed system had good CVCC output characteristics and could maintain constant output under certain coupling offsets. Compared with semi synchronous rectification methods, the proposed method had a higher efficiency, which was 95.6% at the rated load.

Keywords: constant voltage; constant current; double-sided LCC; inductive power transfer; synchronous rectification; zero voltage switch

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1. Introduction

In recent years, with the development of the economy and advancements in technology, electricity has been fully developed and utilized as a high-quality energy source. However, optimizing the method of electricity conversion and improving its efficiency remain pressing issues [1,2]. Inductive power transfer (IPT) technology has been widely employed in electrical energy transmission without the need for electrical hardware connections at both the power supply and receiving sides. It is known for its flexibility, convenience, safety, and reliability, leading to its rapid development in recent years [3–5]. The utilization of IPT technology in electric vehicles facilitates intelligent and convenient charging. With the increasing popularity of plug-in hybrid and electric vehicles, IPT charging solutions have garnered renewed interest [6,7].

When employing the IPT system for charging electric vehicle batteries, it is crucial to consider the charging characteristics. Various charging methods for lithium batteries exist, including constant-current (CC) charging, constant-voltage (CV) charging, and

phased constant-voltage constant-current (CVCC) charging [8,9]. Phased CVCC charging is commonly utilized, as depicted in Figure 1.

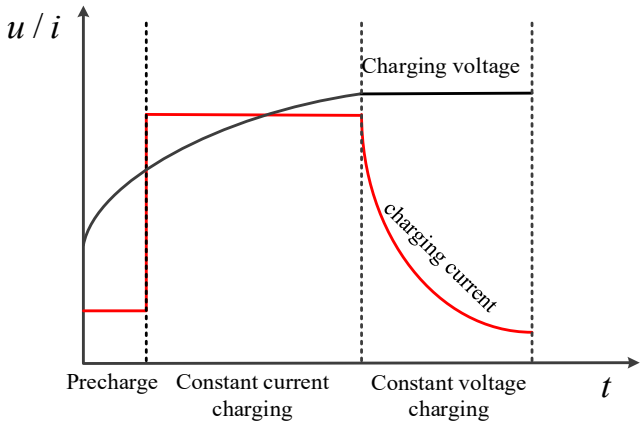


Figure 1. Charging curve of the lithium battery.

To realize CC and CV operations of an IPT system, researchers have proposed many methods, mainly including two categories: (1) By designing the parameters of the compensation network, the CC and CV outputs can be realized separately. (2) To realize CC or CV outputs, they can be realized through DC/DC converter, phase shift control and variable frequency control.

In their examination of compensation network parameters, Lu et al. introduce a comprehensive methodology applicable to diverse higher-order resonant circuits [10]. This approach presents an equivalent circuit and a general resonance technique tailored specifically for higher-order resonant circuits, aiming to achieve CC and CV outputs across varying load conditions while preserving zero-phase angle (ZPA) frequencies. Additionally, Ref. [11] outlines a generalized modeling strategy for arbitrary higher-order resonant networks, facilitating the derivation of voltage and current transfer characteristics unaffected by load variations. Such circuits can be conceptualized as combinations of series-connected LC networks, multi-level T circuits, and multi-level Π circuits.

To complete the entire charging process, transitioning from the CC output to the CV output is essential. Once the topological structure is determined, the output characteristics (either CC or CV) are also established. Thus, a method has been proposed to facilitate the switch from CC to CV using a switching topology [12,13]. Previous studies utilized a double-sided LCC (DLCC) compensation structure for the CC charging stage, while the CV charging stage employed a switch to an LCC-S compensation structure. In [14], the transition from CC to CV was accomplished through frequency modulation. This transition occurred at varying operating frequencies by optimizing the parameters of the DLCC compensation structure. Control elements do not have to be added to these methods. Although they are simple and reliable, they cannot handle situations that demand variable output.

However, the relative positions of the coupling coils are not fixed in practical applications, leading to potential changes in the coupling coefficient of the IPT system. For instance, achieving precise alignment of coupling coils during the charging of electric vehicles is challenging, resulting in output fluctuations. In dynamic wireless transmission scenarios like charging unmanned aerial vehicles [15], electric vehicles [16,17], and underwater equipment [18,19], the relative positions of coupling coils continuously change, leading to system output instability. In such applications, stable CV output cannot be attained through switching topology or operating frequency alone. Therefore, specialized control algorithms are necessary to ensure stable output.

The current methods of controlling system power output encompass transmitter-end regulation, receiver-end regulation, and coordinated regulation between the transmitter

and receiver ends. In transmitter-end regulation, the methods to adjust the input voltage mainly include altering the operating frequency of the inverter [20], adopting phase shift controls for the inverter [21,22], and adding DC/DC elements [23] before the inverter. The transmitter-end regulation often needs communication elements to realize the feedback between the load side and the transmitter side, which increases the complexity of the control and communication circuit. Similarly, the coordinated regulation between the transmitter end and the receiver end also has this same problem [24].

In receiving-end regulation, the methods can directly adjust the output power on the receiving side and avoid communication elements, thus reducing the complexity of the control and communication circuit. Boys et al. [25] have proposed a scheme of cascading a Boost circuit at the back end of the rectifier to improve the series–parallel (SP) compensation structure. To prevent excessive short-circuiting current after switch closing, a large inductor L_{dc} was added in series, thus reducing the power density of the receiving side. Zhang et al. [26] have also proposed a variable inductance control method based on an additional secondary-side boost circuit, achieving CV/CC switching for IPT systems. On the basis of these results, Ref. [27] have proposed a scheme of using a parallel switch in the series–series (SS) and DLCC compensation structures. Since both SS and DLCC compensation structures exhibit CC output characteristics, no additional inductance is required, thereby increasing power density on the receiving side. Ref. [28] proposed a parallel switch in front of the rectifier; however, two switches were needed to function simultaneously. To further minimize device usage and enhance power density on the receiving side, Boys et al. proposed a topological structure for a semi synchronous rectifier [29]. They successfully regulated the output voltage by replacing the two diodes at the lower end of the rectifier bridge with controllable switching devices. Their method did not require additional devices and was able to significantly increase the power density on the receiving side with a higher efficiency than adding one level of DC/DC elements. However, the other two diodes at the higher end of the rectifier bridge still could not achieve soft switching, which will reduce the efficiency of the switches.

To address the myriad issues existing in current technology and achieve seamless switching between CV and CC states in IPT systems while maintaining constant output power, this paper proposes a CVCC control method based on full-bridge synchronous rectification. The main contributions can be summarized as follows:

(1) Compared to the SS topology, the DLCC topology incorporates LC links, enhancing parameter design flexibility and potential output power. The proposed method facilitates the transition from CC to CV output while stabilizing the output voltage. By substituting four diodes of the rectifier bridge with MOSFETs, the circuit adopts a symmetrical topology, enabling bidirectional energy flow with proper control.

(2) In the method presented herein, switch conduction time is regulated to effectuate the transition from CC to CV output. Additionally, a synchronous signal sampling circuit is introduced to achieve Zero-Voltage Switching (ZVS) conditions in the rectifier bridge, thereby controlling switch conduction sequence. Building upon the conduction time sequence, an output voltage regulation model is derived. A Proportional-Integral-Derivative (PID) control algorithm is employed for CV regulation.

(3) A simulation model and an 11 kW prototype were constructed to validate the proposed design methodology. Results demonstrate that the proposed control method successfully transitions from CC to CV output while maintaining output voltage stability within certain deviations. Moreover, the efficiency of the proposed method surpasses that of the semi-synchronous rectifier.

The organization of this paper is as follows: Section 2 presents a theoretical analysis of circuit structure and input-output characteristics. Section 3 introduces the CVCC control method based on a full-bridge rectifier, including analysis of the ZVS state of diodes, operational mode analysis, and principles of output voltage regulation. Section 4 outlines the design of the controllable synchronous rectifier. Section 5 covers simulation and

experimentation. Section 6 comprises a discussion, comparing the proposed method with previous works. Finally, Section 7 concludes the paper.

2. Circuit Topological Structure and Theoretical Analysis

2.1. Circuit Topological Structure Analysis

A DLCC compensation structure for both transmitting and receiving compensations is employed to implement the proposed CVCC method as shown in Figure 2. The circuit included a DC power supply, an inverter, an inductance capacitance resonance network, a synchronous signal sampling circuit, a synchronous signal processing circuit, a rectifier driver, a digital signal processing (DSP) or microcontroller unit (MCU), a synchronous rectifier, an output filter circuit, and a load. The DC power supply is linked to the input side of the inverter, with the output side of the inverter connected to the input side of the inductance capacitance resonance network. The output side of the network is then linked to the input side of the synchronous rectifier. High-frequency current signals from the inductance capacitance resonance network are obtained using the synchronous signal sampling circuit. These signals are processed by the synchronous signal processing circuit, converting them into high-frequency voltage signals, which are subsequently filtered, amplified, and transmitted to the DSP/MCU. The DSP/MCU generates pulse-width modulation (PWM) signals sent to the rectifier driver, connected to the synchronous rectifier, which in turn activates the rectification switches. The output of the synchronous rectifier is connected to the input of the filter output circuit, with its output connected to the load.

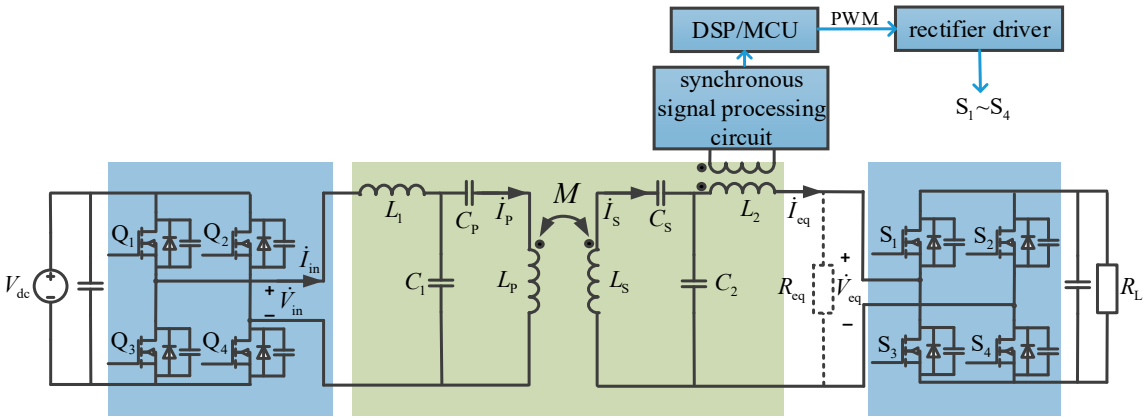


Figure 2. Topological structure diagram of the circuit.

As shown in Figure 2, the input side was the DC power supply V_{dc}. Four power MOSFETs, namely, switches Q_1 through Q_4, together with the body diodes and parasitic capacitors, constituted the full bridge inverter. Q_1 and Q_3 were complementary in conduction, and they were defined as the leading bridge arms of Q_4; Q_2, and Q_4 were complementary in conduction, and they were defined as hysteresis; $\boldsymbol{V_{in}}$ and $\boldsymbol{I_{in}}$ were the output voltage and the output current of the full-bridge inverter circuit, respectively. The parameters in the DLCC type of compensation networks, for example, L_1, C_1, L_2, C_2, C_P, and C_S, along with the coil inductance L_P and L_S, constituted a resonant cavity. The four power MOSFETs S_1 to S_4 constituted a controllable full-bridge rectification circuit. A current signal acquisition device was added to the front end of the rectifier. The device processed signals and drove the rectifier. The rectifier circuit converted the secondary high-frequency AC current to the DC current for the load; R_L was the load resistance; V_o and I_o were the load voltage and current, respectively; $R_{eq} = 8R_L/\pi^2$ was the equivalent resistance of the load resistance and the full-bridge rectifier; and $\boldsymbol{V_{eq}}$ and $\boldsymbol{I_{eq}}$ were the voltage and the current of the equivalent resistance, respectively.

2.2. Analysis of Input and Output Characteristics

According to the energy transmission characteristics of the coupling coils, the system structure shown in Figure 2 was simplified to obtain an equivalent circuit diagram of the DLCC IPT system, as shown in Figure 3. $\boldsymbol{V_{in}}$ was the square wave voltage output by the inverter module; and $\boldsymbol{I_{in}}$ was the output current of the inverter. The capacitance had a filtering effect on the high-order harmonics of the voltage signal on the primary side. Therefore, the input current filtered by LC, $\boldsymbol{I_P}$, could be regarded as a quasi-sine wave. After the current entered into the transmitting coil L_P, it was coupled with the secondary coil through electromagnetic induction, thus generating an induced electromotive potential $j\omega M\boldsymbol{I_P}$ on the secondary side. The current in the secondary coil was $\boldsymbol{I_S}$; R_P and R_S were the equivalent internal resistances of the coils on the primary and secondary sides, respectively; M was the mutual inductance between the transmitting coil and the receiving coil; and $\boldsymbol{I_{in}}$, $\boldsymbol{I_P}$, $\boldsymbol{I_S}$, and $\boldsymbol{I_{eq}}$ were the corresponding mesh currents, respectively. The component impedances of the circuit were $Z_{L1} = j\omega L_1$, $Z_{C1} = 1/j\omega C_1$, $Z_{LP} = j\omega L_P$, $Z_{CP} = 1/j\omega C_P$, $Z_{LS} = j\omega L_S$, $Z_{L2} = j\omega L_2$, and $Z_{C2} = 1/j\omega C_2$. According to Kirchhoff voltage law and Figure 3, the following relationship was obtained:

$$\begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} \boldsymbol{I_{in}} \\ \boldsymbol{I_P} \\ \boldsymbol{I_S} \\ \boldsymbol{I_{eq}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V_{in}} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{1}$$

where each non-zero element in the above matrix satisfies the following equations:

$$\begin{cases} Z_{11} = Z_{L1} + Z_{C1} \\ Z_{12} = -Z_{C1} = Z_{21} \\ Z_{23} = -Z_M = Z_{32} \\ Z_{34} = -Z_{C2} = Z_{43} \\ Z_{44} = Z_{L2} + Z_{C2} + R_{eq} \\ Z_{22} = Z_{CP} + Z_{LP} + Z_{C1} + R_P \\ Z_{33} = Z_{CS} + Z_{LS} + Z_{C2} + R_S \end{cases}. \tag{2}$$

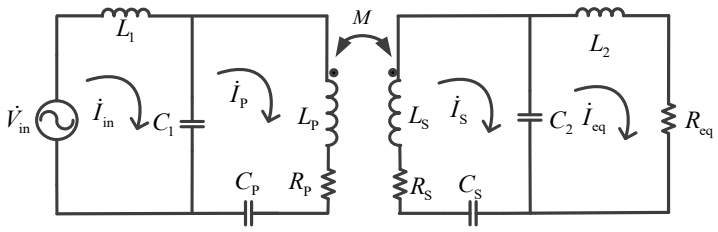


Figure 3. Equivalent circuit of the DLCC IPT system.

To simplify the calculation, Equation (1) is denoted as $ZI = V$, where I and V represent current and voltage vectors, respectively. Z represents the impedance matrix. According to circuit theory, the impedance matrix and the admittance matrix are inverses of each other. Therefore, the current vector is expressed as Equation (3).

$$\boldsymbol{I} = \boldsymbol{Z}^{-1} \cdot \boldsymbol{V}, \tag{3}$$

where $\boldsymbol{I} = [\boldsymbol{I_{in}}\ \boldsymbol{I_P}\ \boldsymbol{I_S}\ \boldsymbol{I_{eq}}]^T$. Equation (3) can be used to calculate the equivalent input impedance of the system, transconductance of the system, and the system efficiency, as follows:

$$\boldsymbol{Z_{in}} = \frac{\boldsymbol{V_{in}}}{\boldsymbol{I_{in}}}, \tag{4}$$

$$G_{VV} = \left| \frac{R_{eq} \cdot \boldsymbol{I_{eq}}}{\mathrm{V}_{\boldsymbol{in}}} \right|, \tag{5}$$

$$\eta = \frac{\left|\boldsymbol{I_{eq}}\right|^2 \cdot R_{eq}}{real(\boldsymbol{V_{in}} \boldsymbol{I_{in}^*})}. \tag{6}$$

Because the derivations of the input and output characteristics of the DLCC compensation structure were provided in the existing literature, they are not repeated here, and the conclusions are used [30]. Under the conditions of Equation (7), the system output is the constant current, and the input is the ZPA.

$$\begin{cases} j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} = 0 \\ j\omega_0 L_2 + \frac{1}{j\omega_0 C_2} = 0 \\ j\omega_0 L_S + \frac{1}{j\omega_0 C_S} + \frac{1}{j\omega_0 C_2} = 0 \\ j\omega_0 L_P + \frac{1}{j\omega_0 C_1} + \frac{1}{j\omega_0 C_P} = 0 \end{cases}, \tag{7}$$

where ω_0 is the system resonant frequency. If the coil resistance is ignored, the output current and voltage of the compensation network are expressed, respectively, as follows:

$$\begin{cases} \boldsymbol{I_{eq}} = -j{\omega_0}^3 C_1 C_2 M \cdot \boldsymbol{V_{in}} \\ \boldsymbol{V_{eq}} = -j{\omega_0}^3 C_1 C_2 R_{eq} M \cdot \boldsymbol{V_{in}} \end{cases}. \tag{8}$$

For the inverter to achieve the ZVS operation, it is necessary for the circuit to maintain weak sensibility. The input impedance can be kept in weak sensibility by fine-tuning C_P.

3. The CVCC Control Method Based on Full-Bridge Synchronous Rectification

3.1. The Condition with ZVS

From the output characteristics of the DLCC circuit that was under the resonant conditions of Equation (7), the circuit had a CC output, and the current was similar to a sine wave. After the control algorithms were implemented, the full bridge could be controlled on its output, and the CC output could be converted into a CV DC output as a power supply for the load. During the rectification process of the rear-end switches of the full bridge, it was necessary to ensure that the switches worked under the ZVS condition with zero voltage to improve the system efficiency. To realize the ZVS condition of the switches, the diode in reverse parallel with the switch had to be turned on, and the switch had to be turned on before the diode was turned off.

As shown in Figure 4, if the four switches were turned off, during the positive half cycle of the sinusoidal current (the red dotted line), the current flowed through the diodes S_1 and S_4, and the voltages at the ends of S_1 and S_4 were approximately zero. When S_1 and S_4 were turned on during this cycle, the ZVS condition could be achieved for S_1 and S_4. In contrast, during the negative half cycle of the sinusoidal current (the blue dotted line), the current flowed through the diodes S_2 and S_3. When S_2 and S_3 were turned on during this cycle, the ZVS condition could be achieved for S_2 and S_3.

The Simulink simulation results in Figure 5 show the driving waveforms of the switches and the output voltage and current waveforms of the compensation network when the switches were under a hard switch-on condition and the ZVS condition. To prevent the straight-through phenomenon of the switches on the same bridge arm, the driving signals of the switches on the same bridge arm were complementary. Therefore, the driving waveforms of S_1 and S_2 are omitted in Figure 4. More interpretation is provided in the operating mode analysis in the next section.

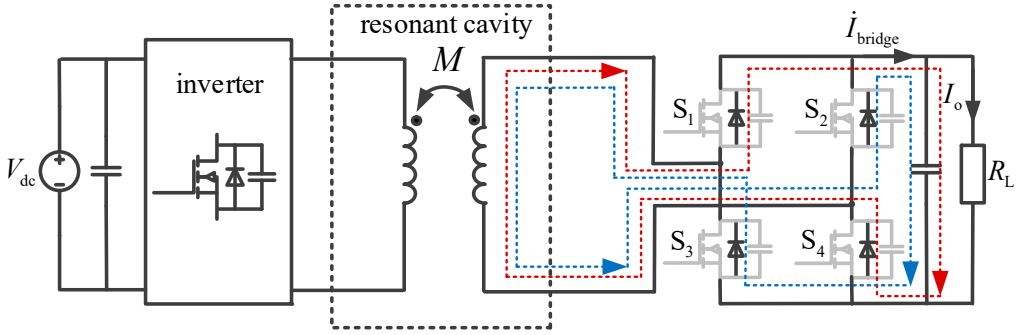


Figure 4. Current path diagram of the rectifier circuit.

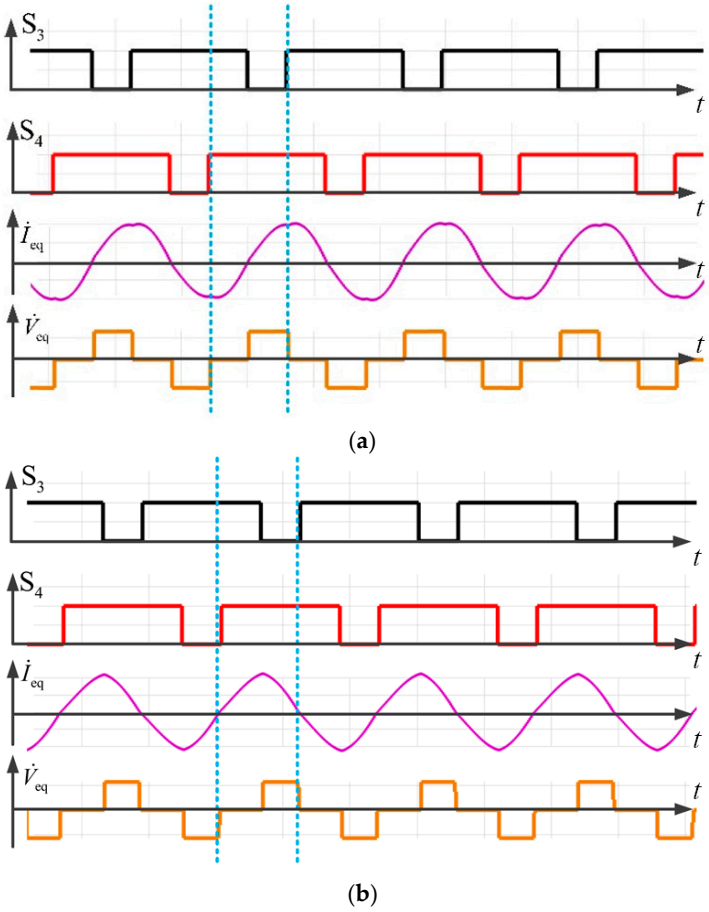


Figure 5. Driving waveforms of the switches and output voltage and current waveforms of the compensation network in two modes. (**a**) Hard switching mode. (**b**) Soft switching mode.

As shown in Figure 5a, the rising edge of the driving signal of S_4 was in the negative half cycle of the output current of the compensation network. At that moment, the voltages at both ends of S_4 were equal to the output voltage of the compensation network and decreased rapidly to zero. Therefore, the energy stored by the junction capacitor in S_4 was consumed on the switch S_4, indicating a hard switch-on condition of S_4. Similarly, the rising edge of the driving signal of S_3 was in the positive half cycle of the output current of the compensation network. At this moment, the voltages at both ends of S_3 were equal to the output voltage of the compensation network, and they decreased rapidly to zero, indicating a hard switch-on condition of S_3. It was observed that when the switch was turned on under the hard condition, the input current waveform of the compensation network exhibited a sunken shape.

As shown in Figure 5b, the rising edge of the driving signal of S_4 was in the positive half cycle of the output current of the compensating network after zero-crossing. At this moment, the voltages at both ends of S_4 were zero and kept at zero, leading to the ZVS condition of S_4. Similarly, the rising edge of the driving signal of S_3 was in the negative half cycle of the output current $\boldsymbol{I_{eq}}$ of the compensating network after zero-crossing. At this moment, the voltages at both ends of S_3 were zero and stayed at zero, leading to the ZVS condition of S_3. We also observed that when the switch was under the condition of zero voltage, the input current waveform of the compensation network exhibited a smooth shape when the switch was turned on.

3.2. Operating Mode Analysis

The previous section analyzed the ZVS condition of the switches in the rectification circuit. This section analyzes the operating modes of the circuit in detail. Figure 6 shows the driving waveforms of the switches under the ZVS condition and the output voltage and current waveforms of the compensation network. In the symmetric control mode, the duty cycles of the switches S_3 and S_4 were the same, represented by d_{34} ($0.5 \leq d_{34} \leq 1$). When the duty cycles of the switches S_1 and S_2 were the same, such a condition was represented by d_{12}. The driving waveform of S_1 was complementary to that of S_3 on the same bridge arm. The driving waveform of S_2 was complementary to that of S_4 on the same bridge arm. Moreover, $d_{12} = 1 - d_{34}$.

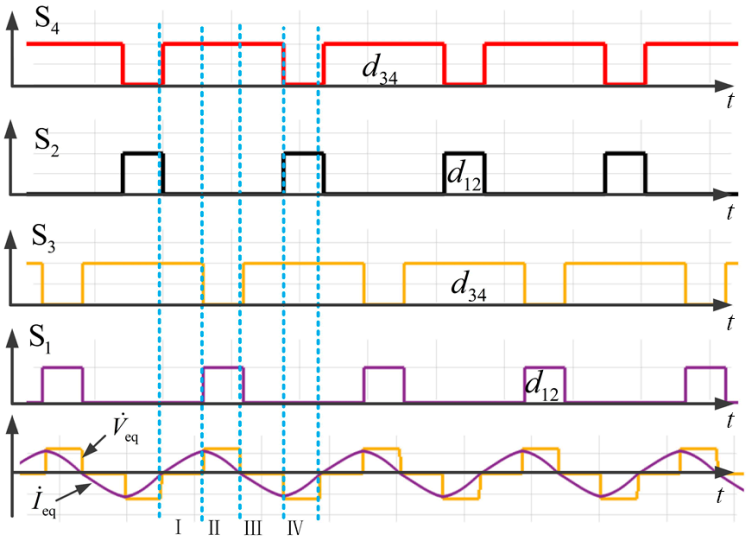


Figure 6. Driving waveforms of the switches and output voltage and current waveforms of the compensation network.

Figure 7 shows the current paths of the four operating modes of the rectification circuit. Each mode is described as follows:

Mode I: As shown in Figure 7a, in this mode, the output current of the compensation network was at a reverse point, and the current changed from negative to positive. Under the action of the synchronous signal, S_2 was shut off, and S_4 was turned on. Because S_4 was turned on in the positive half cycle of the output current of the compensation network, S_4 was switched on under zero voltage. Because S_1 remained off and S_3 remained on, the output current of the compensation network flowed through S_3 and S_4 and returned to the compensation network. The load resistor was short-circuited, resulting in zero-output voltage of the compensation network, and the voltage remained at zero.

Mode II: As shown in Figure 7b, in this mode, the output current of the compensation network was in the positive half cycle; S_3 was off, and S_1 was on. Because S_1 was turned on in the positive half cycle, S_1 was switched on under zero voltage. Because S_2 remained off and S_4 remained on, the output current of the compensation network flowed through

S_1, the load resistance, and S_4. The output voltage of the compensation network was the voltage at both ends of the load.

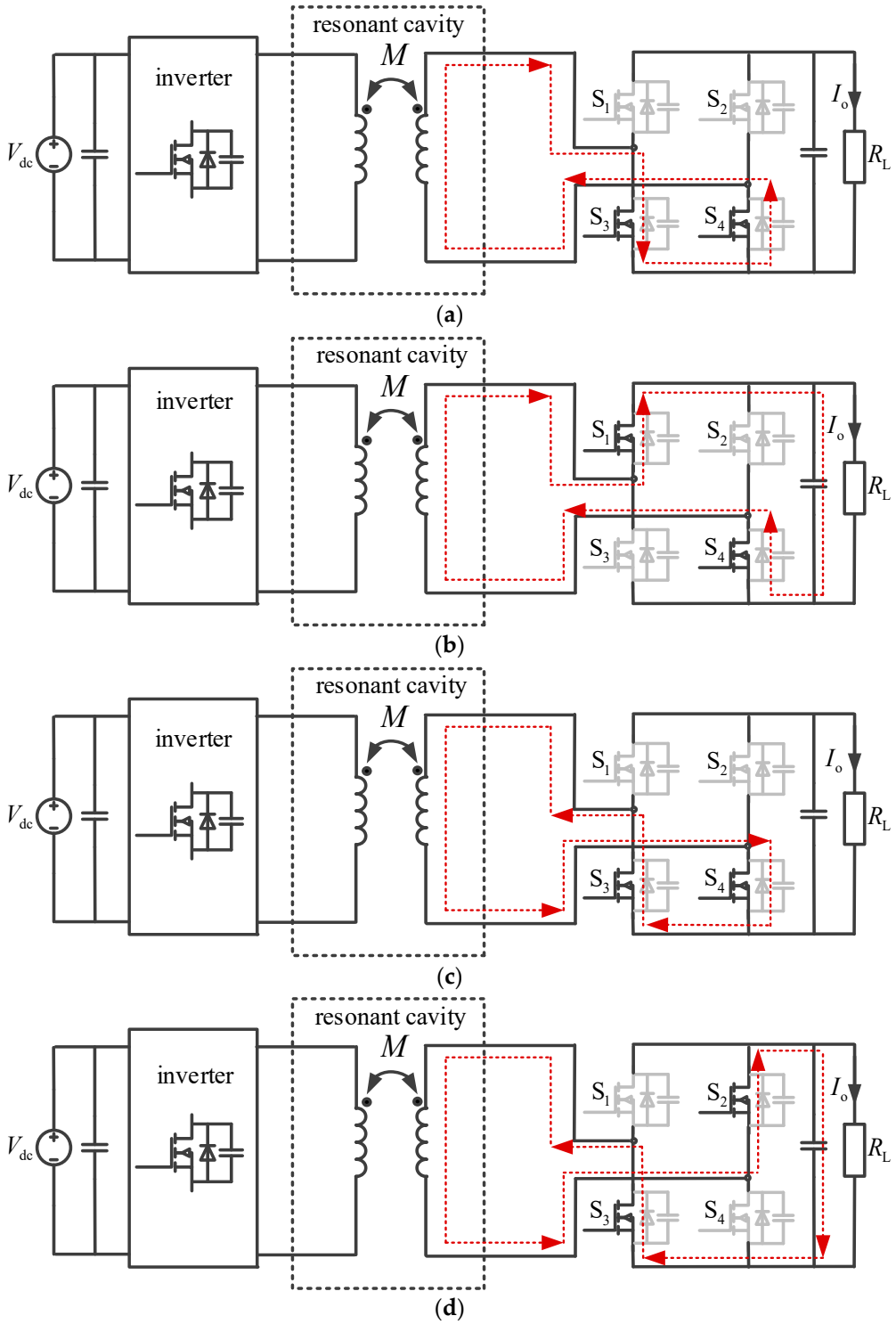


Figure 7. Current paths of the four operating modes. (**a**) Mode I. (**b**) Mode II. (**c**) Mode III. (**d**) Mode IV.

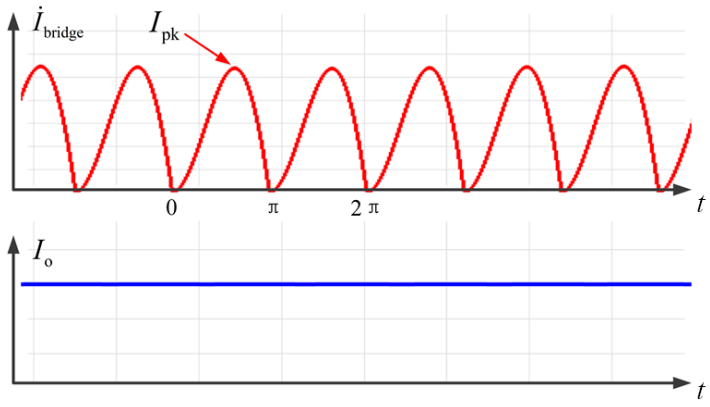
Mode III: As shown in Figure 7c, in this mode, the output current of the compensation network was at a reverse point, and the current changed from positive to negative. Under the action of the synchronous signal, S_1 was shut off, and S_3 was turned on. Because S_3 was turned on in the negative half cycle of the output current of the compensation network, S_3 was switched on under zero voltage. Because S_2 remained off and S_4 remained

on, the output current of the compensation network flowed through S_3 and S_4, and then returned to the compensation network. The load resistor was short-circuited, resulting in zero-output voltage of the compensation network, and the voltage was kept at zero.

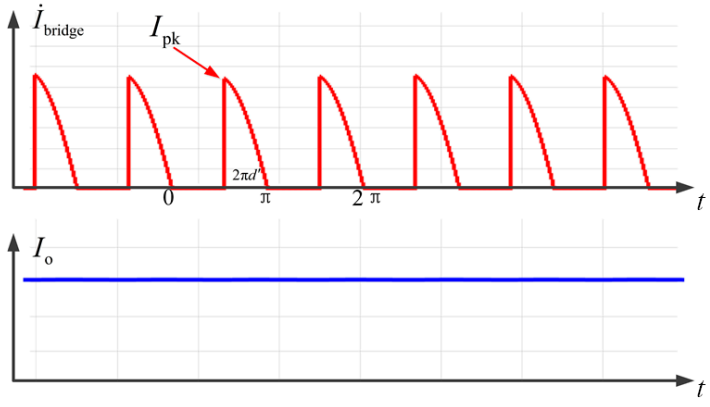
Mode IV: As shown in Figure 7d, in this mode, the output current of the compensation network was in a negative half cycle; S_4 was off, and S_2 was on. Because S_2 was turned on in the negative half cycle, S_2 was switched on under zero voltage. Because S_1 remained off and S_3 remained on, the output current of the compensation network flowed through S_2, the load resistance, and S_3. The output voltage of the compensation network was the voltage at both ends of the load.

3.3. Output Voltage Regulation Model

According to the ZVS condition, when the switches S_1 and S_4 were turned on in the positive half cycle of the output current of the compensating network, or when the switches S_2 and S_3 were turned on in the negative half cycle, the switches could achieve the ZVS condition. In addition to the requirement of operating under the ZVS condition, the system also had to achieve the maximum power output, which occurred in one of the following two scenarios in which all of the output current flowed through the load: (1) when S_1 and S_4 were turned on in the entire positive half cycle and turned off in the entire negative half cycle; and (2) when S_2 and S_3 were turned on in the entire negative half cycle and turned off in the entire positive half cycle. The fully controlled rectification bridge was connected with a voltage capacitor to output the current $\boldsymbol{I_{bridge}}$. The current was then filtered into the DC current $\boldsymbol{I_o}$ with smaller ripples to power the load. The output current waveforms are shown in Figure 8.



(**a**)



(**b**)

Figure 8. Output current waveforms of the rectifier and the system. (**a**) Conduction angle = π. (**b**) Conduction angle = $2\pi d_{12}$.

The peak value of the output current of the rectification bridge was assumed to be I_{pk}. Then, $I_{pk} = \sqrt{2}\,|\,\boldsymbol{I_{eq}}\,|$. The average value of the output current was $\boldsymbol{I_o}$. Figure 8a shows that the maximum output current and the maximum output voltage of the system can be calculated at the maximum power output as follows:

$$I_{omax} = \frac{I_{pk}\int_0^{\pi} \sin\alpha d\alpha}{\pi} = \frac{2I_{pk}}{\pi}, \tag{9}$$

$$V_{omax} = I_{omax}R_L = \frac{2I_{pk}R_L}{\pi}, \tag{10}$$

where α is the angle of the integration interval.

According to the preceding analysis of operating modes, in a symmetric control setting, the duty cycles of switches S_3 and S_4 were identical, denoted as d_{34}, while those of switches S_1 and S_2 shared the same value, represented by d_{12}. Additionally, the driving waveform of S_1 was complementary to that of S_3 within the same bridge arm, and similarly, the driving waveform of S_2 complemented that of S_4 on the same bridge arm. Under these conditions, the conduction angle of the rectification circuit was $2\pi d_{12}$. Figure 8b shows the output current waveform of the rectification circuit corresponding to this conduction angle. Therefore, the output current and voltage of the system can be calculated as follows:

$$I_o = \frac{I_{pk}\int_{\pi-2\pi d_{12}}^{\pi} \sin\alpha d\alpha}{\pi} = \frac{I_{pk}}{\pi}[1-\cos(2\pi d_{12})], \tag{11}$$

$$V_o = I_o R_L = \frac{I_{pk}R_L}{\pi}[1-\cos(2\pi d_{12})], \tag{12}$$

where the range of d_{12} is [0, 0.5], and the range of conduction angle is [0, π]. As the conduction angle increases, the output voltage increases. The regulation range of the output voltage is between 0 and V_{omax}.

From Equation (12), the relationship between the system output voltage and the duty cycle d_{12} is evident. Let us define the system's equilibrium operating point A (d_{12_0}, V_{O_0}) and perform a Taylor series expansion at point A, neglecting higher-order terms, we obtain the following:

$$V_o - V_{o\_0} = 2I_{pk}R_L \sin(2\pi d_{12})(d_{12} - d_{12\_0}), \tag{13}$$

where $\Delta V_O = V_O - V_{O\_0}$, $\Delta d_{12} = d_{12} - d_{12\_0}$, $K = 2I_{pk}R_L\sin(2d_{12\_0})$. Here, the linear equation can be simplified to $\Delta V_O = K\Delta d_{12}$, where K represents a proportionality coefficient. It signifies the tangent slope of function V_O at operating point A, reflecting the rate of change of the output voltage at that point. Since d_{12} ranges from 0 to 0.5, K is a positive real number. The output voltage variation is fastest when the duty cycle is 0.25, while it is slowest at duty cycles of 0 and 0.5 in the rectifier circuit.

4. Compensation Network Design Development of the Synchronous Rectifier

4.1. Controllable Rectifier Design

The power block diagram of the controllable rectifier module on the secondary side is shown in Figure 9. The design of the controllable rectifier was basically the same as that of the high-frequency inverter on the primary side. The major difference was adding a zero-crossing current detection circuit to realize accurate conduction of the rectifier tube. Current sampling was achieved by using 1000:1 Hall coils. The voltage was applied to the series resistances at the output end of the Hall coils. Square wave signals SYNC1 and SYNC2 were obtained after the first-stage and second-stage amplifiers. The zero-crossing current signals were used to judge the function of the MOSFET switch in the synchronous rectifier.

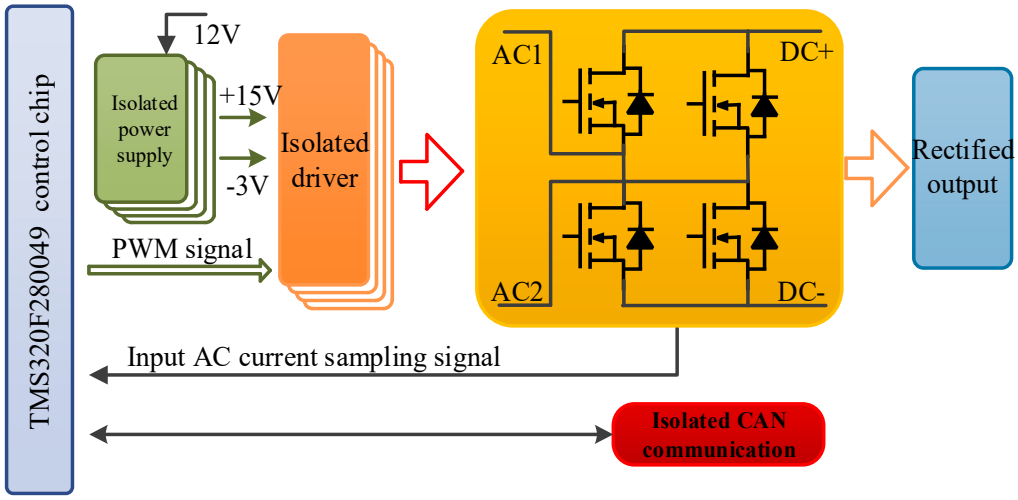


Figure 9. Power block diagram of the synchronous rectifier.

4.2. Implementation of Phase-Locked Loop

Figure 10 shows the schematic diagram of the principle of the phase-locked loop (PLL) with synchronous rectification. The capture (CAP) function port in DSP initialization was set up as the time base of the capture port. The trigger of the rising edge of the capture port was also defined. At time t_0, the rising edge of the synchronous sampling signal SYNC1 appeared, and the internal counter T was cleared to start counting. At time t_1, the rising edge's jump of the S_4 synchronous rectifier tube was detected, and the count value of T, $N_{result1}$, was sent into the register "result1" corresponding to the capture port. At time t_2, the rising edge's jump of SYNC1 in the next cycle was captured, and the count value of T, $N_{result2}$ was sent into the register "result2." Then, the internal counter T was cleared to zero to start counting for the next cycle.

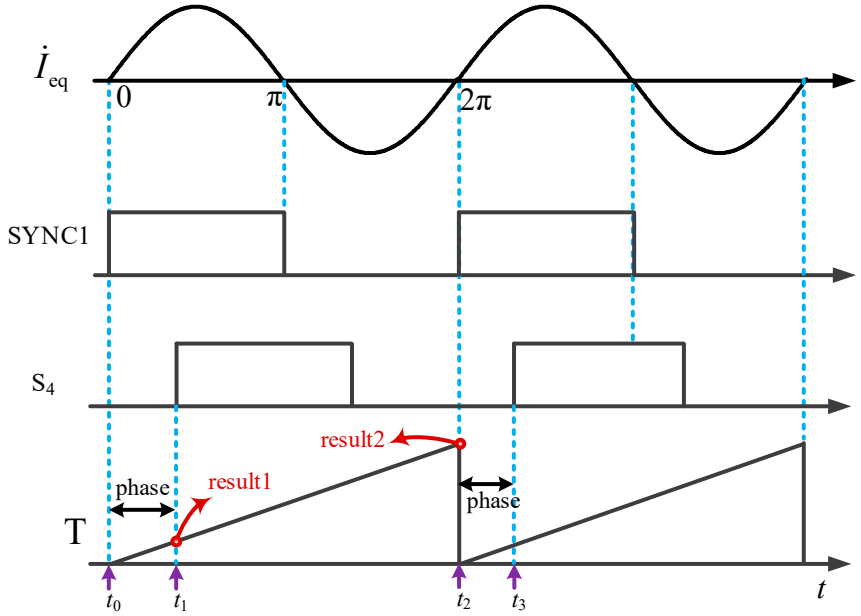


Figure 10. Principle of digital phase-locked loop.

Therefore, the phase difference between the synchronous sampling signal SYNC1 and the synchronous rectifier tube S_4 can be expressed as follows:

$$\alpha_{PLL} = 2\pi \frac{N_{result1}}{N_{result2}} \tag{14}$$

If the calculated phase difference was in the range of 1° to 180°, the phase of S_4 lagged behind SYNC1. If the calculated phase difference was in the range of 180° to 359°, the phase of S_4 led SYNC1. If the calculated absolute value was less than 1°, phase locking was successful.

5. Simulation and Experimental Validation

To validate the proposed design method, we used MATLAB/Simulink 2018a simulation models and a set of 11 kW principle prototypes to produce both computational and experimental verification data. According to the system parameters derived from the theory in Section 2, the components of the compensation network can be calculated from Equations (7) and (8). The parameters used in the validation are given in Table 1.

Table 1. Basic parameters.

Parameter	Value
DC input voltage (V)	560
Rated load (kW)	11
Zero-offset coupling coefficient	0.19
Transmitting coil's self-induction L_P (μH)	116.40
Compensation capacitor at the primary side C_P (nF)	44.45
Compensating inductance at the primary side L_1 (μH)	37.17
Compensation capacitor at the primary side C_1 (nF)	94.41
Operating frequency (kHz)	85
Operating distance (mm)	100
Resistance range (Ω)	25–100
Receiving coil's self-induction L_S (μH)	172.98
Compensation capacitor at the secondary side C_S (nF)	24.80
Compensating inductance at the secondary side L_2 (μH)	25.78
Compensation capacitor at the secondary side C_2 (nF)	136.00
Dimensions of the transmitting coil (mm)	580 × 580 × 32
Dimensions of the receiving coil (mm)	360 × 360 × 32
The plane offset distance of receiving and transmitting coil (mm)	0–100

5.1. Simulation Analysis of the Soft Startup Process

During startup, the duty cycle of the MOSFET on the secondary side rectifier was 1. The duty cycle gradually decreased to achieve the CV output.

Throughout this procedure, the output voltage steadily rose to facilitate a soft startup. As depicted in Figure 11, the waveform of the output voltage and current during startup under the rated load illustrates this progression. Notably, the voltage ascended gradually to the predetermined level with minimal overshooting, while the current exhibited a steady increase, also without overshooting, ensuring a seamless startup. Following startup, the voltage exhibited fluctuations within the range of 499.5 to 500.5 V, with a voltage ripple of 1 V, while the current fluctuated between 19.95 and 20.05 A, with a current ripple of 0.1 A. These findings underscore the efficacy of the proposed design methodology. Further discussions will delve into the simulation and experimental results pertaining to the CV output characteristics at varying loads.

Figure 12 shows the ZVS waveform of the MOSFETs. When the V_{ds} of the MOSFET switch decreased to 0, V_{gs} increased to a high level and achieved the ZVS condition with reduced switch-on losses of MOSFET.

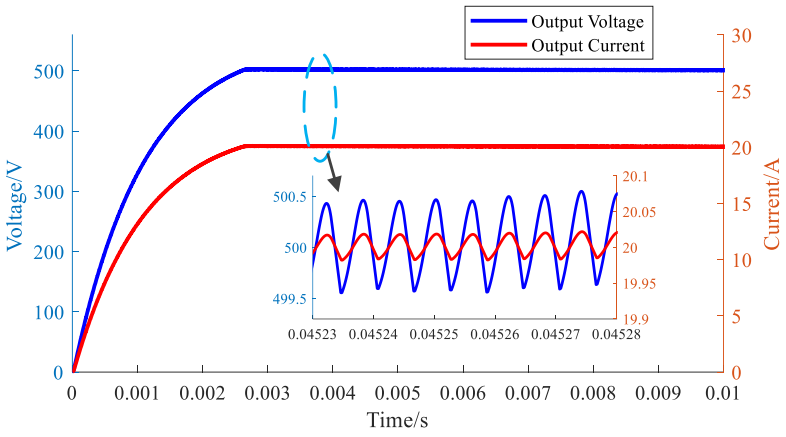


Figure 11. System output voltage and current waveforms during soft startup.

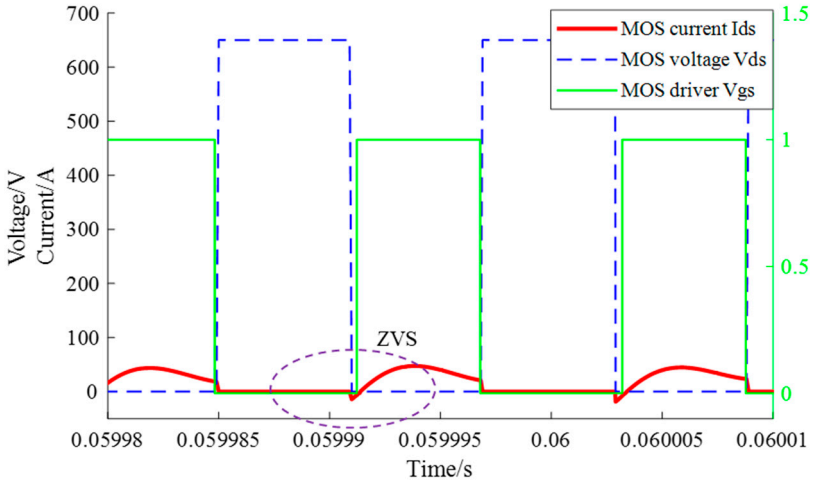


Figure 12. The ZVS waveforms of the rectifier MOSFETs.

5.2. Simulation Analysis of Dynamic Characteristics

After the system was started without any load, the load was successively added to 25%, 50%, 75%, and 100% at 0.05 s, 0.1 s, 0.15 s, and 0.2 s, respectively. The voltage and current waveforms during the loading process are shown in Figure 13. During the loading process, the output voltage decreased to 495 V, with approximately 1% reduction, and the current did not overshoot. The CV output was achieved at approximately 20 ms during each loading.

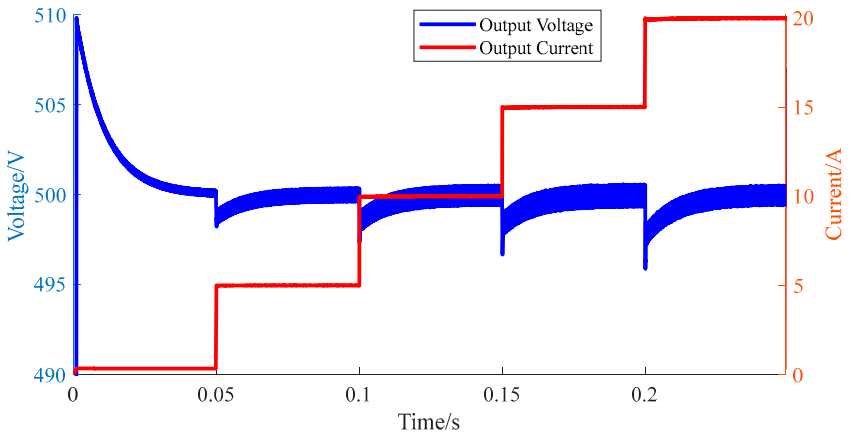


Figure 13. System output voltage and current waveforms during the four-stage loading process.

During the process of no-load startup, the voltage on the load had very little overshooting. The peak voltage was 510 V, with only 2% overshooting, and the current did not have any overshooting.

5.3. Analysis of Experimental Results

To validate the theoretical analysis, a physical experiment platform of the IPT system was built. The platform used B1M040120HC silicon carbide power MOSFET to constitute the full-bridge inverter circuit and the rectification circuit. The driver integrated circuit used the enhanced isolation ISO5852S driver chip. The control module used the TMS320F280049 chip. To increase the resonance quality factor of the transmission coils to avoid magnetic saturation, the coils were wound with the Litz wire. Ferrite was tiled at the bottom of the coils, and an aluminum plate was used as a shielding layer. The output voltage frequency of the inverter was 85 kHz. The distance between the transmitting and receiving coils was 100 mm. The measured coupling coefficient was 0.19. The experimental platform is shown in Figure 14.

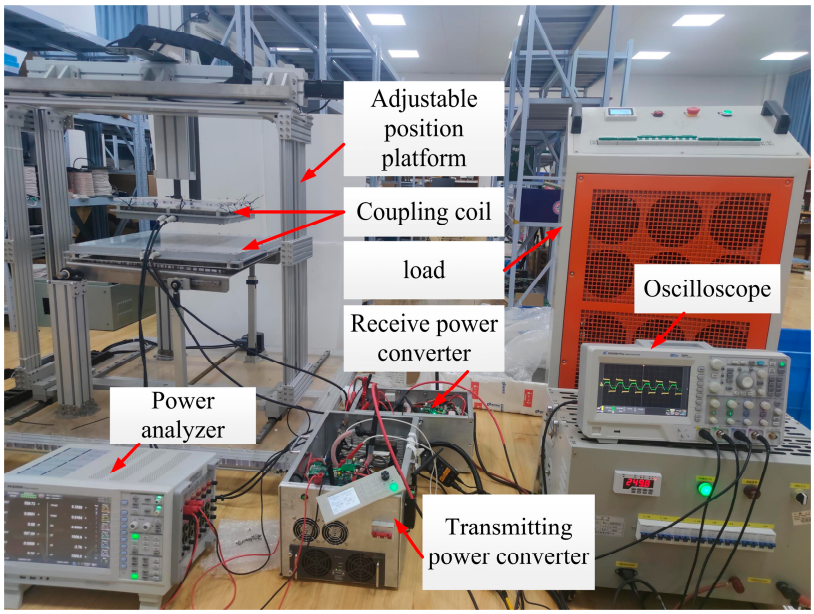


Figure 14. Experimental platform.

This experiment was conducted according to the parameters listed in Table 1 to obtain the input and output waveforms of the system at different loads. The test data was recorded, and the results are shown in Figures 15–18. Figure 15 shows the waveforms of the output voltage and current of the inverter at different loads. Figure 16 shows the waveforms of the output voltage and current of the compensation network at different loads. Both Figures 15 and 16 feature screenshots from the oscilloscope. The model of the oscilloscope is ZDS3024, manufactured by Zhiyuan Electronics in Guangzhou, China. Figure 17 shows the test data of the voltage gains of the system at different loads. Figure 18 shows the test data of the system efficiencies of the full-bridge synchronous rectification and semi synchronous rectification at different loads.

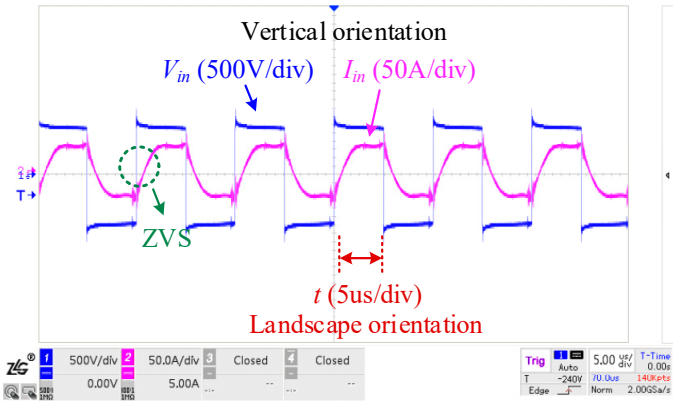
Figure 15 shows that at different loads, the output voltage of the inverter always led the output current, and the input impedance of the system was weakly inductive. These conditions ensured that the inverter was able to function properly under the ZVS condition.

Figure 16 shows that at different loads, the output current of the compensation network was constant. Therefore, the DLCC compensation structure had good CC characteristics. The duty cycle of the output voltage of the compensation network increased with the increase in the load. To maintain the CV output, when the output voltage decreased, the switch-on time of the switch under the rectifier had to decrease to increase the switch-on

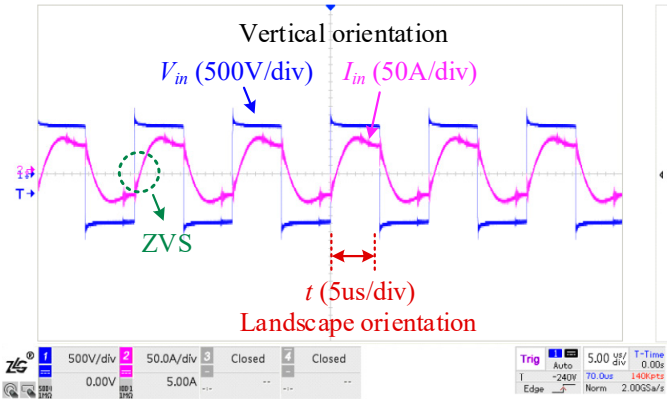
time on the load side, so that the CV output could be maintained. When the output voltage increased, the switch-on time of the switch under the rectifier had to increase to short-circuit the load side to reduce the switch-on time on the load side, so that the CV output could be maintained.

Figure 17 shows the experimental data of the voltage gains at different loads. We observed that the output voltage was always stable. When the coupling coil was offset by 100 mm, the system was able to maintain the same CV output characteristics. These results further verified that the proposed design method was accurate.

Figure 18 shows that the system output efficiencies of the two rectification methods increased with the increase in the load and reached the maximum at the rated load. Moreover, the system output efficiency of the full-bridge synchronous rectifier was higher than that of the semi synchronous rectifier, reaching the maximum efficiency of 95.6% at the rated load. The conduction loss of the MOSFETs was less than that of the diode when the soft switch-on condition was used.



(**a**)



(**b**)

Figure 15. Output voltage and current waveforms of the inverter at different loads from oscilloscope; (**a**) 75% rated load; and (**b**) 100% rated load.

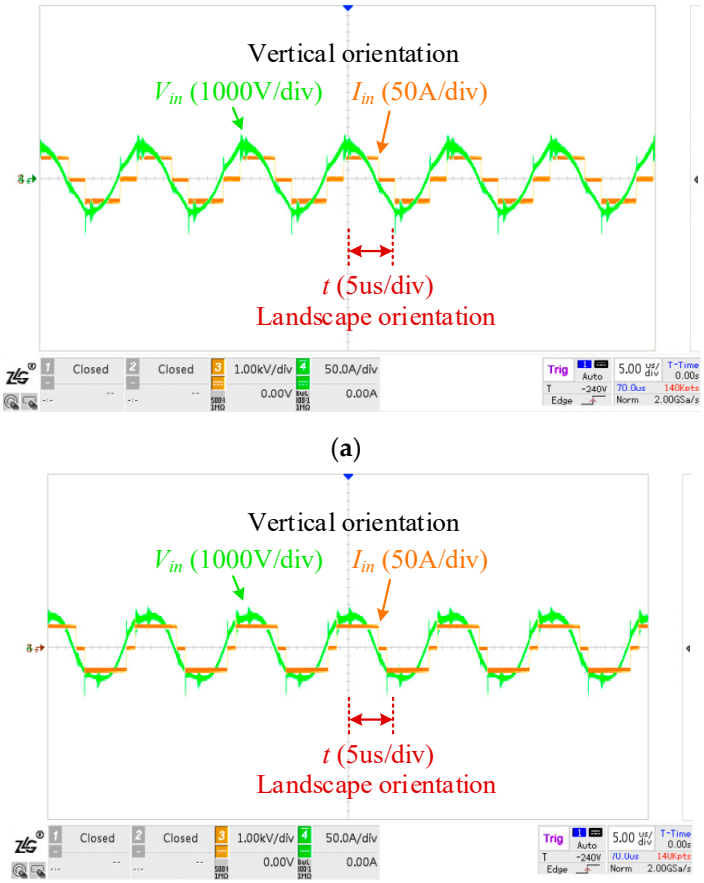


Figure 16. Output voltage and current waveforms of the compensation network at different loads from oscilloscope; (**a**) 75% rated load; and (**b**) 100% rated load.

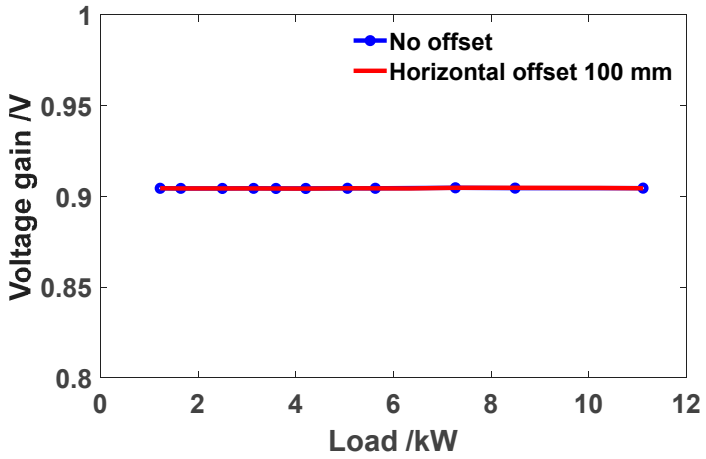


Figure 17. Voltage gain diagram at different loads.

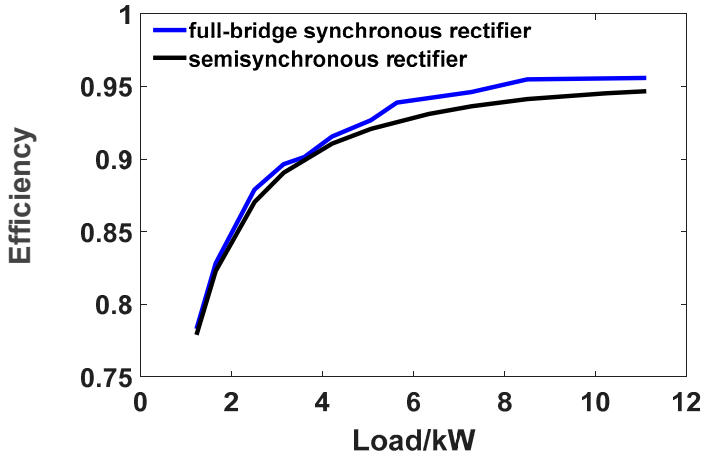


Figure 18. System efficiency diagram at different loads.

6. Discussion

To effectively evaluate the proposed approach and clearly demonstrate the improvements achieved using the proposed method, this paper contrasts with some typical IPT systems featuring CVCC output characteristics. The comparative results are presented in Table 2. Refs. [10,11] analyzed and designed the CVCC state of IPT systems based on LCC-S and DLCC compensation networks, respectively, and validated them using a 3.3 kW prototype, with maximum efficiencies of 89.2% and 92.9%, respectively. Ref. [12] employed a hybrid topology, utilizing switching between two different characteristic compensation networks to achieve CV and CC switching, validated with a 0.12 kW prototype, achieving a maximum efficiency of 92.2%. Ref. [26] realized CVCC operation by adding a Boost converter on the secondary side, with power and efficiency of 0.5 kW and 92.9%, respectively. It is noteworthy that Refs. [12,26] introduced more complex structures, inevitably leading to a decrease in power density. Ref. [29] utilized a semi-synchronous rectifier, with a more compact structure, achieving power and efficiency of 2.5 kW and 88%, respectively.

Table 2. Comparison of IPT systems with CVCC output characteristics.

Ref.	Topology	Power	Efficiency
[10]	LCC-S + Uncontrolled rectifier	3.3 kW	89.2%
[11]	DLCC + Uncontrolled rectifier	3.3 kW	92.9%
[12]	LCC-S + DLCC + Uncontrolled rectifier	0.12 kW	92.2%
[26]	LCC-S + Uncontrolled rectifier + Boost Converter	0.5 kW	92.9%
[29]	DLCC + Semi-synchronous rectifier	2.5 kW	88%
This work	**DLCC + Controllable synchronous rectifier**	**11 kW**	**95.6%**

Compared to previous studies, this work combines the advantages of DLCC compensation networks and controllable synchronous rectifiers, resulting in significant improvements in output power and efficiency. Moreover, without adding additional cascaded modules, the power density is higher. The established prototype achieved an output power of 11 kW and an efficiency of 95.6%, demonstrating the effectiveness and advancement of the proposed method.

While the proposed method demonstrates promising results, there are some limitations to consider. For example, in harsh environments, wireless communication may encounter difficulties; system performance may be affected by sudden changes in load and coupling; and eddy current losses in underwater transmission significantly increase system impedance, leading to decreased control precision, among other issues. Future work could focus on developing adaptive control strategies to mitigate these effects and further enhance system efficiency and robustness. Additionally, exploring advanced modulation

techniques and optimization algorithms could lead to even greater improvements in IPT system performance.

7. Conclusions

This paper presents a dynamic voltage regulation control method for the secondary side circuit in the IPT system, utilizing the DLCC compensation structure to achieve CVCC output. Employing the DLCC compensation structure enables CC output realization. The secondary side circuit employs a full-bridge rectification topological structure to adjust the conduction time of the rectifier bridge switches, facilitating the transition from CC output to CV output. We delve into the conditions and control methods necessary to attain the ZVS condition for the full-bridge controllable rectifier. Additionally, a simulation model and an 11 kW prototype were constructed to validate the proposed design approach. Results demonstrate that the proposed system exhibits favorable CV output characteristics and maintains a constant output amidst certain interference from coupling offset.

In conclusion, this study demonstrates the effectiveness of the proposed dynamic voltage regulation control method for achieving CVCC output in the IPT system. Through simulation analysis and experimental validation, it is evident that the system maintains stable CV output characteristics and exhibits high efficiency, particularly with the utilization of the full-bridge synchronous rectifier. Furthermore, the proposed design method proves to be robust against certain interference conditions, highlighting its practical applicability in real-world scenarios.

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