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A Novel Variable On-Time Control Scheme for Boundary Conduction Mode SEPIC PFC Converter

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Abstract: Power factor correction (PFC) can be achieved by a single-ended primary inductor converter (SEPIC) operating in boundary conduction mode (BCM) with conventional constant on-time (COT) control, but it is challenging to achieve low total harmonic distortion (THD) and high-power factor (PF), particularly at high input voltage. A variable on-time (VOT) control strategy for BCM SEPIC PFC converter without input voltage feedforward and multiplier circuits is proposed to realize unity PF in this paper. By using a variable slope sawtooth generator whose slope is controlled by the duty cycle of the main switch to adjust the conduction time of the main power switch of the converter, the proposed VOT control scheme can use a simple and easy-to-implement circuit to enhance the PF and decrease the THD significantly, especially at high input voltage. The simulation model and 100W experimental prototype are built to verify the feasibility of the suggested control method. Simulation and experiment results demonstrated that the novel VOT control scheme remarkably enhances PF and decreases THD without affecting the efficiency by contrast with the conventional COT control.

Keywords: boundary conduction mode; SEPIC converter; power factor correction; variable on-time control; variable slope sawtooth generator

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1. Introduction

In recent years, the demands for power supplies with power factor correction (PFC) converters have increased to realize low input current harmonic and high-power factor (PF) to conform to the necessary harmonic limits standards, e.g., IEEE STD 519 and IEC61000-3-2 [1–5]. To realize PFC, many different PFC circuit topologies, including Buck, Boost, Cuk, Buck-Boost etc., have been researched to satisfy different application condition requirements [6–12]. The input current ripple of the Boost converter is small because of the series connection of the inductor at the input side, so the Boost converter can realize high PF and has been widely used [8–10]. However, Boost PFC topology cannot achieve the output voltage, which is lower than the magnitude value of AC input voltage. It is hard to handle high input inrush current and short output protection during starting up. To meet applications where the output voltage is lower than the input voltage Buck PFC converter is researched in [6,7], it is easy to achieve short output protection, but it is hard to realize high PF because there is a large input current dead time when the output voltage is higher than the instantaneous input voltage of each AC line period. To achieve a voltage between the maximum and minimum input voltage range, Buck-Boost and Cuk PFC converters are investigated in [11–14], but applications of Buck-Boost and Cuk PFC are limited since the output voltage is negative. Similar to the Boost converter, the current ripple at the input terminal of a single-ended primary inductor converter (SEPIC) is small because the converter has an inductor connected in series at the input terminal, so the SEPIC converter is suitable to achieve PFC [15,16]. Compared to Boost, Buck, Buck-boost, and Cuk PFC converters, SEPIC PFC converter can easily achieve positive polarity output voltage, short output protection, more comprehensive output voltage range [16–18]. Therefore, SEPIC

PFC converter has gained more and more applications such as light emitting diode driving circuits, onboard chargers for plug-in electric vehicles, brushless DC motor drives, air-craft power supplies etc. [19–31].

According to whether the freewheeling diode is always conducting during the power switch of the SEPIC converter is turned off in a switching cycle, SEPIC topology can operate in discontinuous conduction mode (DCM), boundary conduction mode (BCM) and continuous conduction mode (CCM) [24–28]. For CCM operation mode, the SEPIC PFC converter usually requires an outer voltage control loop and an inner current control loop to control the shape of the input current and pre-regulate the output voltage. Furthermore, the additional multiplier is usually required to handle rectified input voltage sensing signal and error signal of output voltage, which increases the complexity of the control circuit [16,17,25,26]. On the other hand, the SEPIC PFC converter operating in DCM can achieve PFC using a simple voltage follower with one voltage control loop [27–32]. However, the efficiency is poor due to the large RMS current and peak current of the power switch and diode, which limits its application in higher output power. Compared with DCM, the SEPIC PFC converter operating in BCM can use a single voltage control loop to achieve PFC. However, it has higher efficiency, especially for higher output power applications [23,24]. Therefore, SEPIC PFC converters operating in BCM have been increasingly widely used.

It is well known that a Boost PFC converter operating at BCM with constant on-time (COT) control can obtain perfect sine-wave input current and unity PF. Therefore, many researchers use COT control as the control strategy for SEPIC PFC converters operating in BCM [20,24,33]. As shown in the test data of [20], PF is 0.97 with 200 V forward voltage and 350 mA rated current LED load at 220 Vac input voltage; as shown in the test data of [24], PF is 0.91 with 1.4 A rated output current and 60 W output power LED load at 230 Vac input voltage; as shown in the test data of [33], with 264 Vac input voltage and 210 W output power, PF and total harmonic distortion (THD) are 0.924 and 18.1% respectively. Therefore, from experimental data and waveforms in [20,24,33], the BCM SEPIC PFC converter with COT control scheme results in a slightly distorted input current, low PF, and high THD, especially with high input voltage. To achieve unity PF and reduce the THD of the PFC converter with the COT control method, a variable on-time (VOT) control method has been proposed for BCM Flyback or Buck PFC converter [6,34–36].

Moreover, a VOT control method for SEPIC PFC converter operating in BCM is proposed to achieve unity [37]. The method uses output and input voltage to calculate and adjust the on-time of the power switch. From experimental results in [37], the PF maintains to be bigger than 0.995 with 100 W output power at 90~265 Vac entire input voltage. With these VOT control strategies mentioned in [6,34–37], the PF and input current harmonic are ameliorated. Still, the extra multiplier, input voltage feedforward, and operational amplifier circuits make the control circuit complicated and expensive.

This paper proposes a novel VOT control strategy for SEPIC PFC converter operating in BCM without input voltage feedforward and multiplier circuits to realize unity PF. By using a variable slope sawtooth generator whose slope is controlled by the main power switch's duty cycle to adjust the main power switch's on-time, the proposed control scheme can use a simple and easy-to-implement circuit to achieve unity PF at the entire input voltage range. The operation principles and performance comparison of VOT and COT control schemes for SEPIC PFC converter operating in BCM are investigated and developed. Finally, the simulation and test results based on the 100 W prototype are presented to validate the feasibility of the proposed VOT control and the correctness of the performance comparison analysis.

This paper consists of 6 sections as follows. Section 2 analyses the SEPIC PFC converter operating in BCM with a traditional COT control scheme. In Section 3, a variable-on-time control scheme with a variable slope sawtooth generator for SEPIC PFC converter operating BCM is proposed and analyzed. Utilizing the proposed control scheme, the performance of PF and THD can be improved. Section 4 analyses performance comparisons of the two

control schemes' input current, power factor, output voltage ripple, switching frequency, and current stress. In Sections 5 and 6, experimental verification results and a conclusion are given, respectively.

2. Boundary Conduction Mode SEPIC Power Factor Correction Converter with Constant-On-Time Control

Figure 1a presents the circuit diagram of SEPIC DC-DC converter topology, which is consisted of input capacitor C_{in}, inductors L_1 and L_2, main switch S_1, freewheeling diode D_1, middle capacitor C_1, output capacitor C_2 [38,39]. When the SEPIC converter operates at BCM mode, the SEPIC converter has two operation modes. Equivalent circuits of two operation modes and operation waveforms of the circuit are presented in Figure 1b–d.

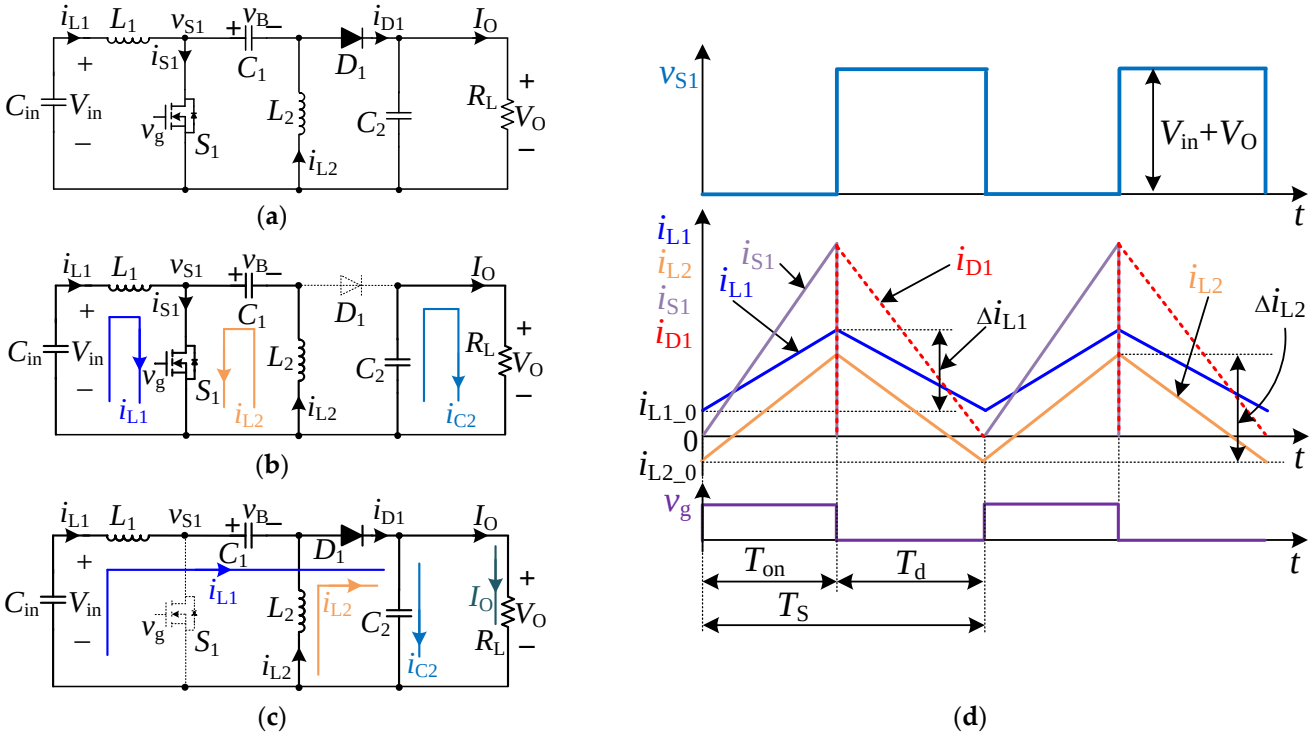


Figure 1. The circuit diagram, equivalent circuits, and key waveforms of BCM SEPIC DC-DC converter. (**a**) Circuit diagram of SEPIC DC-DC converter topology; (**b**) Equivalent circuit when S_1 is on; (**c**) Equivalent circuit when S_1 is off; (**d**) Key waveforms during a switching cycle.

Operation mode A: The main power switch S_1 is switched on at the start of each switching cycle, diode D_1 is reverse-biased, SEPIC converter works at operation mode A when S_1 is on. Figure 1b,d shows the equivalent circuit and key waveforms for mode A. In operation mode A, the voltage of v_{S1} is zero because S_1 is on; C_{in}, L_1, and S_1 form a current loop, the input voltage V_{in} applies to inductor L_1, the inductor current i_{L1} ramps up with the slope of V_{in}/L_1 from the initial value i_{L1_0}; C_1, S_1, and L_2 form a current loop, the middle capacitor voltage v_B applies to inductor L_2, the inductor current i_{L2} ramps up with the slope of v_B/L_2 from the initial value i_{L2_0}; Output capacitor C_2 and output load R_L form a current loop, output capacitor C_2 provides energy to load resistor; Both inductor currents of L_1 and L_2 flow through switch S_1, the currents flowing through S_1 ramp up from zero [38,39].

Operation mode B: When the turn-on time reaches the target value, S_1 is turned off, operation mode A ends, and the converter enters operation mode B Figure 1c,d show the equivalent circuit and key waveforms for mode B. In operation mode B, S_1 is turned off, and D_1 is forward-biased, which makes both inductors L_1 and L_2 release energy to the middle capacitor C_1 and output load through diode D_1. In operation mode B, the voltage

of v_{S1} is $V_{in} + V_O$ because D_1 is forward-biased and v_B is equal to V_{in}; C_{in}, L_1, C_1, D_1, C_2, and R_L form a current loop, the output voltage V_O applies to inductor L_1, the inductor current i_{L1} decreases with the slope of V_O/L_1 from the peak value; L_2, D_1, C_2, and R_L form a current loop, the output voltage V_O applies to inductor L_2, the inductor current i_{L2} decreases with the slope of V_O/L_2 from the peak value; Both inductor currents of L_1 and L_2 flow through diode D_1, when the current i_{D1} decreases to zero, S_1 is turned on, the next switching cycle is started again [38,39].

The block diagram of the SEPIC PFC converter operating in BCM with the conventional COT control is presented in Figure 2a. It consists of rectifier bridge D_{Rec}, inductors L_1 and L_2, main switch S_1, freewheeling diode D_1, middle capacitor C_1, output capacitor C_2, error amplifier EA, comparator CMP, sawtooth generator, zero current detection, SR flip-flop etc. In addition, L_f and C_f are used as low-pass input filters.

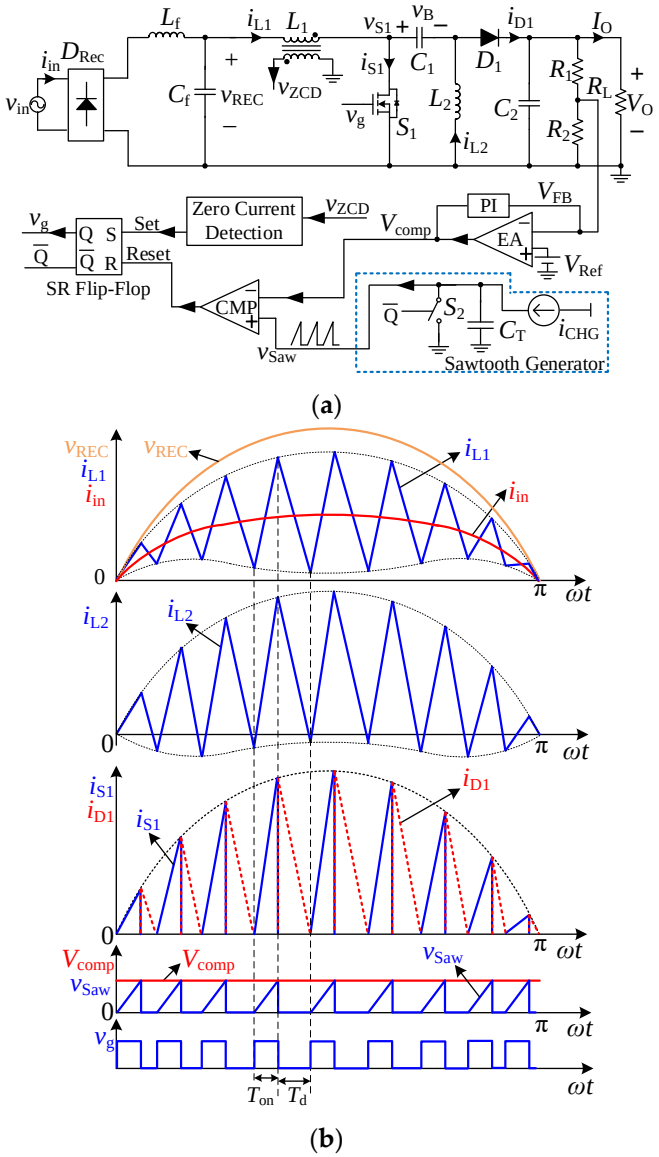


Figure 2. Block diagram and main waveforms of SEPIC PFC converter operating in BCM with the traditional COT control scheme. (**a**) Block diagram; (**b**) Key waveforms during half AC line period.

Figure 2b presents the operation waveforms of the SEPIC PFC circuit working in BCM with traditional COT control during half AC line period. At the start of each switching cycle, S_1 is turned on; when the voltage v_{Saw} of the sawtooth generator at the positive input terminal of comparator CMP increases to V_{comp}, S_1 is turned off. According to Figure 2b,

the output voltage V_{comp} of the error amplifier maintains constant in half the AC line period because the bandwidth of the control loop is usually much lower than the AC line frequency for the PFC converter [34,35]. Furthermore, since the slope of the sawtooth generator of COT control is fixed, the on-time of S_1 is almost fixed when the converter operates in a steady state with a stable input voltage and output load.

By analyzing the operation principle, the inductor current peak-to-peak ripple of L_1 and L_2 of SEPIC PFC converter operating in BCM can be given by

$$\Delta i_{L1}(t) = \frac{V_M|\sin(\omega t)|T_{on}}{L_1} \tag{1}$$

$$\Delta i_{L2}(t) = \frac{v_B(t)T_{on}}{L_2} \tag{2}$$

where V_M and $v_B(t)$ is the amplitude of input voltage and the voltage of the middle capacitor C1 respectively, T_{on} is the on-time of S_1. In the derivation of the following equation, $i_{L1\_0}(t)$ and $i_{L2\_0}(t)$ are the initial values of L_1 and L_2 currents for each switching cycle, respectively, $i_{L1\_avg}(t)$ and $i_{L2\_avg}(t)$ are the average values of the current flowing through L_1 and L_2.

During the steady operation, the average voltage of middle capacitor C_1 in one switching cycle is equal to the rectified input voltage [33], so there is.

$$v_B(t) = V_M|\sin(\omega t)| \tag{3}$$

Because the rectified input current is equal to the average current of the inductor L_1, the input current $i_{in}(t)$ can be expressed as follows.

$$|i_{in}(t)| = i_{L1\_avg}(t) = i_{L1\_0}(t) + \frac{\Delta i_{L1}(t)}{2} \tag{4}$$

The SEPIC converter operates in BCM. Once the current of D_1 decreases to zero, S_1 is turned on, and the initial current of main switch S_1 should be zero, so there is.

$$i_{L1\_0}(t) + i_{L2\_0}(t) = 0 \tag{5}$$

The charge balance of the middle capacitor C_1 in a switching period can be expressed as

$$\left(\frac{\Delta i_{L1}(t)}{2} + i_{L1\_0}(t)\right)T_d(t) = \left(\frac{\Delta i_{L2}(t)}{2} + i_{L2\_0}(t)\right)T_{on} \tag{6}$$

where $T_d(t)$ is the time that diode D_1 is forward biased, and $T_d(t)$ can be obtained as

$$T_d(t) = \frac{V_M|\sin(\omega t)|T_{on}}{V_O} \tag{7}$$

According to (1), (2), (3), (5), (6), and (7), $i_{L1\_0}(t)$ can be expressed as

$$i_{L1\_0}(t) = \frac{T_{on}V_M|\sin(\omega t)|}{2(V_O + V_M|\sin(\omega t)|)}\left(\frac{V_O}{L_2} - \frac{V_M|\sin(\omega t)|}{L_1}\right) \tag{8}$$

From (1), (4), and (8), the input current $i_{in}(t)$ can be obtained as

$$i_{in}(t) = \frac{T_{on}V_M\sin(\omega t)}{2(1 + K_1|\sin(\omega t)|)}\left(\frac{1}{L_1} + \frac{1}{L_2}\right) \tag{9}$$

where $K_1 = V_M/V_O$.

Equation (9) shows that the input current is not an ideal sine-waveform. Therefore, with the traditional COT control, unity PF cannot be achieved except with extreme condition $K_1 = 0$.

3. Variable-On-Time Control Scheme

Observing Equation (9), the denominator of the equation contains $(1 + K_1\sin(\omega t))$, which prevents the input current from being sinusoidal. Based on (9), suppose T_{on} can be controlled to be proportional to $(1 + K_1\sin(\omega t))$, the unity PF may be achieved. Figure 3 illustrates a detailed block diagram for the developed procedure from COT control to VOT control, which can explain how the VOT control with variable slope sawtooth generator is proposed.

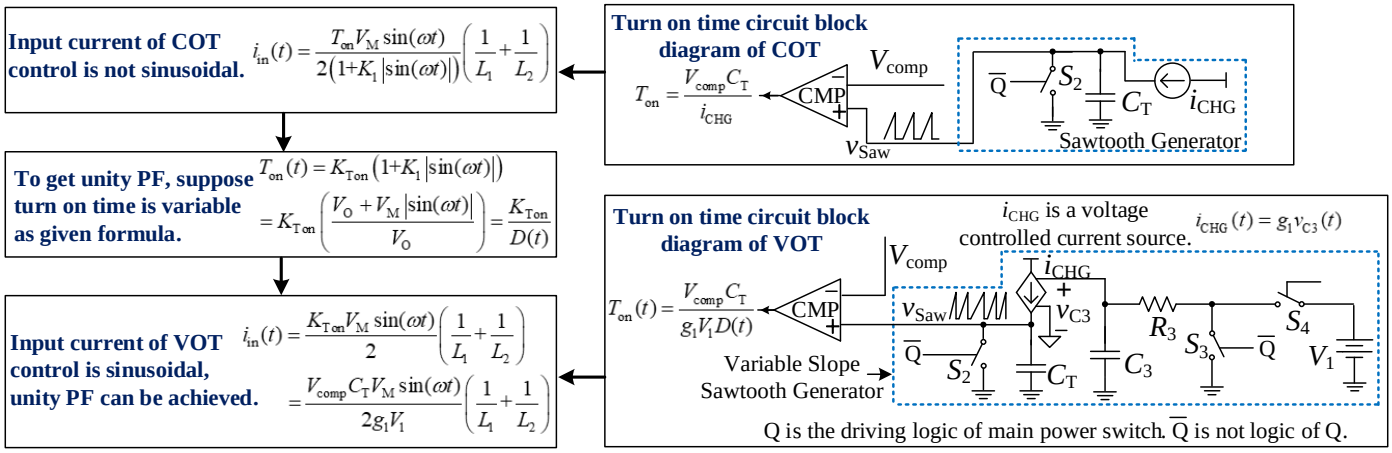


Figure 3. Block diagram for the developed procedure from COT control to VOT control.

By analyzing (9) and Figure 3, to realize sinusoidal input current, the on time of S_1 is supposed as

$$T_{on}(t) = K_{Ton}(1 + K_1|\sin(\omega t)|) \tag{10}$$

where K_{Ton} is a constant parameter about turning on the time control circuit. Combining (9) and (10), the input current can be written as

$$i_{in}(t) = \frac{K_{Ton}V_M\sin(\omega t)}{2}\left(\frac{1}{L_1}+\frac{1}{L_2}\right) \tag{11}$$

Observing (11), it can be seen that the ideal sinusoidal input current can be achieved if the on-time of S_1 can be varied, as in equation (10).

Combing definition of K_1 and SEPIC converter operation theory [38,39], Equation (10) can be written as

$$T_{on}(t) = K_{Ton}\left(\frac{V_O + V_M|\sin(\omega t)|}{V_O}\right) = \frac{K_{Ton}}{D(t)} \tag{12}$$

$D(t)$ is the duty cycle of S_1. Based on Equation (12) and the turn-on time circuit of COT control, it is conceivable to use a variable slope sawtooth generator to produce variable turn-on time, as shown in Figure 3. The variable slope sawtooth generator consists of a charging current i_{CHG}, a voltage-controlled current source (VCCS), a timing capacitor C_T, a reference voltage source V_1, a low pass RC filter comprised of R_3 and C_3, and three signal switches S_2~S_4 etc.

Therefore, using a variable slope sawtooth generator to produce variable turn-on time, a novel VOT control scheme for SEPIC PFC converter operating in BCM, which can get unity PF, is proposed. Figure 4 illustrates the block diagram and key operation waveforms of the SEPIC PFC converter operating in BCM with VOT control. Compared to the COT control strategy shown in Figure 2a, only an additional variable slope sawtooth generator, shown in the blue dashed line of Figure 4a, is required in the VOT control strategy.

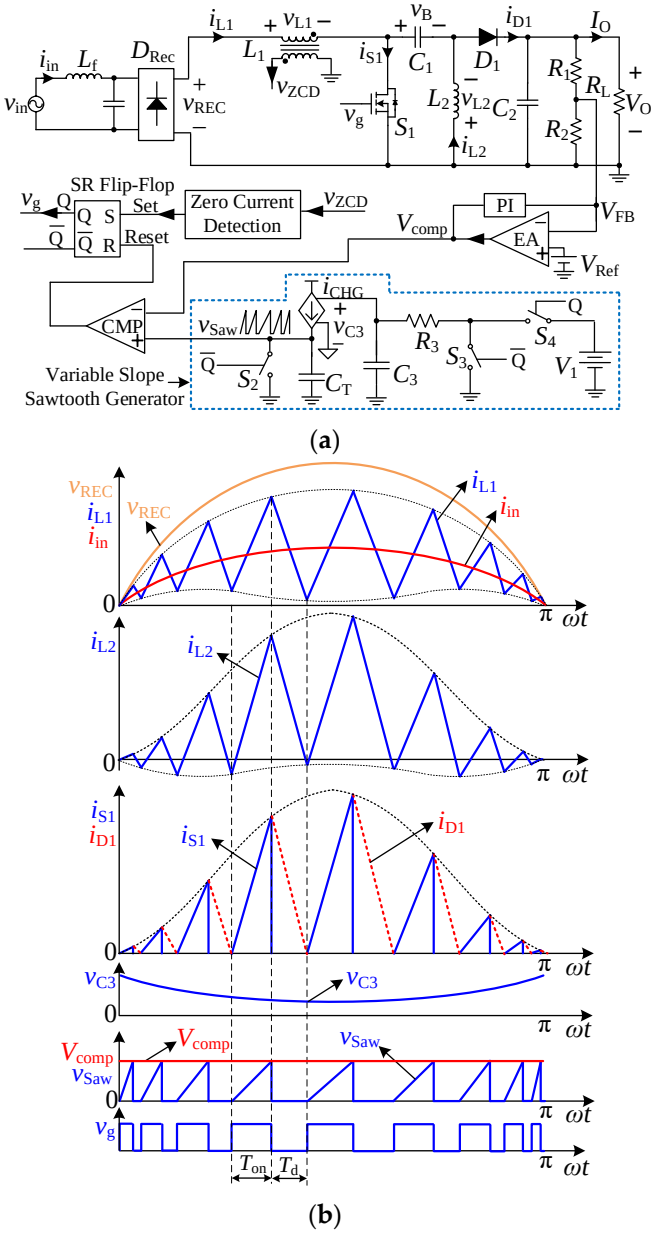


Figure 4. Block diagram and main waveforms of BCM SEPIC PFC converter with VOT control. (**a**) Block diagram; (**b**) Key waveforms during half line cycle.

According to the circuit of the variable slope sawtooth generator in Figure 4a, the signal switch S_4 is controlled by gate drive signal Q of S_1, and the signal switch S_2 and S_3 are controlled by the inverting drive signal Q. Hence, the turn-on time of the signal switches S_4 and S_3 are $T_{on}(t)$ and $T_s(t)$-$T_{on}(t)$ respectively. The low pass RC filter comprised of R_3 and C_3 filters out the switching frequency so that the control voltage v_{C3} of the VCCS remains stable during a switching period. Therefore, the charging current $i_{CHG}(t)$ of the sawtooth generator can be expressed by

$$i_{CHG}(t) = g_1 v_{C3}(t) = \frac{g_1 V_1 T_{on}(t)}{T_S(t)} = g_1 V_1 D(t) \tag{13}$$

where g_1 is the control ratio of the VCCS i_{CHG}, $T_{on}(t)$, $T_S(t)$, and $D(t)$ are the turn-on time, the switching period, and the duty cycle of S_1 respectively. According to Equation (13) and

Figure 4, the slope of the sawtooth generator in the proposed converter is variable with $D(t)$ of S_1. Therefore, the turn-on time of switch S_1 can be expressed as

$$T_{\text{on}}(t) = \frac{V_{\text{comp}} C_{\text{T}}}{i_{\text{CHG}}(t)} = \frac{V_{\text{comp}} C_{\text{T}}}{g_1 V_1 D(t)} \tag{14}$$

Since the SEPIC PFC converter operates in BCM, there are

$$T_{\text{S}}(t) = T_{\text{on}}(t) + T_{\text{d}}(t) \tag{15}$$

$$D(t) = \frac{T_{\text{on}}(t)}{T_{\text{S}}(t)} \tag{16}$$

According to (1), (2), (3), (5), (6), (7), (15), and (16), the initial inductor current $i_{L1\_0}(t)$ of L_1 for the proposed VOT control scheme can be obtained as

$$i_{L1\_0}(t) = \frac{D(t) V_{\text{M}} |\sin(\omega t)| T_{\text{on}}(t)}{2} \left(\frac{1}{L_2} - \frac{1}{L_1} \frac{V_{\text{M}} |\sin(\omega t)|}{V_{\text{O}}} \right) \tag{17}$$

From (1), (4), (17), the input current $i_{\text{in}}(t)$ with VOT control can be derived as

$$i_{\text{in}}(t) = \frac{V_{\text{M}} \sin(\omega t) T_{\text{on}}(t) D(t)}{2} \left(\frac{1}{L_1} + \frac{1}{L_2} \right) \tag{18}$$

By substituting (14) into (18), the input current $i_{\text{in}}(t)$ with VOT control can be obtained as

$$i_{\text{in}}(t) = \frac{V_{\text{comp}} C_{\text{T}} V_{\text{M}} \sin(\omega t)}{2 g_1 V_1} \left(\frac{1}{L_1} + \frac{1}{L_2} \right) \tag{19}$$

During operating at a steady state, the error signal V_{comp} keeps almost constant during half line period because of the quite narrow control loop bandwidth. For a given converter, the timing capacitor C_{T} of the sawtooth generator and the control ratio g_1 of the VCCS i_{CHG} are constant. Therefore, define K_{Ton} in (11) as

$$K_{\text{Ton}} = \frac{V_{\text{comp}} C_{\text{T}}}{g_1 V_1} \tag{20}$$

According to (11), (19), and (20), Equations (11) and (19) are the same. Therefore, the input current with VOT control is an ideal sine-waveform. Hence the proposed VOT control scheme can achieve the theoretical unity PF of the SEPIC PFC converter operating in BCM.

4. Performance Comparison

4.1. Comparison of Input Current and Power Factor

According to (1), (2), and Figure 2, the peak current through D_1 of COT control can be given as

$$i_{D1\ \_\text{PK\_COT}}(t) = \Delta i_{L1\_\text{COT}}(t) + \Delta i_{L2\_\text{COT}}(t) = V_{\text{M}} |\sin(\omega t)| T_{\text{on\_COT}} \left(\frac{1}{L_1} + \frac{1}{L_2} \right) \tag{21}$$

where $T_{\text{on\_COT}}$ is the turn-on time of S_1 with COT control.

The average current flowing through D_1 during each switching period with COT control can be derived as

$$i_{D1\_\text{AVG\_COT}}(t) = \frac{i_{D1\_\text{PK\_COT}}(t) T_{\text{d\_COT}}(t)}{2 T_{\text{S\_COT}}(t)} \tag{22}$$

where $T_{d\_COT}(t)$ and $T_{S\_COT}(t)$ is the forward bias time of diode D_1 and the switching period of COT control.

As the average current of diode D_1 is equal to the output current I_O in half line cycle, the output current I_O with traditional COT control can be given as

$$I_O = \frac{1}{\pi}\int_0^{\pi} i_{D1\_AVG\_COT}(t)d(\omega t) = \frac{K_2 V_M{}^2 T_{on\_COT}}{2\pi V_O}\left(\frac{1}{L_1}+\frac{1}{L_2}\right) \tag{23}$$

where

$$K_2 = \int_0^{\pi} \frac{\sin^2(\omega t)}{(1+K_1|\sin(\omega t)|)}d(\omega t) \tag{24}$$

From (9) and (23), the input current of COT control can be obtained as

$$i_{in\_COT}(t) = \frac{\pi V_O I_O \sin(\omega t)}{K_2 V_M (1+K_1|\sin(\omega t)|)} \tag{25}$$

In the same way, the input current of VOT control can be derived as

$$i_{in\_VOT}(t) = \frac{2V_O I_O \sin(\omega t)}{V_M} \tag{26}$$

To conveniently compare the input currents of both control schemes, the normalized input currents with the base of $(2V_O I_O)/V_M$ can be expressed as

$$i^*_{in\_COT}(t) = \frac{\pi \sin(\omega t)}{2K_2(1+K_1|\sin(\omega t)|)} \tag{27}$$

$$i^*_{in\_VOT}(t) = \sin(\omega t) \tag{28}$$

According to (27) and (28), Figure 5 shows both control schemes' normalized input currents waveform with different K_1 in half-line cycles. Observing Figure 5, the input current of the VOT control scheme is in shape with sinusoidal, but the input current waveform of COT control deviates from sinusoid, especially when K_1 is large.

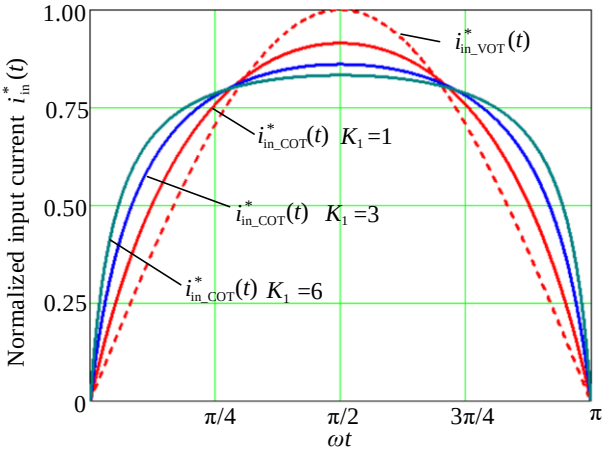


Figure 5. Comparison of the normalized input current waveform.

According to (25), the PF of COT control can be derived as

$$PF_{COT} = \frac{\sqrt{2}P_{in\_COT}}{V_M I_{in\_RMS\_COT}} = \frac{\sqrt{2}\int_0^{\pi} \frac{\sin^2(\omega t)}{1+K_1|\sin(\omega t)|}d(\omega t)}{\sqrt{\pi}\sqrt{\int_0^{\pi}\left(\frac{\sin(\omega t)}{(1+K_1|\sin(\omega t)|)}\right)^2 dt}} \tag{29}$$

According to (26), (29), and the circuit parameters listed in Table 1 of Section 5, the comparison of the PF of COT and VOT control schemes with the variation of input voltage can be depicted in Figure 6. Therefore, it can be known that compared with COT control, the SEPIC PFC converter operating BCM with the proposed VOT control scheme based on variable slope sawtooth generator can improve the PF and realize theoretical unity PF.

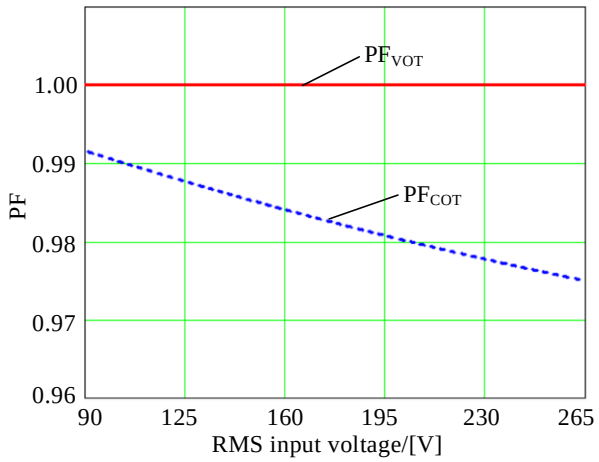


Figure 6. Comparison of the PF with different RMS input voltage.

4.2. Comparison of Output Voltage Ripple

The instantaneous power imbalance between the output and input of the PFC converter leads to a double-line frequency ripple of output voltage [34]. By analyzing the circuit of Figure 2, the double line frequency output voltage ripple is produced by the second-order harmonic current of i_{D1} flowing into output capacitor C_2.

According to the Fourier series formula, the second-order harmonic current's magnitude of D_1 with COT control, $I_{D1\_COT}^{2nd}$, can be derived as

$$\begin{aligned} I_{D1\_COT}^{2nd} &= \left|\tfrac{2}{\pi}\int_0^{\pi} i_{D1\_AVG\_COT}(t)\cos(2\omega t)d(\omega t)\right| \\ &= \tfrac{{V_M}^2 T_{on\_COT}}{\pi V_O}\left(\tfrac{1}{L_1}+\tfrac{1}{L_2}\right)\left|\int_0^{\pi}\tfrac{\sin^2(\omega t)\cos(2\omega t)}{(1+K_1|\sin(\omega t)|)}d(\omega t)\right| \\ &= K_3 I_O \end{aligned} \tag{30}$$

where

$$K_3 = \left|\frac{2\int_0^{\pi}\frac{\sin^2(\omega t)}{(1+K_1|\sin(\omega t)|)}\cos(2\omega t)d(\omega t)}{\int_0^{\pi}\frac{\sin^2(\omega t)}{(1+K_1|\sin(\omega t)|)}d(\omega t)}\right| \tag{31}$$

According to (23), (24), and (30), the output voltage ripple of COT can be derived as

$$\Delta V_{O\_COT} = \frac{I_{D1\_COT}^{2nd}}{2\pi f_L C_2} = \frac{K_3 I_O}{2\pi f_L C_2} \tag{32}$$

In the same way, the output voltage ripple of VOT can be presented as

$$\Delta V_{O\_VOT} = \frac{I_O}{2\pi f_L C_2} \tag{33}$$

According to (32), (33), and the key parameters listed in Table 1 of Section 5, the output voltage ripple of both control schemes with different input voltage can be plotted in Figure 7. It can be known that compared with COT control, the output voltage ripple with the VOT control scheme is slightly larger.

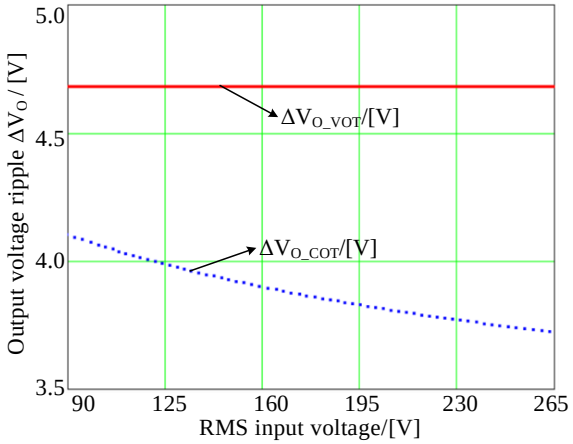


Figure 7. Comparison of the output voltage ripple with the variation of RMS input voltage.

4.3. Comparison of Switching Frequency

From (23), the turn-on time of S_1 with COT control can be given as

$$T_{\text{on\_COT}} = \frac{2\pi I_O V_O}{K_2 {V_M}^2 (\frac{1}{L_1} + \frac{1}{L_2})} \tag{34}$$

From (7) and (15), the switching frequency of COT can be derived as

$$f_{\text{S\_COT}}(t) = \frac{K_2 {V_M}^2}{2\pi V_O I_O (1 + K_1 |\sin(\omega t)|)} (\frac{1}{L_1} + \frac{1}{L_2}) \tag{35}$$

In the same way, the turn-on time, and the switching frequency of S_1 of VOT control can be given respectively as

$$T_{\text{on\_VOT}}(t) = \frac{4 V_O I_O (1 + K_1 |\sin(\omega t)|)}{{V_M}^2 (\frac{1}{L_1} + \frac{1}{L_2})} \tag{36}$$

$$f_{\text{S\_VOT}}(t) = \frac{{V_M}^2}{4 V_O I_O (1 + K_1 |\sin(\omega t)|)^2} (\frac{1}{L_1} + \frac{1}{L_2}) \tag{37}$$

As the peak currents of the inductors L_1 and L_2 occur at $\omega t = \pi/2$, it is important to analyze the switching frequencies of both control schemes at $\omega t = \pi/2$ during designing both inductors L_1 and L_2. According to (35), (37), and the parameters listed in Table 1 of Section 5, the switching frequency of COT and VOT control at $\omega t = \pi/2$ with the variation of RMS input voltage can be obtained in Figure 8.

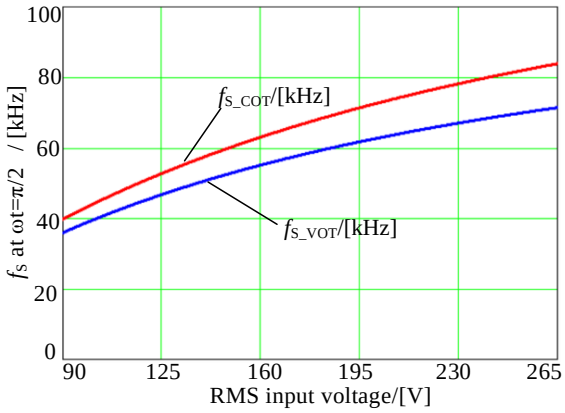


Figure 8. Comparison of the switching frequency at $\omega t = \pi/2$ with different input voltage.

From (35) and (37), with the base of $\frac{V_M^2}{4V_O I_O}(\frac{1}{L_1}+\frac{1}{L_2})$, the normalized switching frequencies with both control schemes are derived as

$$f^*_{s\_COT}(t) = \frac{2K_2}{\pi(1+K_1|\sin(\omega t)|)} \tag{38}$$

$$f^*_{s\_VOT}(t) = \frac{1}{(1+K_1|\sin(\omega t)|)^2} \tag{39}$$

From (38) and (39), the normalized switching frequency variations curves with COT and VOT control schemes during half AC line period can be plotted in Figure 9.

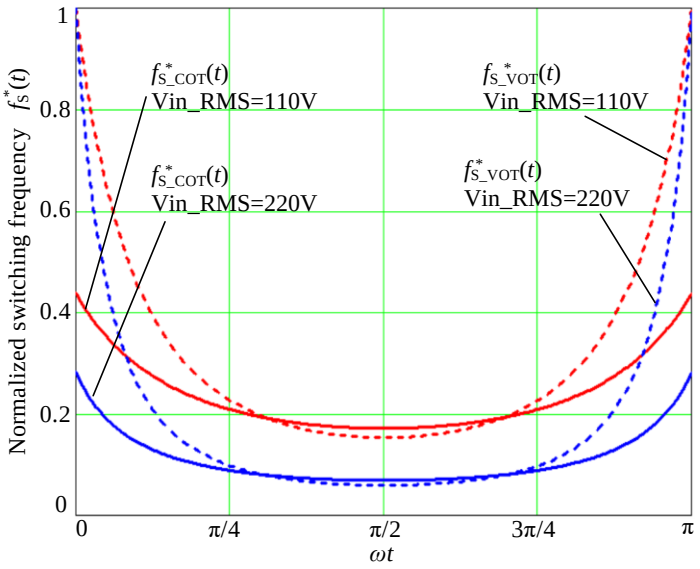


Figure 9. Comparison of the normalized switching frequency curves with COT and VOT control schemes during half AC line period.

Figure 8 shows that the switching frequency of both control schemes increases with the increase of the RMS value of input voltage at $\omega t = \pi/2$. According to Figures 8 and 9, with the same RMS input voltage, the switching frequency of VOT is lower than that of COT control when the transient input voltage is near the peak value, i.e., when ωt is $\pi/2$; the switching frequency of VOT is greater than that of COT when the transient input voltage is near the zero crossing. This is because the range of the VOT control's switching frequency variation is wider than that of the COT control. Hence, compared with COT control, the cut-off frequency of the input low-pass filter of VOT control is lower. Moreover, to avoid extremely high switching frequency, both BCM SEPIC PFC converters with COT and VOT control schemes should limit the main power switch's maximum switching frequency or minimum turning-off time.

4.4. Comparison of Peak Current of Main Switch

From the operation principle of SEPIC PFC converter operating in BCM, the peak currents of main switch S_1 and freewheeling diode D_1 are the same, so only the peak current of S_1 is analyzed in this section.

According to (1), (2), (5), (34), and (36), the peak currents flowing through main switch S_1 with COT and VOT control can be obtained as

$$i_{S1\_PK\_COT}(t) = \frac{2\pi I_O V_O|\sin(\omega t)|}{K_2 V_M} \tag{40}$$

$$i_{S1\_PK\_VOT}(t) = \frac{4I_O V_O|\sin(\omega t)|(1+K_1\sin(\omega t))}{V_M} \tag{41}$$

For the PFC converter, the peak current flowing through the main power switch S_1 reaches a maximum when ωt is $\pi/2$. Therefore, according to (40), (41), and the key parameters listed in Table 1 of Section 5, the comparison of maximum peak currents flowing through S_1 with both control schemes under different RMS input voltage can be depicted in Figure 10.

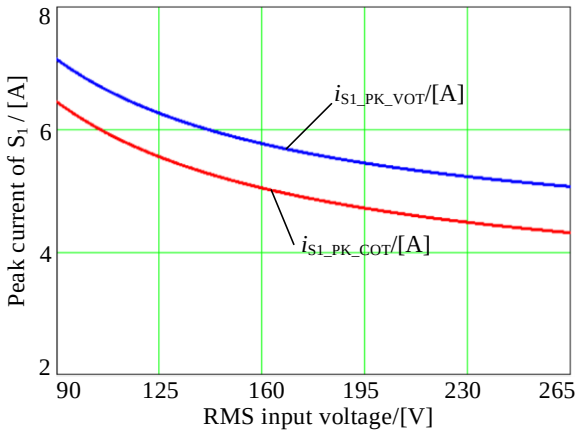


Figure 10. Comparison of the maximum peak current of S_1 under different RMS input voltage.

According to (40) and (41), with the base of $(4I_OV_O)/V_M$, the peak current of main switch S_1 with COT and VOT control is normalized as

$$i^*_{S1\_PK\_COT}(t) = \frac{\pi|\sin(\omega t)|}{2K_2} \tag{42}$$

$$i^*_{S1\_PK\_VOT}(t) = |\sin(\omega t)|(1 + K_1|\sin(\omega t)|) \tag{43}$$

According to (24), (42), and (43), the normalized peak current curve of S_1 of COT and VOT control during half AC line period is depicted in Figure 11. It is indicated that for the same RMS input voltage, compared with COT control, the peak current flowing through S_1 of VOT control is higher when the transient input voltage is close to the peak value, the peak current flowing through S_1 of VOT control is smaller when the transient input voltage is near zero crossing.

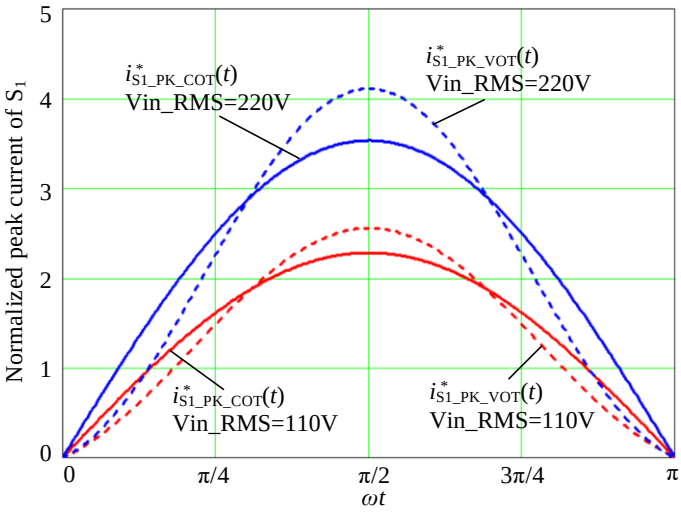


Figure 11. Comparison of the normalized peak current curves of S_1 with COT and VOT control during half line cycle.

4.5. Comparison of RMS Current of Main Switch

According to (1), (2), (5), (7), and (34)–(37), the RMS current of S_1 with COT and VOT control can be obtained as

$$I_{S1\_RMS\_COT} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{\int_0^{T_{on\_COT}} (V_M|\sin(\omega t)|(\frac{1}{L_1}+\frac{1}{L_2})u)^2 du}{T_{S\_COT}(t)}\, d\omega t} = \frac{2I_O V_O}{V_M}\sqrt{\frac{\pi}{3K_2}} \quad (44)$$

$$I_{S1\_RMS\_VOT} = \frac{4V_O I_O}{V_M}\sqrt{\frac{\int_0^{\pi}(1+K_1|\sin(\omega t)|)\sin^2(\omega t)\, d\omega t}{3\pi}} \quad (45)$$

From (44), (45), and the key parameters listed in Table 1 of Section 5, the comparison of RMS currents of the main power switch with COT and VOT control under different RMS input voltages is given in Figure 12. Figure 12 shows that the RMS currents flowing through the main power switch with both control schemes are almost the same.

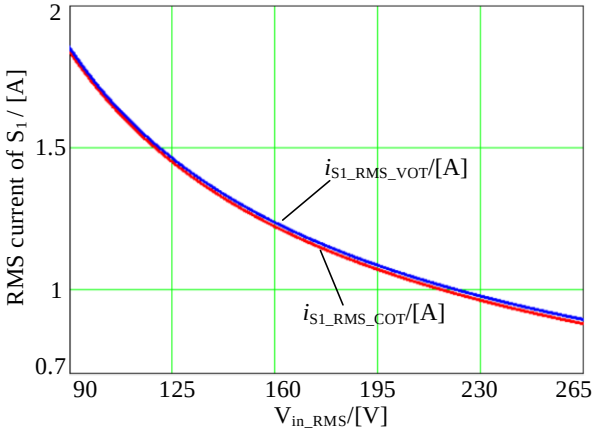


Figure 12. RMS currents of the main switch with VOT and COT control under different RMS input voltage.

As mentioned above, when the instantaneous input voltage approaches the magnitude, the peak current flowing through S_1 of COT control is smaller than that of VOT control, but the switching frequency of COT control is higher than that of VOT control; when the instantaneous input voltage approaches zero crossing point, the switching frequency of VOT control is higher than that of COT control, but the peak current of S_1 of VOT control is smaller than that of COT control. Moreover, the RMS current of S_1 of both control schemes is almost the same. Consequently, the power loss, including conduction loss and switching loss of the main power switch of both COT and VOT control, should be almost the same, and the efficiency of both control schemes should be almost the same.

5. Analysis of Simulation and Experimental Results

5.1. Analysis of Simulation Results

With the use of PSIM software, a simulation environment for power conversion and motor control, a computer simulation model shown in Figure 13 is designed to evaluate whether the VOT control of the SEPIC PFC converter operating at BCM is feasible. The specification and key circuit parameters are shown in Table 1. The differential probes are put at the AC input voltage terminal, and the output load terminal and the current probe are put in a series of AC input sources. After the RUN simulation model with PSIM, as shown in Figure 13, the simulation waveforms of input voltage, input current, and output voltage can be presented in Simview's waveform windows of PSIM.

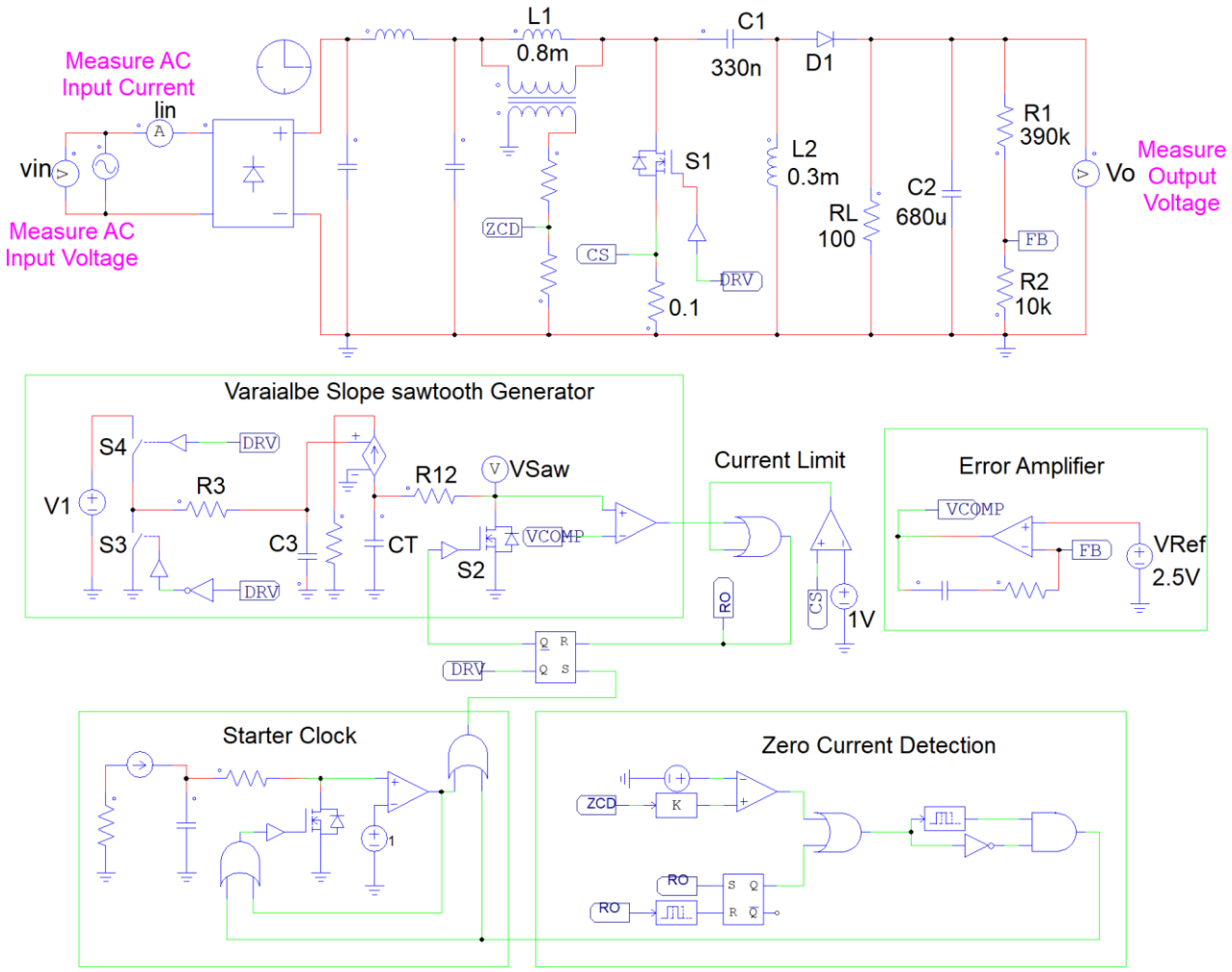


Figure 13. Simulation model of SEPIC PFC converter operating in BCM with VOT control.

Table 1. Key Circuit Parameters.

Key Parameters	VOT and COT
AC Input Voltage Range V_{in_RMS}	90–265 V
Output Voltage V_O	100 V
Line Frequency f_L	50 Hz
Rated Output Current I_O	1 A
Output Filter Capacitor C_O	680 µF
Middle capacitor C_1	1 µF
Inductor L_1	800 µH
Inductor L_2	300 µH
Main switch S_1	FCPF190N60
Freewheeling diode D_1	RHRP1560

Figure 14 gives the simulation waveforms of output voltage, input voltage, and input current at rated load current with 110 Vac and 220 Vac input voltage. As the simulation data indicates, the PF of COT with 110 Vac and 220 Vac is 0.991 and 0.977, respectively, while the PF of VOT with 110 Vac and 220 Vac is 0.999 and 0.995. The THD of COT when operating at 110 Vac and 220 Vac is 13.5% and 19.5%, respectively, while the THD of VOT when operating at 110 Vac and 220 Vac is 2.2% and 4.3%, respectively. The simulation results show that the input current of VOT is closer to the ideal sine-wave than that of COT, the THD of VOT is smaller than COT control, and the output voltage ripple of VOT is just a little larger than that of COT. The simulation results match the theoretical analysis results.

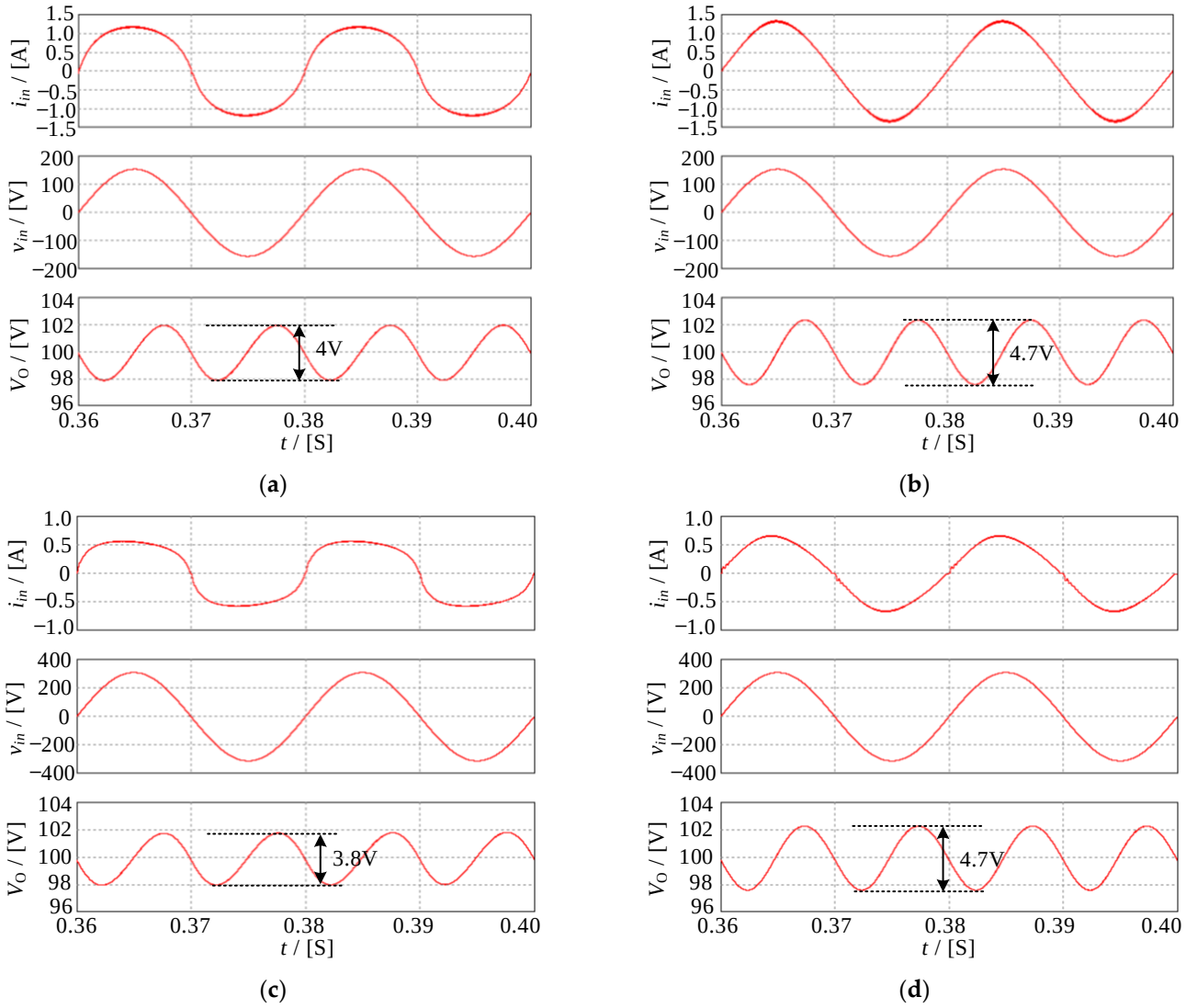


Figure 14. Simulation waveforms at rated load current with 110 Vac and 220 Vac input voltage. (**a**) COT with 110 Vac; (**b**) VOT with 110 Vac; (**c**) COT with 220 Vac; (**d**) VOT with 220 Vac.

5.2. Experimental Results

The experimental verifications of both COT and VOT control methods are performed to prove the feasibility of the suggested VOT control for BCM SEPIC PFC converter and the theoretical performance comparison analysis results of both control schemes. The major parameters and specifications of the experimental board are shown in Table 1. The experimental prototype and platform are shown in Figures 15 and 16, respectively. The block diagram of the experimental platform is presented in Figure 17. In the experimental platform, the programmable AC source Chroma 61602 provides an AC input voltage source to the BCM SEPIC PFC converter, the programmable electronic load Chroma 6314 A and 63,115 A provides the adjustable load for the SEPIC PFC converter, the power analyzer Yokogawa WT1800 measures the PF, THD, input current harmonic, and input power, the digital oscilloscope DPO3014 and its current and voltage probes measure voltage and current waveform of the SEPIC PFC converter, network analyzer Bode100 is used to test the loop stability of the converter.

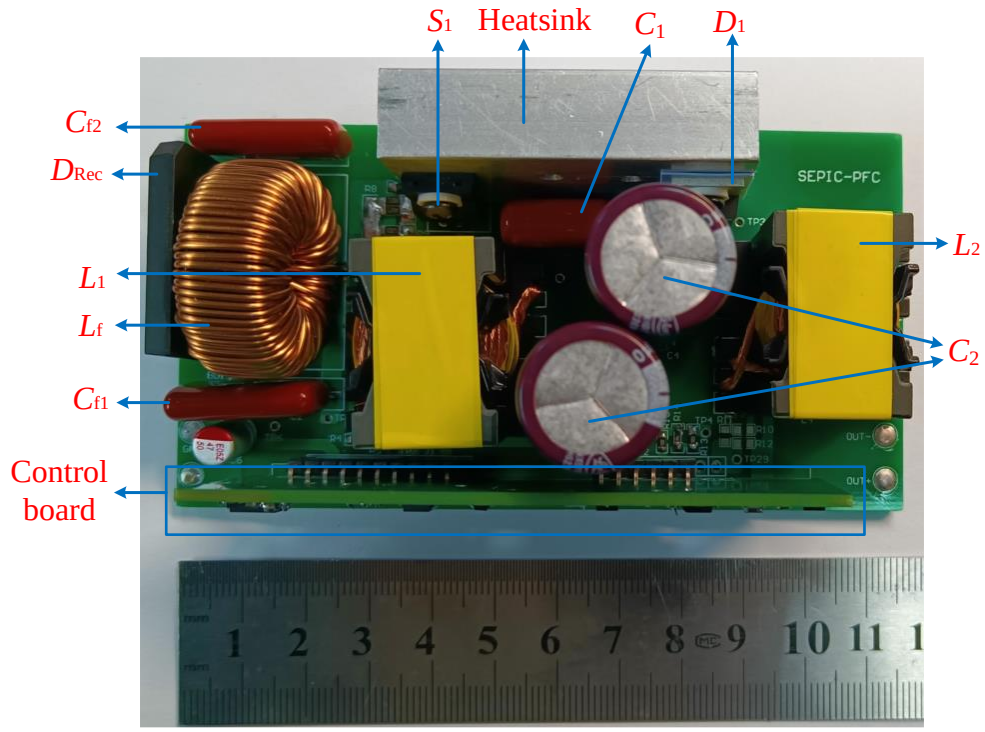


Figure 15. Experimental Prototype.

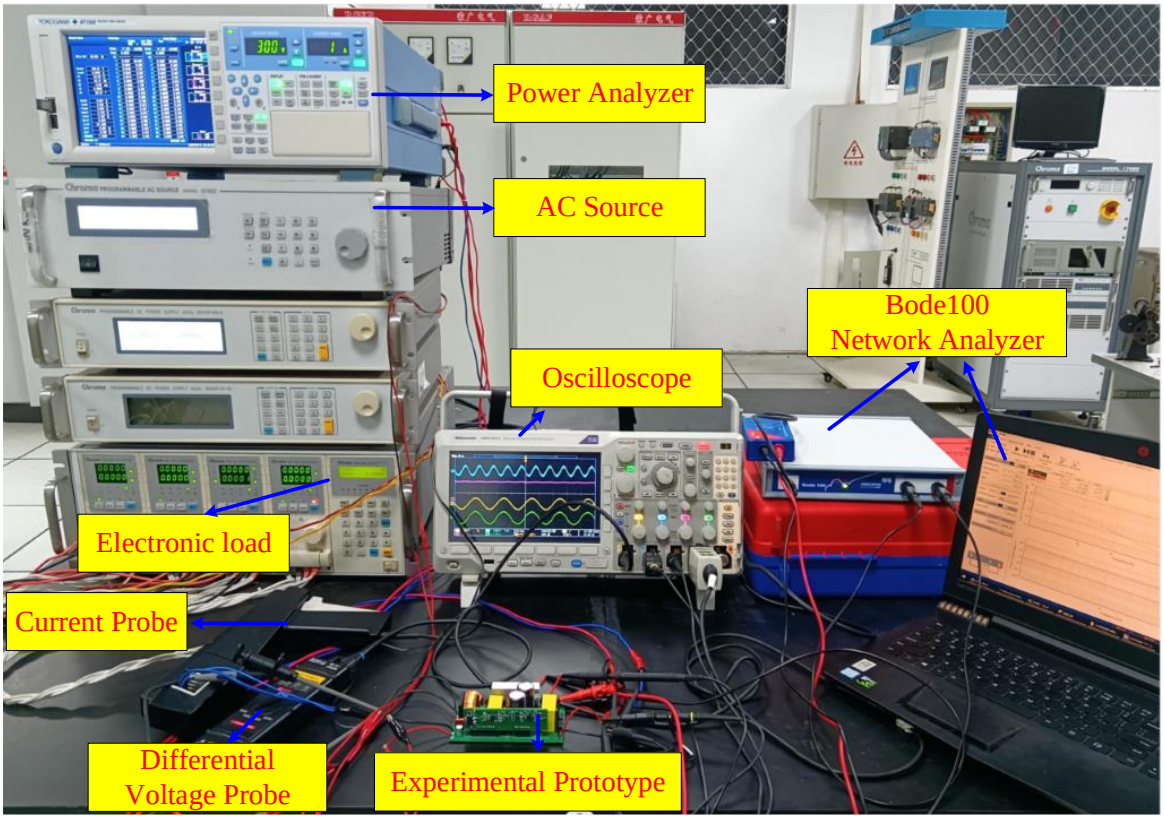


Figure 16. Experimental Platform.

The experimental comparison waveforms, including input current, output voltage with 110 Vac and 220 Vac input voltage and rated load, are shown in Figure 18a–d. The experimental comparison waveforms with 0.1 A and 0.5 A output load and 110 Vac input

voltage are shown in Figure 19a–d. The input current waveforms of VOT control are more sinusoidal and nearly ideal sine-wave when compared to that of COT control, particularly with higher output power. With the rated load current, the output voltage ripple ΔV_O of COT and VOT control with 110 Vac input voltage is 4 V and 4.6 V, respectively, ΔV_O of COT and VOT control with 220 Vac input voltage is 3.8 V and 4.6 V, respectively, ΔV_O of COT control is slightly smaller than that of VOT control, which is the same as the analysis result of Figure 7 and simulation result of Figure 14.

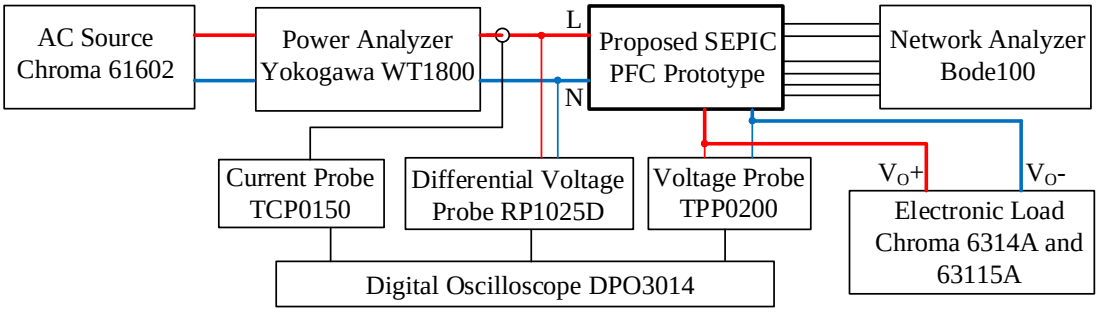


Figure 17. Block diagram of the experimental platform.

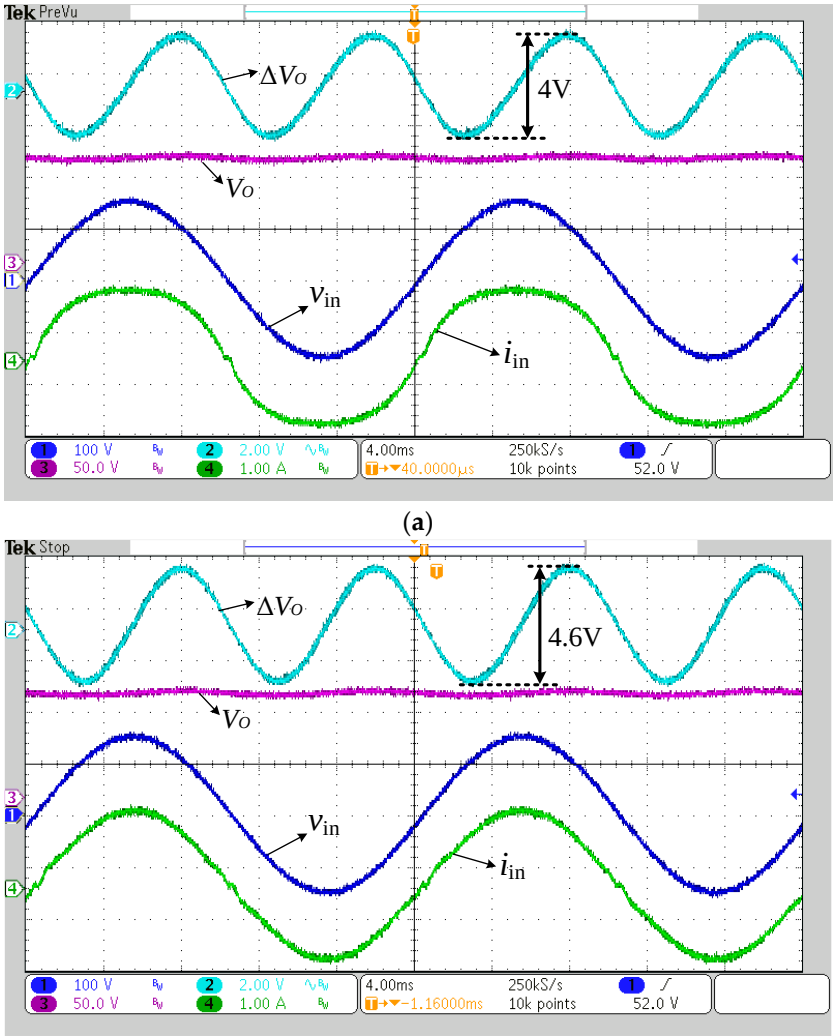
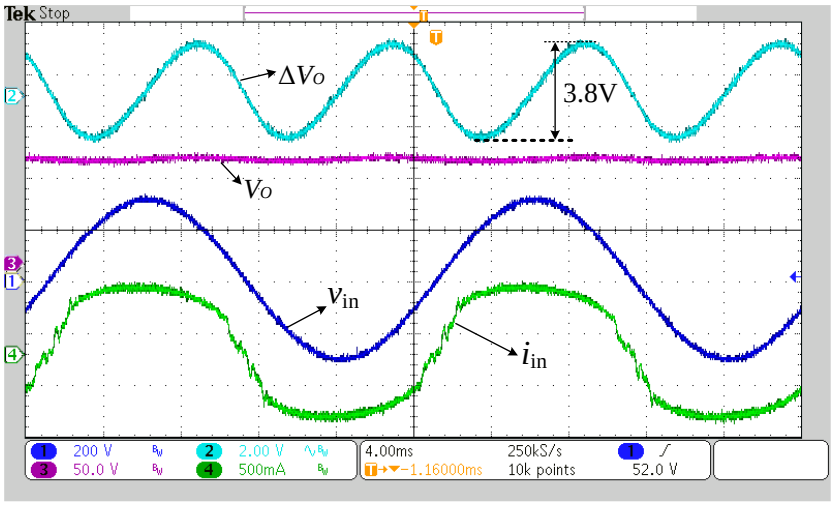
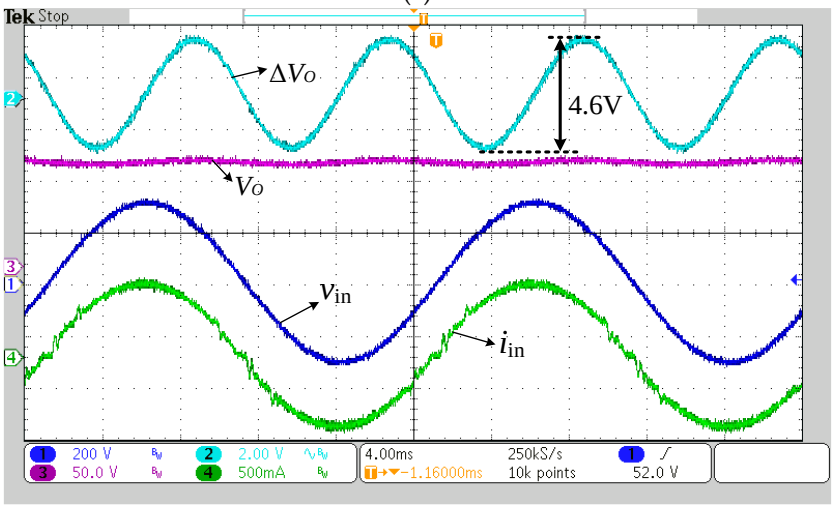


Figure 18. *Cont.*

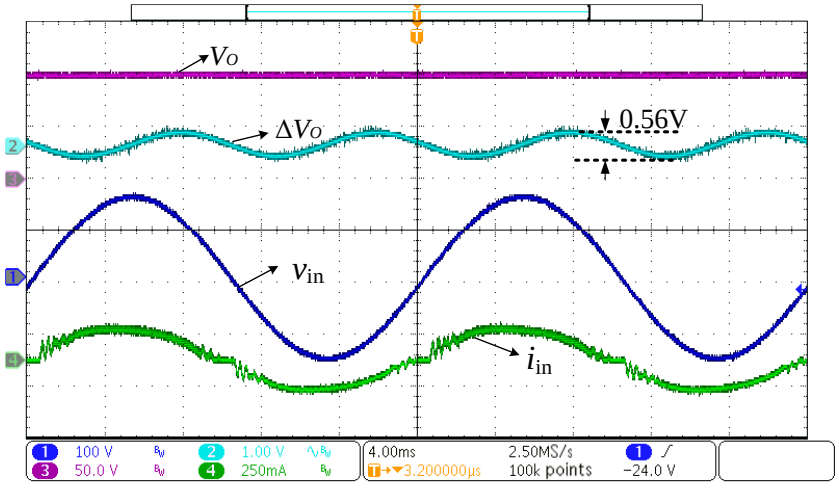


(**c**)



(**d**)

Figure 18. Experimental waveforms of ΔV_O, V_O, v_{in}, and i_{in} with rated output current, 110 Vac and 220 Vac input voltage. (**a**) COT with 110 Vac; (**b**) VOT with 110 Vac; (**c**) COT with 220 Vac; (**d**) VOT with 220 Vac.



(**a**)

Figure 19. *Cont.*

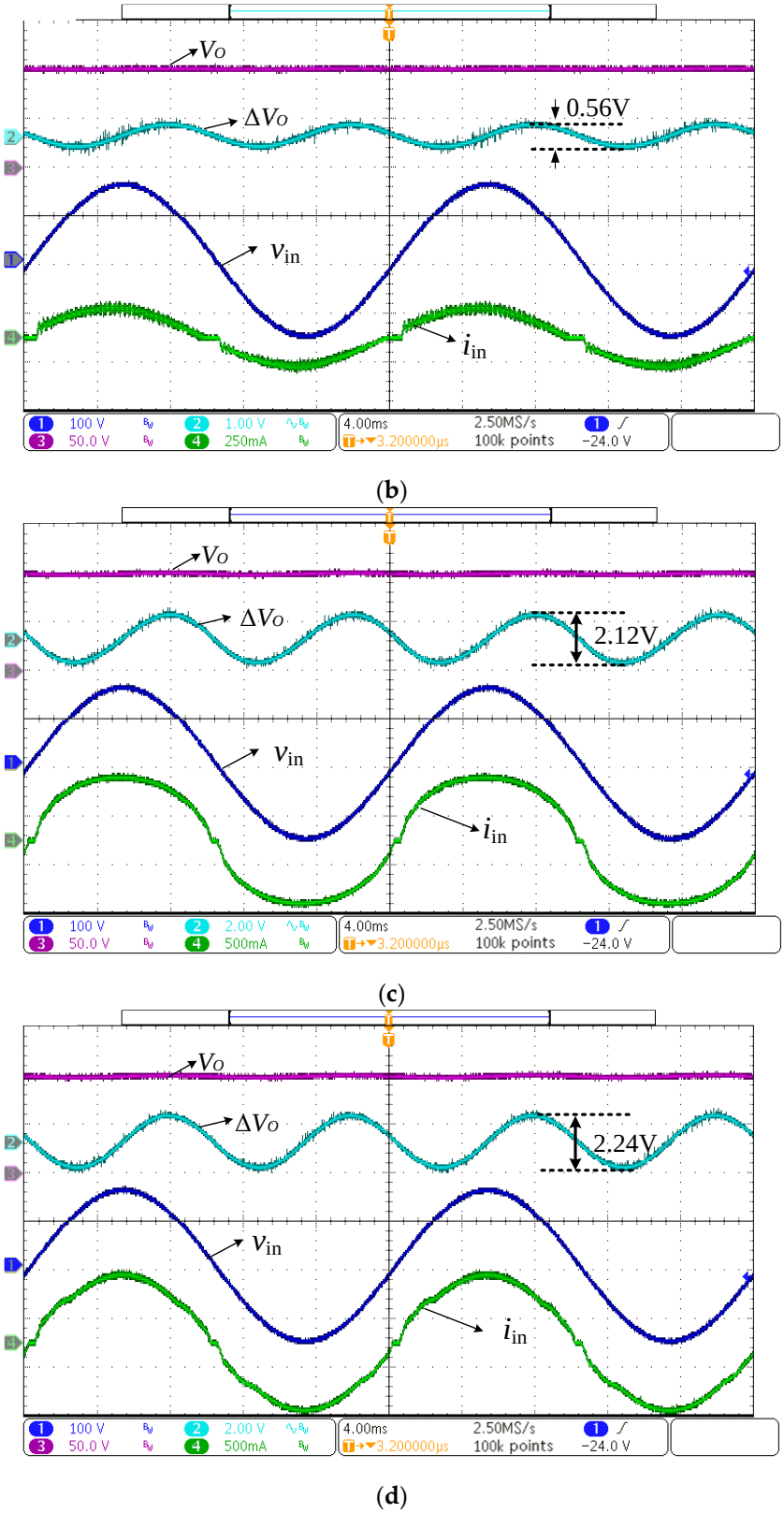
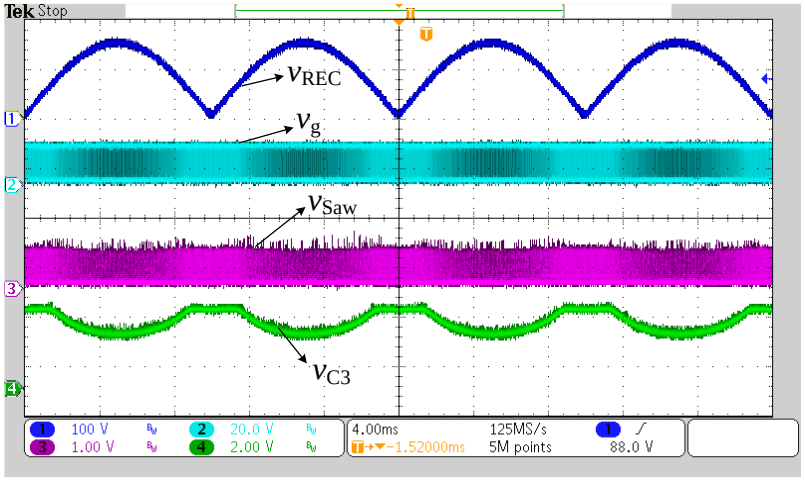


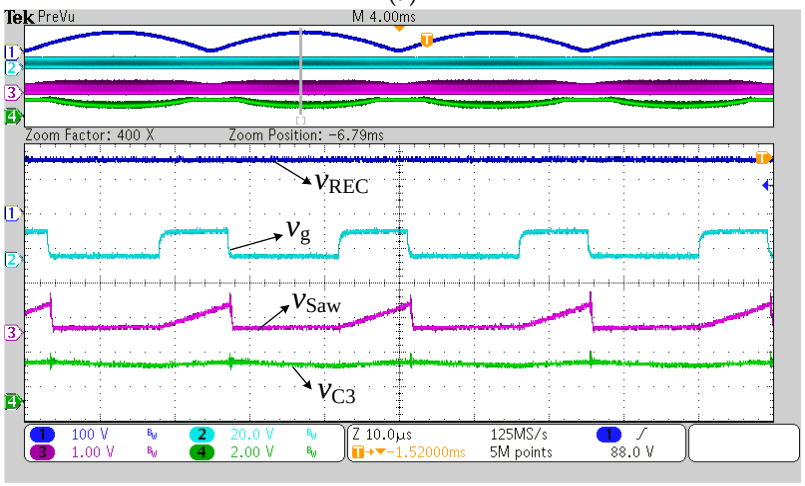
Figure 19. Experimental waveforms of ΔV_O, V_O, v_{in}, and i_{in} with 110 Vac input voltage, 0.1 A and 0.5 A output current. (**a**) COT with 0.1 A output current; (**b**) VOT with 0.5 A output current; (**c**) COT with 0.5 A output current; (**d**) VOT with 0.5 A output current.

Figure 20a–d show the experimental waveforms of the sawtooth waveform v_{Saw}, the control voltage v_{C3} of the VCCS, the rectified input voltage v_{REC}, and gate driver signal v_g

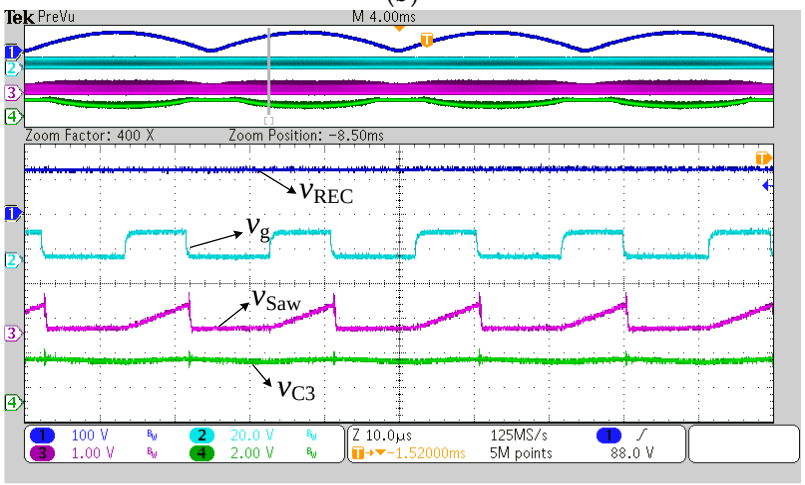
of a main switch for the proposed VOT control with 110 Vac input voltage and rated output current. Figure 20b–d is the zoom-in waveforms of Figure 20a at different transient rectified input voltage. Comparing with Figure 20b–d, it can be known that with the transient rectified input voltage decreasing from peak to valley, the control voltage v_{C3} of the VCCS and the slope of the sawtooth generator increase, the turn-on time of S_1 decreases, which is the same as the analysis result in Figure 4.



(**a**)

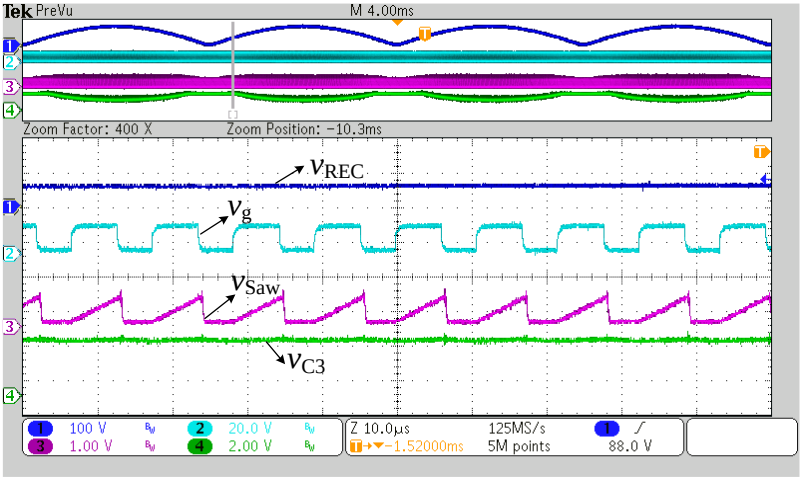


(**b**)



(**c**)

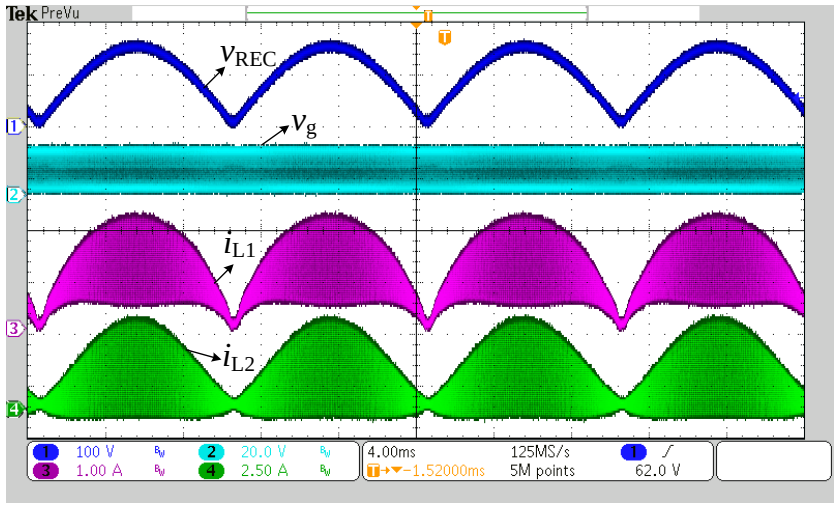
Figure 20. *Cont.*



(**d**)

Figure 20. Experimental waveforms of v_{REC}, v_g, v_{Saw}, and v_{C3} of VOT control with 110 Vac input voltage and rated output current. (**a**) overall waveform; (**b**) zoom in waveform at $\omega t = \pi/2$; (**c**) zoom in waveform at 120 V transient rectified input voltage; (**d**) zoom in waveform near zero-cross point of input voltage.

Figures 21 and 22 show both inductor currents i_{L1} and i_{L2}, the rectified input voltage v_{REC}, and gate driver signal v_g of the main switch of COT and VOT control with 110 Vac input voltage and rated output current. According to Figure 21b,c, it can be shown that the turn-on time of the main power switch S_1 of COT control with different transient rectified input voltage is maintained at 8.8 µS. However, from Figure 22b,c, it can be shown that the turn-on time values of S_1 of the proposed VOT control are 9.6 µS and 6.6 µS near the peak of the transient rectified input voltage and the zero-cross point of the input voltage, respectively. Therefore, it is verified that the turn-on time of S_1 of COT control maintains constant, but the turn-on time of S_1 of VOT control reduces with the transient rectified input voltage decreasing.



(**a**)

Figure 21. *Cont.*

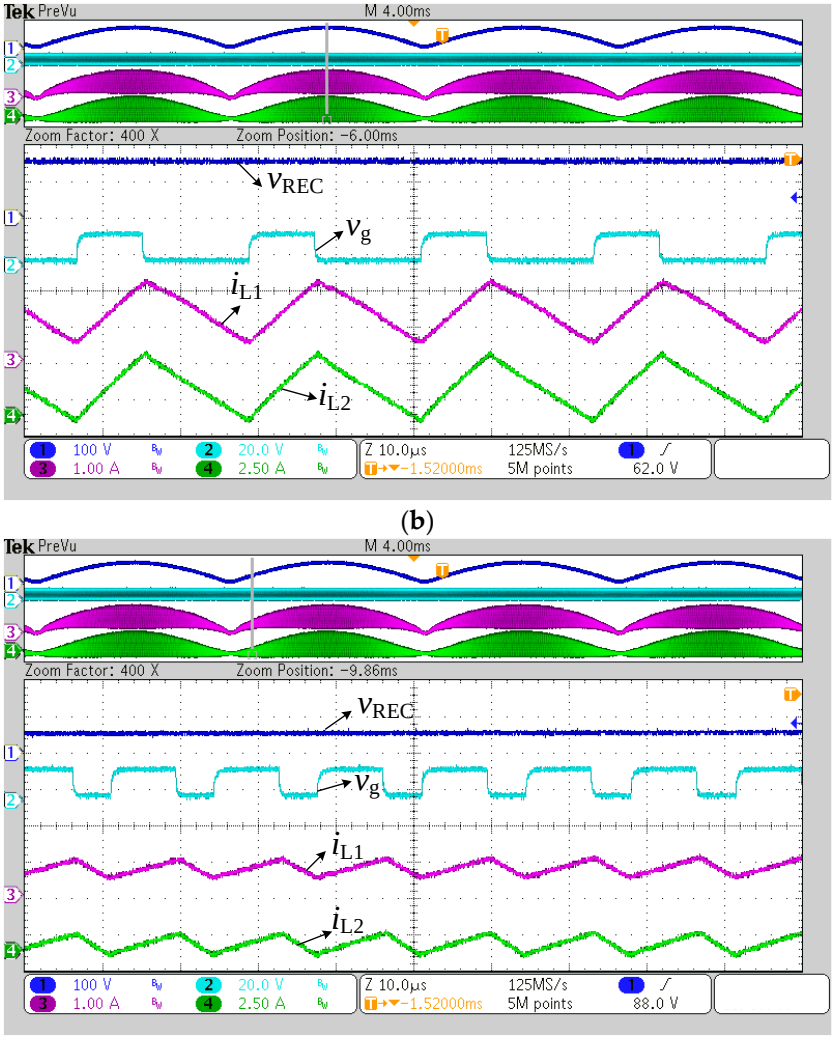


Figure 21. Experimental waveforms of v_{REC}, v_g, i_{L1}, and i_{L2} of COT control with 110 Vac input voltage and rated output current. (**a**) overall waveform; (**b**) zoomed-in waveform at $\omega t = \pi/2$, i.e., v_{Rec} is 155 V; (**c**) zoomed-in waveform around zero-cross point of input voltage, v_{Rec} is 50 V.

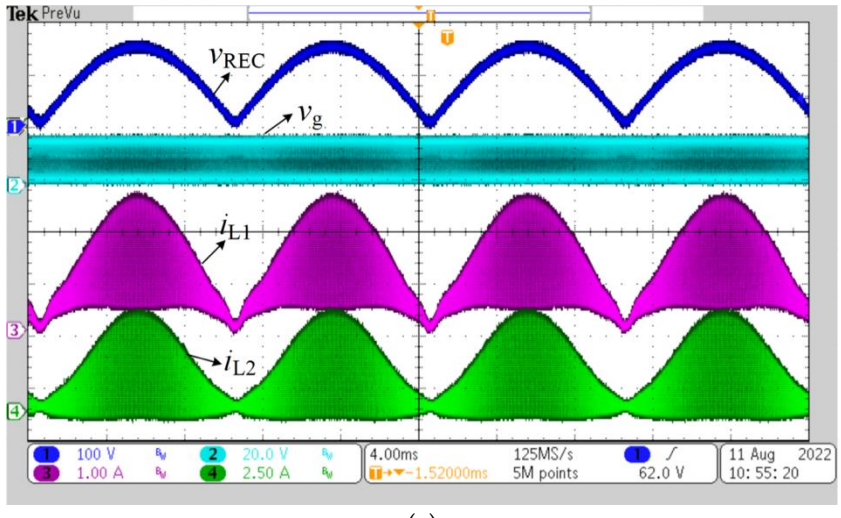
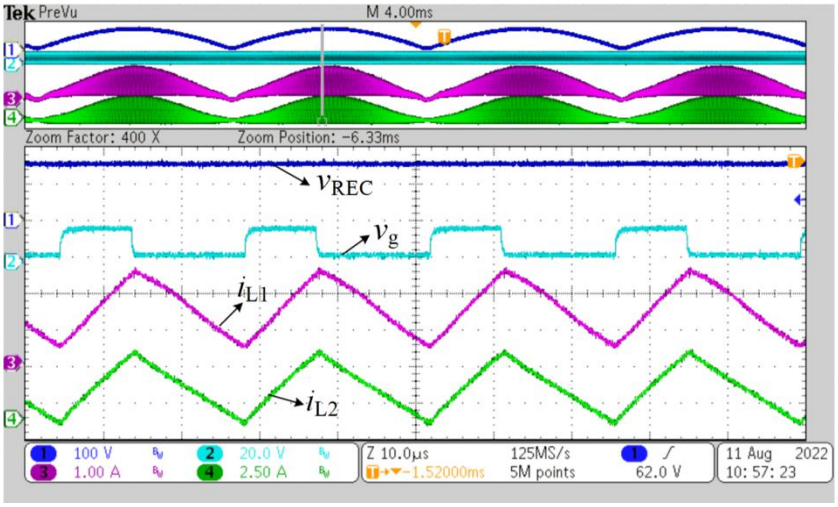
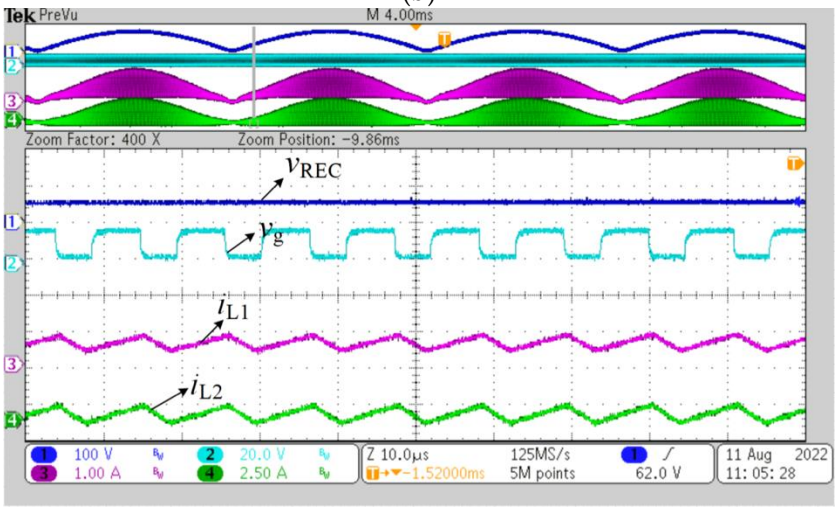


Figure 22. *Cont.*



(**b**)



(**c**)

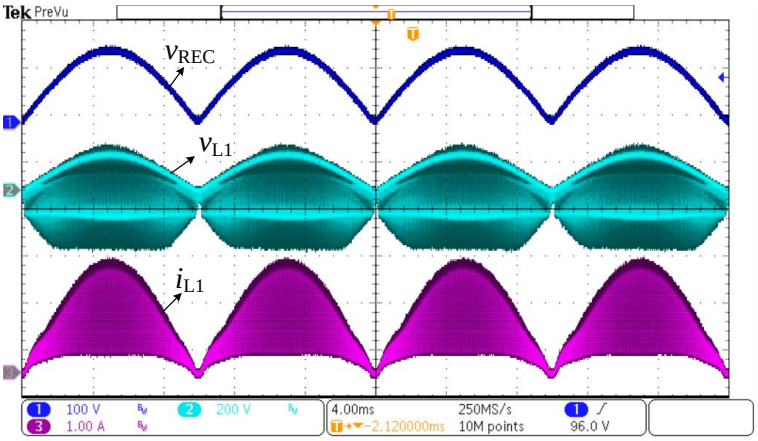
Figure 22. Experimental waveforms of v_{REC}, v_g, i_{L1}, and i_{L2} of VOT control with 110 Vac input voltage and rated current load. (**a**) overall waveform; (**b**) zoomed-in waveform at $\omega t = \pi/2$, i.e., v_{Rec} is 155 V; (**c**) zoomed-in waveform around zero-cross point of input voltage, v_{Rec} is 50 V.

Figures 21b and 22b show that the switching frequencies of COT and VOT control at $\omega t = \pi/2$ are 44.5 kHz and 42 kHz, respectively, almost the same as the analysis result of (35), (37) and Figure 8. Figures 21c and 22c show that the switching frequencies of COT and VOT control with 50 V transient rectified input voltage are 75.2 kHz and 91.7 kHz, respectively. Therefore, compared with COT control, the switching frequency of VOT control is lower when ωt is $\pi/2$, and the switching frequency of VOT control is higher when ωt is near zero, which is the same as the analysis result of Figure 9.

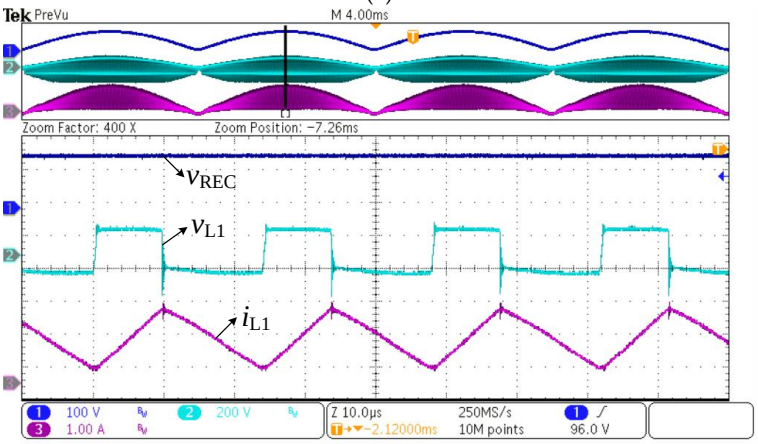
Figures 21b and 22b also show that the maximum peak currents of S_1 of COT and VOT control are 6.4 A and 7.3 A, respectively. Experimental results prove that the maximum peak currents of S_1 of VOT control are slightly bigger than that of COT control, which almost matches the analysis result in Figure 10.

Figure 23 shows the experimental waveforms of the rectified input voltage v_{REC}, L_1 inductor current i_{L1}, and L_1 inductor voltage v_{L1} with VOT control at 110 Vac input voltage and rated output current. Figure 24 shows the experimental waveforms of the rectified input voltage v_{REC}, L_2 inductor current i_{L2}, and L_2 inductor voltage v_{L2} with VOT control at 110 Vac input voltage and rated output current. From Figures 23 and 24, when the rectified input voltage is near 155 V and 50 V, the inductors' L_1 and L_2 voltage is also around 155 V and 50 V, respectively. While S_1 is switched on, the voltage of inductors L_1 and L_2 always

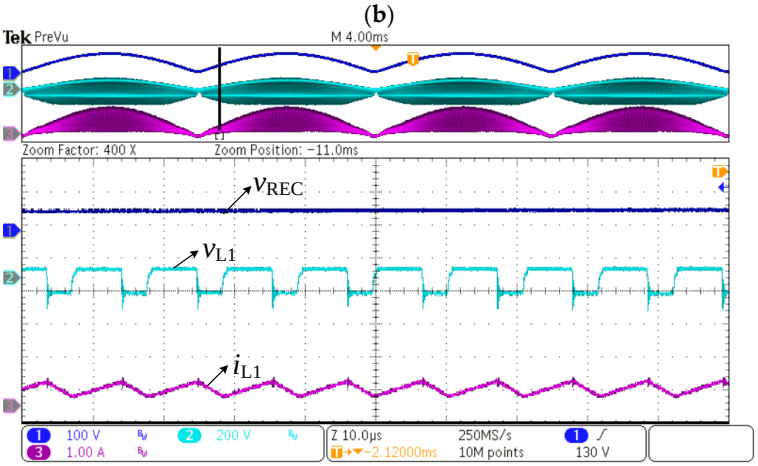
maintain 100 V during S_1 is turned off. Therefore, Figures 23 and 24 can verify that the voltage of both inductors L_1 and L_2 are equal to the rectified input voltage when S_1 is switched on, the voltage of both inductor L_1 and L_2 are equal to output voltage when S_1 is turned off during the whole line period, which is the same as the operation theory analysis.



(**a**)



(**b**)



(**c**)

Figure 23. Experimental waveforms of v_{REC}, v_{L1}, and i_{L1} of VOT control with 110 Vac input voltage and rated current load. (**a**) overall waveform; (**b**) zoomed-in waveform at $\omega t = \pi/2$, i.e., v_{Rec} is 155 V; (**c**) zoomed-in waveform around zero-cross point of input voltage, v_{Rec} is 50 V.

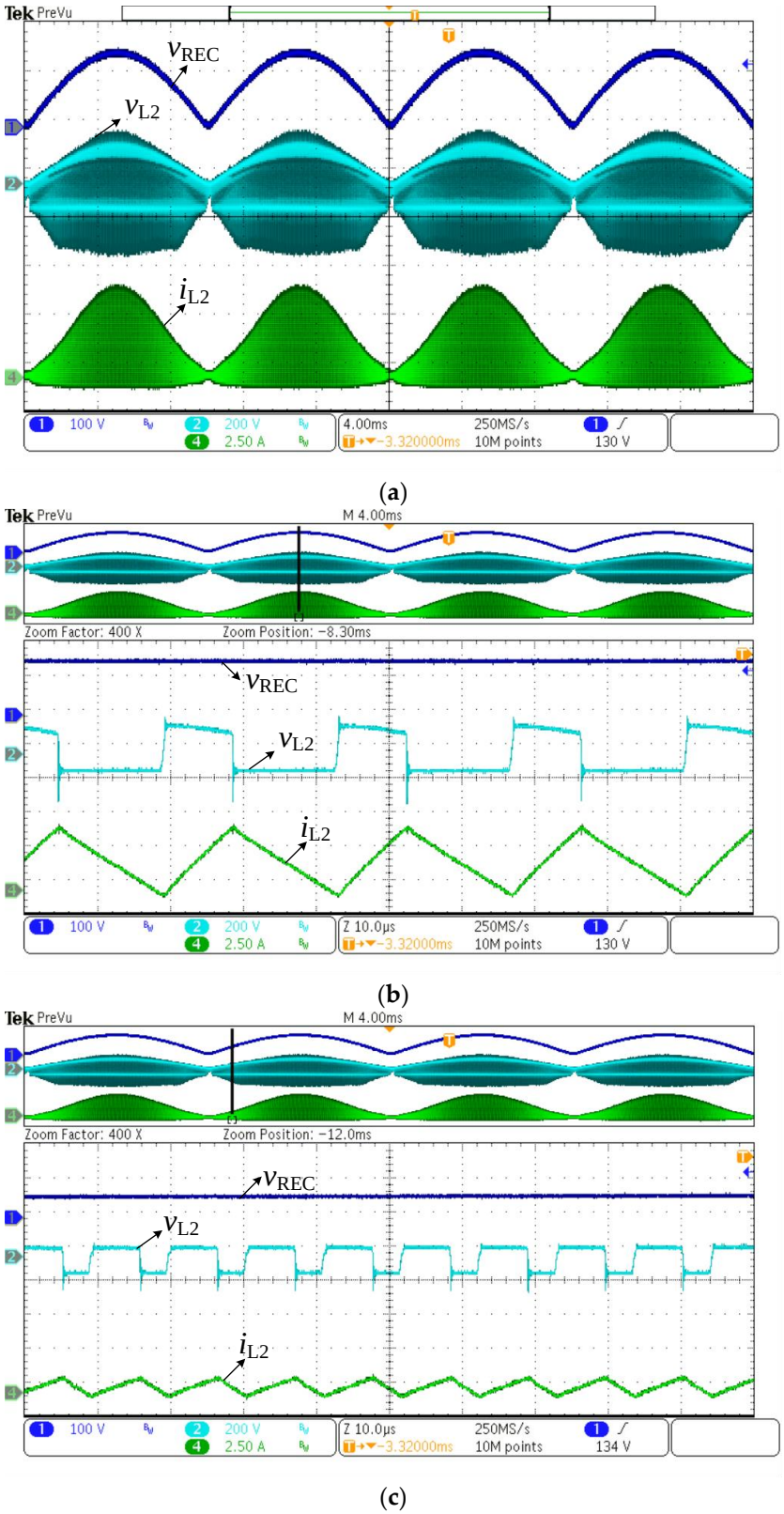


Figure 24. Experimental waveforms of v_{REC}, v_{L2}, and i_{L2} of VOT control with 110 Vac input voltage and rated current load. (**a**) overall waveform; (**b**) zoomed-in waveform at $\omega t = \pi/2$, i.e., v_{Rec} is 155 V; (**c**) zoomed-in waveform around zero-cross point of input voltage, v_{Rec} is 50 V.

The bode diagram of the closed-loop gain of the whole system with the controller can be used to judge the stability of the PFC converter [40,41]. To analyze the stability, the

bode diagram of the closed-loop gain of the SEPIC PFC prototype operating in BCM with VOT control is tested by network analyzer Bode 100. The loop gain test result with 110 Vac input voltage and rated output current load is shown in Figure 25. For the PFC converter, the bandwidth should be lower than 20 Hz. Otherwise, the twice-line frequency 100 Hz output voltage ripple will be coupled into the voltage control loop. As a result, the input current control signal becomes distorted, creating a third harmonic current in the input current [34,37,42]. The phase margin of the power converter should be bigger than 45° to ensure the converter's stability [41–44]. According to Figure 25, it can be observed that the bandwidths, which is the frequency of 0 dB gain magnitude and the phase margin of the whole loop, which is the phase of 0 dB gain magnitude, are 13.26 Hz and around 90° respectively, so the proposed prototype can work stably.

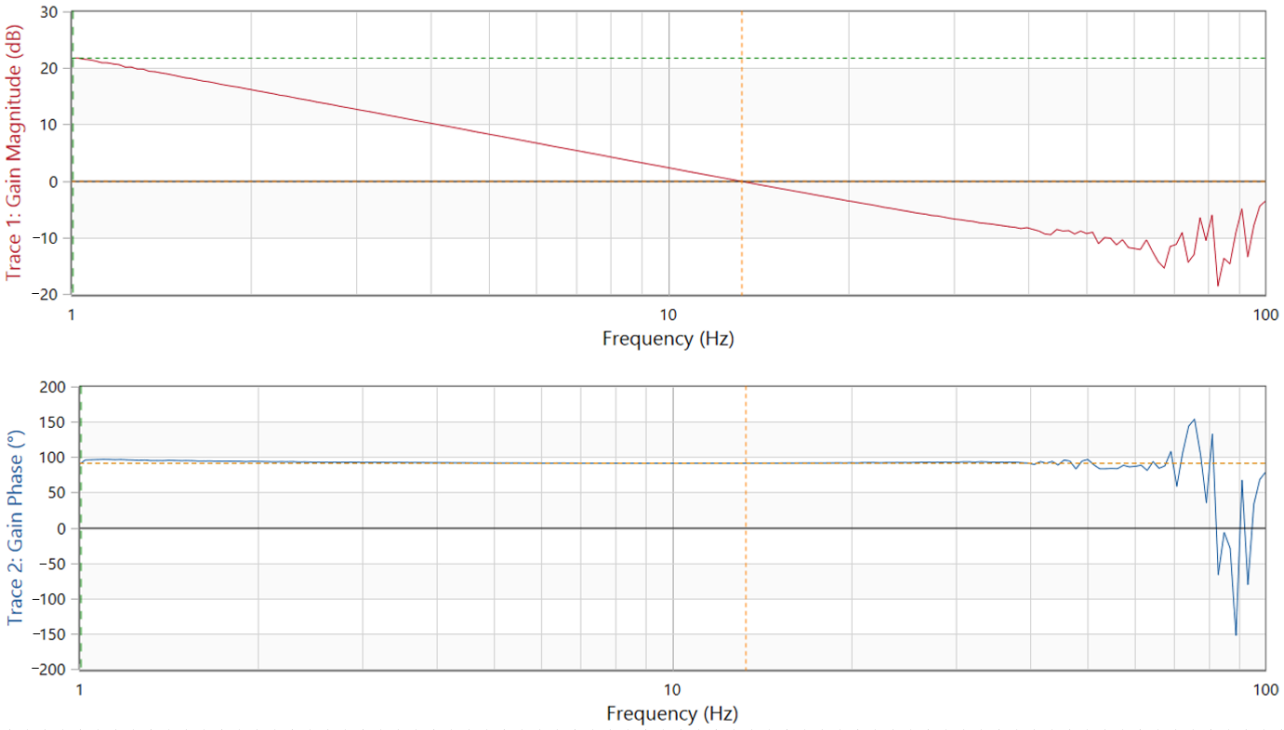


Figure 25. Loop gain test result of VOT control scheme with 110 Vac and rated output current load.

To verify the performance with the variation of different input voltage, the experimental comparison results of efficiency, PF, and THD with COT and VOT control at 90~265 Vac input voltage and rated 1 A output current are presented in Figure 26. To verify the performance with the different load currents, the experimental comparison results of efficiency, PF, and THD of COT and VOT control with 110 Vac input voltage and 0.1~1 A output current are shown in Figure 27. From both figures, it can be shown that the PF of VOT control is higher than that of COT control, THD of VOT control is lower than that of COT control over the entire input voltage range and output load current range. Especially with higher output current load, the proposed VOT control scheme can almost achieve unity PF. From the above experimental data, the PF of the VOT control is enhanced significantly, the THD of the VOT control is reduced remarkably, and the efficiency of both controls is almost the same. Therefore, compared to COT control, VOT control enhances the performance of PF and THD without reducing efficiency.

The comparison results of IEC61000-3-2 Class C requirements and the input current harmonic of both control schemes with a rated output current, 110 Vac and 220 Vac input voltage, are shown in Figure 28. It shows that the input current harmonic of VOT control is lower than that of COT control. Although both control schemes can meet the harmonic

standard limit of IEC61000-3-2 Class C, the VOT control scheme will be easier to meet the applications with stricter input current harmonic requirements.

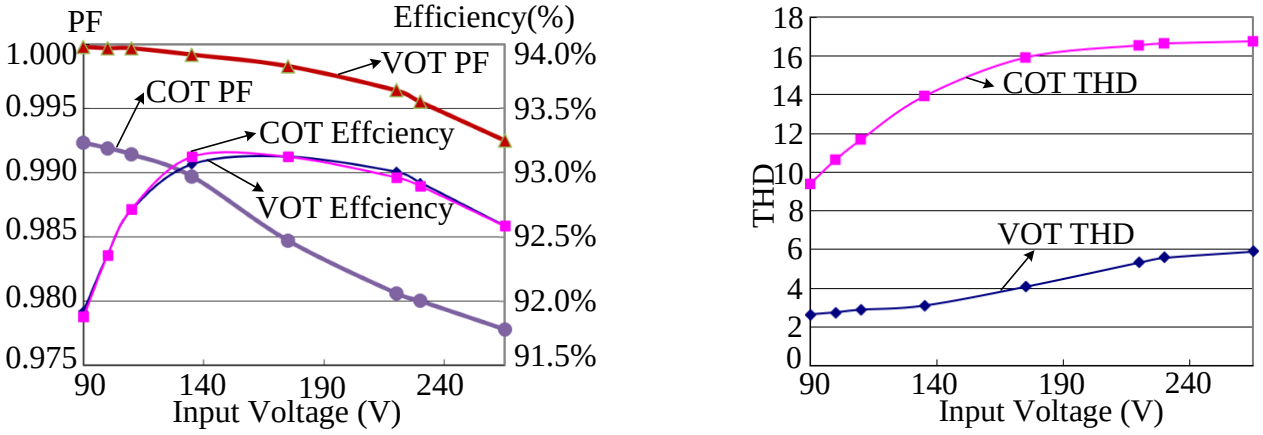


Figure 26. Experimental comparison of PF, Efficiency, and THD data with 90~265 Vac input voltage and rated 1 A output current. (**a**) PF and efficiency; (**b**) THD.

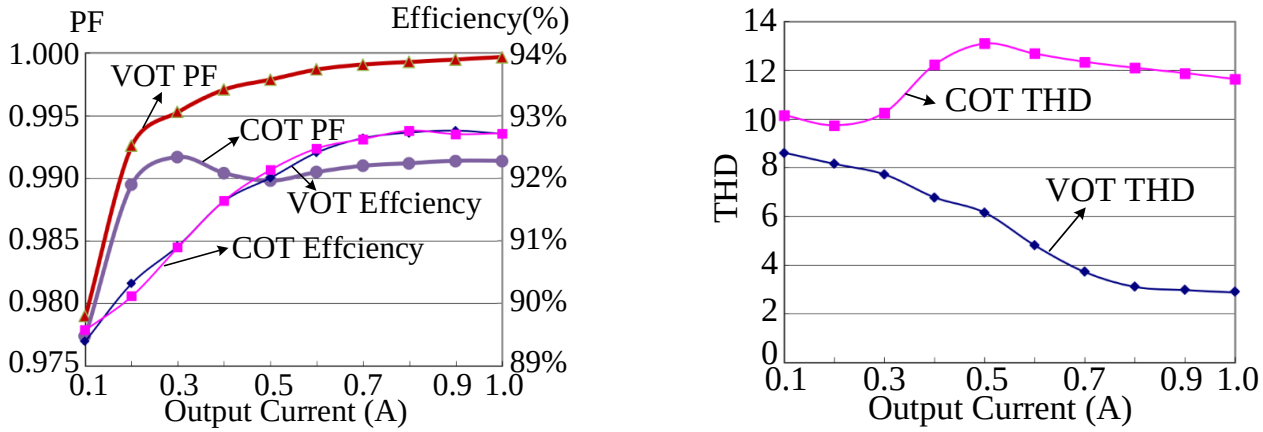


Figure 27. Experimental comparison of PF, Efficiency, and THD data with 0.1~1 A output current and 110 Vac input voltage. (**a**) PF and efficiency; (**b**) THD.

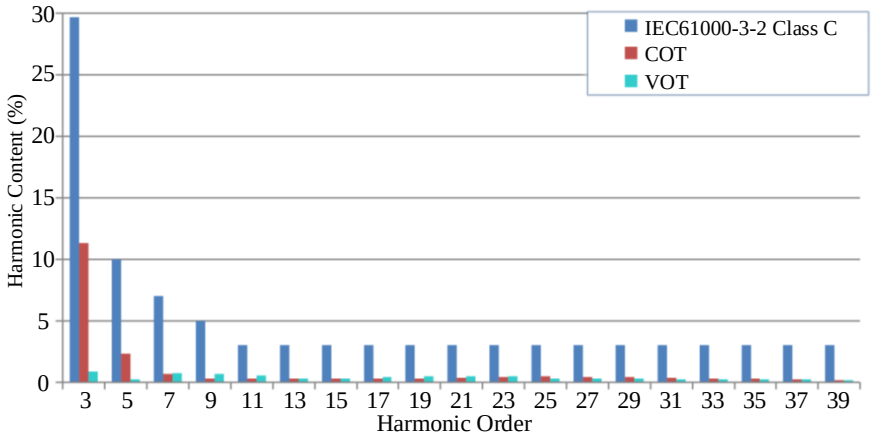
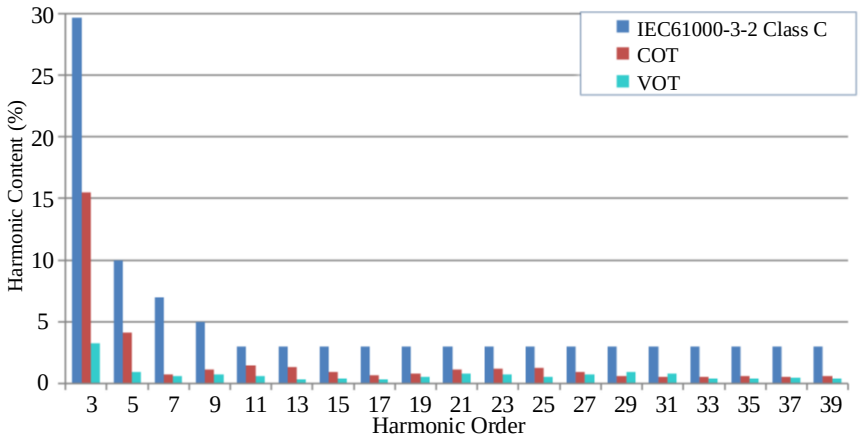


Figure 28. *Cont.*



(**b**)

Figure 28. Input current harmonic content comparison data with rated 1 A output current. (**a**) 110 Vac input voltage; (**b**) 220 Vac input voltage.

6. Conclusions

To enhance the PF and decrease the THD of SEPIC PFC converter operating in BCM, a novel VOT control scheme which can almost realize unity PF is proposed. This novel VOT control scheme doesn't need input voltage feedforward and multiplier circuits required by many PFC control strategies. The proposed VOT control scheme uses a simple and easy-to-implement variable slope sawtooth generator whose slope is controlled by the duty cycle of the main switch to modulate the turn-on time of the main switch. Based on performance analysis, simulation, and experiment comparison results of the 100 W prototype, it is verified that the proposed VOT control scheme with variable slope sawtooth generator remarkably enhances the performance of PF and THD without affecting the efficiency by contrast with the conventional COT control.

Author Contributions: Conceptualization, X.S. and W.C.; methodology, X.S., Q.L. and W.C.; formal analysis, X.S., W.C., Q.L. and Y.W.; validation, X.S., W.C. and Q.L.; investigation, X.S. and W.C.; writing—original draft preparation, X.S.; writing—review and editing, X.S., W.C., Q.L. and Y.W. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

AC	Alternating Current
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
COT	Constant On-Time
DC	Direct Current
DCM	Discontinuous Conduction Mode
PFC	Power Factor Correction
PF	Power Factor
RMS	Root Mean Square
SEPIC	Single Ended Primary Inductor Converter
THD	Total Harmonic Distortion
VOT	Variable On-Time
VCCS	Voltage-Controlled Current Source

Notation

C	Capacitance
$D(t)$	The duty cycle of the main power switch S_1
f_{L}	Line frequency of AC input power source
$f_{\mathrm{S\_COT}}$	Switching frequency of COT control
$f_{\mathrm{S\_VOT}}$	Switching frequency of VOT control
$f^*_{\mathrm{S\_COT}}$	Normalized switching frequency of COT control
$f^*_{\mathrm{S\_VOT}}$	Normalized switching frequency of VOT control
g_1	Control ratio of voltage-controlled current source i_{CHG}
i_{CHG}	Charge current for capacitor C_{T}
i_{D1}	Current flowing through diode D_1
$i_{D1\_AVG\_COT}$	Average current flowing through diode D_1 with COT control
$i_{D1\_PK\_COT}$	Peak current flowing through diode D_1 with COT control
$I^{2nd}_{D1\_COT}$	Input current
i_{in}	The amplitude of second-order harmonic current of D_1 with COT control
$i_{\mathrm{in\_COT}}$	Input current with COT control
$I_{\mathrm{in\_RMS\_COT}}$	RMS value of input current with COT control
$i_{\mathrm{in\_VOT}}$	Input current with VOT control
$i^*_{\mathrm{in\_COT}}$	Normalized input current with COT control
$i^*_{\mathrm{in\_VOT}}$	Normalized input current with VOT control
i_{L1}	Current flowing through inductor L_1
i_{L1_0}	Initial value of i_{L1} when the main switch S_1 starts to turn on
i_{L1_avg}	The average value of the current flowing through L_1
i_{L2}	Current flowing through inductor L_2
i_{L2_0}	Initial value of i_{L2} when the main switch S_1 starts to turn on
I_{O}	Output current of SEPIC PFC converter
i_{S1}	Current flowing through S_1
$i_{S1\_PK\_COT}$	Peak current of S_1 with COT control
$i_{S1\_PK\_VOT}$	Peak current of S_1 with VOT control
$i^*_{S1\_PK\_COT}$	Normalized peak current of S_1 with COT control
$i^*_{S1\_PK\_VOT}$	Normalized peak current of S_1 with VOT control
$I_{S1\_RMS\_COT}$	RMS current of S_1 with COT control
$I_{S1\_RMS\_VOT}$	RMS current of S_1 with VOT control
L	Inductance
PF_{COT}	Power factor with COT control
PF_{VOT}	Power factor with VOT control
$P_{\mathrm{in\_COT}}$	Input power with COT control
R	Resistance
T_{d}	Time of diode D_1 forward bias
$T_{\mathrm{d\_COT}}$	Time of diode D_1 forward bias with COT control
T_{on}	Turn-on time of main power switch S_1
$T_{\mathrm{on\_COT}}$	Turn-on time of S_1 with COT control
$T_{\mathrm{on\_VOT}}$	Turn-on time of S_1 with VOT control
T_{S}	Switching period
$T_{\mathrm{S\_COT}}$	Switching period with COT control
V_1	Voltage source V_1 in variable slope sawtooth generator shown in Figure 4
v_{B}	Voltage of the middle capacitor C_1
V_{comp}	Output voltage of error amplifier
v_{C3}	The voltage of C_3
v_{g}	Driving signal of S_1
v_{in}	Input voltage
V_{M}	Amplitude of AC input power source
V_{O}	Output voltage
v_{REC}	Rectified AC input voltage
v_{Saw}	The voltage of sawtooth generator at the positive input terminal of comparator
Δi_{L1}	Inductor current ripple of L_1
Δi_{L1_COT}	Inductor current ripple of L_1 with COT control
Δi_{L2}	Inductor current ripple of L_2
ΔV_{O}	Output voltage ripple

ΔV_{O_COT}	Output voltage ripple with COT control
ΔV_{O_VOT}	Output voltage ripple with VOT control
ω	Angular frequency of AC input power source

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