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New Fixed-Frequency Digital Control to Improve the Light-Load Efficiency of an Isolated Regulated Converter

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Abstract: With the development of environmental and economic requirements, the light-load efficiency of DC/DC converters is increasingly important. However, many isolated regulated converters still use fixed-frequency control, which has low light-load efficiency. This paper proposes a new digital control method to improve the light-load efficiency under fixed-frequency control. On the one hand, new gate-drive timing control is proposed to achieve the soft-switching of the primary switch. On the other, the software voltage–second balance method realizes the synchronous rectification in the discontinuous conduction mode, which reduces the conduction loss. The diagram and workflow of the proposed control scheme are demonstrated at length. A 100-Watt prototype was designed, and the test results show that synchronous rectification and quasi-zero-voltage-switching are realized in the whole operating range at the light load. The light-load efficiency is 81% to 87%, which improves by 5% to 10% in comparison to the traditional forward converter. The prototype also functions well under the load transient. The proposed control scheme is implemented in one digital controller without additional components, and the circuit is low loss and low cost.

Keywords: discontinuous conduction mode; isolated regulated converters; light-load efficiency; synchronous rectification; soft-switching; voltage–second balance; zero voltage switching

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1. Introduction

A DC/DC isolated-regulated converter (IRC) converts high bus voltage into low DC voltage, isolates the input and output, and supplies power to electrical equipment. IRCs are widely used in various electronic systems, such as in industry, railways, and satellites. With the application of synchronous rectification, planar transformers, and low-loss components, IRC's full-load efficiency has been improved by 10–20% in the past twenty years, which ranges from 87% to 95%. However, many power loads only operate for a short time; thus, light-load efficiency is becoming more critical for power converters [1]. For example, many organizations and programs (such as the U.S. Energy Star, Climate Savers, and 80 Plus) [2,3] require high efficiency over a wide load range.

Variable-frequency control (VFC) [4] is an effective method to improve light-load efficiency, which is adopted in computing and fast-charging equipment. However, it has some disadvantages. (1) Many VFC strategies are patent protected, which means that the circuits are difficult to replace. (2) VFC may result in a slower transient response and larger output voltage ripple. (3) EMC (electromagnetic magnetic compatibility) design is difficult over a wide frequency range. Thus, fixed-frequency PWM (pulse width modulation) control is still widely used in high-reliability fields such as aerospace, the military, railways, and in industry, which leads to low light-load efficiency [5].

The mode hopping (MH) technique [6] means that the converter operates in continuous conduction mode (CCM) under medium to heavy load in synchronous mode, while it operates at the discontinuous conduction mode (DCM) under light load in asynchronous mode. In DCM, the inductor current has low ripple and low root-mean-square value,

the active switch is zero-current switching (ZCS) turn-on, and reverse recovery loss is eliminated. Thus, the converter has low loss and low noise in DCM.

To further reduce conduction loss, synchronous rectification (SR) in DCM has been researched, where synchronous switches operate in a non-complementary manner [7]. There are mainly three control methods. (1) Detecting the drain–source voltage of the freewheeling switch. The switch is disabled when its voltage drops below the threshold voltage [8]. The threshold voltage requires high precision. (2) Detecting the zero current of the inductor current by a ZCD (zero-cross detector) circuit and turning off the freewheeling switch [9–11]. (3) Using the voltage–second balance method [6,12,13]. The freewheeling switch turns off when the inductor current returns to the initial value. However, the above techniques are realized by analog circuits and specific controllers, which are expensive, and difficult to replace, and it is hard to obtain hi-rel products.

Although the active switch is naturally ZCS turn-on under DCM, its parasitic capacitive loss still exists. Thus, ZVS (zero voltage switching) turn-on under DCM has been studied for decades. In the flyback circuit [14,15], a coupled inductor is in series with a resonant capacitor and an auxiliary switch. When the auxiliary switch turns on, the resonant capacitor produces a reverse inductor current. The reverse current discharges the parasitic capacitor, and the primary switch turns on under ZVS. In [16], the ZVS turn-on is realized by turning on the active clamp switch for a short time. In the synchronous buck circuit [17–20], two auxiliary switches are parallel with the inductor. The reverse inductor current is retained when the auxiliary switches turn on, and the active switch is ZVS turn-on. However, the continuous reverse current causes extra conduction loss. The systems in the above papers need additional power components and gate-drive circuits, increasing the cost and circuit area.

In this paper, a new fixed-frequency digital control scheme is implemented to improve the light-load efficiency of IRC. The proposed software voltage–second balance method realizes the synchronous rectification in DCM and reduces the conduction loss. The quasi-ZVS turn-on of the primary switch is realized by new gate-drive timing. In addition, the control mode is digital peak current mode (DPCM). The control scheme is implemented in a digital MCU (micro-controller unit), with low cost and low loss. The circuit has no additional power components and specific integrated circuits (ICs).

Section 2 analyzes the working principle of the synchronous forward converter in DCM, then introduces the voltage–second balance method and operation modes. The control block diagram and its workflow are demonstrated in Section 3, with key parameters designed. Section 4 gives the specifications and parameter selection of the 100-Watt prototype. Section 5 shows the test waveforms and results and compares them with other papers. Finally, Section 6 concludes the work.

2. Working Principles in DCM

2.1. Soft-Switching of the Primary Switch

The forward converter with synchronous rectification is shown in Figure 1a. The magnetizing inductor of the transformer is reset and is resonant with the equivalent resonant capacitor C_S. The gate-drive signals of metal-oxide-semiconductor field-effect transistors (MOSFETs) come from the control circuit. Figure 1b shows that the converter works in CCM at medium and heavy loads. The synchronous rectifiers, SR_1 and SR_2, conduct complementarily; thus, the output current i_{Lo} forms a triangular waveform above zero.

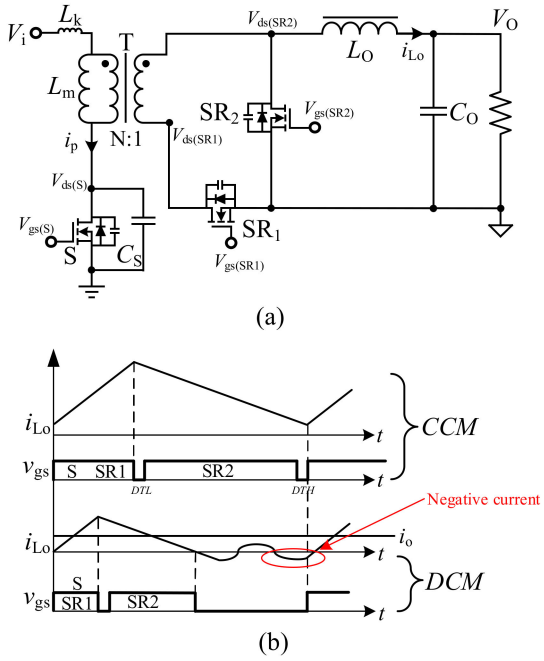

Figure 1. (**a**) Forward circuit with synchronous rectifiers. and (**b**) inductor current and gate-drive signal in continuous conduction mode and discontinuous conduction mode.

In contrast, the converter operates in DCM at light load. SR_2 turns off when i_{Lo} drops to zero, then C_S reflects to the secondary side and resonates with L_O. The resonant current oscillates around zero. If SR_1 turns on when i_{Lo} goes negative, the resonant current reflects to the primary side, and C_S discharges quickly. Thus, the primary switch's voltage drops, preparing for the ZVS turn-on. The resonant frequency's expression is shown in Equation (1), where N is the turns ratio of the transformer and C_r is the parasitic capacitance of the secondary side.

$$f_r = \frac{1}{2\pi\sqrt{\left(\frac{C_S}{N^2} + C_r\right)L_O}} \tag{1}$$

2.2. The Voltage–Second Balance Method

As mentioned above, SR_2 turns off exactly when i_{Lo} drops to zero. The voltage-second (volt-sec) balance method can generate the gate-drive signal of SR_2. In the steady state, the inductor obeys the volt-sec balance principle. That is, the inductor's magnetization and demagnetization energy are equal in one cycle. For the output inductor L_O in Figure 1a, the volt-sec balance is expressed as:

$$(V_{ds(SR2)} - V_O)t_{mag} - V_O t_{dmg} = 0 \tag{2}$$

where the dead time is ignored. In Equation (2), t_{mag} is the magnetizing time, and $t_{mag} = DT_s$, where D is the duty cycle and T_{sw} is the switching period. t_{dmg} is the demagnetizing time, which equals the on-time of the freewheeling switch SR_2. $V_{ds(SR2)} = V_i/N$, which means the input voltage reflects to the secondary side. Substituting the above parameters into Equation (2), we obtain t_{dmg} in Equation (3).

$$t_{dmg} = \left(\frac{V_i}{NV_O} - 1\right)DT_{sw} \tag{3}$$

We derive from Equation (3) that $t_{dmg} = (1 - D)T_{sw}$ in CCM. Thus, SR_1 and SR_2 turn on in a complementary manner. While in DCM, SR_2 turns off when the demagnetization completes, and the inductor current decreases to zero. Thus, the voltage–second balance principle holds both in CCM and DCM.

As stated in the introduction, the analog circuit implementation of the volt-sec balance method has disadvantages. Thus, a software volt-sec balance method is proposed in this paper. From Equations (2) and (3), we can calculate the turn-off time of SR_2, t_{SR2off}.

$$t_{SR2off} \approx t_{mag} + t_{dmg} \approx \frac{V_{ds(SR2)} D T_{sw}}{V_O} \tag{4}$$

If we sample V_O, $V_{ds(SR2)}$, and duty cycle D, t_{SR2off} is calculated by the program. The software implementation method is more flexible and does not require additional hardware components.

2.3. Operation Modes

The operating cycle is divided into five modes, the key waveforms are shown in Figure 2, and the equivalent circuits of each mode are shown in Figure 3.

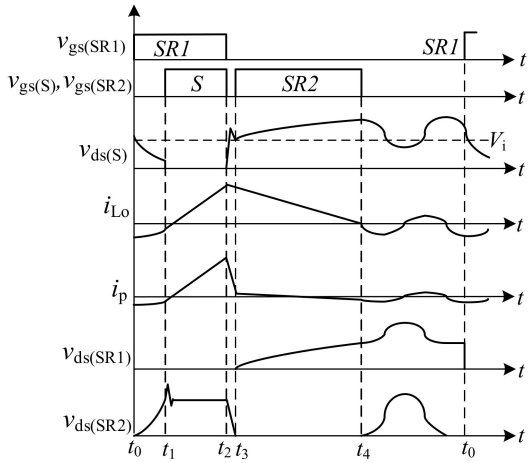

Figure 2. Key voltage and current waveforms of the proposed circuit.

Mode 1 (t_0–t_1): SR_1 turns on at t_0, and the reverse current reflects to the primary side. Magnetizing inductor L_m resonates with reset capacitor C_S, and C_S is discharged. The drain–source voltage of S ($V_{ds(S)}$) drops to a minimum value, providing quasi-ZVS conditions for S. The duration of this mode is t_{ZVS}, which is set by the software.

Mode 2 (t_1–t_2): S turns on under quasi-ZVS at t_1. Inductance L_m and L_O are both magnetizing, which causes the current to rise linearly and reach its peak at t_2. The expressions are shown in Equations (5) and (6). On the secondary side, SR_1 continues conducting, and SR_2 is off. The duration of this mode DT_S, which is the on-time of S.

$$I_p(t) = \frac{V_i}{L_m + L_k} t \tag{5}$$

$$I_{Lo}(t) = \frac{\frac{V_i}{N} - V_O}{L_O} t \tag{6}$$

Mode 3 (t_2–t_3): S and SR_1 turn off at t_2, and the secondary-side current flows through the body diode of SR_1. When $V_{ds(S)}$ rises to input voltage V_i, a voltage spike occurs by the leakage inductance L_k, and SR switches start to commutate. The duration of this mode is

the dead time *DTL*, which is very short. Thus, the inductor current is considered constant. $V_{ds(S)}$ expression is shown in Equation (7).

$$V_{ds(S)}(t) = V_i + \sqrt{\frac{L_k}{C_S}} I_p(t_2) \tag{7}$$

Mode 4 (t_3–t_4): When the SR commutation completes, SR_2 turns on under ZVS. L_m resonates with C_S. L_O demagnetizes, and the current I_{Lo} decrease linearly. I_{Lo} decrease to zero at t_4, and SR_2 turns off by the voltage–second balance logic in MCU. The duration of this mode is shown in Equation (3). The expressions of $V_{ds(S)}$, I_p, and I_{Lo} are shown in Equations (8) and (9).

$$\begin{cases} V_{ds(S)}(t) = V_i + V_{cp}\sin(\omega_1 t) \\ I_p(t) = C_S \omega_1 V_{cp}\cos(\omega_1 t) \\ I_{Lo}(t) = I_{Lo}(t_3) - \frac{V_O}{L_O} t \\ \omega_1 = \frac{1}{\sqrt{C_S L_m}} \end{cases} \tag{8}$$

where

$$V_{cp} = \sqrt{\frac{L_m}{C_S}} \frac{I_{Lm(max)}}{2} \tag{9}$$

Mode 5 (t_4–t_0): All of the power switches are off at t_4, and the output energy is maintained by the output capacitor C_O. C_S reflects to the secondary side and resonates with L_O. The $V_{ds(S)}$ and I_{Lo} expressions of this stage are shown in Equation (10).

$$\begin{cases} V_{ds(S)}(t) = V_i \sin(\omega_2 t + \frac{\pi}{2}) \\ I_{Lo}(t) = NC_S V_i \omega_2 \cos(\omega_2 t + \frac{\pi}{2}) \\ \omega_2 = \dfrac{1}{N\sqrt{C_S L_O}} \end{cases} \tag{10}$$

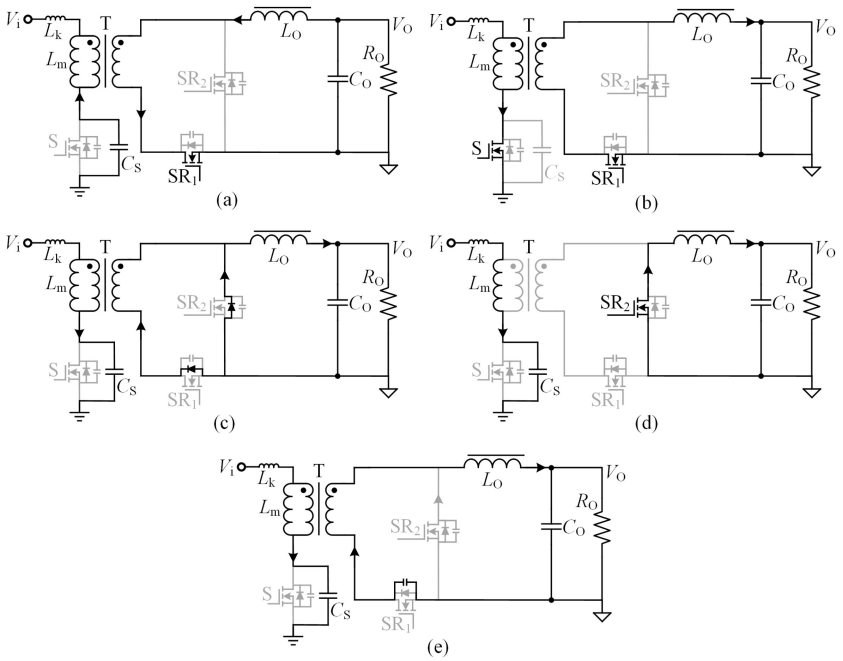

Figure 3. Equivalent circuits of each mode. (**a**) Mode 1 (t_0–t_1); (**b**) mode 2 (t_1–t_2); (**c**) mode 3 (t_2–t_3); (**d**) mode 4 (t_3–t_4); (**e**) mode 5 (t_4–t_0).

3. The Proposed Control Scheme

3.1. Control Diagram in DCM

The functional block diagram of the proposed control scheme is shown in Figure 4, which works in DCM and in steady state. The power stage is an SR forward circuit with the resonant capacitor reset. Because SR is realized under full load, there is no need for parallel Schottky diodes. The control mode is digital peak-current-mode (DPCM), which consists of an MCU, a signal isolator, and three gate drivers. The MCU controller's upper part is the SR timing generate circuit, and the lower part is the DPCM control loop.

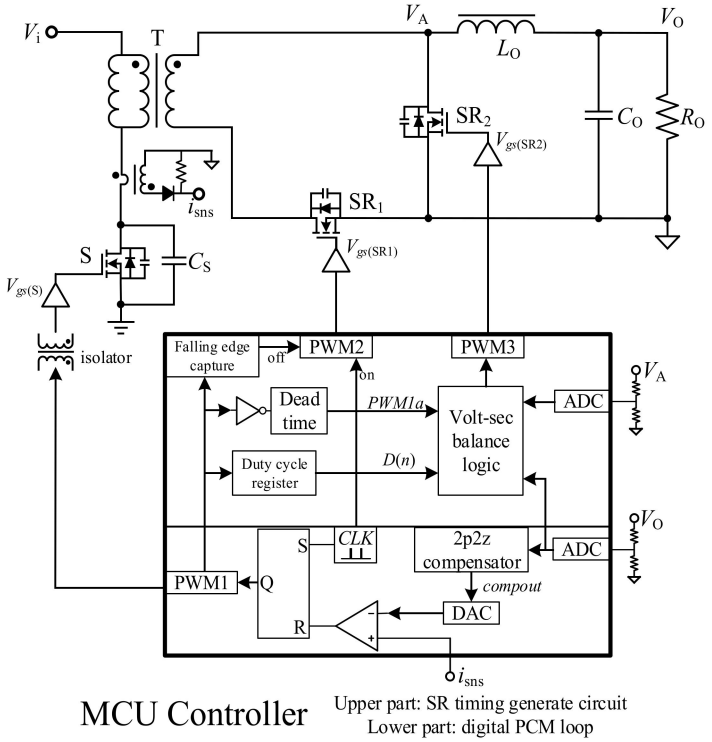

Figure 4. The proposed control diagram in DCM.

The DPCM control loop generates the switching signal of PWM1. After the DTH delay of the system clock pulse, the PWM1 turn-on signal is generated. Then, the controller samples the output voltage and calculates the 2p2z compensator program. The output signal *compout* is converted by DAC and is compared with sampled primary current i_{sns}. Finally, the turn-off signal of PWM1 is generated.

In DCM, PWM2, PWM3, and *PWM4* are enabled. The PWM2 turn-on signal synchronizes with the clock pulse, and its turn-off signal synchronizes with the PWM1 turn-off signal. The complementary signal of PWM1 is generated, and its duty cycle *D*(n) is updated. *PWM1a*, *D*(*n*), and V_A are processed by volt-sec balance logic and generate the PWM3 signal. The detailed workflow will be demonstrated in the next subsection.

3.2. The Principle of Control Flow

The control flow chart in DCM is shown in Figure 5. The program code is on the left, mainly for loop compensation, working mode judgement, and voltage–second balance calculation. The initialize program enables PWM1 and sets dead time values. Then, the system clock pulse triggers the analog to digital converter (ADC) sample and enters the interrupt program. In the interrupt, a two-poles-two-zeros (2p2z) compensator is calculated, and the result is stored in *compout*. Then, the working state of the circuit is judged, and the corresponding configuration is performed. Here, it works in DCM. The program ends after exiting the interrupt program.

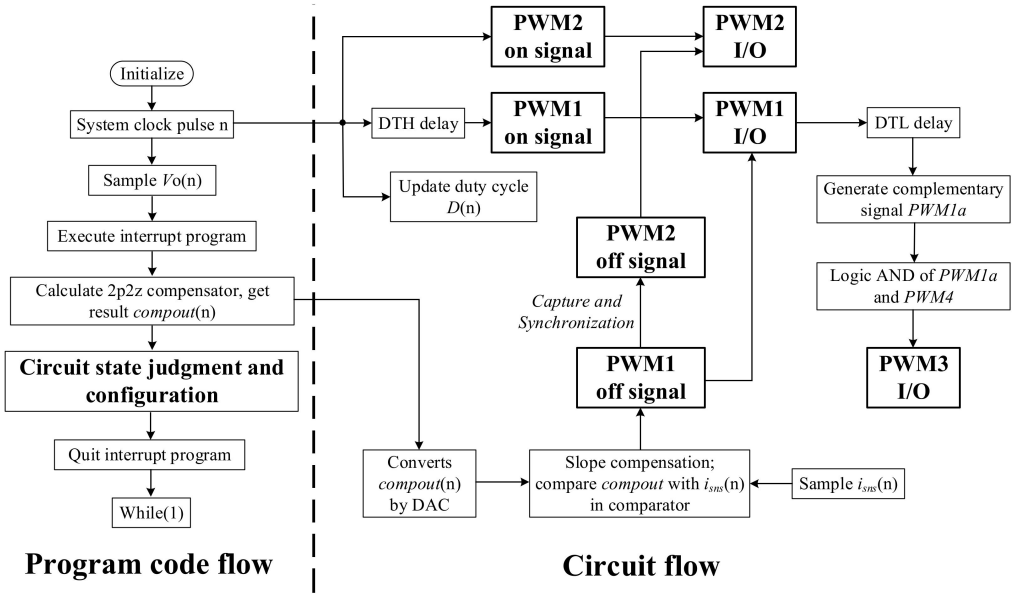

Figure 5. The control flow chart in DCM.

The right part is the circuit flow in MCU. The clock pulse also triggers the PWM2 rising edge and updates the duty cycle; PWM1 goes high after the DTH delay. When quitting the interrupt program, the circuit executes slope compensation and PWM comparison, finally generating the turn-off signal of PWM1. The falling edge of PWM2 is synchronized with PWM1, and outputs to PWM2 input/output (I/O) port. Then, PWM1 generates a complementary signal *PWM1a* after DTL delay. *PWM4* is obtained by voltage–second balance, passes through AND gate with *PWM1a*, and outputs to the PWM2 I/O port.

The program flow of circuit state judgement and configuration is shown in Figure 6. If the output voltage is lower than the nominal value (V_{Oset}), or the variation of *compout* signal over a threshold (ΔV_{comp}), the circuit is considered to operate in a transient state; otherwise, it operates in a steady state. In the transient state, PWM2 and PWM3 are disabled. Thus, SR switches are turned off. If the circuit works in a steady state, further judgement is made by comparing the *compout* signal with the other threshold (V_{th}). The circuit works in CCM if *compout* > V_{th}. PWM2 synchronizes with PWM1 and PWM3 synchronizes with PWM1a. On the other, the circuit works in DCM if *compout* < V_{th}.

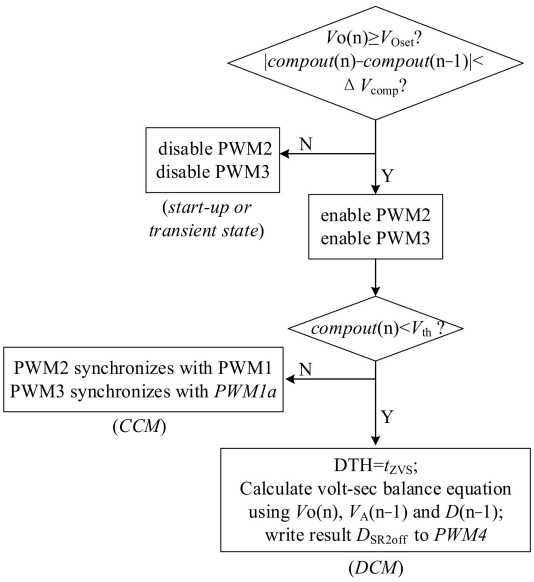

Figure 6. The workflow of circuit state judgement and configuration.

In DCM, the program assigns t_{ZVS} to DTH, performs the volt-sec balance calculation, and finally obtains the turn-off timing of SR2, whose value is stored in variable D_{SR2off}. The expression of D_{SR2off} is:

$$D_{SR2off}(n) = \frac{V_A(n-1) \cdot D(n-1)}{V_O(n)} \tag{11}$$

Then, the program assigns $D_{SR2off}(n)$ to the duty cycle register of *PWM4*. Finally, the hardware circuit performs the AND logic of *PWM1a* and *PWM4*, which generates the PWM3 signal. The timing sequence and relationship of PWM signals are drawn in Figure 7.

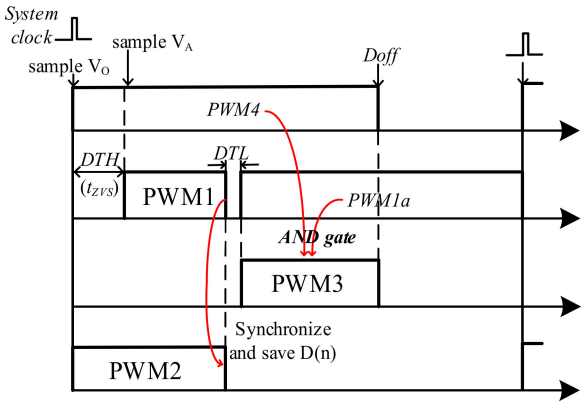

Figure 7. The waveform and generation of PWM signals.

3.3. Design Considerations

3.3.1. Dead Time in DCM

In operation Mode 1 (t_0–t_1), the initial values of the drain–source voltage of S, $V_{ds((t0)}$, and the primary-side current $I_{p(t0)}$ are related to the load current and dead-time. The dead-time DTH value is t_{ZVS} in DCM, which should be carefully designed to realize soft switching. If t_{ZVS} is too large, the positive current at the secondary side will reflect to the primary side, and $V_{ds(S)}$ will increase. If t_{ZVS} is too small, the negative current energy transferred to the primary side will be small, and ZVS will not be realized. t_{ZVS} should not exceed half of the resonant period in Mode 5, whose expression is Equation (1). Here, we set t_{ZVS} as 2/3 of the half resonant period; see Equation (12).

$$t_{ZVS} = \frac{2\pi}{3}\sqrt{(\frac{C_S}{N^2} + C_r\, L_O} \tag{12}$$

According to energy conservation law, the relationship between $V_{ds(S)}$ and I_p in Mode 1 is:

$$\frac{1}{2}C_S{V_{ds(t0)}}^2 - \frac{1}{2}C_S{V_{ds(t1)}}^2 = \frac{1}{2}L_m{I_{Lm(t0)}}^2 - \frac{1}{2}L_m{I_{Lm(t1)}}^2 \tag{13}$$

$$V_{ds(t1)} = \sqrt{{V_{ds(t0)}}^2 - \frac{L_m}{C_S}{I_{Lm(t0)}}^2 + \frac{L_m}{C_S}{I_{Lm(t1)}}^2} \tag{14}$$

where

$$\begin{aligned} I_{Lm(t1)} &\approx 0 \\ I_{Lm(t0)} &= NV_{in}\sqrt{\frac{C_S+N^2C_r}{L_O}} \end{aligned} \tag{15}$$

The $V_{ds(t1)}$ value should be as low as possible to realize the ZVS turn-on.

3.3.2. The Voltage Threshold of the Compout Signal

In DPCM control, the PWM waveform is generated by comparing *compout* and i_{sns}. Thus, *compout* is proportional to the peak primary current I_{pp} and the load current I_{O}. This way, *compout* can judge whether the circuit is working in CCM or DCM. The relationship between *compout* and I_{pp} is:

$$V_{compout} = I_{\mathrm{pp}} \frac{R_{\mathrm{S}}}{\mathrm{N_S}} \tag{16}$$

$\mathrm{N_S}$ is the turns ratio of the current sample transformer, and R_{S} is the sampling resistor. In forward topology, the relationship between I_{pp} and I_{O} is:

$$\begin{aligned} I_{\mathrm{pp}} &= \tfrac{I_{\mathrm{O}}}{\mathrm{N}} + \Delta i_{\mathrm{pp}} \\ \Delta i_{\mathrm{pp}} &= \tfrac{D\mathrm{T_{sw}}}{2}[\tfrac{V_{\mathrm{i}}}{L_{\mathrm{m}}} + \tfrac{V_{\mathrm{i}} - \mathrm{N}V_{\mathrm{O}}}{L_{\mathrm{O}}}] \end{aligned} \tag{17}$$

The expression of CCM/DCM boundary load current I_{OB} is:

$$I_{\mathrm{OB}} = \frac{(V_{\mathrm{i}} - \mathrm{N}V_{\mathrm{O}})D\mathrm{T_{sw}}}{2L_{\mathrm{O}}} \tag{18}$$

Consider Equations (16) and (17) simultaneously. When the load current equals I_{OB}, the *compout* threshold voltage V_{th} is obtained, whose expression is:

$$V_{\mathrm{th}} = \frac{R_{\mathrm{S}} D_{\min} T_{\mathrm{sw}}}{2\mathrm{N_S}} [\frac{V_{\mathrm{i(max)}}}{L_{\mathrm{m}}} + \frac{V_{\mathrm{i(max)}} - \mathrm{N}V_{\mathrm{O}}}{L_{\mathrm{O}}} \cdot \frac{\mathrm{N}+1}{\mathrm{N}}] \tag{19}$$

3.3.3. The Voltage Threshold of the Compout Variation Rate

In the start-up or transient state, the load current changes quickly, and so it is the *compout* signal. Comparing the difference between the *compout* value with the previous cycle, when it is greater than ΔV_{comp}, the circuit operates in a transient state. Suppose the transient load current slope is $x\mathrm{A}/\mu\mathrm{s}$. We assume ΔV_{comp} is 50% of the transient load slope. The ΔV_{comp} expression is:

$$\Delta V_{\mathrm{comp}} = \frac{0.5x \cdot \mathrm{T_{sw}} \cdot R_S}{\mathrm{N} \cdot \mathrm{N}_S} \tag{20}$$

3.3.4. Controller Selection and Comparison

The program occupies 6.7 kB of the MCU memory, and the data occupy 1.03 kB. We used 16-bit MCU dsPIC33CK32MP502. Its memory size is 32 kB, central processing unit (CPU) frequency is 100 MHz, and it has four PWM outputs. We compared dsPIC33CK32MP502 with other forward SR controllers in Table 1. This controller has a comparable price with old controllers and is much cheaper than the latest controllers.

Table 1. Comparison with other SR forward controllers.

Controller Type (Company)	Price (Source: DigiKey)	Released Year	Description
dsPIC33CK32MP502 (Microchip)	US$3.4	2018	Twenty-Eight-Pin Digital Signal Controllers with High-Resolution PWM
LTC3726 (ADI)	US$5.8	2008	Secondary-Side Synchronous Forward Controller
LTC3766 (ADI)	US$11	2016	High Efficiency Secondary-Side Synchronous Forward Controller
SC4910A (Semtech)	US$2.5	2005	Current-Mode PWM Controller with Complementary Output

4. Circuit Design

To verify the above theories, we designed an SR forward converter with DPCM, whose key parameters are shown in Table 2. The 28 V bus voltage is widely used in the military, in satellites, and in industrial applications, while 15 V is the input voltage of various loads, such as airborne computers, industrial computers, and cameras.

Table 2. Key parameters of the prototype.

Parameters	Value
Input voltage (V_i)	20 V to 36 V (28 V typical)
Output voltage (V_O)	15 V
Maximum output power (P_O)	100 W
Switching frequency (f_s)	350 kHz
Transformer turns ratio (N)	3:5
Output inductance (L_O)	12 µH
Magnetizing inductance (L_m)	33 µH
Output capacitance (C_O)	110 µF
Transformer leakage inductance (L_k)	0.1 µH
Current transformer turns ratio (N_S)	100:1
Sampling resistor (R_S)	22 Ω

4.1. Hardware Parameters

Based on Equation (18), the CCM/DCM boundary current I_{OB} at the minimum input voltage (20 V) is 0.8 A; at the typical input (28 V), it is 1 A; at the maximum input (36 V), it is 1.15 A.

$V_{ds(S)}$ should drop to V_i to reset the transformer before the next period. Thus, half of the resonant reset period should be smaller than the minimum reset time, which is expressed in (21).

$$\pi\sqrt{C_S L_m} < (1 - D_{max})T_{sw} \tag{21}$$

By substituting known parameters into (23), we obtain Cs < 3nF. From Equation (14), $V_{ds(t1)}$ should be as small as possible, and C_S should be large to realize soft switching. Here, we set C_S = 2.2 nF.

The primary switch's maximum voltage may occur at the turn-off spikes or the resonant reset peak. Spike voltage can be calculated by Equation (7). At max input and full load, we derive that the max peak primary current is 12 A, and the max voltage spike is 116 V. Equations (8) and (9) show that the max peak reset voltage is 60 V at maximum input. Therefore, the switch stress is 12 A/116 V. Based on a 70% derating design, we choose a 30 A/150 V MOSFET as the primary switch. Ten A/One hundred V MOSFETs were chosen as synchronous rectifiers.

It is worth noting that the prototype is oriented to high-reliability applications such as ground systems, railways, and avionics. Thus, high-reliability components are selected, that is, components that have been screened for reliability.

4.2. Software Parameters

By substituting parameters and calculating Equation (12), we obtain $t_{ZVS} \approx 420$ ns, where $C_r \approx 2$ nF. Here, we set t_{ZVS} = 400 ns. Substituting $V_{ds(t0)}$ = 28 V into Equation (14), we obtain $V_{ds(t1)} \approx 5$ V. Thus, quasi-ZVS turn-on is realized.

DTL is the dead time between the falling edge of S and the rising edge of SR_2. *DTL* should be as small as possible to minimize the body diode conducting time. In the worst case, the maximum turn-off time of S is about 30 ns, the maximum turn-on time of SR_2 is about 20 ns, and the typical delay of the isolator and gate driver is 20 ns. Here, we set *DTL* equal to 100 ns.

The slope of the transient response is x = 0.6 A/µs. Substituting known parameters into Equations (19) and (20), we calculate $V_{th} \approx 0.502$ V and $\Delta V_{comp} \approx 0.314$ V, where V_{Oset} = 15 V.

4.3. Power Loss, Ripple, and Regulation Estimation

With the synchronous rectification and quasi-ZVS turn-on under DCM, the prototype has low conduction loss and low switching loss. However, the traditional forward circuit still uses hard-switching and Schottky rectification. The estimated light-load power loss comparison between the proposed and the traditional circuit is shown in Figure 8, under 0.5 A load and 28 V input. The hard-switching loss is high; the primary switch loss is reduced by 82% when soft switching is realized. The secondary conduction loss reduces with SR, but the gate-drive loss is introduced; thus, the rectifier switch loss is reduced by 20%. The control board loss slightly increases because of the additional gate-drive signals. To sum up, the light-load efficiency increased by 10% using the proposed control scheme.

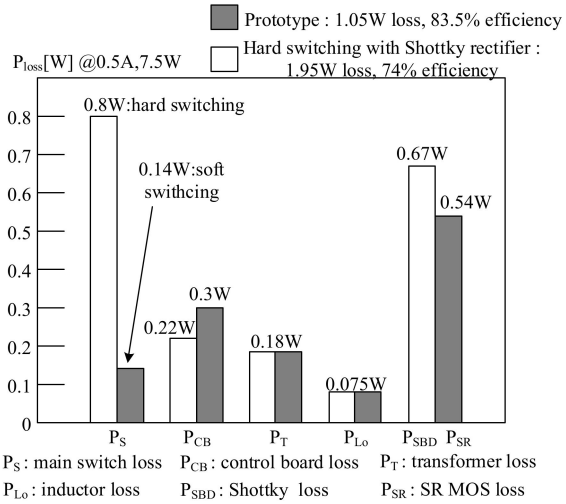

Figure 8. Estimated power loss comparison between the prototype and the traditional forward converter at 0.5 A load and 28 V input.

The output voltage ripple estimation is shown in Equation (22), where the ESR of output capacitors is 10 mΩ, and the calculated ripple voltage is 30 mV.

$$\Delta V_{\mathrm{O}} = (ESR + \frac{1}{8C_{\mathrm{O}}f_{\mathrm{s}}}) \cdot \frac{V_{\mathrm{O}}(1 - \frac{\mathrm{N}V_{\mathrm{O}}}{V_{\mathrm{i}}})}{L_{\mathrm{O}} \cdot f_{\mathrm{s}}} \tag{22}$$

The output voltage regulation estimation is shown in Equation (23), the input disturbance is the second item, and the load disturbance is the third item, where T(s) is the loop gain, G_{vg}(s) is the audio sensitivity, and Z_O(s) is the output impedance. In forward topology, the DC gain of G_{vg}(s) is the duty cycle D, and the DC gain of Z_O(s) is the load $\mathrm{R_L}$. Assuming that the DC loop gain is 40 dB, it can be estimated that the input regulation is 28 mV and the load regulation is 47 mV.

$$V_O(s) = \frac{V_{\mathrm{ref}}(s)}{k}\frac{T(s)}{1+T(s)} + V_{\mathrm{i}}(s)\frac{G_{\mathrm{vg}}(s)}{1+T(s)} - i_{\mathrm{O}}(s)\frac{Z_{\mathrm{O}}(s)}{1+T(s)} \tag{23}$$

5. Experimental Results

The prototype is fabricated based on the above parameters, and its picture is shown in Figure 9. The circuit board consists of a power board and a control board. The USB (universal serial bus) port of the PC powers the control board. The program downloader downloads the program to MCU from the PC. The control board samples the input signals from the power board, processes input signals by MCU, and then outputs gate-drive signals to the MOSFET drivers on the power board. The connection wire length between the control board and the power board has been minimized. It was found that the connection wire delay is less than 10 ns, which can be ignored.

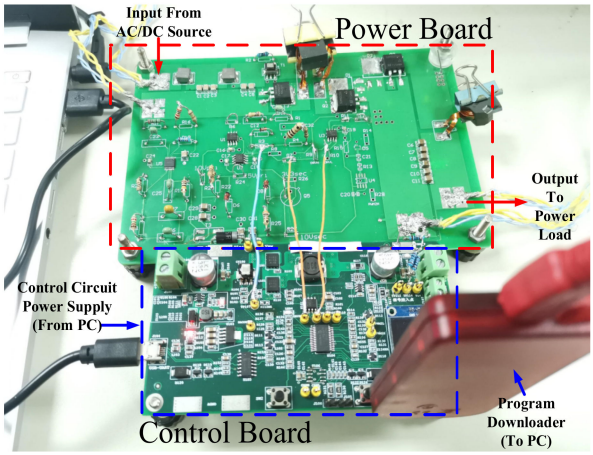

Figure 9. The prototype and environment.

5.1. Waveforms in DCM

Figure 10 shows the gate-drive signal and inductor current waveforms under different input voltages and different loads in DCM. The waveforms in each figure are $V_{gs(SR1)}$ and $V_{gs(S)}$, $V_{gs(SR2)}$, and I_{Lo}, from top to bottom. From each figure, SR_1 always turns on 400 ns earlier than S, which is t_{ZVS}. With the proposed software voltage–second balance method, SR_2 turns off exactly when I_{Lo} drops close to zero. Therefore, synchronous rectification in DCM is achieved.

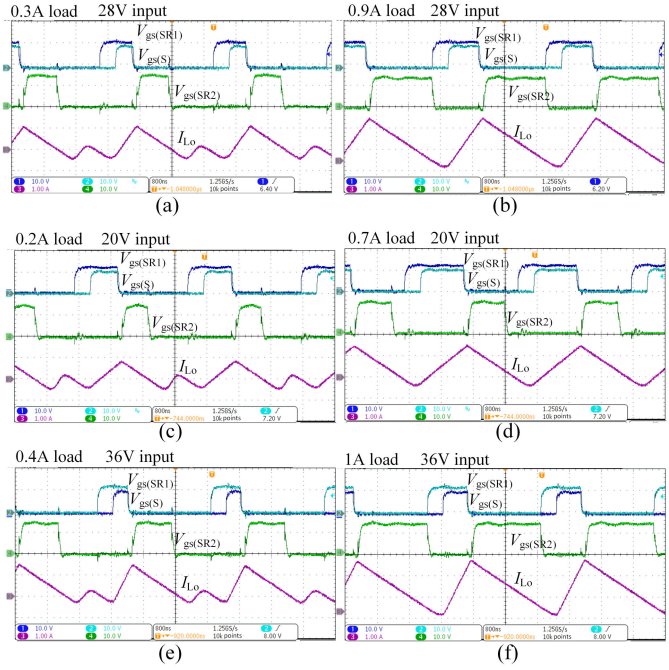

Figure 10. Gate-drive signal $V_{gs(S)}$, $V_{gs(SR1)}$, and $V_{gs(SR2)}$; inductor current waveforms I_{Lo} at (**a**) 28 V input, 0.3 A load; (**b**) 28 V input, 0.9 A load; (**c**) 20 V input, 0.2 A load; (**d**) 20 V input, 0.7 A load; (**e**) 36 V input, 0.4 A load; (**f**) 36 V input, 1 A load. (*X*-axis: 800 ns/div; *Y*-axis: $V_{gs(S)}/V_{gs(SR1)}/V_{gs(SR2)}$: 10 V/div, ILo: 1 A/div). The small symbol "T" is the zero position of the time axis.

Figure 11 shows the drain–source voltage $V_{ds(S)}$ and gate-drive voltage $V_{gs(S)}$ of the primary switch S under different input voltages and loads in DCM. After S turns off, $V_{ds(S)}$ rises to its peak. The maximum $V_{ds(S)}$ is 60 V at 36 V input, which is consistent with the calculated value. After SR_1 turns on, $V_{ds(S)}$ decreases in resonance, and S turns on when $V_{ds(S)}$ drops to the minimum value. (1) At 28 V input, which is shown in Figure 10a, $V_{ds(S)}$ resonances from 44 V to 10 V at 0.3 A load; it resonances from 46 V to 8 V at 0.9 A load. The

minimum voltage is basically consistent with the calculated value (5 V). (2) At 20 V input, which is shown in Figure 10b, $V_{ds(S)}$ resonances from 40 V to 8 V at 0.2 A load; from 52 V to 6 V at 0.7 A load. (3) At 36 V input, which is shown in Figure 10c, $V_{ds(S)}$ resonances from 46 V to 20 V at 0.4 A load; it resonances from 46 V to 14 V at 1 A load. Thus, S turns on under quasi-ZVS is realized in DCM.

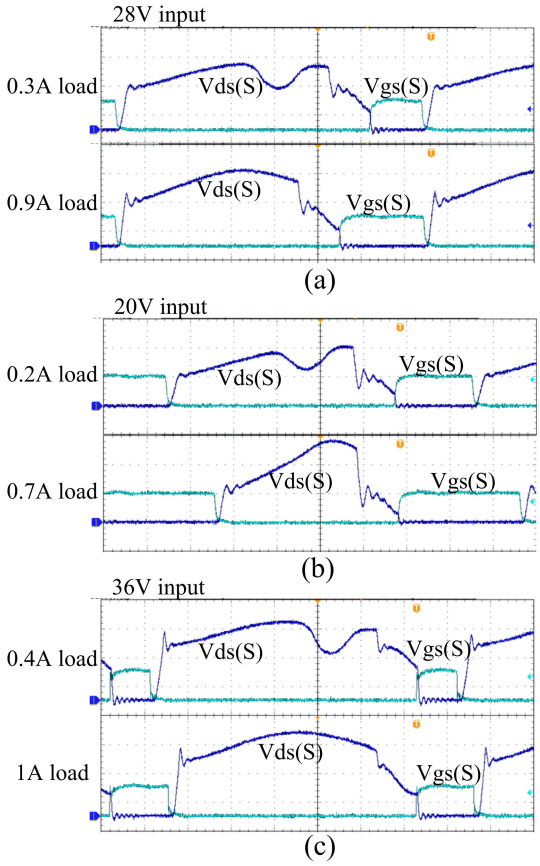

Figure 11. Drain-source voltage and gate-driver voltage of the primary switch at (**a**) 28 V input; (**b**) 20 V input; and (**c**) 36 V input. (*X*-axis: 400 ns/div; *Y*-axis: $V_{ds(S)}$: 20 V/div; $V_{gs(S)}$: 10 V/div). The small symbol "T" is the zero position of the time axis.

5.2. Transient, Ripple, and Regulation

The load-transient output voltage waveform is shown in Figure 12 under 28 V input. The load current switches between 0.5 A and half load, with a 0.6 A/μs slew rate. The circuit switches between DCM and CCM. Because SR switches are disabled, the output voltage is stable. The recovery time is 170 μs, and the maximum voltage overshoot/undershoot is 550 mV.

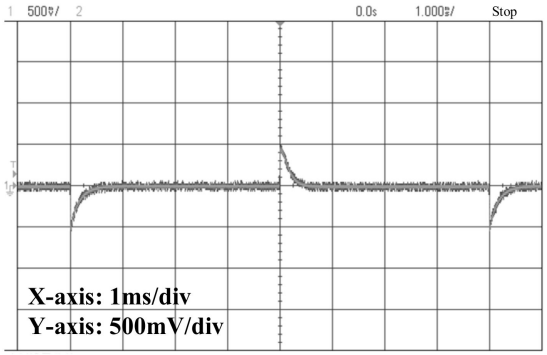

Figure 12. The output voltage waveform under load-step transient from 0.5 A to half load.

The output ripple voltages (including switching noise) at light load and full load are shown in Figure 13a,b, under 28 V input. The light-load output ripple voltage is 30 mV; it is 114 mV when noise is considered. The full-load output ripple voltage is 40 mV; it is 106 mV when noise is considered. The experimental value is consistent with the estimated value. The proposed light-load control does not affect the output ripple voltage.

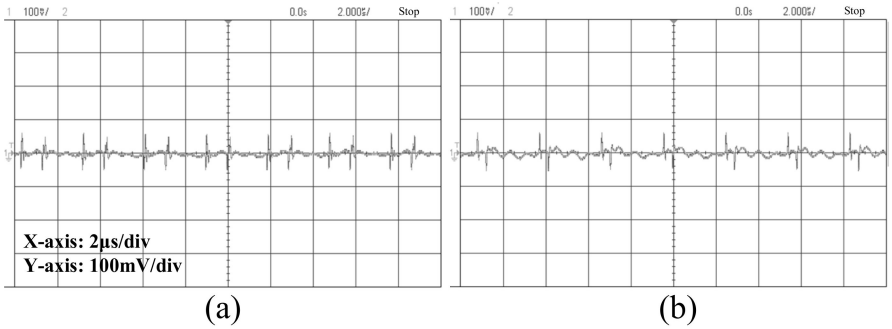

Figure 13. The output voltage ripple under (**a**) 0.5 A load and (**b**) full load.

In addition, the test results show that the load regulation (no load to full load) is 43 mV, and the line regulation (input 20 V to 36 V) is 23 mV; thus, the voltage regulation is accurate, which is consistent with the calculation result. According to the test, the stand-by current under no load is 12 mA.

5.3. Efficiency Discussion and Comparison

The efficiency curves at 28 V input are shown in Figure 14. The prototype is compared with the traditional converter, which has hard-switching and Schottky rectification. At 0% to 20% load (0 A to 1.4 A), the efficiency is above 81%, which is 5% to 10% higher than the traditional converter. Especially, the efficiency is 84% at 0.5 A, 9.5% higher than the traditional converter. The result is consistent with the estimated efficiency in Figure 8. It is noteworthy that the control board loss is considered in the efficiency test. Losses of the control board and the power board at light load are shown in Table 3.

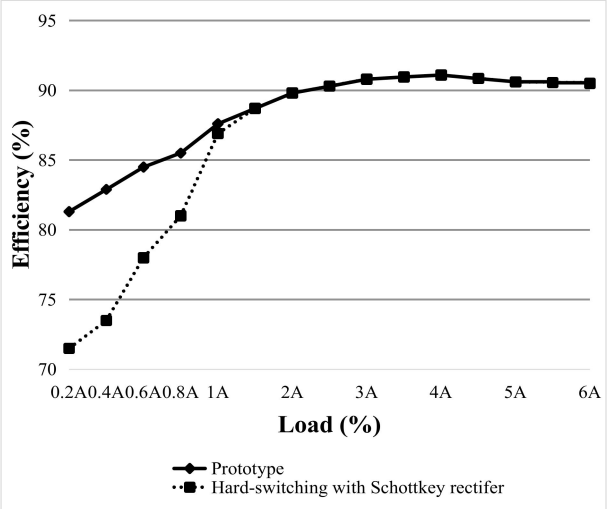

Figure 14. Efficiency comparison between the prototype and traditional forward converter at 28 V input.

Table 3. Loss and efficiency test results at light load.

Total Input Power (@ Load Current)	Power Board Loss	Control Board Loss	Total Efficiency
3.7 W (0.2 A)	0.4 W	0.29 W	81.3%
7.3 W (0.4 A)	0.94 W	0.3 W	82.9%
10.7 W (0.6 A)	1.34 W	0.31 W	84.5%
14 W (0.8 A)	1.73 W	0.31 W	85.5%
17.1 W (1 A)	1.81 W	0.31 W	87.6%

The comparison between the proposed circuit and the latest articles is shown in Table 4. Compared with other forward/buck circuits, the prototype does not require additional circuits to achieve light-load soft-switching. It has higher output power compared with flyback circuits. The prototype adopts the derating design and high-grade components, suitable for high-rel applications such as in industry, aerospace, and the military. In addition, the proposed control scheme can also be used in the two-switch forward converter, which can expand the output power further.

Table 4. Comparison with other soft-switching converters.

Author, Year	Topology	Additional Component Count	Light-Load Efficiency, (Load Range)	Maximum Output Power	Application Fields
This paper	SR forward	0	81–87%, (0–20%)	100 W	Industry, aerospace, military
[10], 2020	Flyback	0	82–88%, (0–30%)	60 W	Fast-charging
[21], 2016	Flyback	0	84.9–87.4%, (8–25%)	40 W	Fast-charging
[22], 2018	Forward	>2, ZVT circuit	<86%, (<20%)	150 W	Home appliances, industry
[23], 2020	Forward	>3, ZCT circuit	<86%, (<20%)	200 W	Medical, industry
[24], 2017	Buck	>3, ZVS circuit	<91%, (<20%)	500 W	Industry

6. Conclusions

This paper proposes a digital control method for an isolated regulated converter, which realizes synchronous rectification and soft-switching under DCM. First, the theories of soft-switching in DCM and volt-sec balance are demonstrated. Then, the control scheme is introduced, with the circuit state judgement and configuration program. In the judgement program, SR only operates in the steady state and t_{ZVS} is assigned to DTH in DCM, which is 400 ns. Other parameters, including the controller type and the circuit state judgement's threshold voltage, were designed in detail. The experimental results show that the quasi-ZVS of the primary switch is realized in DCM, and the software voltage–second balance logic turns off SR_2 accurately. The light-load efficiency is 5%-10% higher than the traditional forward circuit. The transient response, output ripple, and voltage regulation are consistent with the calculation results, proving that the circuit performs well under both light load and in a transient state. The proposed control scheme has a low component count and high light-load efficiency compared with other papers.

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