

Annealing and Doping Effects on Transition Metal Dichalcogenides—Based Devices: A Review

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Abstract: Transition metal dichalcogenides (TMDC) have been considered promising electronic materials in recent years. Annealing and chemical doping are two core processes used in manufacturing electronic devices to modify properties and improve device performance, where annealing enhances crystal quality, reduces defects, and enhances carrier mobility, while chemical doping modifies conductivity and introduces new energy levels within the bandgap. In this study, we investigate the annealing effects of various types of dopants, time, and ambient conditions on the diverse material properties of TMDCs, including crystal structure quality, defect density, carrier mobility, electronic properties, and energy levels within the bandgap.

Keywords: two-dimensional transition metal dichalcogenides; field effect transistor; annealing process; chemical doping

1. Introduction

Transition metal dichalcogenides (TMDCs) have received considerable attention over the years. TMDC is a type of two-dimensional (2D) material similar to graphene [1–4], but rather than a single layer of carbon atoms in graphene, it consists of a single layer of transition metal atoms including molybdenum (Mo) [5–8], tungsten (W) [9–11], and platinum (Pt) [12–15] sandwiched between two layers of chalcogen. An atom includes sulfur (S) [16–19], selenium (Se) [20–23], and tellurium (Te) [24–26]. TMDCs offer various interesting properties, such as high electron mobility, strong optical-matter interactions, and mechanical flexibility. These properties make them promising candidates for a variety of applications in fields such as thin-film transistors [27–30], photosensors [31–33], gas detectors [34–36], neuromorphic devices [37–40], biosensors [41–44] and energy harvesting devices [45–47]. In recent years, significant efforts have been made to develop new methods for synthesizing TMDC and to explore its properties in more detail. This allowed a better understanding of the fundamental physics of TMDCs and opened new avenues for their use in a variety of applications.

Annealing is a simple yet effective method for controlling the properties of TMDCs [48–51]. This process involves heating the material to a specific temperature for a defined duration and slowly cooling it in a controlled environment. The outcome of annealing on TMDCs can be influenced by various factors, such as the annealing temperature [52–55], duration [56–58], and atmosphere [59–62]. One of the most significant advantages of annealing on TMDCs is the elimination of defects and impurities that can degrade their electronic and optical properties, thus enhancing device performance [63–65].

In addition, annealing can also affect the electronic and optical properties of TMDCs [66–69]. For instance, it can cause shifts in the bandgap energy [70,71], making it useful in optoelectronic devices [72–74]. Furthermore, annealing can improve electron mobility [75–77] and carrier concentration [78,79] and enhance electrical conductivity [80–82]. The effect of annealing on TMDC is also dependent on the atmosphere in which the process



Citation: Ko, R.; Lee, D.H.; Yoo, H. Annealing and Doping Effects on Transition Metal Dichalcogenides—Based Devices: A Review. *Coatings* **2023**, *13*, 1364. <https://doi.org/10.3390/coatings13081364>

Academic Editor: Ning Sun

Received: 2 July 2023

Revised: 25 July 2023

Accepted: 26 July 2023

Published: 3 August 2023



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is carried out. For example, annealing in a controlled atmosphere can create sulfur or selenium voids that can alter the electronic and optical properties of the material [83,84]. Annealing in an oxidizing atmosphere can also generate an oxide layer on the material surface, which can impact electronic and optical properties [85–87].

In addition, the chemical doping method is considered to improve electrical properties of TMDC while minimizing lattice structure damage. Chemical dopant could modulate the distance between the Fermi level and the conduction band or valence band [88]. Therefore, doping the TMDC with an appropriate dopant reduces the height of the Schottky barrier and enhances the carrier density [89].

Here, we present the effects of annealing and chemical doping on the various TMDC—Based transistors. This review provides details on the TMDC transistor's annealing process in different environments, including air, nitrogen, and vacuum. Additionally, we discuss changes in the electrical characteristics of TMDC transistors resulting from organic dopants such as dielectrics and SAM. Finally, we examine the potential for performance enhancement in electronic engineering based on TMDC materials and suggest future directions for research.

2. Synthesis of Transition Metal Dichalcogenides

TMDC materials possess unique electronic and optical properties, valuable for electronic and optoelectronic devices. High-quality TMDC monolayers or few-layer structures are crucial for these applications. Mechanical exfoliation, using Scotch tape or metal assistance, provides a simple and cost-effective method for obtaining single layers from bulk crystals [90–92]. Meanwhile, chemical vapor deposition (CVD) allows controlled growth of large-area monolayers with desired properties on different substrates [93,94]. Liquid-phase exfoliation is a low-cost, scalable method for mass production but faces challenges in obtaining single atomic layers with specific structures [95,96]. Ongoing research aims to optimize exfoliation processes for addressing this issue.

3. The Fundamental Processes Occurring during Annealing in the TMDC

Annealing is utilized in shaping the crystal structure, crystallinity, and defects of TMDC, exerting crucial control over the material's electrical and optical properties [97–101]. Different from graphene, monolayer TMDC consists of sandwich structures with chalcogen atoms forming upper and lower layers and a transition metal ion plane in between. These TMDCs can be classified into 2H and 1T phases, each with distinct properties. The 2H phase exhibits excellent optical emission characteristics but limited electrical catalytic properties, while the 1T phase demonstrates superior catalytic properties but lacks light-absorbing capabilities due to its metallic nature. Through annealing, transitions between these crystal structures can be induced, enabling precise control to achieve desired characteristics.

Moreover, annealing influences the growth of crystalline domains, impacting crystal boundaries and thereby regulating charge transport and electrical properties. Additionally, the annealing process reduces defects and imperfections, leading to enhanced electrical and optical properties. In intentionally doped TMDC, annealing facilitates the diffusion of dopants into the crystal lattice, resulting in improved electronic properties and the ability to tailor specific functionalities. The outcomes of these annealing effects depend on various conditions such as temperature, time, and environment, allowing for fine tuning of TMDC properties for diverse applications.

4. Annealing Effects of TMDC—Based Transistors

4.1. Annealing Effects of MoS₂—Based Transistors

The n-doping effect of molybdenum disulfide (MoS₂) FET was demonstrated through a simple annealing process. This study performed annealing for 2 h in a nitrogen atmosphere [102]. Figure 1a shows the transfer curve of a MoS₂ FET with the effect of vacuum annealing, where the pristine MoS₂ FET exhibits a low on/off-current ratio of 100 A/A due to its high off current of 10^{−5} A. The off current of the MoS₂ FET annealed at 200 °C was

below 10^{-11} A at negative gate voltage, indicating the n-type doping effect. The off current of the MoS₂ FET annealed at 300 °C shows a slight increase compared to that at 200 °C. The decrease in the off current is due to the rearranged surface of the MoS₂ channel and the removal of residual material through heat. On the other hand, increasing the annealing temperature to 400 °C resulted in a decrease in the on current and an increase in the off current, with a drain current of 10^{-5} A and an ambiguous boundary between the on/off currents. The high off current of the MoS₂ FET is attributed to the phase transformation to Mo₂S₅ caused by high-temperature energy. Moreover, when the electrical characteristics are measured in atmospheric environments, the adsorption of water and oxygen molecules on the annealing-treated MoS₂ channel region leads to an increase in the off current. Figure 1b shows the on/off current of the MoS₂ FET as a function of annealing temperature. The on current continues to decrease as the annealing temperature current becomes the initial drain current value. Figure 1c shows the extracted charge carrier mobility of the MoS₂ FET with annealing temperature. The electron mobility of a pristine MoS₂ FET is $8.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, but the highest electron mobility of $20.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ appears at the lowest off-state current under annealing conditions of 200 °C, and as the annealing temperature increases above 200 °C, the electron mobility decreases.

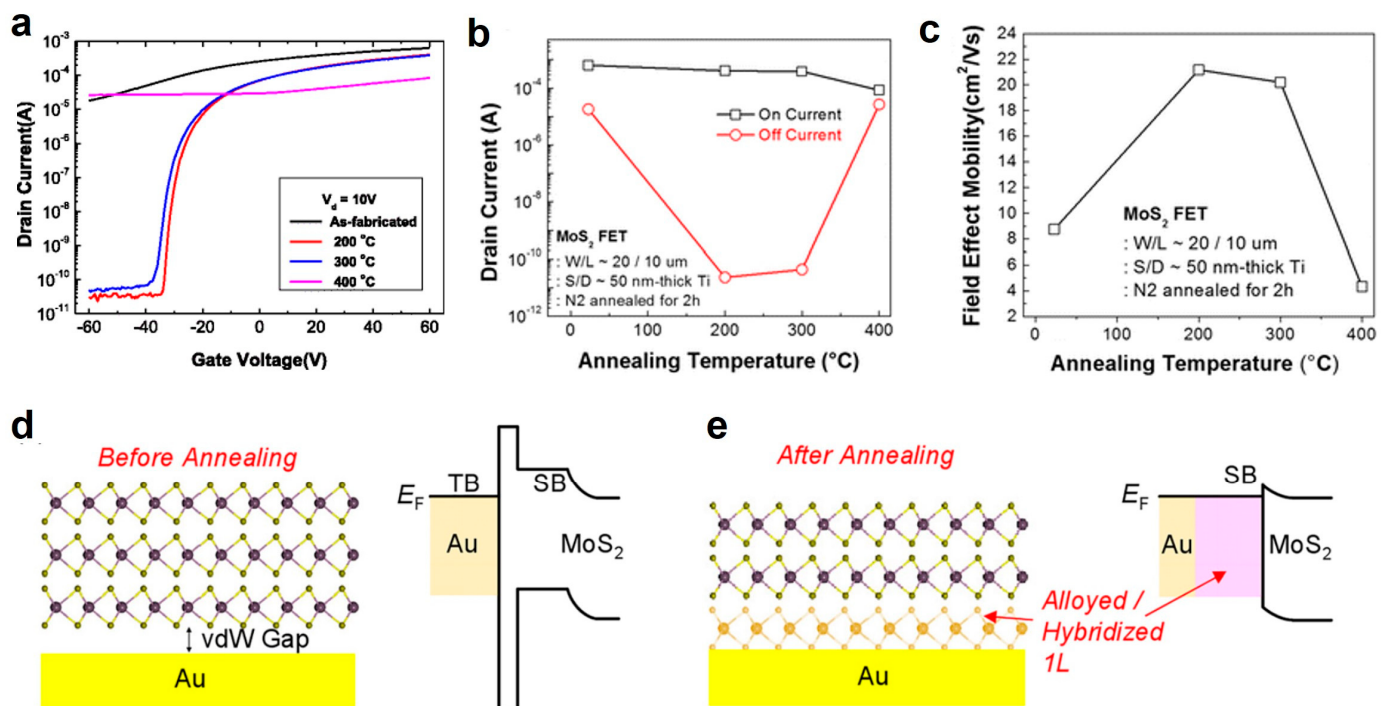


Figure 1. (a) Transfer curve of MoS₂ FET according to annealing temperature; (b) The plotted on- and off-current values of MoS₂ FET; (c) The extracted field effect mobility of MoS₂ FET according to annealing temperature (adapted from [102] with permission from the Springer Science and Business Media); Band structure of the Au contact electrode and MoS₂ channel (d) before annealing and, (e) after annealing (adapted from [103] with permission from the AIP Publishing LLC).

As another example, the induced n-doping effect in MoS₂ FET through a vacuum annealing process was reported by Islam et al. [103]. The pristine MoS₂ FET was mounted on a furnace and annealed at 250 °C under a vacuum of 15 mTorr for 1 h. The contact and channel resistances of the pristine MoS₂ FET were 4 MΩ and 112 kΩ, respectively, while the annealed MoS₂ FET had a contact resistance of 2 kΩ and a channel resistance of 171 kΩ. Figure 1d shows the band structure of the pristine MoS₂ FET. A vacuum annealing process reduced the contact and channel resistances of the device, despite the presence of a high contact resistance caused by the tunneling barrier between the Au contact electrode and the MoS₂ channel due to the Van der Waals gap. The vacuum-annealed interface

between the Au contact electrode and MoS₂ channel is alloyed, eliminating the Van der Waals gap and tunneling barrier (Figure 1e). Additionally, the alloyed Au contact electrode and MoS₂ channel had reduced work function, leading to a decreased Schottky barrier, and consequently lowering the contact resistance. This vacuum annealing process increases the mobility of MoS₂ FET from 0.1 to 8 cm² V⁻¹ s⁻¹ and enhances the on/off ratio 10 fold.

4.2. Annealing Effects of MoTe₂—Based Transistors

To change the electrical characteristics of n-type molybdenum ditelluride (MoTe₂) FETs, a *p*-type doping method through an annealing process was reported [104]. This annealing process led to a MoTe₂—Based complementary metal-oxide semiconductor (CMOS) inverter using a *p*-type MoTe₂ FET with an annealing process and an n-type MoTe₂ FET with electron beam irradiation. To manufacture a *p*-type MoTe₂ FET, a rapid thermal annealing (RTA) process was performed at 250 °C for 3 h. Figure 2a shows the molecular structure of oxidized MoTe₂ resulting from the annealing process. MoTe₂ has bonds such as Te vacancy and antisites. Upon high-temperature annealing treatment, the Te vacancy was increased and induced the absorption of oxygen molecules. As a result, oxygen molecules with high electronegativity are adsorbed onto the Te vacancy in oxidized MoTe₂, acting as electron acceptors and inducing a *p*-type doping effect on MoTe₂ FET. Figure 2b shows the electrical properties of the pristine MoTe₂ FET and the annealed MoTe₂ FET. After the annealing process, the MoTe₂ FET enhanced *p*-type behavior, and the hysteresis was reduced. Also, the doping effect of *p*-type MoTe₂ FET induced by high-temperature annealing lasted for 2 weeks. Figure 2c shows the voltage transfer characteristics (VTC) of a CMOS inverter implemented using an annealed treated *p*-type MoTe₂ FET and an n-type MoTe₂ FET fabricated by electron beam irradiation. The CMOS inverter exhibits full-swing operation over a drain voltage range of 1 V to 5 V.

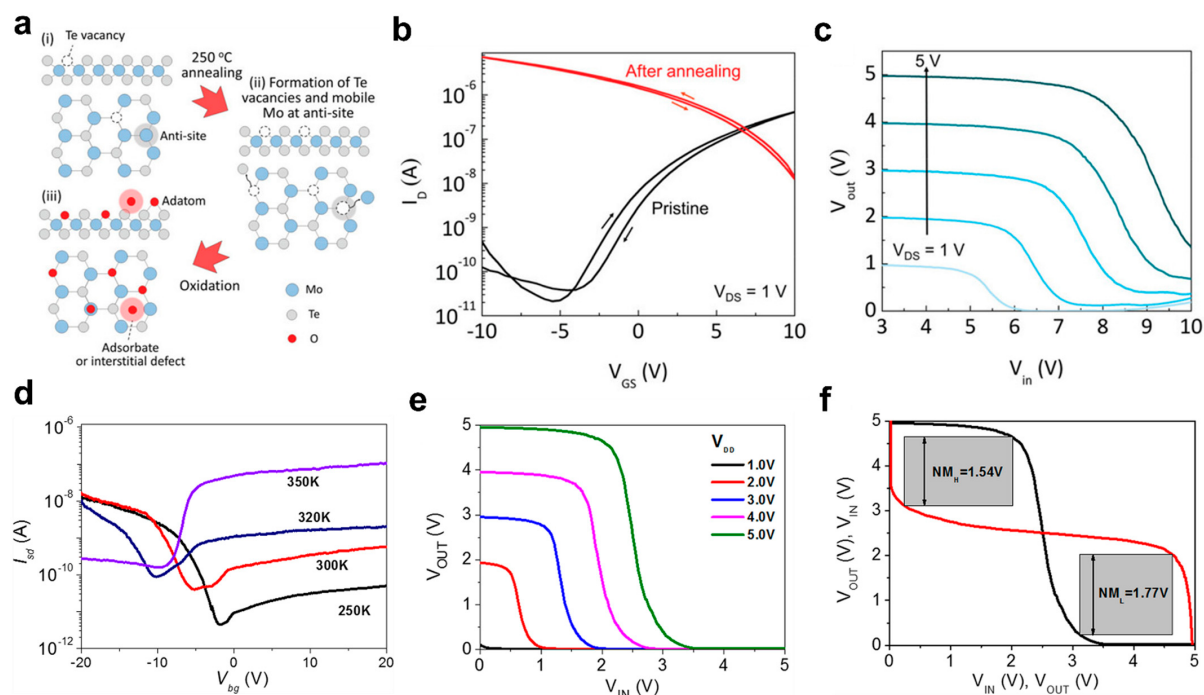


Figure 2. (a) Schematic of MoTe₂ structure with annealing and oxidation; (b) Transfer curve of pristine MoTe₂ FET and annealed MoTe₂ FET; (c) Voltage transfer characteristics of MoTe₂ based CMOS inverter (V_{DS} was applied from 1 V to 5 V at 1 V interval). (adapted from [104] with permission from the John Wiley and Sons); (d) Transfer curve of MoTe₂ FET according to vacuum annealing temperature; (e) Voltage transfer characteristics of MoTe₂ inverter; (f) Voltage transfer characteristics (black lines) and their mirrors (red lines) of MoTe₂ inverter at $V_{DD} = 5$ V (adapted from [105] with permission from the Springer Science and Business Media).

When oxygen or water molecules in the air are adsorbed onto the MoTe₂ channel, it operates as a *p*-type transistor. However, the vacuum annealing process removes the adsorbed molecules from the MoTe₂ channel. Consequently, Te vacancies are generated in the MoTe₂ channel due to the removed adsorbates, resulting in the acquisition of *n*-type conductivity [105]. Figure 2d shows the transfer curves of the *n*-type MoTe₂ FET through the vacuum annealing process. The pristine MoTe₂ FET operates as a *p*-type due to the incomplete removal of adsorbates from the MoTe₂ channel. In contrast, when the temperature is increased to 76.85 °C, the drain current at both positive and negative gate voltages decreases and increases, respectively. The *n*-type MoTe₂ FET has on/off ratio of 3.8×10^2 A/A, an S.S of 1.1 V/dec, and electron mobility of $2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. In addition, the inverter was demonstrated using unipolar *p*-type and *n*-type MoTe₂ FETs. Figure 2e shows the VTC characteristics of the MoTe₂ inverter. The transition voltage was half of V_{DD} due to the transfer curve of *p*- and *n*-type of MoTe₂ FET being symmetrical. Figure 2f shows the noise margin and VTC curve of the MoTe₂ inverter when V_{DD} is 5 V. The low-level noise margin (NM_L) is 1.54 V, while the high-level noise margin (NM_H) is 1.77 V.

4.3. Annealing Effects of WSe₂—Based Transistors

The work function of the electrode and the subsequent annealing process changed the electrical characteristics of the tungsten diselenide (WSe₂) FET. Bandyopadhyay et al. fabricated WSe₂ FET using various metal electrodes with different work functions, such as gold (Au, $\phi_m = \sim 5.4 \text{ eV}$), molybdenum (Mo, $\phi_m = \sim 4.53 \text{ eV}$), and aluminum (Al, $\phi_m = \sim 4.08 \text{ eV}$) [106]. The WSe₂ FET with metal electrodes of different work functions operates as both *n*-type and *p*-type transistors. Furthermore, the field effect mobility and on current were increased by 300 °C vacuum, annealing for 3 h. Figure 3a shows the transfer curve of a WSe₂ FET with Au/Ti electrodes. The hole mobility of the pristine Au/Ti/WSe₂ FET was $432 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, but it increased by 150% to $625 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ after the annealing process with enhancing *p*-type operation. This indicates the interface properties between the WSe₂ channel and gate dielectric are enhanced by annealing effects. Figure 3b shows the transfer curve of WSe₂ FETs with Mo electrodes. The pristine Mo/WSe₂ FET had ambipolar behavior with *p*-type dominance, and the hole and electron mobilities were 210 and $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. The additional annealing process further improved the ambipolar conduction of the Mo/WSe₂ FET. The annealed Mo/WSe₂ FET had a hole mobility of $410 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an electron mobility of $70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. On the other hand, WSe₂ FET with Al electrodes resulted in an *n*-type operation (Figure 3c). The electron mobility of the Al/WSe₂ FET before and after annealing was 242 and $366 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. In summary, the conductivity of WSe₂ FETs with dissimilar electrode work functions can be controlled as either *n*-type or *p*-type, and additional vacuum annealing shows the annealing effects of the device, inducing high mobility.

The annealing process performed in ambient air causes the formation of an oxide layer (WO₃) due to the interaction between the WSe₂ surface and oxygen molecules. The *p*-doping effect on ambipolar WSe₂ FET using an annealing process in ambient environment was observed [107]. The work function of WO₃ ($\sim 6.7 \text{ eV}$) formed on the WSe₂ surface under this condition is lower than that of WSe₂ ($\sim 4.4 \text{ eV}$), resulting in a WSe₂ FET operating as a *p*-type transistor. Figure 3d shows the modified transfer curves of the ambipolar WSe₂ FET after annealing in air ambient. The WSe₂ FET was annealed at 200 °C on a hot plate for 1 h. After annealing, the *n*-type current ($V_G = 70 \text{ V}$) of the ambipolar WSe₂ FET decreased at all drain voltages ($V_D = 4 \text{ V}, 6 \text{ V}$), and the *p*-type current increased ($V_G = -70 \text{ V}$). Also, the hole and electron mobility before annealing are 0.13 and $5.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. In contrast, when WSe₂ FET was annealed, the extracted hole mobility increased up to $1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, while the electron mobility decreased to $0.69 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Figure 3e,f show the photo-switching characteristics of the pristine WSe₂ FET and the annealed WSe₂ FET. A 405 nm laser with a power density of 11 mW/cm^2 was applied. In the switching operation, the rise time and decay time of the pristine WSe₂ FET were 92.3 s and 57.6 s, respectively. In contrast, the rise time of the annealed WSe₂ FET decreased

significantly by 610 times to 0.15 s. Also, the decay time decreased to less than 0.33 s with a 170 times difference. The improved optical switching behavior is attributed to the lattice mismatch between WSe₂ and WO₃ generated by the proposed annealing process, and the recombination of photo-generated electron-hole pairs is facilitated by the trap regions resulting from the lattice mismatch.

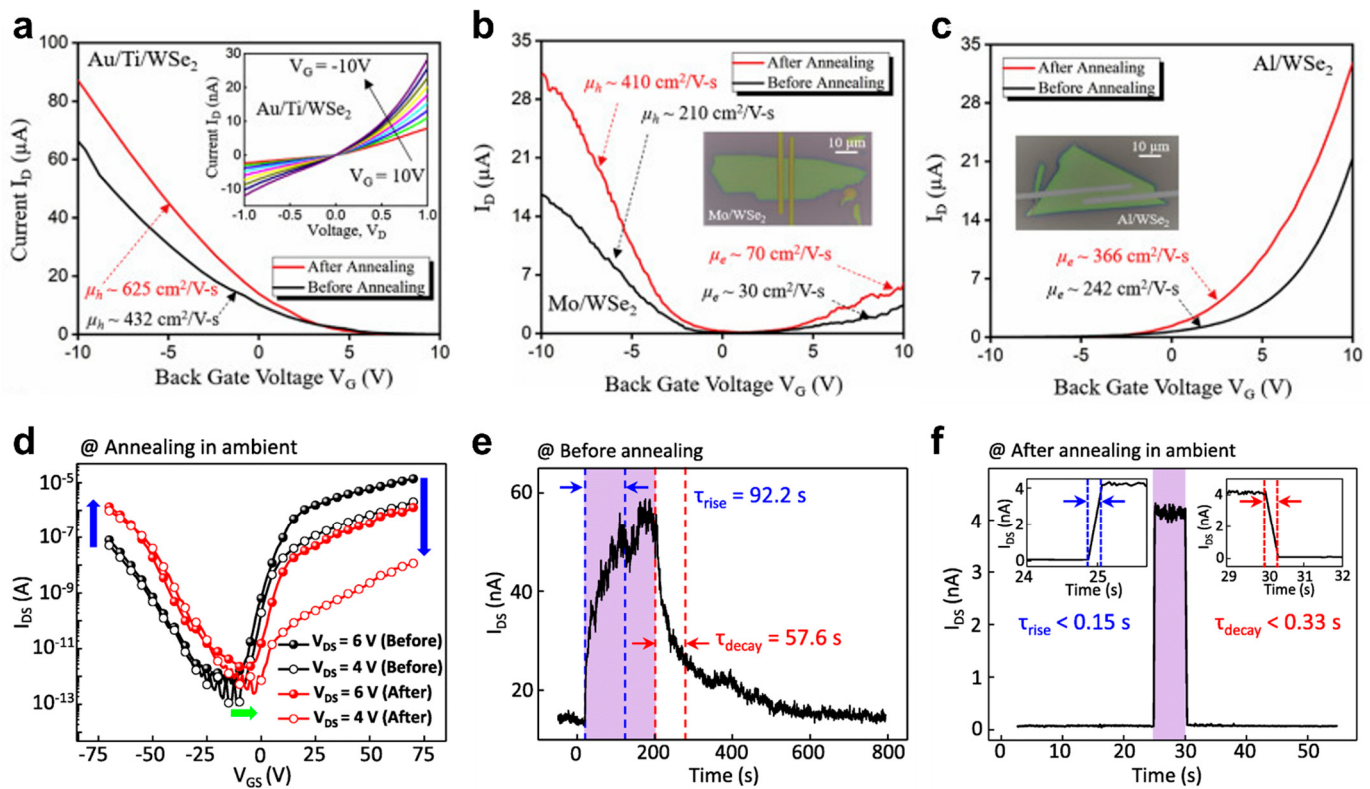


Figure 3. Transfer curve of WSe₂ FETs with various metal electrodes such as (a) gold/titanium, (b) molybdenum, and (c) aluminum (adapted from [106] with permission from the Elsevier B.V.); (d) Transfer curve of pristine WSe₂ FET and annealed WSe₂ FET under air ambient; Photo-switching behavior of (e) pristine WSe₂ FET and, (f) WSe₂ FET annealing at air ambient (adapted from [107] with permission from the Springer Science and Business Media).

4.4. Annealing Effects of WS₂—Based Transistors

The n-type behavior of multilayer tungsten disulfide (WS₂) FET through a double annealing process, performed both before and after electrode deposition, was demonstrated by Ji et al. in 2022 [108]. The first annealing process was carried out for 2 h at 200 °C on a WS₂ transferred substrate mounted in a vacuum tube furnace. The first annealing process removed the organic residue and improved the WS₂/electrode interface by desorbing the surface adsorbent. The second annealing process was also performed in a vacuum tube furnace at 200 °C after electrode deposition. Figure 4a shows the transfer curve of pristine WS₂ FET (Group A) and annealed after electrode deposition WS₂ FET (Group B). The on/off ratio and field effect mobility of pristine WS₂ FET were 1.9×10^5 A/A and 11.1 cm² V⁻¹ s⁻¹, respectively. In contrast, the WS₂ FET performed by annealing process after electrode deposition had 1.6×10^6 A/A of on/off ratio and 20.8 cm² V⁻¹ s⁻¹ of field effect mobility. Also, the output curves of WS₂ FET from groups A and B showed a decrease in contact resistance from $\sim 6.7 \times 10^2$ k Ω · μ m to $\sim 3.8 \times 10^2$ k Ω · μ m (Figure 4b). Statistical analysis of the field effect mobility for 50 WS₂ FET in each group was also performed (Figure 4c). Group C performed with an annealing process after the WS₂ flake transfer, while Group D comprised WS₂ FETs that carried out a double annealing process. The average field effect mobility of pristine WS₂ FET was the lowest at 5.6 cm² V⁻¹ s⁻¹.

The average field effect mobility with the first and second annealing processes was 14.8 and $16.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. In contrast, the average field effect mobility of WS_2 FET performed double annealing process was the highest at $23.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Thus, the mobility and contact resistance of the WS_2 FET were improved through double annealing processing.

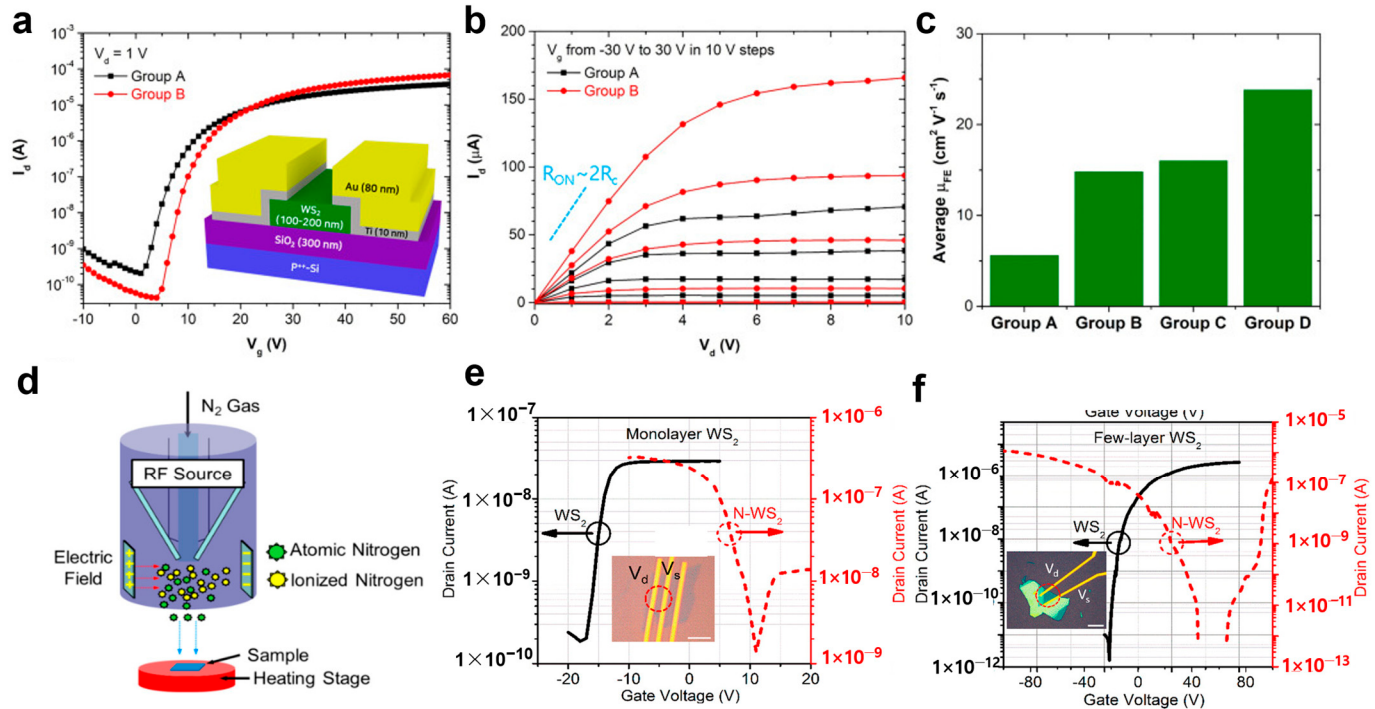


Figure 4. Electrical characteristics comparison between the pristine WS_2 FET and the annealed after electrode deposition WS_2 FET using (a) Transfer curves and, (b) Output curves; (c) Statistical analysis of 50 WS_2 FET with A to D groups (adapted from [108] with permission from the Elsevier B.V.); (d) 3D schematic of the WS_2 nitrogen substitutional doping and annealing process; Transfer curves of pristine WS_2 FET and nitrogen doping WS_2 FET with (e) monolayer WS_2 and, (f) few layer WS_2 (adapted from [109] with permission from the American Chemical Society).

WS_2 typically exhibits n-type conductivity in both exfoliated flakes and chemical vapor deposition (CVD) growth. Nitrogen substitution doping and annealing manifest p-doping effects on WS_2 FETs through Fermi-level pinning, which is a technological achievement for implementing TMDC—Based CMOS FETs [109]. The WS_2 films were grown using radio frequency (RF) magnetron sputtering, followed by nitrogen annealing at 300°C under a pressure of $7.0 \times 10^{-5} \text{ mbar}$. The nitrogen radicals composed of ionized nitrogen and atomic nitrogen were effused into WS_2 samples mounted on the main chamber and created W–N bonds (Figure 4d). The W–N bonds created by substituting S atoms in WS_2 with N atoms result in an acceptor level 0.24 eV lower than the conduction band edge of WS_2 , enabling p-type doping. Figure 4e shows the transfer curves of a monolayer n-type WS_2 and a p-type WS_2 FET after nitrogen treatment. The hole mobility and the threshold voltage of the n-type WS_2 FET are $0.53 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 9 V , respectively. However, a p-type WS_2 FET with nitrogen substitutional doping had $1.70 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ of hole mobility and -12 V of the threshold voltage. Similarly, nitrogen annealing also enables the p-type operation of multilayer WS_2 FET (Figure 4f). The p-type doping effect of WS_2 FET by nitrogen substitutional doping and the annealing process is due to Fermi-level pinning.

The electrical properties of TMDCs can be changed depending on the annealing temperature and the environment (Table 1). Thus, depending on the intended application, the appropriate type of TMDC should be selected, and the required electrical properties should be achieved with suitable processing methods. Table 1 summarizes the characteristics of TMDC—Based transistors depending on the annealing conditions.

Table 1. The influence of annealing on the characteristics of TMDC—Based transistors.

Materials	Annealing Temperature	Annealing Time	Annealing Ambient	Doping Effect	Mobility	Ref.
MoS ₂	200 °C	2 h	Nitrogen	n-type doping	20.7 cm ² V ^{−1} s ^{−1}	[102]
MoS ₂	250 °C	1 h	Vacuum	n-type doping	8 cm ² V ^{−1} s ^{−1}	[103]
MoTe ₂	250 °C	3 h	Vacuum	p-type doping	N/A	[104]
MoTe ₂	76.85 °C	N/A	Vacuum	n-type doping	2 cm ² V ^{−1} s ^{−1}	[105]
WSe ₂	300 °C	3 h	Vacuum	p-type doping	625 cm ² V ^{−1} s ^{−1}	[106]
WSe ₂	200 °C	1 h	air	p-type doping	1.3 cm ² V ^{−1} s ^{−1}	[107]
WS ₂	200 °C (double)	2 h	Vacuum	n-type doping	23.8 cm ² V ^{−1} s ^{−1}	[108]
WS ₂	300 °C	N/A	Nitrogen	p-type doping	1.7 cm ² V ^{−1} s ^{−1}	[109]

5. Annealing and Chemical Doping Effects in TMDC—Based Transistors

5.1. Annealing and Chemical Doping Effects in MoS₂—Based Transistors

The formation of a triphenylphosphine (PPh₃) layer can be controlled by annealing temperature. The use of PPh₃ provided the n-doping effect of MoS₂ FET through continuous annealing at three different temperatures (150, 250, and 350 °C) after spin coating a 7.5 wt% PPh₃ solution on the surface of transistor [110]. The coated phosphorus atoms of PPh₃ transfer electrons to the MoS₂ surface, inducing an n-doping effect. Also, the PPh₃ layers increase the number of electrons moving to the MoS₂ channel as the annealing temperature increases. Raman spectroscopy was performed to analyze the n-doping effect of MoS₂. Figure 5a shows the redshift values of the E_{2g}¹ peak and the A_{1g} peak of MoS₂ according to the annealing temperature. At 150 °C annealing conditions, both the E_{2g}¹ peak and the A_{1g} peak are redshifted by −0.78 cm^{−1}. As the annealing temperature increases to 350 °C, the E_{2g}^{−1} peak and the A_{1g} peak are redshifted by −2.16 cm^{−1} and −2.75 cm^{−1}, respectively. This indicates that PPh₃ formation at higher annealing temperatures results in an enhanced n-doping effect. Figure 5b shows the transfer curve of pristine MoS₂ and PPh₃-doped MoS₂ FET with annealed from 150 °C to 350 °C. As the annealing temperature increases, the on current of the PPh₃-doped MoS₂ FET increases, and the threshold voltage shifts towards negative gate voltages. Furthermore, the energy barrier height of PPh₃ decreases, resulting in a decrease in contact resistance from 2.82 kΩ to 0.24 kΩ (Figure 5c). In addition, the on/off-current ratio and carrier mobility of PPh₃-doped MoS₂ FET improved to 8.70 × 10⁵ A/A and 241 cm² V^{−1} s^{−1}, respectively, from their initial values of 8.72 × 10⁴ A/A and 12.1 cm² V^{−1} s^{−1}.

In the demonstration, an ambipolar MoS₂ FET with strong p-type conductivity was achieved through chemical doping and annealing effects. In 2021, Lee et al. spin-coated a 10 mg mL^{−1} solution of poly(9,9-di-n-octylfluorenyl-2,7-diyl) (PFO) onto the device and annealed it on a hotplate at various temperatures of 60, 300, and 350 °C for 10 min [111]. Figure 5d illustrates the 3D schematic diagram of the doping process of a PFO-doped MoS₂ FET. Additionally, the electrical characteristics of a PFO-doped MoS₂ FET were measured at various annealing temperatures (Figure 5e). The pristine MoS₂ FET shows conventional n-type behavior and has 0.93 μA of on current at V_G = 30 V and 10² A/A of on/off ratio. However, as the annealing temperature was increased, the PFO-doped MoS₂ FET exhibited ambipolar behavior due to the enhanced p-type conductivity. Also, at an annealing temperature of 350 °C, the reduced n-type current and increased p-type current suggest ambipolar behavior of MoS₂ FETs by PFO doping. Figure 5f shows the variation of n-type and p-type currents with pristine MoS₂ FET and PFO-doped MoS₂ FET. As PFO doping was performed and the annealing temperature increases, the p-type current gradually increases. Also, the p-type current of 350 °C annealed PFO-doped MoS₂ FET was 0.20 μA with 24 times increase compared to the pristine MoS₂ FET. On the other hand, the on current decreased 14 times from 0.93 μA to 0.06 μA.

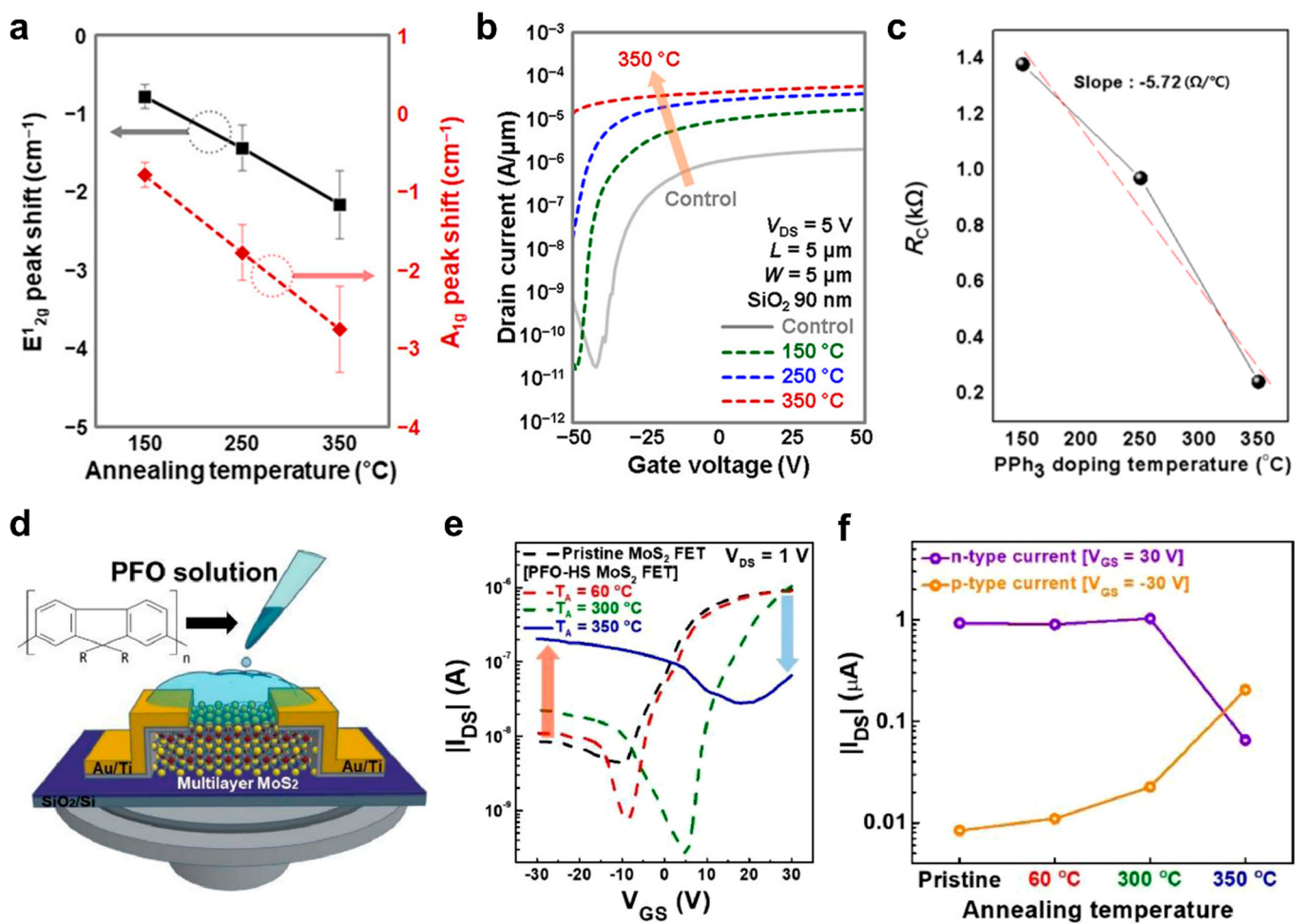


Figure 5. (a) Raman peak shift values against the formation temperatures of PPh₃ (black line: E_{2g}¹ peak, red line: A_{1g} peak); (b) Transfer curve of pristine MoS₂ FET and PPh₃-doped MoS₂ FET annealing at 3 different temperatures (150, 250, and 350 °C); (c) Contact resistance of PPh₃-doped MoS₂ FET measured at various annealing temperatures (black line: 150, 250, and 350 °C, red line: line profile of contact resistance); (adapted from [110] with permission from the American Chemical Society); (d) 3D schematic of PFO-doped MoS₂ FET, where red spheres represent Mo atoms, and yellow spheres represent S atoms. The inset shows the chemical structure of poly(9,9-di-n-octylfluorenyl-2,7-diyl) (PFO); Electrical characteristics of the pristine MoS₂ FET and PFO-doped MoS₂ FET annealed at various temperature (60, 300, and 350 °C); (e) Transfer curve; (f) Extracted n- and p-type current variation (adapted from [111] with permission from the Elsevier B.V.).

5.2. Annealing and Chemical Doping Effects in MoTe₂—Based Transistors

MoTe₂ exhibits instability in the surrounding environment due to oxidation. The oxidation achieved p-type doping of the device and improved stability in the surrounding environment through bis(trifluoromethane)sulfonamide (TFSI) doping and PMMA encapsulation [112]. The mechanically exfoliated MoTe₂ flakes were transferred onto a substrate and coated with PMMA, followed by annealing at 100 °C. The flakes and half of the electrodes were etched to expose the PMMA-coated device and the uncoated device. Subsequently, both samples were immersed in a nonreactive atmosphere for a 5 min period in a chlorobenzene (CB) solvent solution containing TFSI. Figure 6a illustrates a schematic diagram of the device. Chlorobenzene (CB), a chlorine—Based solvent containing lone electron pairs, can act as an electron donor to MoTe₂, resulting in an n-type doping effect. However, the electron-donating effect is nullified by the electron-withdrawing effect of TFSI. Figure 6b illustrates the transfer characteristics of TFSI-MoTe₂ FETs with and without a PMMA layer, compared to the pristine MoTe₂ FET. After TFSI doping, the device without

a PMMA layer exhibited unipolar *p*-type behavior with an on/off ratio exceeding 10^3 A/A and a maximum mobility of $0.58 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The decrease in current in the n-branch indicates that TSFI induces *p*-type doping. The significant shift of the threshold voltage to 0 V after PMMA coating reflects the improved efficiency of TSFI doping for achieving *p*-type operation in the device. Conclusively, the device doped with TSFI along with a PMMA layer exhibited unipolar *p*-type behavior with an on/off ratio exceeding 10^6 A/A and a maximum mobility of $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, demonstrating a 250-fold improvement compared to the pristine device. This demonstrates superior on/off ratio and mobility enhancement characteristics compared to other doped TMD FETs.

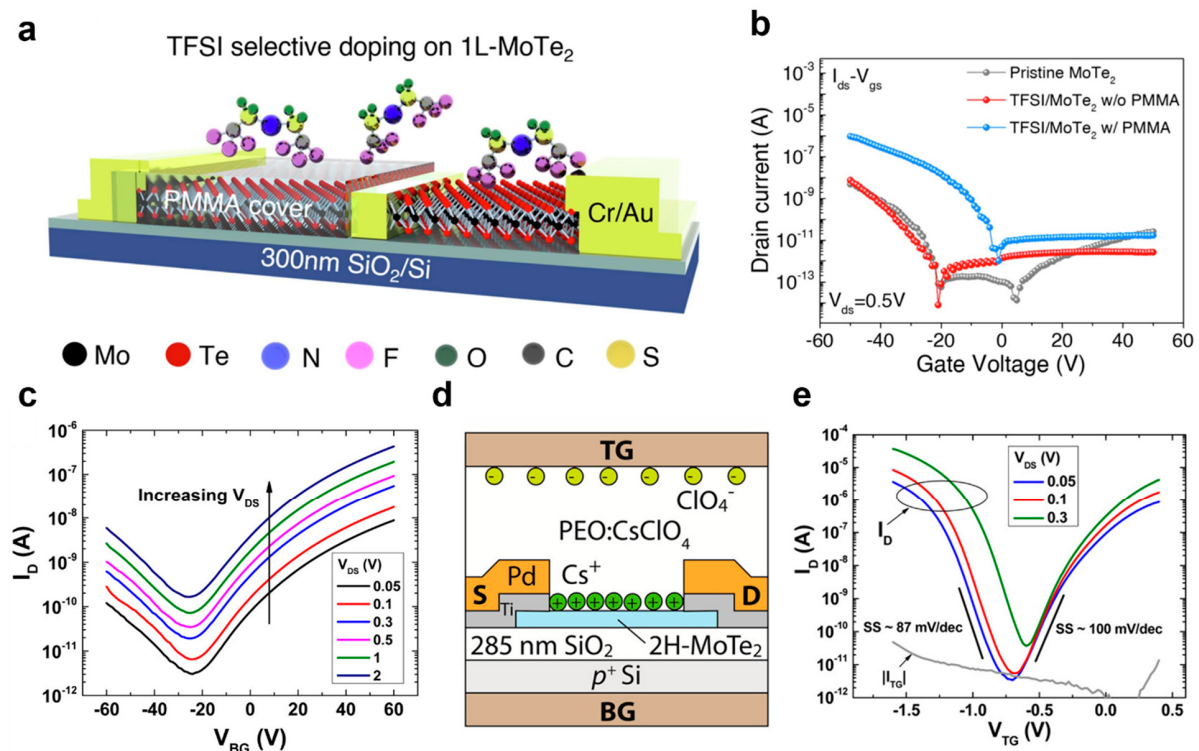


Figure 6. (a) Structure of TSFI-MoTe₂ with areas encapsulated by PMMA and those without encapsulation; (b) Transfer characteristics of pristine MoTe₂ device compared to TSFI-MoTe₂ with areas encapsulated by PMMA and those without encapsulation (adapted from [112] with permission from the Applied Surface Science); (c) Transfer curve of pristine MoTe₂ FET with back-gate structure; (d) Cross section of ion gate MoTe₂ FET; (e) Transfer curve of ion gate MoTe₂ FET with various supply voltage (adapted from [113] with permission from the American Chemical Society).

The ambipolar MoTe₂ FET doped with poly(ethylene oxide) (PEO) and CsClO₄ as the top-gate dielectric exhibited both *n*-doping and *p*-doping effects [113]. The PEO:CsClO₄ solution was drop cast on the pristine MoTe₂ FET with back-gated structure and was annealed at 90 °C for 3 min. Figure 6c shows the transfer curve of a pristine MoTe₂ FET. The pristine MoTe₂ FET shows ambipolar behavior at various drain-source voltages (0.05 V to 2 V). Figure 6d shows a cross-section of a MoTe₂ FET doped with a top-gate dielectric of PEO:CsClO₄. To construct the ion gate, the PEO:CsClO₄ with gate dielectric and palladium (Pd) top gate electrodes were sequentially deposited on the MoTe₂ channel. A positive or negative gate voltage applied to the top gate electrode induces *n*-type and *p*-type doping, respectively. The positive gate voltage applied to the top gate electrode induces electrons in the channel due to Cs⁺ ions, resulting in *n*-type doping effect. On the other hand, a negative gate voltage results in *p*-type doping of MoTe₂ due to ClO₄[−] ions. Figure 6e shows the transfer curve of an ion-gate MoTe₂ FET. Compared to pristine MoTe₂ FETs, the on/off ratio and on current of ion-gate MoTe₂ FET increased 20 times and 40 times in the *n*-branch and *p*-branch, respectively (*V*_{DS} = 0.05 V).

5.3. Annealing and Chemical Doping Effects in WSe₂—Based Transistors

Using self-assembled monolayers (SAM) and a double annealing process, the changes in the characteristics of WSe₂ FET was observed. The device was immersed in an octadecyltrichlorosilane (OTS) solution, which served as the material for SAM, and annealed at 120 °C for 20 min [114]. Figure 7a shows the 3D schematic and energy band diagram of the OTS-doped WSe₂ FET. The methyl groups of OTS doping on the WSe₂ surface possess positive poles, and the electrons accumulate on the WSe₂ surface due to the dipolar effect of OTS, resulting in the occurrence of a *p*-type doping effect. Also, as the concentration of OTS solution was increased, the *p*-type doping effect on WSe₂ FET was enhanced. The OTS doping effect on WSe₂ FETs reduces the Schottky barrier height. The upward valence band of the OTS-doped WSe₂ FET enhances the hole injection by the narrowed tunneling barrier. Figure 7b shows the transfer curves of a pristine WSe₂ FET and a WSe₂ FET doped with OTS at a concentration of 1.2%. The pristine WSe₂ FET has a threshold voltage of −9.1 V and on current of 1.64×10^{-6} A/μm. On the other hand, threshold voltage and on current of WSe₂ FET doped with 1.2% OTS were −0.45 V and 1.42×10^{-5} A/μm, respectively. In addition, the mobility increased from 30 ± 4 cm² V^{−1} s^{−1} (before doping) to 192 cm² V^{−1} s^{−1} for the device doped with 0.024% OTS (~ 105 cm² V^{−1} s^{−1} in the 1.2% OTS-doped device). Figure 7c shows the extracted threshold voltage of OTS-doped WSe₂ FETs according to time in an air ambient. The threshold voltage of WSe₂ FETs doped with various OTS concentrations (0.024, 0.24, 0.12, 1.2%) is shifted towards a negative gate voltage due to moisture in the air. However, an additional annealing process at 120 °C confirmed that shifts in the threshold voltage back to positive values restores the *p*-doping effect. The additional annealing process reduces the Si–O–Si bonds of OTS formed in an air exposure and increases the Si–OH bonds that enhance the *p*-doping effect.

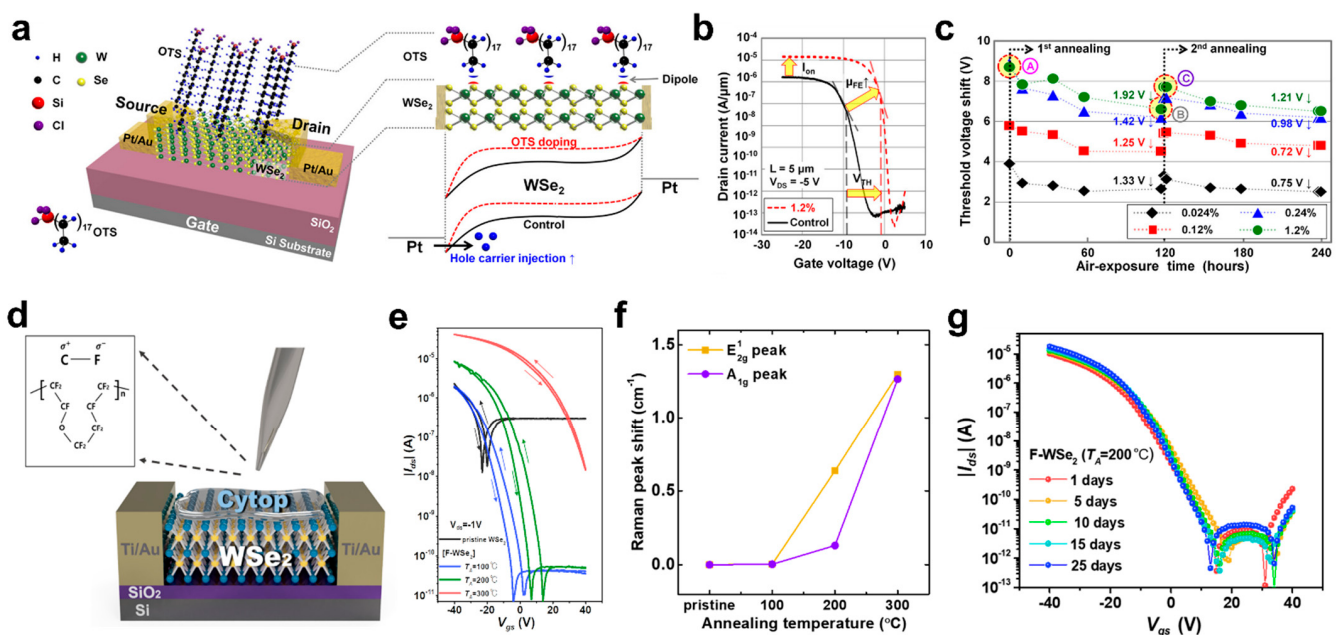


Figure 7. (a) 3D structure and energy band diagram of OTS-doped WSe₂ FET; (b) Transfer curve of pristine WSe₂ FET and OTS-doped WSe₂ FET; (c) Extracted threshold voltage of OTS-doped WSe₂ FET according to air exposure time (adapted from [114] with permission from the American Chemical Society); (d) 3D schematic of CYTOP-doped WSe₂ FET and inset shows the chemical structure of CYTOP; (e) Transfer curve of pristine WSe₂ FET and CYTOP-doped WSe₂ FET with various annealing temperature (100, 200, and 300 °C); (f) Raman peak shift of pristine WSe₂ FET and CYTOP-doped WSe₂ FET; (g) Electrical stability of CYTOP-doped WSe₂ FET over 25 days in air condition (adapted from [115] with permission from the MDPI).

Meanwhile, In 2021, the *p*-doping effect of WSe₂ FET was reported by means of the fluoropolymer CYTOP as a *p*-type dopant [115]. The pristine WSe₂ FETs were coated with CYTOP solution and annealed at various temperatures (100, 200, and 300 °C). Figure 7d shows a 3D schematic of the CYTOP-doped WSe₂ FET. The C–F bond of CYTOP coated on the WSe₂ surface enhances hole accumulation, resulting in the increased *p*-type current. Figure 7e shows the transfer curves of pristine WSe₂ FET and CYTOP-doped WSe₂ FETs. The on and off currents of the pristine WSe₂ FET are 2.30×10^{-6} A and 1.26×10^{-8} A, respectively. However, as CYTOP is doped and the annealing temperature increases, the *p*-type current increases and the n-type current significantly decreases. The off current of the CYTOP-doped WSe₂ FET annealed at 100 °C is reduced to 8.46×10^{-12} A. Subsequently, at the annealing temperature of 200 °C, the on current increases to 8.52×10^{-6} A. In particular, the CYTOP-doped WSe₂ FET with 300 °C annealing processed has an on current of 4.10×10^{-5} A, which is 6 times higher than the initial value, and off current of 3.15×10^{-6} A. In addition, CYTOP coating and additional annealing treatments remove impurities on the surface of WSe₂ and reduce hysteresis due to reduced traps. Also, the *p*-doping effect of CYTOP was investigated by Raman analysis (Figure 7f). The A_{1g} and E_{2g}¹ peaks of CYTOP-coated WSe₂ become blue shifted, and their values increase as the annealing temperature increases. At last, the electrical characteristics of a CYTOP-doped WSe₂ FET annealed at 100 °C were stable for 25 days in air exposure (Figure 7g).

5.4. Annealing and Chemical Doping Effects in MoSe₂ and WS₂—Based Transistor

The molecular arrangement of poly-(diketopyrrolopyrrole terthiophene) (PDPP3T) can be controlled through the adjustment of annealing temperature. Yoo et al. demonstrated the n-doping effect in multilayer molybdenum diselenide (MoSe₂) FET by doping PDPP3T [116]. In particular, at annealing temperatures above 200 °C, the molecular structure of PDPP3T changed edge-on state with molecules oriented vertically. As a result, the edge-on PDPP3T induced an enhanced charge transport effect to MoSe₂ FET due to the superimposed molecular dipole moment. Figure 8a shows the 3D schematic of the PDPP3T-doped MoSe₂ FET. The coated PDPP3T was annealed at various temperatures (100, 200, and 300 °C). Figure 8b shows the transfer curves of pristine MoSe₂ FET and PDPP3T-doped MoSe₂ FET according to the annealing temperature. The pristine MoSe₂ FET had ambipolar behavior with enhanced *p*-type conductivity with 10⁴ A/A of on/off ratio. Annealing temperatures of 100 °C and 200 °C slightly increase the n-type current and *p*-type current of the PDPP3T-doped MoSe₂ FET. However, the annealing process at 300 °C increased the n-type current rapidly and decreased the *p*-type current. In particular, the n-type current of 1.5×10^{-6} A has improved 2000 times compared to the initial value of 7×10^{-10} A. Also, the PDPP3T-doped MoSe₂ FET has enhanced photoresponsivity compared to the pristine device at different wavelengths of light (832, 638, and 405 nm) (Figure 8c). Also, a maximum photoresponsivity of 91.2 AW^{−1} was obtained when light with a wavelength of 638 nm is applied at an intensity of 20 mW/cm².

The n-doping effect in WS₂ FETs has been reported using lithium fluoride (LiF) as a dopant [117]. The pristine WS₂ FET is immersed in 0.01 M of dopant solution and then annealed at 80 °C for 2 min to achieve the n-doping effect. Figure 8d shows the transfer curve of the n-type doped WS₂ FET using LiF dopant. The on/off ratio and the threshold voltage of the pristine WS₂ FET are 4.83×10^5 A/A and 14 V, respectively. However, the LiF-doped WS₂ FET has an on/off ratio of 1.05×10^6 A/A and a threshold voltage of −6 V due to the negative shifted gate voltage. Also, the contact resistance was extracted using the transfer length method (TLM). Figure 8e shows the TLM resistance of the WS₂ FET before and after doping according to the channel length. The doping effect of the WS₂ FET on the LiF significantly reduces the channel and contact resistance, especially leading to the lowest contact resistance of 0.9 kΩ·μm. Figure 8f shows the changed mobility and threshold voltage according to LiF immersing time. As the immersion time in the LiF solution increases, the mobility increases, and the threshold voltage shifts towards the

negative gate voltage. Also, the LiF immersing time of 120 min improves the mobility of the WS₂ FET from 13.2 to 34.7 cm² V⁻¹ s⁻¹.

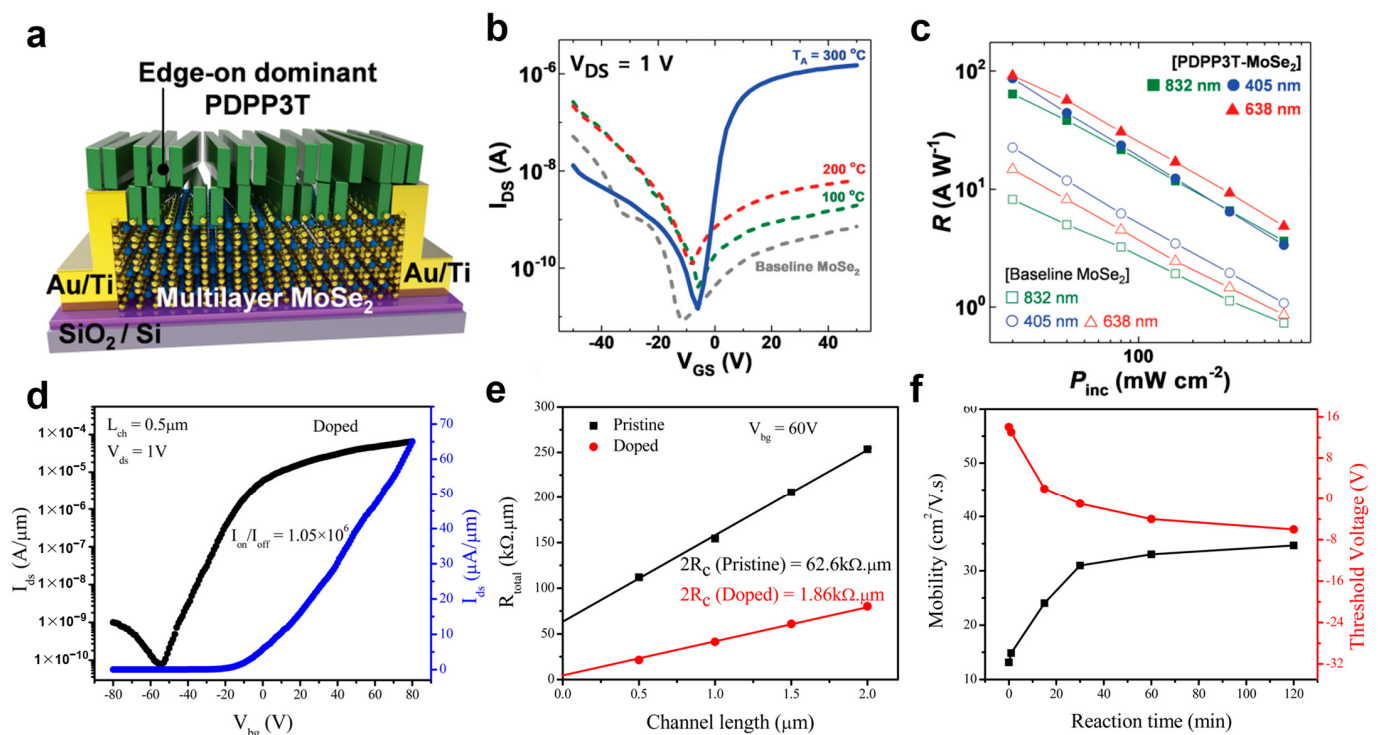


Figure 8. (a) 3D schematic of PDPP3T-doped MoSe₂ FET; (b) Transfer curve of pristine MoSe₂ FET and PDPP3T-doped MoSe₂ FET with various annealing temperatures (100, 200, and 300 °C); (c) comparison photoresponsivity under various light irradiation (832, 638, and 405 nm) (adapted from [116] with permission from the John Wiley and Sons); (d) Transfer curve of LiF-doped WS₂ FET with log and linear scale; (e) Channel and contact resistance of pristine WS₂ FET and LiF-doped WS₂ FET according to channel length; (f) Extracted mobility and threshold voltage of LiF-doped WS₂ FET with Lif immersing time (adapted from [117] with permission from the American Chemical Society).

Chemically doped TMDC FETs exhibit changes in electrical properties as both the TMDC and the chemical dopant are affected by the annealing process. Hence, to achieve the target electrical properties, optimized annealing conditions and appropriate chemical doping should be employed. Table 2 summarizes the post-annealing characteristics of chemically doped TMDC—Based transistors.

Table 2. The annealing effect on the characteristics of TMDC—Based transistors doped with chemical dopants.

Materials	Dopant	Doping Method	Annealing Temperature	Doping Effect	Mobility	Ref.
MoS ₂	PPh ₃	Spin-coating	350 °C	n-type doping	241 cm ² V ⁻¹ s ⁻¹	[110]
MoS ₂	PFO	Spin-coating	350 °C	p-type doping	0.24 cm ² V ⁻¹ s ⁻¹	[111]
MoTe ₂	TFSI	Dipping	100 °C	p-type doping	30 cm ² V ⁻¹ s ⁻¹	[112]
MoTe ₂	PEO:CsClO ₄	Drop-casting	90 °C	n- and p-type doping	7 cm ² V ⁻¹ s ⁻¹ (electron) 26 cm ² V ⁻¹ s ⁻¹ (hole)	[113]
WSe ₂	OTS	Dipping	120 °C	p-type doping	192 cm ² V ⁻¹ s ⁻¹	[114]
WSe ₂	CYTOP	Spin-coating	200 °C	p-type doping	85 cm ² V ⁻¹ s ⁻¹	[115]
MoSe ₂	PDPP3T	Spin-coating	300 °C	n-type doping	75.6 cm ² V ⁻¹ s ⁻¹	[116]
WS ₂	LiF	Dipping	80 °C	n-type doping	34.7 cm ² V ⁻¹ s ⁻¹	[117]

6. Conclusions and Future Aspect

This review discusses diverse techniques aimed at enhancing the electrical characteristics of transistors using TMDCs. The methods explored include annealing processes and chemical doping, which serve as effective means for engineering the electrical properties of TMDC transistors. Studies have examined the impact of annealing processes performed in various atmospheres, such as air, vacuum, and nitrogen, on the performance of TMDC—Based transistors. Additionally, the bandgap structure and Schottky barrier of TMDC can be controlled through functionalization with chemical dopants, such as polymers, SAMs, organic molecules, and inorganic compounds. Optimized annealing processes can further enhance the doping effect of TMDC—Based transistors.

However, several technological barriers remain to be addressed for the development and industrialization of annealing processing and chemical doping techniques for TMDC. Precise control of temperature, humidity, and ambient conditions during the TMDC annealing process is essential to achieve consistent experimental results. Ensuring uniform functionalization of dopants on the TMDC surface is crucial for accurately identifying the doping mechanism. Moreover, the thermal and chemical stability of the dopants should be considered to improve compatibility with subsequent processes. Efforts are ongoing to overcome these barriers through various technological advancements and research initiatives. Continuous optimization of research has significantly expanded the applicability of TMDC—Based devices in diverse fields, including photodetectors, neuromorphic sensors, and logic circuits. Innovative approaches, such as advanced annealing processes, chemical doping methods, integration with other materials, and the development of new device architectures, are actively being explored. As a result of these efforts, TMDC—Based FETs demonstrate great potential as semiconductor devices and are poised for success in industrialization. With the ongoing improvements and innovations, TMDC—Based FETs are expected to play a crucial role in various technological applications.

Author Contributions: Conceptualization: H.Y.; Literature survey: R.K. and D.H.L.; Writing draft: R.K. and D.H.L.; review and editing, R.K., D.H.L. and H.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Technology Innovation Program (00144300, Interface Technology of 3D Stacked Heterogeneous System for SCM—Based Process-in-Memory) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea). This work was supported in part by the Gachon University Research Fund of 2021 (GCU-202106380001).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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